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Quick Start Guide for using the Triggered Capture Feature of the ADS7-V2 Capture Board with the AD9695 ADC Evaluation Board

TYPICAL SETUP

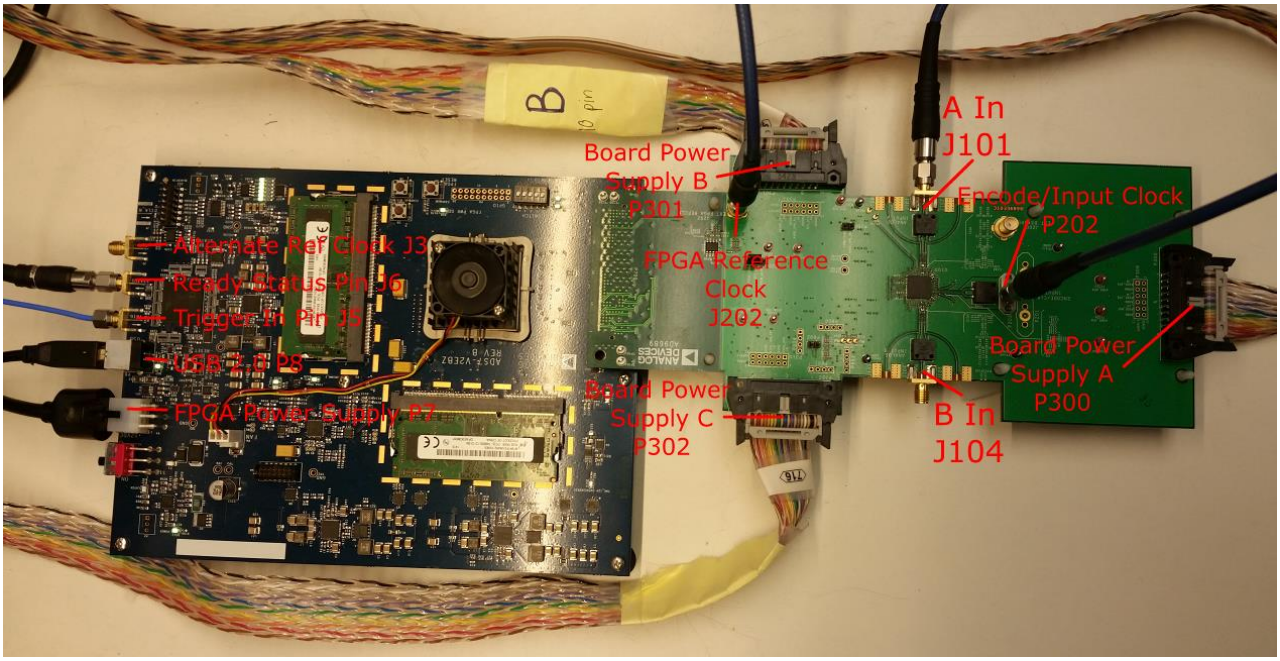

Figure 1. AD9695-1300EBZ Evaluation Board and ADS7-V2 Data Capture Board

EQUIPMENT NEEDED

- Data Capture Evaluation Board
  - ADS7-V2 Data Capture Board
  - 12VDC Power Supply and USB2.0 Cable
  - External Pulse Generator (Such as Stanford Research Systems DS345)
- ADC Evaluation Board
  - AD9695 Evaluation Board, or others in family (Such as AD9689 or AD9208)
  - External Power Supply and Three 10-pin Ribbon Cables
  - External Input Clock (Such as Rohde&Schwarz SMA100A)
  - External Reference Clock (Such as Stanford Research Systems SG384)
  - External Signal Input (Any signal generator, such as Rohde&Schwarz SMA100A)

HELPFUL DOCUMENTS

- AD9695 Evaluation Board User Guide
- VisualAnalog Converter Evaluation Tool User Manual, AN-905
- High Speed ADC SPI Control Software User Manual, AN-878
- Interfacing to High Speed ADCs via SPI, AN-877

SOFTWARE NEEDED

- VisualAnalog (VA) (http://www.analog.com/en/design-center/interactive-design-tools/visualanalog.html)
- Analysis | Control | Evaluation (ACE) (http://www.analog.com/en/design-center/evaluation-hardware-and-software/ace-software.html)
- Appropriate .bin FPGA file (supplied separately)

Documents are available at http://www.analog.com.
For any questions, please send an email to highspeed.converters@analog.com.

TESTING

(Note: Though AD9695 is mentioned in this document, this procedure also applies to the AD9689 and AD9208)

1. Setup the AD9695 evaluation board as described in the AD9695 User Guide. Verify that the evaluation board is converting and processing data normally as specified in the User Guide.

2. Additionally, hardware connections to the SMA connectors SMA1 J5 (Trigger Input Pin) and SMA2 J6 (Ready Status Output Pin) are needed (See figure 1). The FPGA will send an output signal on SMA2 J6 when the FPGA is ready for another capture – see Figure 2 below.

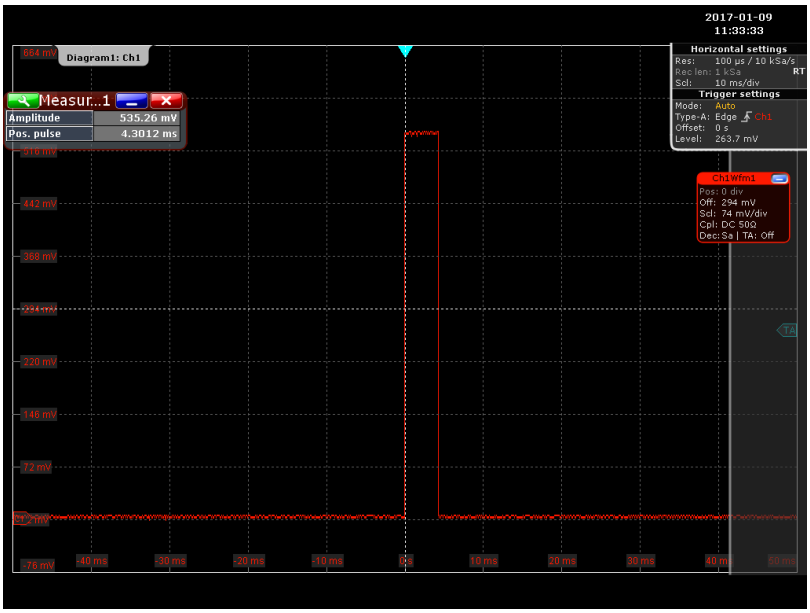

Figure 2: Time Capture of Ready Pin Output

A pulse input on SMA1 J5 will signal to the FPGA to start a capture. The trigger requires an active high pulse width that is longer than the FPGA internal memory clock. See Figure 3 below for an example of a pulsing signal that might be sent.

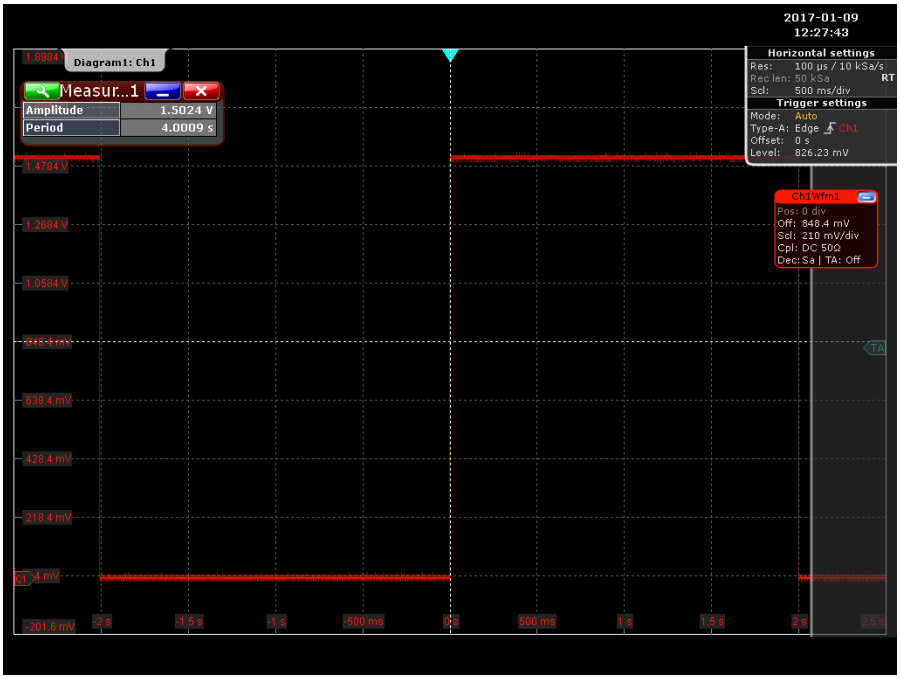

Figure 3: Time Capture of Trigger Pulse

Setup an external signal generator or other appropriate hardware, using the Ready signal if desired, to provide a 0 →1.5V+ rising edge on SMA1 J5 to trigger a capture. Note that the external pin must be driven for external trigger mode – if it is left floating, the FPGA will function as though it is not in external trigger mode, regardless of the mode it is put into.

3. In VisualAnalog, open and setup a new canvas of the desired capture type – for example, an FFT canvas – and click the Settings button on the ADC Capture Block.

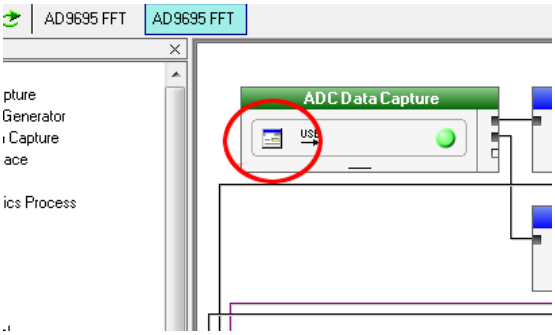

Figure 4: ADC Data Capture Settings Button

4. Clicking the Settings button above will bring up a window with three tabs. In the Capture Board tab, enter a number like 10000 into the Fill Delay (ms) field. This is the amount of time the FPGA will poll the FIFO for a data capture before timing out. Program the FPGA with the appropriate .bin file if not already programmed.

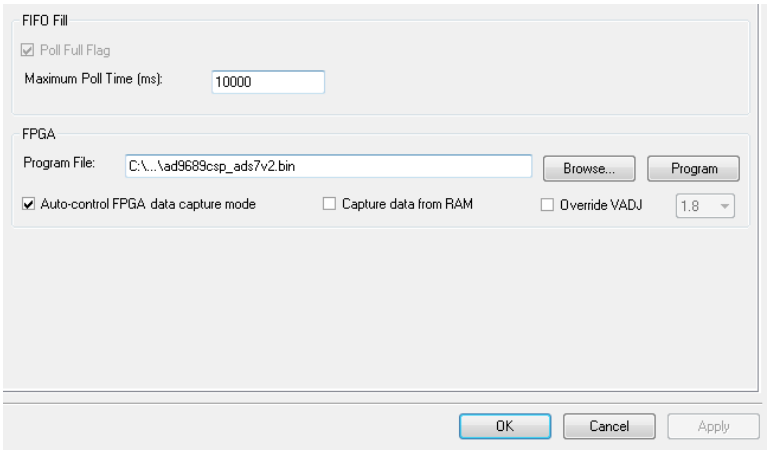

Figure 5: Capture Board Tab

5. In the Device tab, click the Enable External Trigger checkbox (as well as any other settings necessary to your setup, such as Enable Alternate REFCLK). This will program the FPGA for External Trigger Mode.

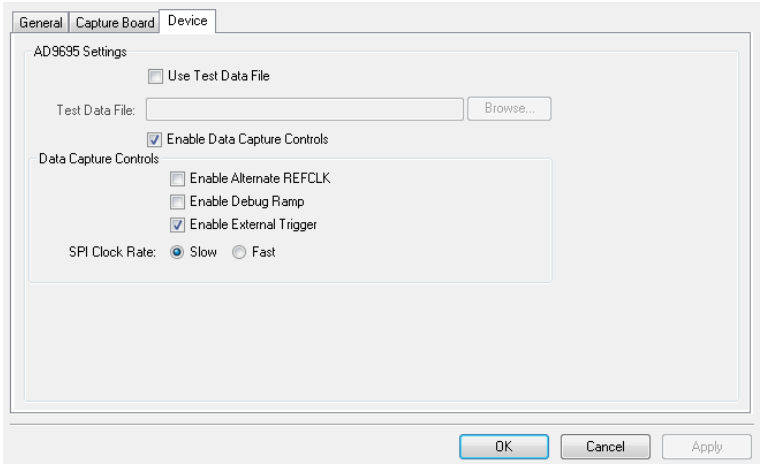

Figure 6: Device Tab

6. Now the evaluation setup is configured for externally triggered capture. Push the Run button on the VisualAnalog top bar.

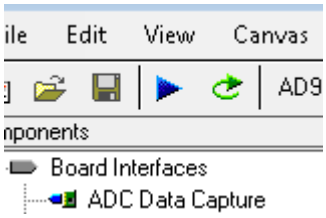

Figure 7: Data Capture Run Button

The evaluation board will now wait for a rising edge to be applied to J5. The rising edge on J5 should wait for a ready status from the FPGA – if it is sent before, the FPGA may not capture data.

7. Apply the rising edge on J5. This edge needs to be applied before the end of the Fill Delay interval specified in Step 4. If 10000 was entered in Step 6, you will have 10000 milliseconds from when the Run button was pushed, to apply the edge.

8. After the Fill Delay interval has passed, data that was captured by external trigger will appear graphically on the Visual Analog canvas. Note that the data will not appear when the trigger edge is applied, but actually after the Fill Delay has passed. Save the data as desired.

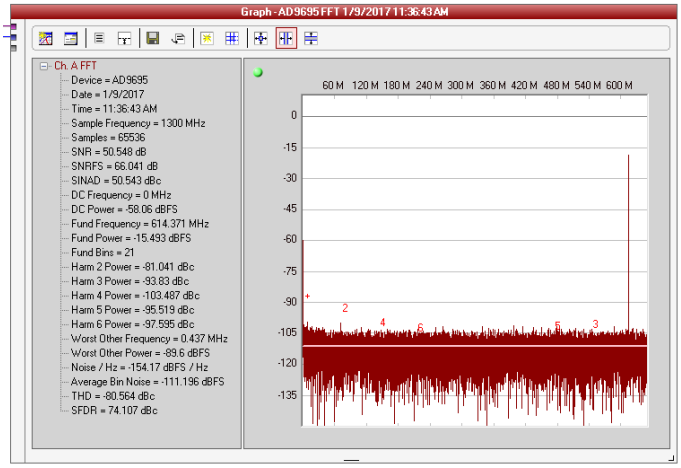

Figure 8: Successful Data Capture

TROUBLESHOOTING

1. The data capture is not waiting for an external input / is acting like a normal capture / is triggering instantly/constantly.

The external pin must be driven for external trigger mode – if it is left floating, the FPGA will function as though it is not in external trigger mode, regardless of the mode it is put into. Check your input and make sure that it is not floating and that the timing of the signal is setup correctly.

2. The data capture is timing out before a capture is taken / I'm getting the following error message:

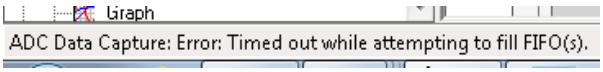

Figure 9: FIFO Timeout

The FPGA did not see a rising edge or the FPGA polling time may not be set for a long enough time – see Step 4. If the polling time is not long enough to see the input trigger, or the input trigger is not timed to coincide with the capture time, the data capture may time out. Ensure that the polling time is set in milliseconds, and not seconds. The voltage or frequency of the input pulse may need to be adjusted, if the polling time is correct. Additionally, this could be a normal error with the evaluation board such as with the JESD lane timing and the input/reference clocks, etc. Make sure that you are getting a regular capture without the external trigger mode.

3. I'm getting the following error message:

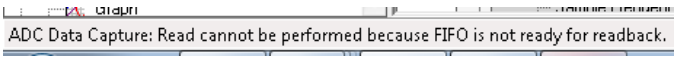

Figure 10: FIFO Not Ready

This is a similar error to Error 2 that may result from the Ready status and Trigger Input signals being mistimed, or it may just be a program error. The best thing to do is to try to reopen the canvas, reopen Visual Analog, or try completely restarting the Evaluation Boards.