AD9625 Timestamp Feature – October 20, 2014

AD9625 can use the SYSREF± pins in either of 2 modes

- LMFC Alignment - A JESD204B subclass 1 mode, where SYSREF± is used to align framing clocks to the local multi-frame clock rate
- Timestamp - A JESD204B subclass 0 mode, where the SYSREF± edge is used to timestamp a sample using extra control bits in the JESD204B information.

Multichip Synchronization Using SYSREF± Timestamp

The SYSREF± pin in the AD9625 can be used as a timestamp of data as it passes through the ADC and out the JESD204B interface.

- Use the extra output JESD204B control bits to insert the synchronous low to high captured SYSREF± signal. These extra control bits are only available while in the JESD204B generic 2, 4, and 8 lane modes.
- Disable SYSREF± from updating and resetting the clock for LMFC alignment by setting register 0x8A to 0x22

ADC Output Control Bits on JESD204B Samples

When N' = 16 and the ADC resolution is 12, there are four spare bits available per sample. Two of these spare bits can be used as control bits, depending on the configuration options. The control bits are set in Register 0x072, Bits[7:6]. (CS means control bits per sample.)

- 00: no control bits sent per sample (CS = 0).
- 01: one control bit sent per sample, overrange bit enabled, (CS = 1).
- 10: two control bits sent per sample, overrange and time stamped SYSREF± control bit (marks the sample of a rising edge seen on the SYSREF± pin), (CS = 2). Use of the SYSREF± control bit (CS = 2) time stamps a particular analog sample that is seen coincident with a rising signal on the SYSREF± pins.

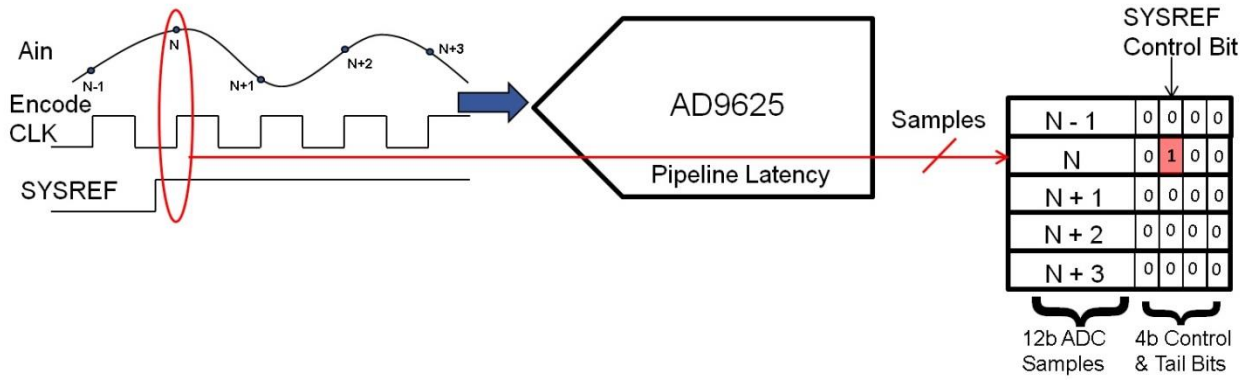

Figure1. A SYSREF± Control Bit is Used to Timestamp the Same Analog Sample that is Coincident with a Sampled SYSREF± Edge by CLK±

Using Rising/Falling Edges of the CLK to Latch SYSREF±

The SYSREF± signal can be latched on either the rising or falling edge of the encode clock, based on the value of register 0x03A[3] = 0 (latch on rising edge) or 0x03A[3] = 1 (latch on falling edge). This will not impact the analog input, which will always be sampled on the rising edge of the encode clock. For sampling SYSREF±, the falling edge encode capture of CLK±[N] will precede the rising edge encode capture of CLK±[N], both corresponding to the same analog sample.

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