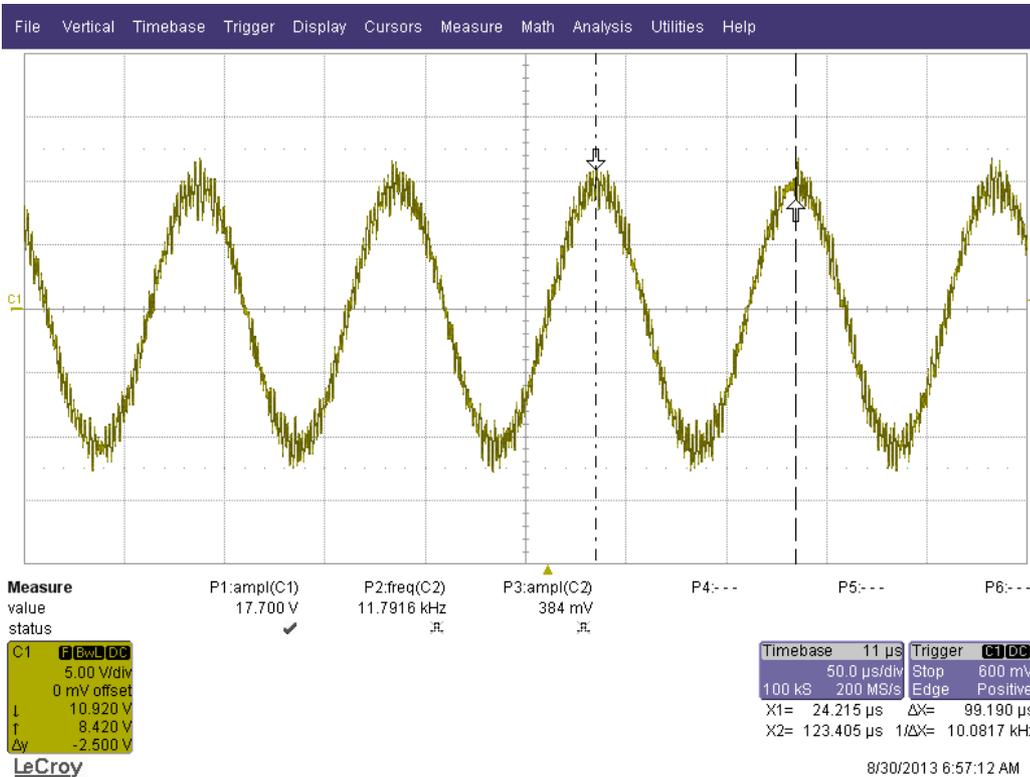


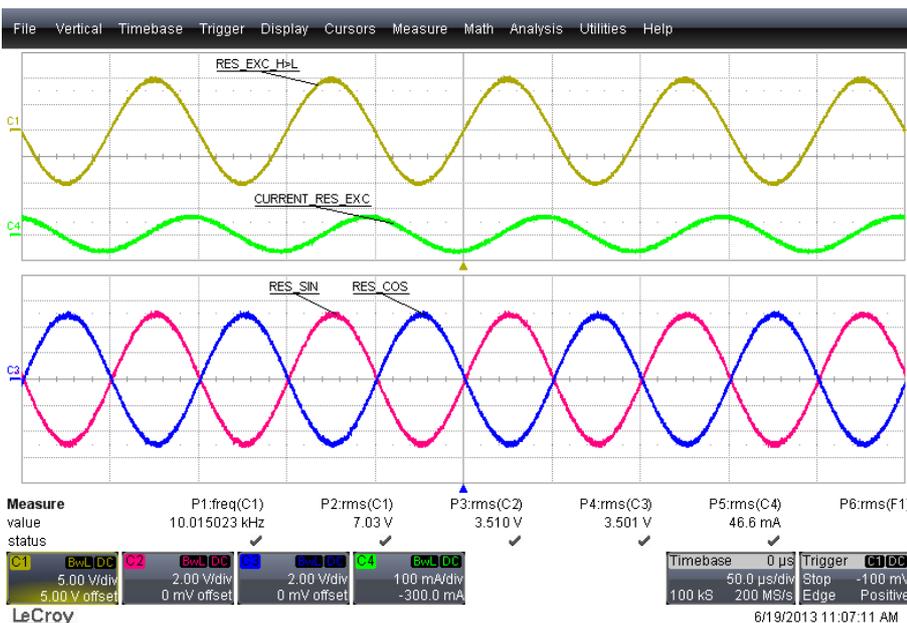
The output of the operational amplifier is fed in to a buffer stage for the generation of the required voltage levels.

3 MEASUREMENTS

After receiving the final code of the FPGA a commissioning of the Resolver circuit was done and the output of the Excitation shows a sinusoidal voltage, 10kHz 7Vrms with an overlaid noise.



At the beginning (board delivery without FPGA code) the excitation circuit was tested by lifting the input resistors of the operational amplifier and inject the EXC and NEXC with an external function generator. The output shows a good-looking sine wave (yellow).



The first assumption was, that the distortion comes from the Supply voltages and the Supply-Pins are lifted and the following circuit was used for filtering each supply (AVDD, DVDD and VDRIVE) and the corresponding ground.

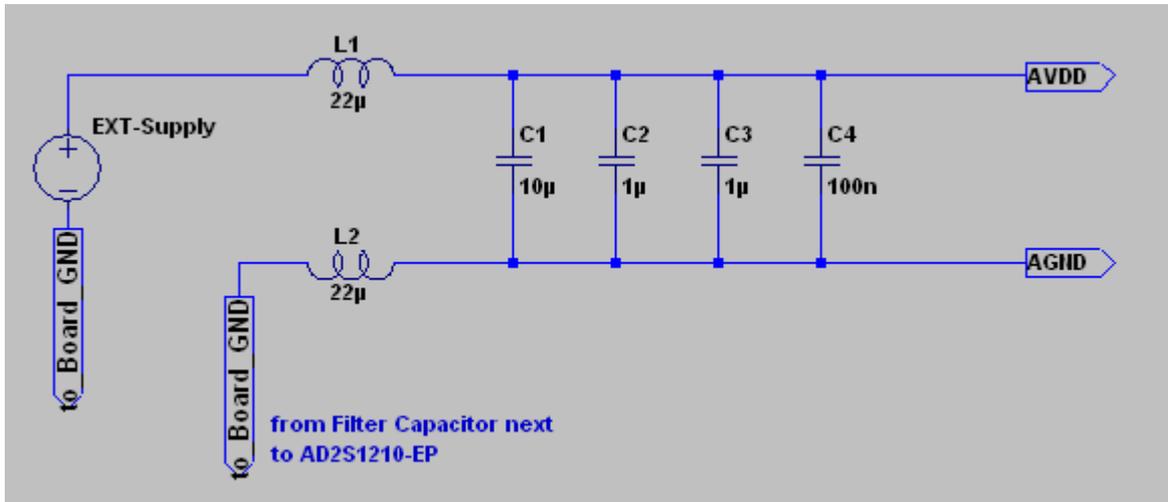
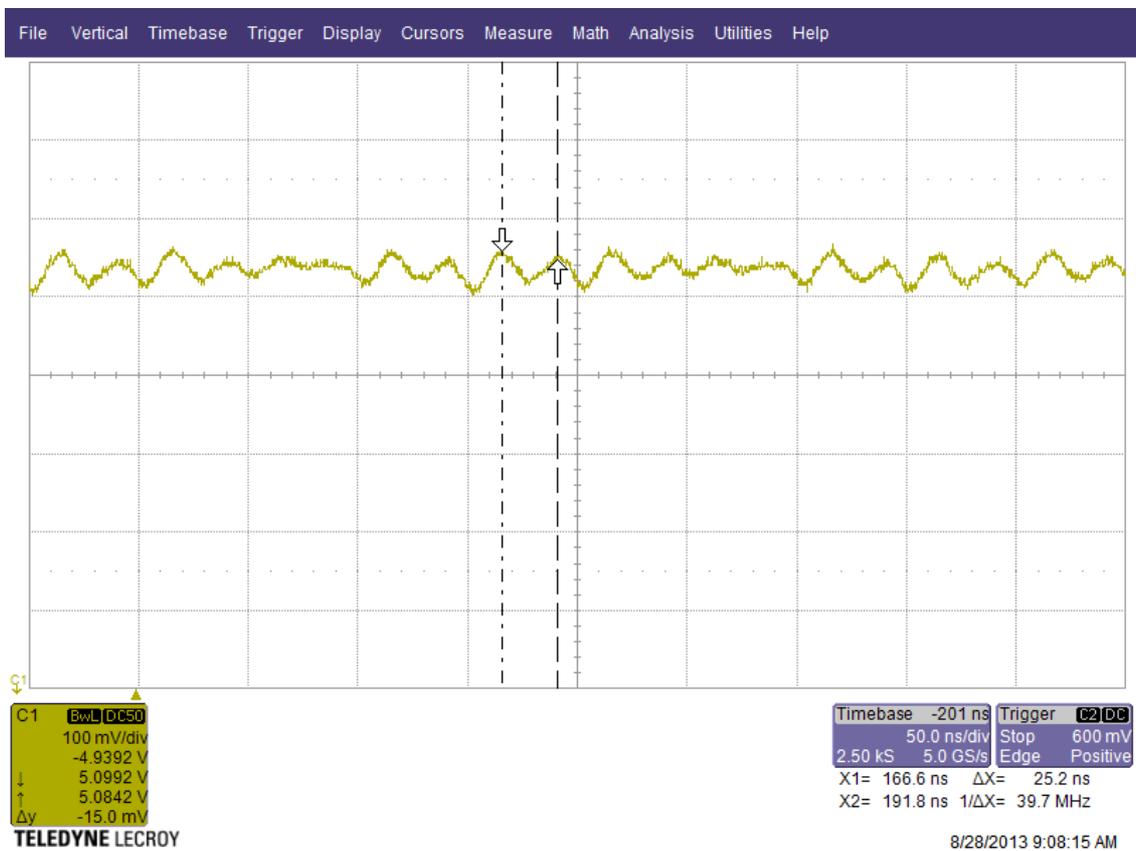
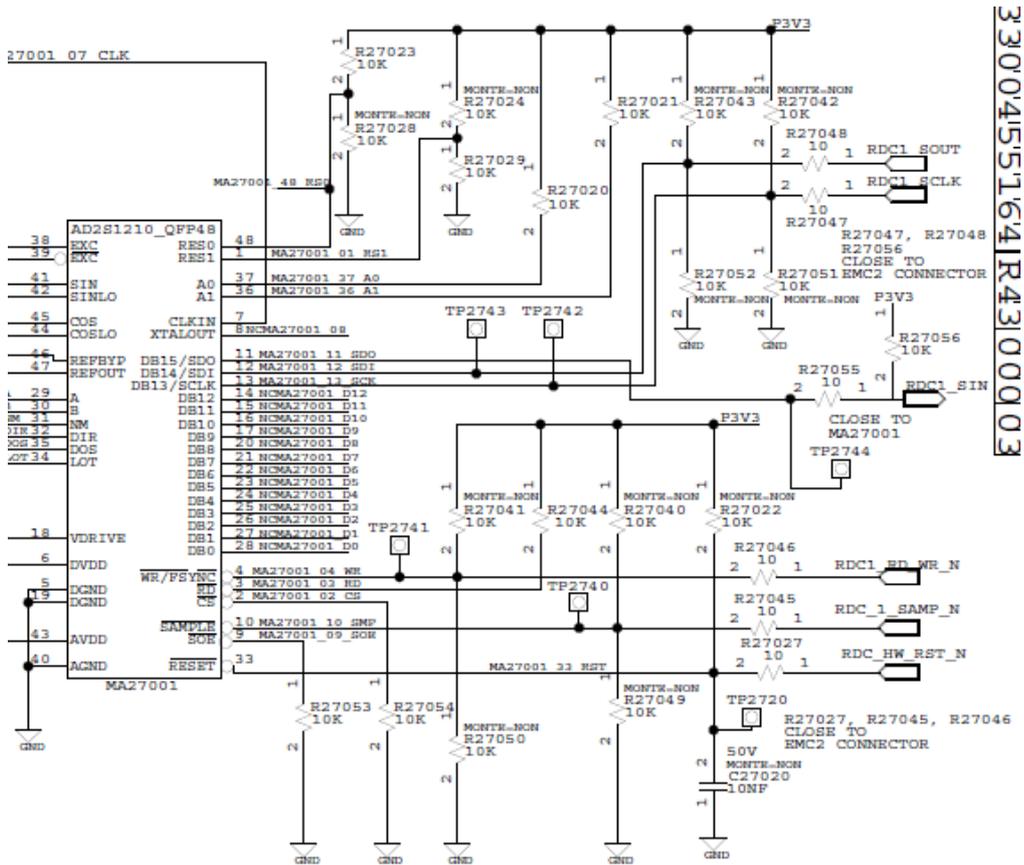


Figure 3-1: Filter circuit for AVDD supply

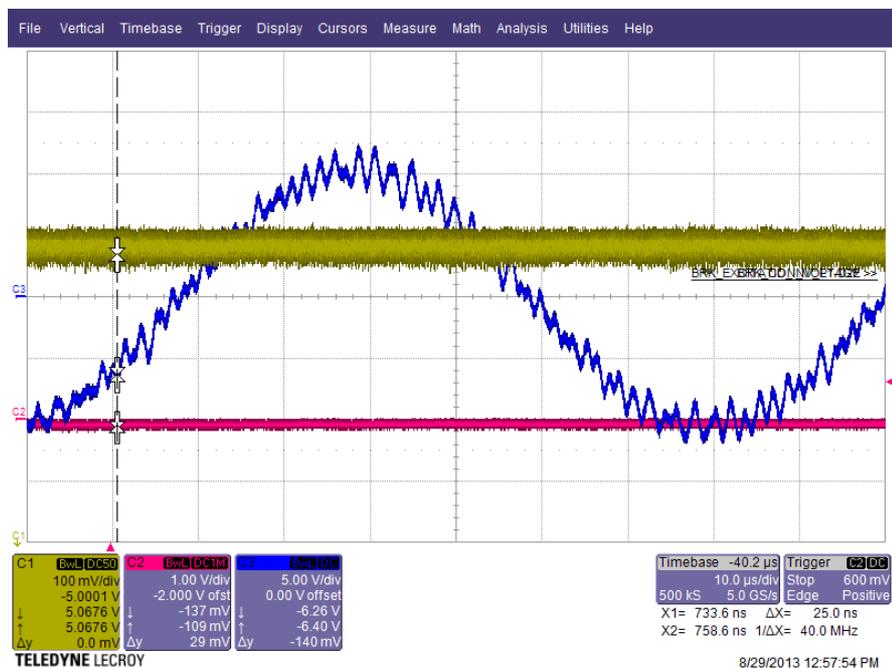
An external supply was used for the following tests, but the output signal does not change. The measurement of the supplies show no disturbance for AVDD and VDRIVE and a small ripple of 50mV 40MHz on DVDD (see Picture).



Assumption: these small ripple is not the reason for the disturbance!



Continuing with test by removing the clock for the serial communication (R27047 removed), SDI (R27048 removed) and the RESET was set also by the external supply via a pull up and R27027 removed.

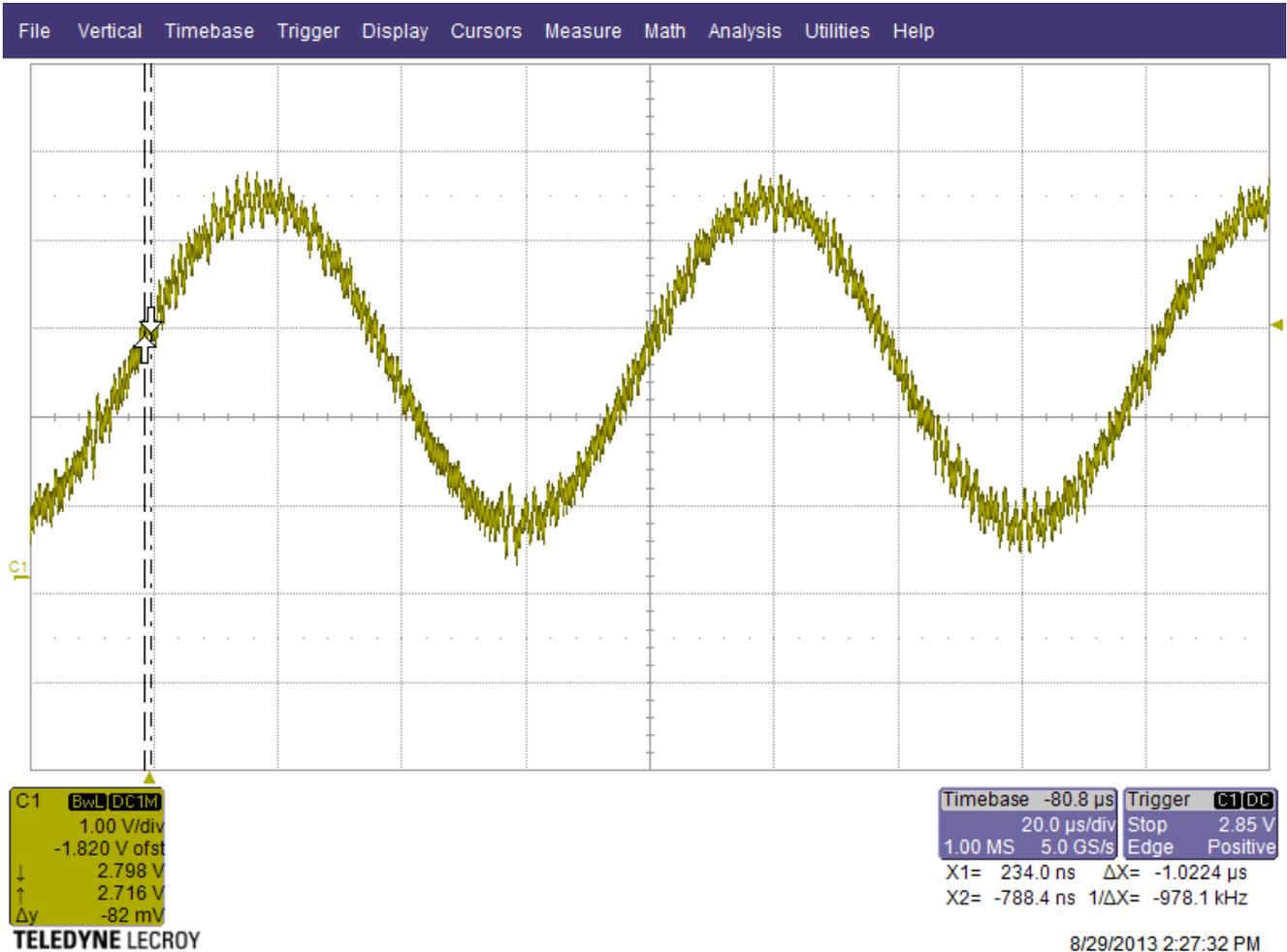


The disturbances already exists.

At this point, the CLKIN (Pin7) was lifted and supplied via an external function generator and it was possible to run the AD2S1210-EP alone.

The switch off of all other board functions and only run the RDC, the same disturbances appear.

Signal is measured at EXC (Pin38).



4 INVESTIGATION SUMMARY

4.1 STATUS

At these state the investigation is stopped because the assumption for reason of disturbance is the AD2S1210-EP itself. A service request is initiated to Analog Device (AD2S1210-EP (case#: E13H202443)) and an answer is outstanding.