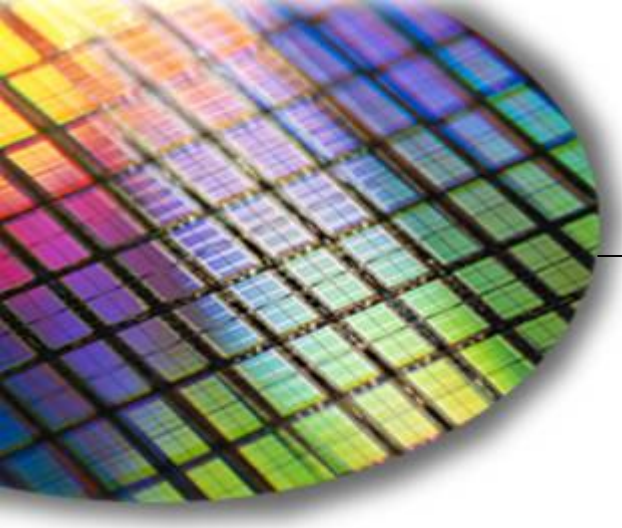


The World Leader in High Performance Signal Processing Solutions

ADSP-BF70x Guide to Power Estimation
Rev 1 (08/27/2015)

ANALOG DEVICES

Revision history

Revision	Changes
Rev 0 (08/13/2014)	Initial Revision
Rev 1 (08/31/2015)	Updates to maximum static power, DMA data rate power, USB suspend mode power, hibernate power, and power example.

Introduction

This document describes how to estimate power consumption for the BF70x processors.

The application note EE-297: Estimating Power for ADSP-BF534/BF536/BF537 Blackfin® Processors should be used as a reference since much of it also applies to BF70x. EE-297 is available at www.analog.com/blackfin under application notes.

Please consult the following sections of the ADSP-BF70x Data Sheet (PrC or later) for the following specifications referred to throughout this document:

- See the Operating Conditions section for the voltage ranges of the various power domains (VDD_INT, VDD_EXT, etc.)
- See the Ordering Guide section for a list of the presently available ADSP-BF70x models processors.

Power Consumption

Derived Power Consumption (PDD_TOT)

- **PDD_TOT = ΣP_{DDn} where n = each V_{DD} domain**

Standard Power Domains (All Blackfin Products)

- **Internal Power Consumption (PDD_INT)**
  - Static and Dynamic Components

    Static (Leakage) is a function of Voltage (VDD_INT) and Operating Junction Temperature (T_J)

    Dynamic is a function of Voltage and Frequency
- **External Power Consumption (PDD_EXT)**
  - PDD_EXT factors several components

    Voltage, Frequency, Output Pins Toggling, and Usage

    Largely an estimation based on application run-time averages

Other Power Domains

Some have the same rules as PDD_EXT

- **MEM (P_{DDMEM}) – ADSP-BF51x and ADSP-BF52x**
- **FLASH ($P_{DDFLASH}$) – ADSP-BF51x**
- **DDR Memory (P_{DDDMC} /P_{DDDDR}) – ADSP-BF54x, ADSP-BF70x**

Others Are Specified In Datasheet

- **OTP Memory (P_{DDOTP}) – ADSP-BF51x, ADSP-BF52x, ADSP-BF70x**
- **USB (P_{DDUSB}) –ADSP-BF52x, ADSP-BF54x, ADSP-BF70x**
- **Thermal Diode (P_{DDTD}) – ADSP-BF60x**
- **RTC ($P_{DDRTC)}$ – ADSP-BF5xx, ADSP-BF70x**
- **HADC ($P_{DDHADC)}$ – ADSP-BF70x**

Maximum Internal Power (PDD_INT)

Internal Power Consumption (PDD_INT)

Consumed by core, PLL, peripherals, and other internal circuitry

- **Voltage, Frequency, and Temperature influence numbers**
- **Dependent on the application code running**

Typical and Maximum specifications for IDD_INT are given at specific voltages, frequencies, and temperatures

I_{DDINT} Estimation

IDDINT is the sum of the following 9 components:

Component	Description
IDDINT_DEEPSLEEP	Static Component - Depends on voltage and temperature. Varies from part to part.
IDDINT_CCLK_DYN	Dynamic current from the core clock domain. Depends on the ASF (activities scaling factor) of each core, CCLK frequency, and VDD_INT.
IDDINT_PLLCLK_DYN IDDINT_SYSCLK_DYN IDDINT_SCLK0_DYN IDDINT_SCLK1_DYN IDDINT_DCLK_DYN	Dynamic components calculated from the frequency of the clock, VDD_INT, and an ADI-provided coefficient which was measured for each clock domain.
IDDINT_DMA_DR_DYN	Dynamic component that represents the total data rate used in non-CCLK clocking domains. Calculated by adding the data rate of each DMA and core driven access to peripherals and L2/external memory. This number is then multiplied by an ADI-provided coefficient and VDD_INT.
IDDINT_USBCLK_DYN	Dynamic component that is added if USB is used

$I_{DDINT\_DEEPSLEEP}$ – Static Component of Power (Maximum)

Tj (°C)	Voltage (VDDINT)												
	1.045	1.050	1.060	1.070	1.080	1.090	1.100	1.110	1.120	1.130	1.140	1.150	1.155
-40	0.6	0.6	0.7	0.7	0.7	0.8	0.8	0.8	0.9	0.9	0.9	1.0	1.0
-20	1.1	1.1	1.2	1.2	1.2	1.3	1.4	1.4	1.5	1.5	1.6	1.7	1.7
0	2.0	2.0	2.1	2.2	2.3	2.4	2.5	2.5	2.6	2.7	2.8	3.0	3.0
25	4.3	4.3	4.5	4.7	4.8	5.0	5.2	5.3	5.5	5.7	5.9	6.1	6.2
40	6.7	6.8	7.0	7.3	7.5	7.8	8.0	8.3	8.6	8.8	9.1	9.4	9.6
55	10.3	10.5	10.8	11.2	11.5	11.9	12.3	12.6	13.0	13.4	13.9	14.3	14.5
70	15.7	15.9	16.4	16.8	17.4	17.9	18.4	18.9	19.5	20.1	20.7	21.3	21.6
85	23.3	23.6	24.3	25.0	25.7	26.4	27.2	27.9	28.7	29.5	30.4	31.2	31.7
100	34.2	34.6	35.5	36.5	37.5	38.5	39.5	40.6	41.7	42.8	43.9	45.1	45.7
105	38.7	39.2	40.2	41.3	42.4	43.5	44.6	45.8	47.0	48.2	49.5	50.8	51.5
115	48.9	49.5	50.7	52.0	53.4	54.7	56.0	57.5	59.0	60.5	62.0	63.6	64.4
125	61.5	62.1	63.6	65.1	66.7	68.3	69.9	71.7	73.4	75.2	77.0	79.0	79.9

- **Static Component (IDDINT_DEEPSLEEP, in mA) is exactly the value in this table**
  - Recall: Deep Sleep Mode – PLLCLK = CCLK = SYSCLK = DCLK = SCLK0 = SCLK1 = 0 MHz with Power On
  - Specification is a maximum current across process. In other words, Analog Devices does not sell any production grade BF70x parts with IDDINT_DEEPSLEEP above the values in the table above.
  - Changes with VDD_INT and Tj (junction temperature)
- **VDD_INT plots of IDD_INT vs. Temperature follow exponential curve**

IDDINT_CCLK_DYN

CCLK Dynamic Current per core(mA at ASF = 1.0), Typical Material

f_{CCLK}(MHz)	Voltage (V_{DDINT})												
	1.045	1.050	1.060	1.070	1.080	1.090	1.100	1.110	1.120	1.130	1.140	1.150	1.155
400	66.7	67.2	67.9	68.7	69.4	70.2	71.1	71.8	72.6	73.4	74.2	74.9	75.4
350	58.6	59.0	59.6	60.3	61.0	61.7	62.4	63.0	63.7	64.4	65.1	65.8	66.1
300	50.2	50.5	51.1	51.7	52.3	52.9	53.5	54.1	54.7	55.3	55.9	56.4	56.8
250	42.1	42.3	42.8	43.3	43.8	44.3	44.7	45.3	45.8	46.3	46.8	47.4	47.6
200	33.7	33.9	34.3	34.7	35.1	35.5	35.9	36.3	36.7	37.1	37.5	37.9	38.0
150	25.4	25.5	25.8	26.1	26.4	26.7	27.0	27.3	27.6	27.9	28.2	28.5	28.8
100	17.0	17.1	17.3	17.5	17.7	17.9	18.1	18.3	18.5	18.6	18.8	19.0	19.1

"Typ1" Testcase Represents an ASF = 1.0

IDDINT_CCLK_DYN (mA) = (CCLK Dynamic Current per core) · (ASF)

- **CCLK Dynamic Current is measured by Analog Devices and can be taken straight from the table above**
- **ASF indicates activity level on the core**
  - **1.00 is Baseline – uses "Typical1" application previously defined (See the next slide)**
    - Core Performing 70% Dual-MAC, 20% Load/Store, and 10% NOP Operations
    - No DMA Activity
    - Core fetches a data pattern from L1 (half the data bits toggling)
  - **Multipliers are specifications based on characterization**
  - **User must determine which Activity Level most closely matches their own application**

ASF Table

Power Vector	Activity Scaling Factor
App1	0.79
App2	0.83
App3	0.78
High1	1.39
High2	1.54
High3	1.39
Idle1	0.05
Idle2	0.05
Nop1	0.56
Nop2	0.59
Typ1	1.00
Typ2	1.03
Typ3	1.01

Activity Scale Factors (ASF)

$I_{DD-IDLE1}$

- **Core executing the IDLE instruction only, with no core memory accesses, no DMA, and no interrupts. IDLE2 turns on the branch predictor (BP)**

$I_{DD-NOP1}$

- **Core executing the NOP instruction only, with no core memory accesses, no DMA, and no interrupts. NOP2 turns on BP**
  - Useful for software delay loops

$I_{DD-APPn}$

- **Core executing an application comprised of 30% MAC instructions and 70% load-store and NOP instructions**
- **All instructions and data are located in L1 SRAM, and peripherals/DMA are not enabled**

$I_{DD-TYPn}$

- **Core Performing 70% MAC, 20% Load/Store, and 10% NOP Operations**
  - Datasheet baseline

$I_{DD-HIGHn}$

- **Same as I_{DD-APP} except application is 100% MAC instructions**

For I_{DD-APP},I_{DD-TYP}, and $I_{DD-HIGH}$:

- **BP is on**
- **n = 1 - Dual 16-bit MAC operations**
- **n = 2 - Complex MAC operations**
- **n = 3 - 32-bit MAC operations**

IDDINT_PLLCLK_DYN IDDINT_SYSCLK_DYN, IDDINT_SCLK0_DYN, IDDINT_SCLK1_DYN, and IDDINT_DCLK_DYN

The following equation is used to estimate the dynamic current due to each of the clock domains listed, where *x* represents the clock domain:

$$IDDINT\_xCLK\_DYN\ (mA) = fxCLK(MHz) \cdot VDD\_INT\ (V) \cdot xCOEFFICIENT\left(\frac{mA}{MHz \cdot V}\right)$$

To calculate the current due to a particular clock domain plug in the frequency for that domain, the VDD_INT voltage, and the domain-specific coefficient from the table below:

Clock Domain Frequency (xCLK)	Dynamic Power Co-efficient (xCOEFFICIENT)
PLLCLK	0.012
SYSCLK	0.120
SCLK0	0.110
SCLK1	0.068
DCLK	0.055

IDDINT_USBCLK_DYN

There is a dynamic adder to IDDINT when the USB peripheral is in use:

Is USB Used?	IDDINT_USBCLK_DYN (mA)
Yes – High-Speed Mode	13.94
Yes – Full-Speed Mode	10.83
Yes – Suspend Mode	5.20
No	0.34

IDDINT_DMA_DR_DYN (1 of 2)

The following equation is used to estimate the data-rate-dependent dynamic component in BF70x processors:

$$\text{IDDINT\_DMADR\_DYN (mA)} = TotalDataRate(MBPS) \cdot VDD_{INT}(V) \cdot WeightedDRC(\frac{mA}{MBPS \cdot V})$$

Data Rate

- Represents the total data rate used to move data between a given source (a) and destination (b) in the system
- Expressed in MBPS (MBytes/second)
- Calculated for the end application by adding the data rate of each DMA and core driven access to and from peripherals and L2/external memory.
- Because it is expressed in MBPS the frequency is already taken into account
- Basic example for a single peripheral transferring data L2 memory: SPORT receive clock is running at 25 MHz and the SPORT is in DMA mode. 2 data lines are being used:

  2 bits/cycle · 25 M cycles/second · 1/8 bytes/bit = 6.25 MBPS from SPORT to L2 Memory

Weighted DRC (Data Rate Coefficient)

- Units are $\frac{mA}{MBPS \cdot V}$
- When multiplied by Total Data Rate and VDDINT the result is IDDINT_DMA_DR_DYN (mA)
- Different coefficients exist depending on the source and destination of the transfer
- A weighted coefficient can be created taking the percentage of total bandwidth for a given source/destination, multiplying by the specific coefficient for that source/destination, and adding all the weighted coefficients together
- See the next slide for a list of coefficients and the equation

IDDINT_DMA_DR_DYN (2 of 2)

Let the set S equal each possible permutation of data source and data destination shown in the table below.

$$WeightedDRC = \sum_{s \in S} DRC_s \cdot \left(\frac{DataRate_s(MBPS)}{TotalDataRate\ (MBPS)} \right)$$

Data Source	Data Destination	Coefficient
Peripheral	L1	0.0252
Peripheral	L2	0.0166
Peripheral	L3	0.0168
L1	Peripheral	0.0246
L1	L1	0.0497
L1	L2	0.0349
L1	L3	0.0309
L2	Peripheral	0.0264
L2	L1	0.0462
L2	L2	0.0350
L2	L3	0.0321
L3	Peripheral	0.0320
L3	L1	0.0359
L3	L2	0.0375

Typical Internal Power (PDD_INT Typical)

How to Read Typical IDD_INT Data

How is typical power usually defined?

- Nominal VDD_INT (typical data across the operating voltage range is also available)
- Tjunction = 25˚ C (typical data across the operating temperature range is also available)
- ASF (Activity Scaling Factor) = 1.0 for each core
- Typical silicon - some individual BF70x parts will consume more IDDINT_DEEPSLEEP (static current) and some individual BF70x parts will consume less IDDINT_DEEPSLEEP.
- The most useful information is the typical IDDINT_DEEPSLEEP (static current) since IDDINT_DEEPSLEEP varies from part to part whereas the rest of the components of IDD_INT are the same on every part.

DO:

- Do use for back of the envelope calculations
- Do use typical data to estimate AVERAGE battery life
- Compare to other manufacturers typical data (carefully because of different definitions of typical)
- Make your own estimate of ASF and I/O Power when using typical data

DO NOT

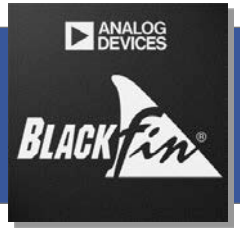
- Do not use typical data to size a power supply
- Do not confuse typical data with maximum data
- Do not assume that all parts are typical
- Do not use typical data for system thermal analysis

$I_{DDINT\_DEEPSLEEP}$ – Static Component of Power (Typical)

WARNING: Typical power is in the middle of the product distribution. A significant number of devices will exceed typical power. It is recommended that maximum power is used for system analysis.

T_J (°C)	Voltage (V_{DDINT})												
	1.045	1.050	1.060	1.070	1.080	1.090	1.100	1.110	1.120	1.130	1.140	1.150	1.155
-40	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.4	0.4	0.4	0.4	0.4
-20	0.3	0.3	0.4	0.4	0.4	0.4	0.4	0.5	0.5	0.5	0.5	0.5	0.5
0	0.5	0.5	0.5	0.6	0.6	0.6	0.6	0.7	0.7	0.7	0.7	0.8	0.8
25	1.1	1.1	1.1	1.2	1.2	1.3	1.3	1.4	1.4	1.5	1.5	1.5	1.6
40	1.6	1.6	1.6	1.7	1.8	1.8	1.9	1.9	2.0	2.1	2.1	2.2	2.2
55	2.5	2.5	2.6	2.7	2.8	2.9	2.9	3.0	3.1	3.2	3.3	3.4	3.4
70	3.9	4.0	4.1	4.2	4.3	4.5	4.6	4.7	4.9	5.0	5.1	5.3	5.3
85	6.1	6.2	6.4	6.6	6.8	7.0	7.1	7.3	7.5	7.7	7.9	8.1	8.2
100	9.5	9.6	9.9	10.1	10.4	10.7	10.9	11.2	11.5	11.7	12.0	12.3	12.4
105	11.0	11.1	11.4	11.7	11.9	12.2	12.5	12.8	13.1	13.4	13.7	14.1	14.2
115	14.3	14.5	14.8	15.2	15.6	16.0	16.2	16.7	17.1	17.4	17.8	18.2	18.4
125	18.5	18.7	19.1	19.6	20.0	20.5	20.9	21.4	21.9	22.3	22.8	23.3	23.6

- **Typical Static Component (typical IDDINT_DEEPSLEEP) is the value in this table**
  - Recall: Deep Sleep Mode – CCLK = PLLCLK = SYSCLK = DCLK = SCLK0 = SCLK1 = 0 MHz with power on
  - The data provided is represents the middle of the product distribution. In other words, static power on an individual device may be higher (up to the maximum IDDINT_DEEPSLEEP specification) or lower
  - Changes with VDD_INT and Tj (junction temperature)
- **VDD_INT plots of IDD_INT vs. Temperature follow exponential curve**



External Power (PDD_EXT) and Others

External Power Consumption (PDD_EXT)

For each unique group of pins, magnitude depends on

- **Number of output pins that switch during each cycle (O)**
- **Maximum frequency at which they can switch (f)**
- **Load capacitance (C)**
- **Voltage swing (VDD_EXT^2)**
- **Utilization factor (U)**

External power estimation calculation

- **$PDD\_EXT = \frac{1}{2} (VDD\_EXT^2) * C * f * O * U$**
  - Model assumes ½ power dissipated by external components
- **Equation extends to cover PDD_DMC**

IDD_RTC & IDD_HADC

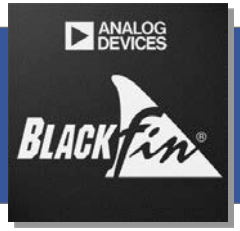
Is RTC Enabled?	IDD_RTC (mA)
Yes	0.01
No	0.003

HADC State	IDDHADC (mA)
Disabled	0.01
Idle	2.00
Converting	2.50

IDD_USB & IDD_OTP

Is USB Used?	IDDUSB (mA)
Yes – High-Speed Mode	33.31
Yes – Full-Speed Mode	13.46
Yes – Suspend Mode	0.05
No	0.05

OTP Mode of Operation	IDDOTP (mA) Typical	IDDOTP (mA) Maximum
Read	6.6	8.1
Write	10.5	14.9
Inactive	0.04	0.1



Hibernate Current/Power

Hibernate Current With USB (Only applies when the processor is in the HIBERNATE state)

Test Conditions:

VDD_INT = 0V

VDD_DMC = 1.8V

VDD_EXT = VDD_HADC = VDD_OTP = VDD_RTC = VDD_USB = 3.3V

fCLKIN = 0MHz, 25C, USB_PHY_CTL.DIS = 0.

Typical silicon - some individual BF70x parts will consume more hibernate current and some individual BF70x parts will consume less hibernate current.

Total current including IDD_DMC, IDD_EXT, IDD_HADC, IDD_RTC, IDD_OTP and IDD_USB during hibernate: **33uA (typical)**

Total power consumption including PDD_DMC, PDD_EXT, PDD_HADC, PDD_RTC, PDD_OTP and PDD_USB: **100uW (typical)**

Hibernate Current Without USB (Only applies when the processor is in the HIBERNATE state)

Test Conditions:

VDD_INT = 0V

VDD_DMC = 1.8V

VDD_EXT = VDD_HADC = VDD_OTP = VDD_RTC = VDD_USB = 3.3V

fCLKIN = 0MHz, 25C, USB_PHY_CTL.DIS = 1.

Typical silicon - some individual BF70x parts will consume more hibernate current and some individual BF70x parts will consume less hibernate current.

Total current including IDD_DMC, IDD_EXT, IDD_HADC, IDD_RTC, IDD_OTP and IDD_USB during hibernate: **15uA (typical)**

Total power consumption including PDD_DMC, PDD_EXT, PDD_HADC, PDD_RTC, PDD_OTP and PDD_USB: **41uW (typical)**

Example Power Calculation

For typical examples see the BF70x data sheet

Power Supply Design Sizing Guideline

The power supply design for this product must be able to meet the peak current consumption for your specific application. Specifically this means maximum ASF, maximum VDDINT, maximum junction temperature (maximum static current), maximum clock frequencies, and maximum data rate. This is intended to account for worst case short duration bursts of activity and all possible component variations.

- **DO:**
  - Use maximum voltage for power supply sizing
  - Use maximum Tjunction (as appropriate for your application maximum Tambient)
  - Use peak power calculation (could occur for a short duration in the application code – but not sustainable)
  - Calculate each unique voltage domain separately
- **DO NOT**
  - Do not use typical Idd or nominal voltage or room temperature to size a power supply
  - Do not use average power
  - Do not use total device power to size a power supply

Total Device Thermal Power Design Guideline

The system thermal design for this product must be designed not to exceed the Tjunction datasheet specification. Time-averaged power should be used for thermal calculations. Specifically this means typical ASF, nominal VDDINT, maximum junction temperature (maximum static current), time-averaged clock frequencies, and time-averaged data rates. This is intended to account for the average power consumption.

- **DO:**
  - Use nominal voltages to calculate thermal power
  - Use maximum Tjunction (as appropriate for your application maximum Tambient)
  - Use Full-on-Typical or lower ASF (to match realistic application code activity levels)
  - Calculate total power for all voltage domains
  - Do use time-averaged clock and data rates if these vary in the application
- **DO NOT**
  - Do not use typical Idd data or room temperature to calculate thermal power
  - Do not use maximum voltage (this is not realistic since any transient will exceed max voltage spec)
  - Do not use peak power

Total Device Thermal Power Example BF70x – Input Data

The following input data is used to calculate IDD_INT in this example:

VDDINT (V)	1.1
VDDEXT (V)	3.30
Tjunction (°C)	100
PLLCLK (MHz)	800
CCLK (MHz)	400
SYSCLK (MHz)	200
SCLK0 (MHz)	50
SCLK1 (MHz)	25
DCLK (MHz)	0
ASF_core0	1.03

USB, DDR2/LPDDR, HADC, RTC, and OTP aren't actively used.

PPI, SPORT, UART, and MDMA are used. Detailed assumptions are shown on the IDDINT_DMA_DR_DYN and PDD_EXT pages.

Note that PLLCLK must be 800 MHz to support CCLK = 400 MHz and SYSCLK = 200 MHz according to data sheet specifications.

First, Obtain Static Component

	Voltage (VDDINT)												
Tj (°C)	1.045	1.050	1.060	1.070	1.080	1.090	1.100	1.110	1.120	1.130	1.140	1.150	1.155
-40	0.6	0.6	0.7	0.7	0.7	0.8	0.8	0.8	0.9	0.9	0.9	1.0	1.0
-20	1.1	1.1	1.2	1.2	1.2	1.3	1.4	1.4	1.5	1.5	1.6	1.7	1.7
0	2.0	2.0	2.1	2.2	2.3	2.4	2.5	2.5	2.6	2.7	2.8	3.0	3.0
25	4.3	4.3	4.5	4.7	4.8	5.0	5.2	5.3	5.5	5.7	5.9	6.1	6.2
40	6.7	6.8	7.0	7.3	7.5	7.8	8.0	8.3	8.6	8.8	9.1	9.4	9.6
55	10.3	10.5	10.8	11.2	11.5	11.9	12.3	12.6	13.0	13.4	13.9	14.3	14.5
70	15.7	15.9	16.4	16.8	17.4	17.9	18.4	18.9	19.5	20.1	20.7	21.3	21.6
85	23.3	23.6	24.3	25.0	25.7	26.4	27.2	27.9	28.7	29.5	30.4	31.2	31.7
100	34.2	34.6	35.5	36.5	37.5	38.5	39.5	40.6	41.7	42.8	43.9	45.1	45.7
105	38.7	39.2	40.2	41.3	42.4	43.5	44.6	45.8	47.0	48.2	49.5	50.8	51.5
115	48.9	49.5	50.7	52.0	53.4	54.7	56.0	57.5	59.0	60.5	62.0	63.6	64.4
125	61.5	62.1	63.6	65.1	66.7	68.3	69.9	71.7	73.4	75.2	77.0	79.0	79.9

Use the Maximum Static Current table (since this is a thermal power example)

- **VDD_INT = 1.10 V, T_J = 100 C**
- **IDDINT_DEEPSLEEP = 39.5 mA**

Calculate the IDDINT_CCLK_DYN Component

CCLK Dynamic Current per core(mA at ASF = 1.0), Typical Material

f_{CCLK}(MHz)	Voltage (V_{DDINT})												
	1.045	1.050	1.060	1.070	1.080	1.090	1.100	1.110	1.120	1.130	1.140	1.150	1.155
400	66.7	67.2	67.9	68.7	69.4	70.2	71.1	71.8	72.6	73.4	74.2	74.9	75.4
350	58.6	59.0	59.6	60.3	61.0	61.7	62.4	63.0	63.7	64.4	65.1	65.8	66.1
300	50.2	50.5	51.1	51.7	52.3	52.9	53.5	54.1	54.7	55.3	55.9	56.4	56.8
250	42.1	42.3	42.8	43.3	43.8	44.3	44.7	45.3	45.8	46.3	46.8	47.4	47.6
200	33.7	33.9	34.3	34.7	35.1	35.5	35.9	36.3	36.7	37.1	37.5	37.9	38.0
150	25.4	25.5	25.8	26.1	26.4	26.7	27.0	27.3	27.6	27.9	28.2	28.5	28.8
100	17.0	17.1	17.3	17.5	17.7	17.9	18.1	18.3	18.5	18.6	18.8	19.0	19.1

"Typ1" Testcase Represents an ASF = 1.0

VDD_INT = 1.10 V, f_{CCLK} = 400 MHz

ASF highly dependent on application. The core is running the typical2 instructions.

IDDINT_CCLK_DYN (mA) = (CCLK Dynamic Current per core) ·ASF

IDDINT_CCLK_DYN (mA) = 71.1 · (1.03) = 73.99 mA

Power Vector	Activity Scaling Factor
App1	0.79
App2	0.83
App3	0.78
High1	1.39
High2	1.54
High3	1.39
Idle1	0.05
Idle2	0.05
Nop1	0.56
Nop2	0.59
Typ1	1.00
Typ2	1.03
Typ3	1.01

Calculate IDDINT_SYSCLK_DYN, IDDINT_SCLK0_DYN, IDDINT_SCLK1_DYN, and IDDINT_DCLK_DYN

PLLCLK (MHz)	800
SYSCLK (MHz)	200
SCLK0 (MHz)	50
SCLK1 (MHz)	25
DCLK (MHz)	0

IDD_PLLCLK_DYN = 0.012 * VDDINT * PLLCLK_FREQ = 10.56 mA

IDD_SYSCLK_DYN = 0.120 * VDDINT * SYSCLK_FREQ = 26.40 mA

IDD_SCLK0_DYN = 0.110 * VDDINT * SCLK0_FREQ = 6.05 mA

IDD_SCLK1_DYN = 0.068 * VDDINT * SCLK1_FREQ = 1.87 mA

IDD_DCLK_DYN = 0.055 * VDDINT * DCLK_FREQ = 0 mA

Calculate IDDINT_DMA_DR_DYN

Peripheral	Frequency in Hz (f)	Number of Data Bits	Data Transfer Direction	Data Rate (MBPS)
8-bit PPI	27000000	8	L2 to Peripheral	25.75
SPORT0	4000000	2	L2 to Peripheral	0.95
SPORT1	4000000	2	L2 to Peripheral	0.95
UART	115000	1	L2 to Peripheral	0.01
MDMA1	5.00E+06	32	L2 to L2	19.07
Total Data Rate				**46.74**

Data Transfer Direction	Coefficient	Weight %
Peripheral to L1	0.025	0.00%
Peripheral to L2	0.017	0.00%
Peripheral to L3	0.017	0.00%
L1 to Peripheral	0.025	0.00%
L1 to L1	0.050	0.00%
L1 to L2	0.035	0.00%
L1 to L3	0.031	0.00%
L2 to Peripheral	0.026	59.20%
L2 to L1	0.046	0.00%
L2 to L2	0.035	40.80%
L2 to L3	0.032	0.00%
L3 to Peripheral	0.032	0.00%
L3 to L1	0.036	0.00%
L3 to L2	0.038	0.00%
Weighted Data Rate Coefficient	***0.0299***	

$$WeightedDRC = 0.026 \cdot \left(\frac{27.67}{46.74}\right) + 0.035 \cdot \left(\frac{19.07}{46.74}\right) = 0.0299$$

$$\text{IDDINT\_DMADR\_DYN (mA)} = 46.74 \cdot 1.10 \cdot 0.0299 = 1.54\ mA$$

IDD_INT Total & PDD_INT Calculation

IDD_PLL (mA)	10.56	
IDD_CCLK_DYN (mA)	72.99	
IDD_SYSCLK_DYN(mA)	26.40	
IDD_SCLK0_DYN(mA)	6.05	
IDD_SCLK1_DYN(mA)	1.87	
IDD_DCLK_DYN(mA)	0.00	
IDD_USBCLK_DYN(mA)	0.34	
IDD_DMA_DR_DYN(mA)	1.54	
IDD_DEEPSLEEP (mA)	39.48	
IDD_INT	159.22	mA

$$P_{DD\_INT} = IDD\_INT \times V_{DD\_INT}$$

$$P_{DD\_INT} = 159.22\ mA \times 1.1\ V$$

$$P_{DDINT} = \underline{175.14\ mW}$$

Calculating PDD_EXT

Peripheral	Freq (Hz)	# of Output Pins	C/pin (F)	Toggle ratio	Util	VDD_EXT (V)	Pout @ 3.30V (mW)
8-bit PPI	2.70E+07	9	3.00E-11	1	1	3.30	39.69
SPORT0	4.00E+06	2	3.00E-11	1	1	3.30	1.31
SPORT1	4.00E+06	2	3.00E-11	1	1	3.30	1.31
UART	1.15E+05	2	3.00E-11	1	0.25	3.30	0.01
Total Peripheral Power Dissipation @ 3.3V (estimated)						**PDD_EXT**	**42.32**

Total Power Consumption

- **PDD_TOT = ΣP_{DDn} where n = each V_{DD} domain**
- **For this example ADSP-BF70x application:**
  - PDD_TOT = PDD_INT + PDD_EXT + PDD_USB + PDD_OTP + PDD_HADC + PDD_RTC
  - PDD_TOT = 175.14 + 42.32 + 0.055 + 0.11 + 0.011 + 0.011
  - PDD_TOT = 217.7 mW

Questions?

- **E-mail processor.support@analog.com**