

PLL & PLLVCO Serial Programming Interface (SPI) Mode Selection Design Considerations

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Application Note

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Revision History

Revision	Date	Description
Rev 1.0	August, 2013	First release
Rev 2.0	September, 2013	Second release – added effect of floating SPI lines description
Rev 3.0	October 2013	Third release – changed startup sequencing

2 Introduction

This application note discusses best practices for use of the Serial Port Interface (SPI) Mode selection feature of Hittite's PLL and PLLVCO product lines. In this note, we will refer to them all, simply as the PLL/VCOs.

3 Applicable Products

This application note applies to the following products:

PLLs:

HMC703LP4E, HMC704LP4E

Narrowband & Triband RF PLLVCOs:

HMC820LP6CE, HMC821LP6CE, HMC822LP6CE, HMC824LP6CE, HMC826LP6CE, HMC828LP6CE, HMC831LP6CE, HMC836LP6CE, HMC837LP6CE, HMC838LP6CE, HMC839LP6CE, HMC840LP6CE

Wideband RF PLLVCOs:

HMC829LP6GE, HMC830LP6GE, HMC832LP6GE, HMC833LP6GE, HMC834LP6GE

Clock Generation:

HMC1032LP6GE, HMC1033LP6GE, HMC1034LP6GE

4 How does the Serial Interface (SPI) Mode Selection Work?

The PLL/VCO devices covered in this document support two different serial interface modes or protocols: Open Mode and HMC Mode.

The serial interface mode selection occurs after power-up and Power-On-Reset (POR) in the PLL/VCO. The PLL/VCO is reset and ready for mode selection after an internal Power-On-Reset occurs, automatically about 450usec after the PLL/VCO digital supply rises past half of its nominal value. The mode selection is then determined by the first occurrence of a rising edge on either the SCK (Open Mode) or SEN (HMC Mode) after the POR event.

Once the mode is selected on the initial bus transaction, the mode cannot be changed without powering down the power supply. Activity on the SPI lines prior to POR is ignored assuming both MPU and the PLL/VCO are powered up at the same time.

It should be noted that circuits with VCO subsystems, such as the RF PLLVCOs have a second POR circuit in the VCO subsystem on the VCC2 supply. The POR in the VCO subsystem does not affect mode selection but it does affect proper operation of the VCO and has certain conditions for minimum rise time, and maximum voltage on start up. It is typically recommended to be less than 1msec rise time and less than 150mV on startup. See the Hittite Application note ["RF PLL + VCO Power-Up & Brown-Out Design Considerations"](#) for details on power supply design and use with low noise regulators which may have slower rise times.

5 How to Reliably Select the Desired Serial Interface Mode

Reliable selection of the SPI mode is dependent upon the first bus transaction and the first arrival of SCK or SEN. The state of the SPI bus controller (referred to here as the “Controller” or the “MPU”) on power up determines the needed approach for startup.

A number of controller states on power up are possible. In general, the state of the controller on power up is unique to the controller type being used in the customer application, and to the power supply sequencing:

Possible controller states upon power up may include the following:

- a) Controller is guaranteed to start up with all outputs low.
- b) Controller is guaranteed to start up in tri-state mode.
- c) Controller has random SPI outputs for a short period of time after power up.
- d) Controller has random SPI outputs for a long period of time after power up.

Reliable configuration of the device in the desired serial interface mode requires the power-up sequence described in the following sections to be used.

5.1 Low State Start Up, Start Together

If the controller is guaranteed to start with logic lows on the SPI lines, then SPI Open mode selection and PCB wiring are as shown in Figure 1 and Figure 2 respectively.

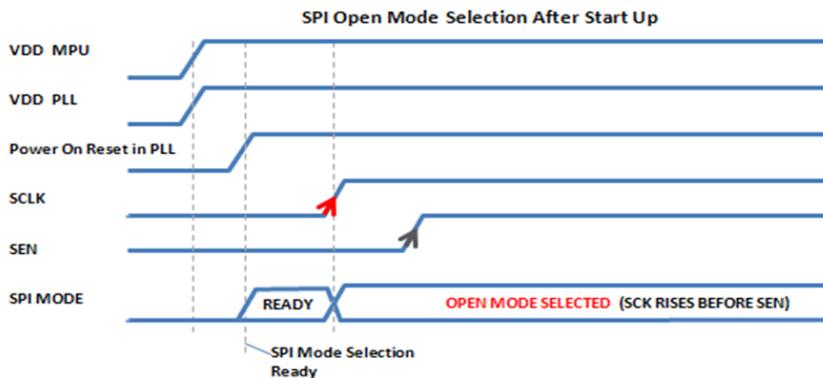


Figure 1 SPI Open Mode Selection, MPU Guaranteed Low on Start Up

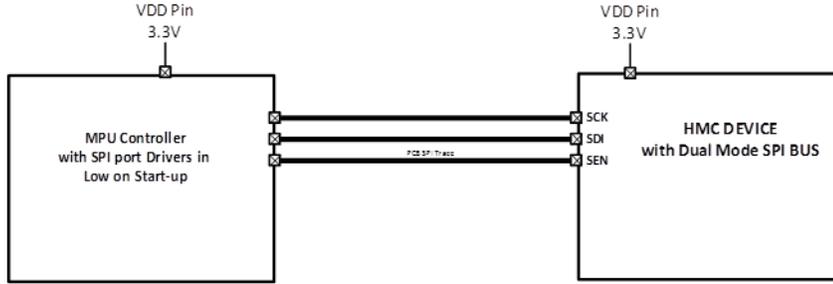


Figure 2 SPI Open Mode Selection, MPU Guaranteed Low on Start Up, No Pull Downs

SPI HMC Mode Selection timing is shown in Figure 3 and uses the same schematic of Figure 2.

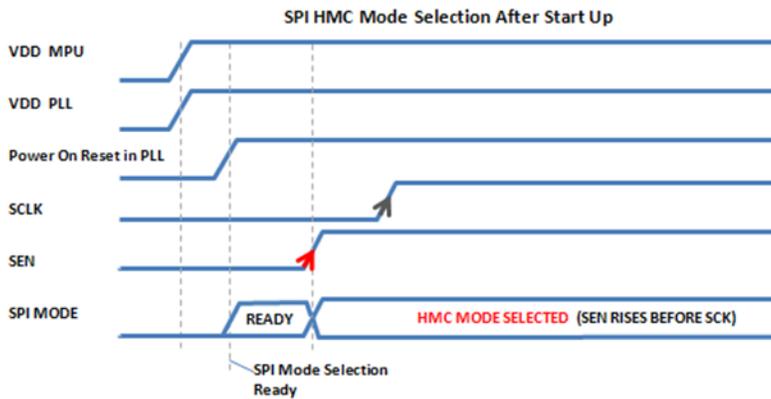


Figure 3 SPI HMC Mode Selection, MPU Guaranteed Low on Start Up

It is always possible that for some short duration glitches in state could happen on start up. For higher immunity to such events it is recommended to use pull down resistors as shown in Figure 5.

5.2 Tri-State Start-up, Use Pull Downs, Power Up together

If the MPU controller is guaranteed to start up in Tri-state mode, that is the tri-state controller does not drive the SPI lines on start up, and the outputs of the controller SPI lines are effectively open circuit, then the voltage on the SPI lines is not well controlled. In tri-state, input impedances are very high and stray charge can randomly change the input state high or low. Even very small changes in moisture or temperature can cause a floating input to change state randomly.

In such a case, stray charge or charge injection on the SPI lines during the start up transient could cause the lines to float high or low, and a false mode selection could happen. Such a condition is shown in Figure 4.

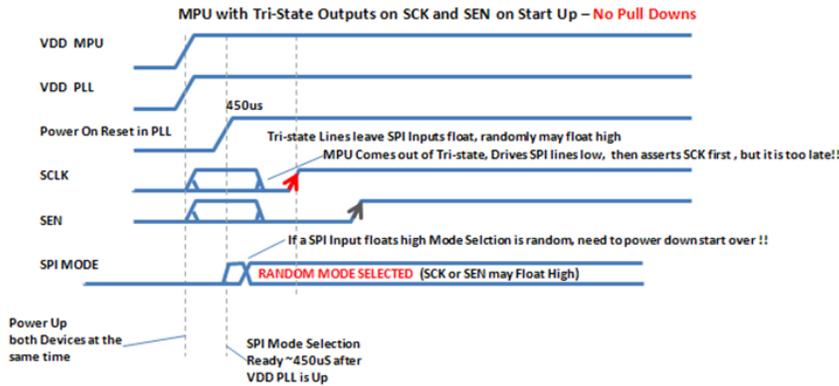


Figure 4 SPI Mode Selection Error Cause by Floating SPI Lines on Start-Up

The use of pull down resistors on the SPI lines avoids any erroneous SPI line toggling caused by small amounts of stray charge during start up. Both the controller and the PLL/VCO can be started together when tri-state is guaranteed. In such a case the PLL/VCO will reset about 450µs after the PLL/VCO supply reaches half voltage. The host should wait a minimum of a few msec after the reset before placing logic zero's on the SPI lines, and then following with the required SPI bus signal leading edge for mode selection.

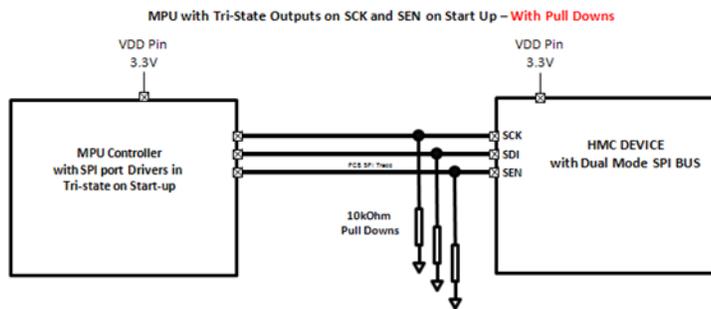


Figure 5 SPI Lines with Pull Downs Used with Tri-state Startup MPU

5.3 Short Uncontrolled MPU SPI Lines at Startup, Start PLL/VCO and MPU at Same Time

Customers should always power up the PLL/VCO at the same time as the MPU.

If the MPU controller is powered up prior to power up of the PLL/VCO, and the MPU controller output SPI lines have random states on power up, then the MPU outputs can actually bias up the PLL/VCO via the input pin ESD diode path to the digital supply. Such a condition can result in incorrect mode selection and can interfere with the proper operation of the Power On Reset circuit in the PLL/VCO.

This can be avoided by powering up the PLL/VCO at the same time as the MPU controller.

If the MPU controller has random outputs on the SPI bus for a short period of time after startup, prior to the Power On Reset (POR) in the PLL/VCO, and the MPU controller lines are stable after the POR event, then the PLL/VCO will ignore the uncontrolled bus activity prior to the POR event, and mode selection will occur as planned after the POR. Any high or low state is allowed on SCK or SEN after POR, only the first rising edge is used for the mode selection, as shown in Figure 6

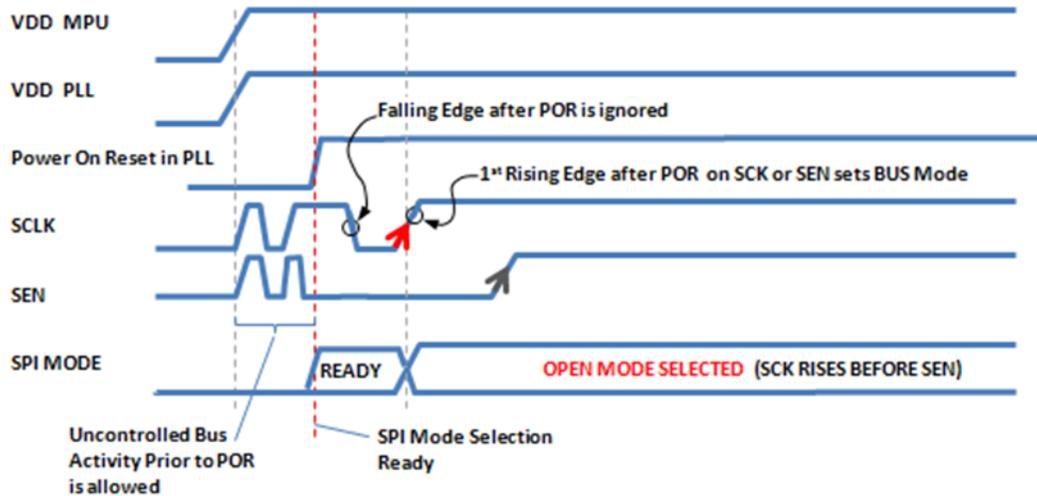


Figure 6 Uncontrolled SPI Bus Activity before POR is Ignored

The PLL/VCO will ignore toggles prior to the POR and will respond only to the first rising edge after the POR. POR occurs typically at 450 μ s after the PLL/VCO power supply reaches VDD/2. If the rise time of the PLL/VCO regulator is slow, POR may take longer. If the rise time of the PLL/VCO is extremely slow the POR may fail. See the Hittite Application note [“RF PLL + VCO Power-Up & Brown-Out Design Considerations”](#) for details on power supply design.

5.4 Long Uncontrolled MPU Outputs after Startup

If the MPU controller has uncontrolled states which may toggle randomly for longer than the POR 450 usec holdoff time +20%, then an incorrect SPI mode selection can result. The best solution is to use an MPU controller with better output control on startup, as discussed earlier.

If this is not possible, the PLL/VCO will need to be powered down after the MPU controller brings its outputs under control. Once this has happened the power supply to the PLL/VCO must be powered down, and kept off for a sufficient amount of time for the VDD supply to drop to below 150mV. If the power supply rise time to the PLL/VCO is very slow, for example longer than 1msec, then the start voltage should be discharged lower for a proper POR function.

A low start voltage is necessary on the digital supply to allow the POR reset to function properly when the chip is restarted.

If the VDD digital supply has a large decoupling cap on it, the time for the power supply to discharge to the 150mV level can be long. In cases where this is an issue a discharge resistor may be necessary on the digital supply to speed up the reset time.

If we use a simple RC charge model we can estimate the amount of time for the DVDD supply to discharge via a 3.3V DVDD to 150mV as $t = RC \cdot \ln(1 - 0.15/3.3) = 309\text{ms}$, where, for example, R is 10kOhm and C is 10 μF .

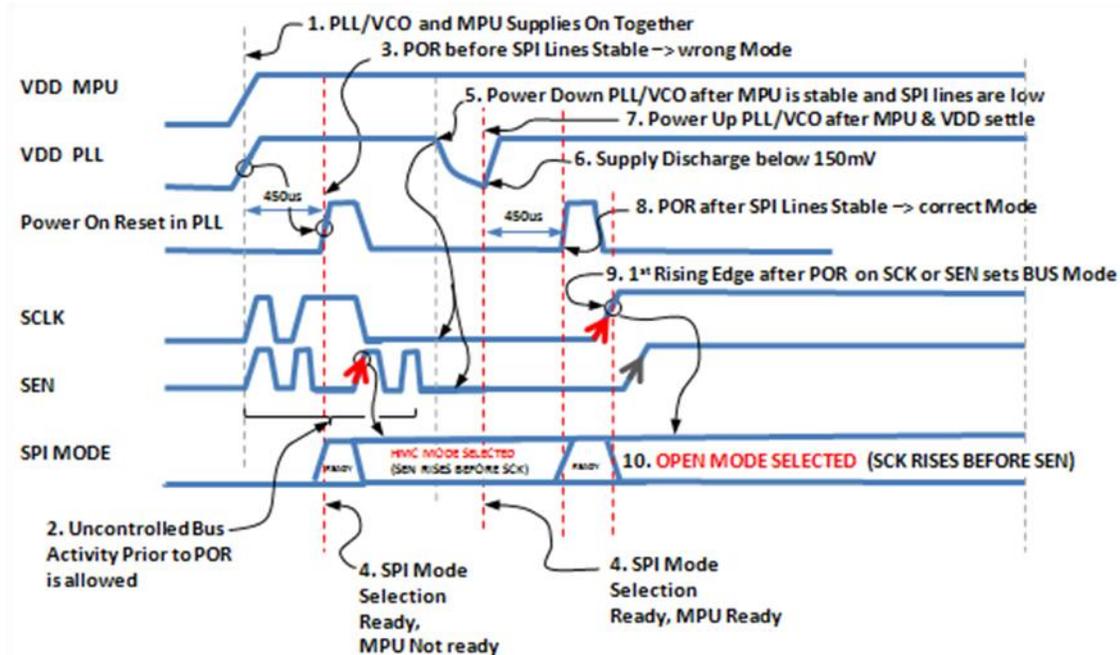


Figure 7 Mode Selection with Uncontrolled MPU on Startup

In summary the procedure to operate with a long uncontrolled MPU controller startup is shown in Figure 7 and is described as follows:

1. First power up both chips together.
2. Note the duration of the uncontrolled SPI line activity from the MPU controller
3. Wait for the PLL to reset, (min 450 μs)
4. Note the PLL is ready but the MPU is not ready, hence incorrect Mode selection occurs
5. Power down the PLL/VCO after the MPU lines settle and are brought low. NOTE: SPI lines must be low since the PLL/VCO is powered down and we wish to avoid charging the digital supply via the ESD diodes.
6. Wait for the PLL/VCO supply to settle to below 150mV See HMC App Note " RF PLL + VCO Power -Up & Brown-Out Design Considerations" for more details, may be longer with slow supply rise times).
7. Power up the PLL/VCO for a second time
8. Wait for the Power on Reset in the PLL/VCO (at least 450 μs). This resets the mode selection and the PLL/VCO is now ready to select the SPI mode.
9. Start the SPI communication in the desired mode, rising edge on SCK first for Open Mode or SEN first for HMC Mode.
10. SPI Mode is now set correctly and cannot be reset without removing the PLL/VCO power supply and repeating steps 5 through 9.

As a check, any write to a PLL/VCO register followed by a read back transaction will fail if the SPI mode is not the correct one.

We can see from Figure 7, in note 2, that if the MPU controller places a logic high on one of the SPI lines for an extended period of time then it is possible that the PLL/VCO could be partially powered up via the ESD diode between the SPI line input and the DVDD supply. This can also happen if the MPU controller is powered on before the PLL/VCO. The amount of charging via the SPI lines can be minimized by placing series resistors in the SPI lines as shown in Figure 8. Here, we see that the RC time constant for the DVDD power supply charging is set by the series resistor and the size of the decoupling cap on the DVDD supply. For example if a 10kOhm series resistor is used on the SPI lines and a 10 μ F decoupling cap is used on the digital supply DVDD, then the time constant to charge up the PLL via the SPI lines would be $RC = 10k \cdot 10\mu F = 100ms$.

We can observe from this simple example, that it is not strictly necessary to power up the PLL/VCO at the same time as the MPU, as shown in Figure 7, it is simply necessary to ensure that the start voltage on DVDD is below 150mV at the time that the MPU is ready with SPI lines stable.

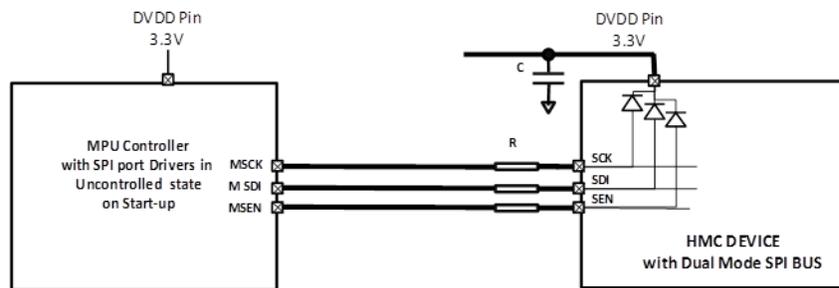


Figure 8 Reduced Impact from SPI Line Charging Uses Series Resistors on SPI Lines

Hence we could avoid the need to power the PLL/VCO up twice by using the above example 10kOhm series resistors, and 10 μ F DVD decoupling, if the SPI lines are stable in less than about 4msec. We should note that the series resistors do slow the maximum data rate possible on the SPI lines. If the effective input capacitance of the PLLVCO SPI lines is about 3pF, then the RC rise time of the SPI communication is about $10k \cdot 3pF = 30ns$. A safe clock speed would be about $1/10RC \sim 3.3MHz$ in this example.

6 How to Reliably Select Serial Interface Mode on Multi-PLL or PLL/VCO systems

In multi-device platforms that have more than one PLL or PLL/VCO device and the intended serial interface mode is HMC Mode, it is critical that all devices be configured for the serial interface mode prior to writing/reading to/from any device.

If this is not done, using a dedicated SEN#1 line the access to the device #1 will also apply a common SCK to all the other non-accessed devices. This will force the non-accessed devices to enter Open Mode unless these devices have had a rising SEN edge applied prior to SCK.

In multi-device platforms that have more than one PLL/VCO device and the intended serial interface mode is Open Mode, a write to any device will configure all devices for Open Mode because SCK is common to all devices, provided all SEN lines are held low until the first SCK edge occurs.

In summary the recommended procedure to configure devices on a multi-PLL/VCO bus, is to broadcast SEN and SCK to all devices on the first bus transaction. That will force all devices into the same mode. Subsequent transactions can then be done using unique SEN lines for each device.