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Evaluation Board for Fractional-N/Integer-N PLL Frequency Synthesizer

FEATURES

Self-contained board, including ADF4355-2 frequency synthesizer with integrated VCO, differential 122.88 MHz temperature controlled crystal oscillator (TCXO), loop filter (20 kHz), USB interface, and voltage regulators.
Windows-based software allows control of synthesizer functions from a PC
Externally powered by 6 Volts (V)

EVALUATION KIT CONTENTS

EV-ADF4355-2SD1Z
USB cable

REQUIRED ADDITIONAL EQUIPMENT

Windows®-based PC with USB port for evaluation software
SDP-S board (system demonstation platform, serial only)
Power supply (6 V)
Spectrum analyzer
50 Ω terminators

DOCUMENTS NEEDED

ADF4355-2 data sheet
EV-ADF4355-SD1Z user guide
UG-476 user guide

REQUIRED SOFTWARE

Analog Devices ADF4355-2 software, Version 0.46.1 or higher (available for download at www.analog.com/ADF4355-2)

GENERAL DESCRIPTION

The EV-ADF4355-2SD1Z evaluates the performance of the ADF4355-2 frequency synthesizer with integrated VCO for phase-locked loops (PLLs). A picture of the evaluation board is shown in Figure 1. The evaluation board contains the ADF4355-2 frequency synthesizer with integrated VCO, a differential 122.88MHz reference (TCXO), the loop filter, a USB interface, power supply connectors, and SMA connectors. A USB cable is included to connect the board to a PC USB port.

Windows-based software to allow easy programming of the synthesizer can be downloaded from www.analog.com/ADF4355-2.

This board requires an SDP-S (shown in Figure 1, but not supplied with the kit).

The SDP-S allows software programming of the EV-ADF4355-2 device

EVALUATION BOARD PHOTOGRAPH

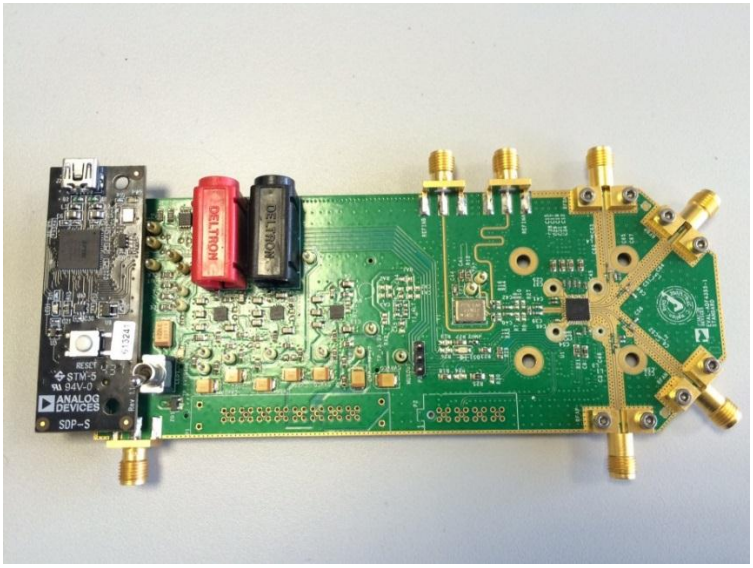

Figure 1. EV-ADF4355-2SD1Z

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REVISION HISTORY

21/11 —Revision PrF: Initial Preliminary Version

Edited evaluation setup.

19/11 —Revision PrE: Initial Preliminary Version

Edited figures and rearranged document format.

14/07—Revision PrD: Initial Preliminary Version

Edited description.

14/05—Revision PrC: Initial Preliminary Version

Updated screenshots.

13/08—Revision PrB: Initial Preliminary Version

Updated screenshots.

13/06—Revision PrA: Initial Preliminary Version

EVALUATION BOARD HARDWARE

The EV-ADF4355-2SD1Z requires the SPD-S platform which uses the EVAL-SDP-CS1Z**. (SDP-B is not recommended).**

The EV-ADF4355-2SD1Z schematics are shown in Figure 7, 8 and 9. The silkscreen for the evaluation board is shown in Figure 10 and Figure11.

POWER SUPPLIES

The board is powered by a 6 V power supply connected to the red and black banana connectors. Connect the red connector to a 6 V power supply and the black connector to ground.

The power supply circuitry allows the user to use two or three separate LDOs to feed the ADF4355-2 (using fewer LDOs increases the risk of spur contaminated dc feeds).

The charge pump and VCO supply pins are driven from a 5V ADM7150 high performance low noise regulator. The remaining supplies are powered from 3.3V ADM7150's.

LED1, indicates when the ADF4355-2 is powered on. Switch S1 is used to switch on/off the 6V power to the board.

RF OUTPUT

The EV-ADF4355-2SD1Z has two pairs of SMA output connectors (differential outputs RFAP/RFAN and RFBP/RFBN). The RF outputs are sensitive to impedance mismatch, and should be connected to equal load impedances. If only one port of a differential pair is used, the complementary port should be terminated with an equal load terminator (in general a 50Ω terminator).

LOOP FILTER

The loop filter schematic is included in the board schematic in Figure 7. The loop filter component placements are shown in Figure 2.

For lowest rms phase noise we recommend:

C60 = 1.2nF, C59 = 33nF, C14 = 390pF, C73 = 10pF.

R14 = 1kOhms, R17 = 3.3kOhm, with a charge pump current of 0.9 mA. Narrower loop filter bandwidths will have lower spurious signals.

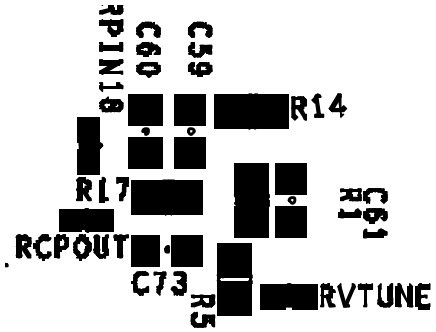

Figure 2. Loop Filter Placement

REFERENCE SOURCE

The evaluation board contains a 122.88 MHz differential output TCXO from Vectron. If preferred, the user may supply either a single-ended or differential reference input to SMA connectors REFINA and REFINB. When using an external reference, remove R12 to disconnect the power rail to the TCXO.

To use a single ended REFIN, connect a low noise 122.88 MHz reference source to SMA REFINB, and connect 50Ω terminator to SMA REFINA. To use a differential REFIN connect the differential signal to SMA REFINA and SMA REFINB. The differential REFINA/REFINB can operate to 500 MHz input frequency.

Note: In the schematic in Figure 7, the REFINA pin of U1 (ADF4355-2) is connected to SMA REFINB, and the REFINB pin of U1 (ADF4355-2) is connected to SMA REFINA. This schematic matches the evaluation board connections.

DEFAULT CONFIGURATION

All components necessary for LO generation are inserted on the board. This board is shipped with the ADF4355-2 synthesizer with integrated VCO, a differential 122.88 MHz reference TCXO, and a 20 kHz loop filter (I_{CP} = 0.9 milliamps).

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION PROCEDURES

The control software for the EV-ADF4355-2SD1Z is available at analog.com/ADF4355-2. For the software installation procedure, see UG-476.

EVALUATION BOARD SETUP PROCEDURES

To run the software,

1. Click the **ADF4355** file on the desktop or from the **Start** menu.
2. On the **Select Device and Connection** tab, choose **ADF4355-2** and **SDP board (black)**, and then click **Connect** (see Figure 3).
3. Note that when connecting the board; allow 5 sec to 10 sec for the status label to change.

Under the **File** menu, the current settings can be saved to, and loaded from a text file.

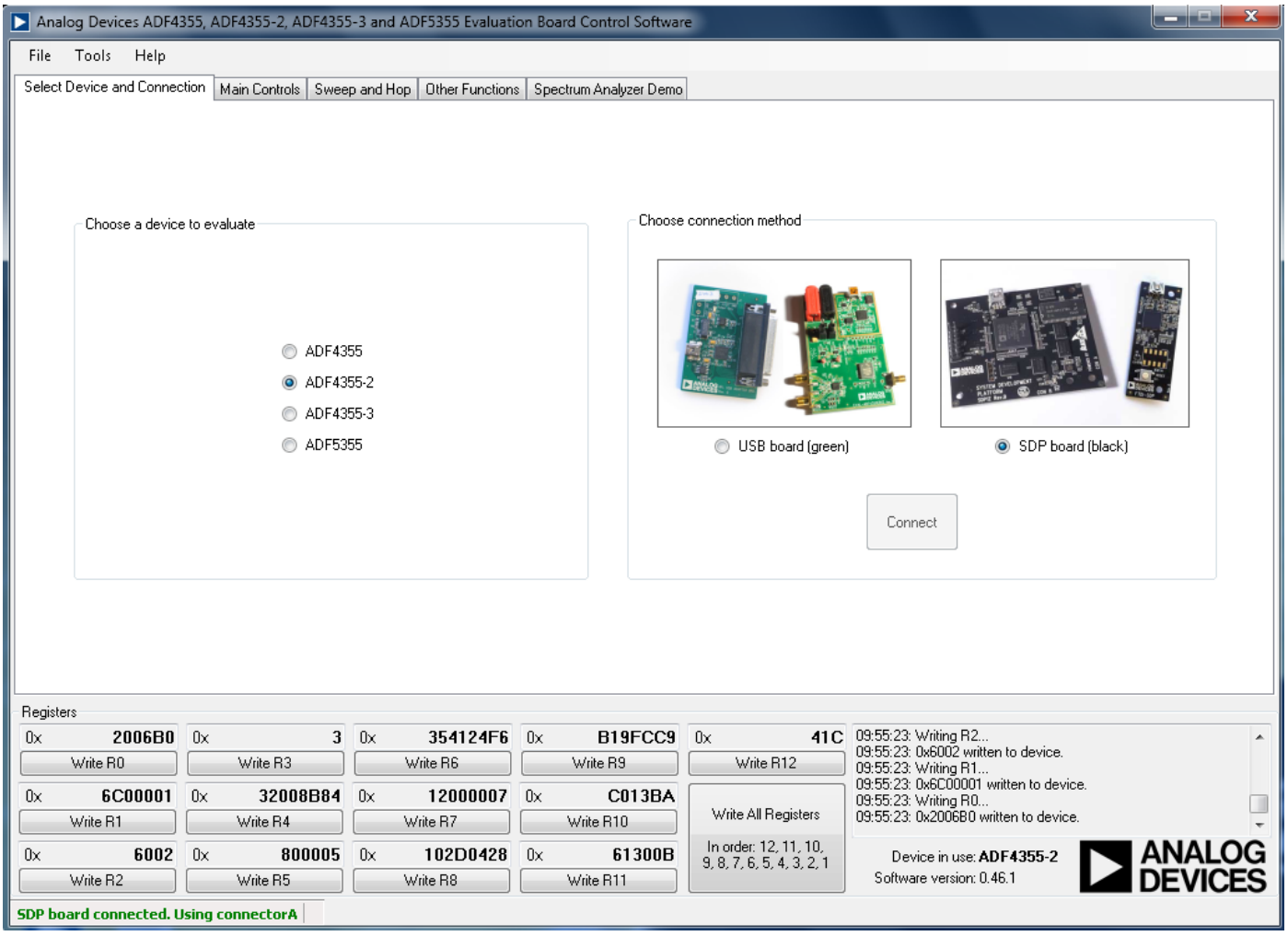

Figure 3. Software Front Panel Display—Select Device and Connection

MAIN CONTROLS

The **Main Controls** tab (see Figure 4) selects the RF and user configurable register settings. Consult the register description of the ADF4355-2 data sheet for details. Default settings are recommended for most registers.

In the **RF Settings**, the **VCOout(MHz)** should equal the VCO frequency. Set the **Output divider** to give the required **RFoutA+/-(MHz)**.

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Reference Freq should be the same as the applied reference signal. The PFD frequency is calculated from the reference frequency, the R-counter, the reference doubler, and the reference-divide-by-2. Ensure that the value in **PFD(MHz)** matches the value specified in the loop filter design.

In **Register 4**, program the **Charge pump current** to match the value used for the loop filter design

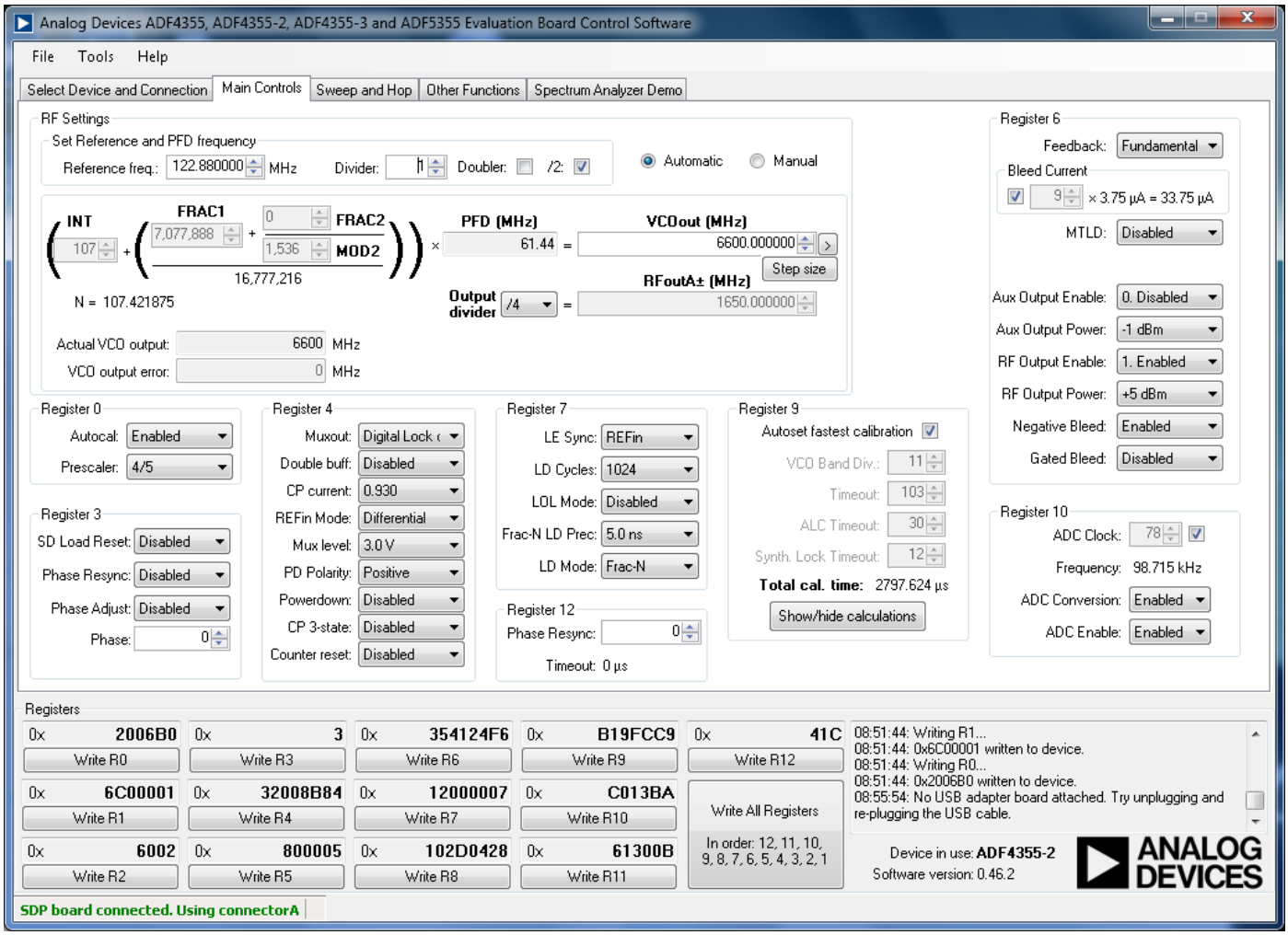


Figure 4. Software Front Panel Display—Main Controls

EVALUATION SET UP

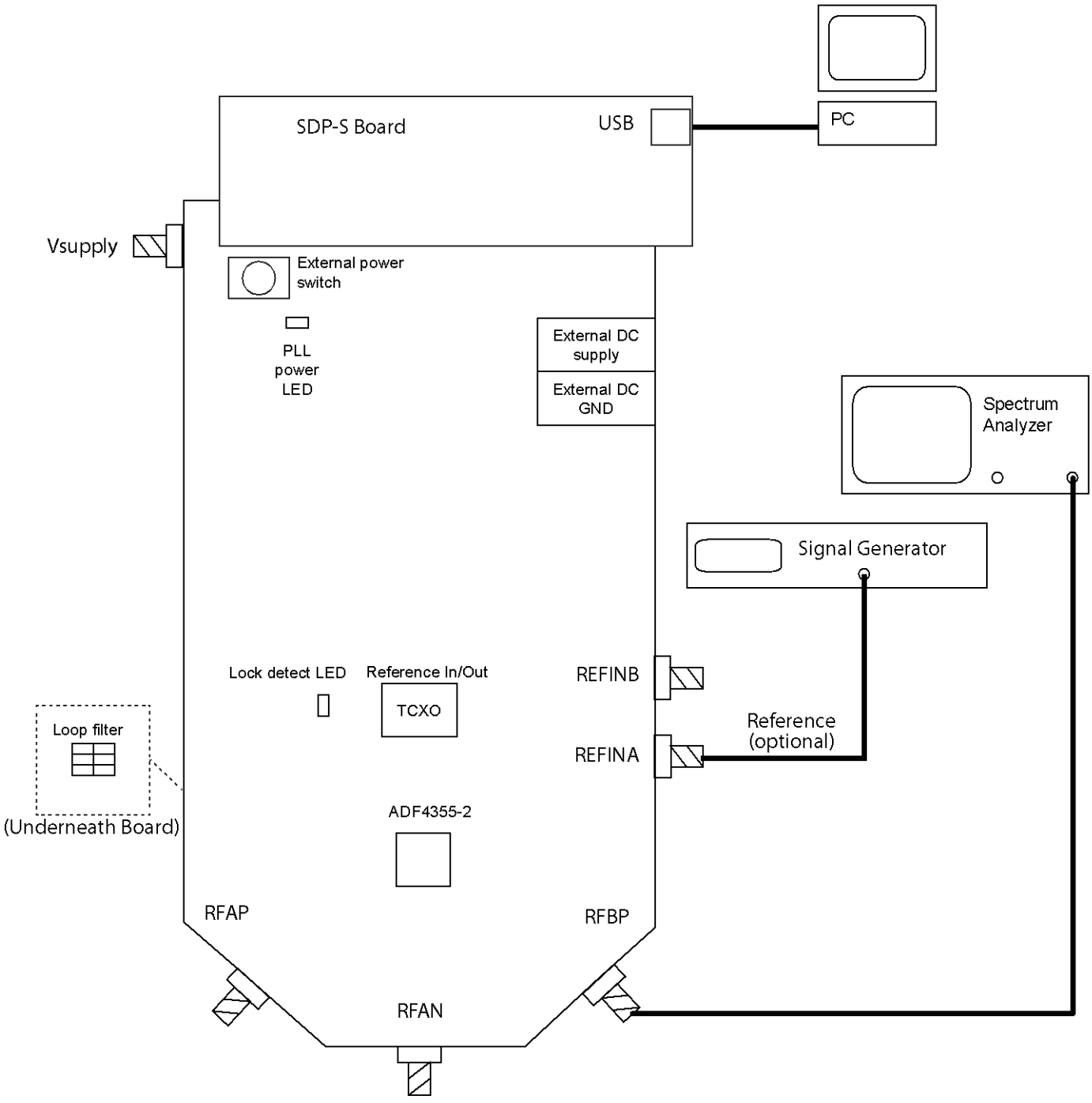


Figure 5. Evaluation SetUp Block Diagram

EVALUATION AND TEST

To evaluate and test the performance of the ADF4355-2, use the following procedure:

1. Install the ADF4355-2 software (see the UG-476 user guide).
2. Follow the hardware driver installation procedure (Windows XP only).
3. Connect a 50 Ω terminator to RFAN.
4. Connect the EV-ADF4355-2SD1Z board to the SDP-S board.
5. Connect the 6(V) power supply to the banana connectors and power-on the board using S1 (check that LED1 is on).
6. Connect the USB cable from the SDP-S board to the PC.
7. Run the ADF4355-2 software.
8. Select **SDP board (black)** and **ADF4355-2** in the **Select Device and Connection** tab of the software front panel display window.
9. Click the **Main Controls** tab, set the **VCOout(MHz) = 6600MHz** freq and the **Output divider** = 4 so that **RFoutA+/-(MHz)** =1.65GHz. Click **Write All Registers**.
10. Connect the spectrum analyzer to SMA connector RFAP, see Figure 5 for a typical evaluation setup.
11. Measure the output spectrum and single sideband phase noise.
12. Figure 6 shows a phase noise plot of the SMA RFAP = 1.65 GHz.

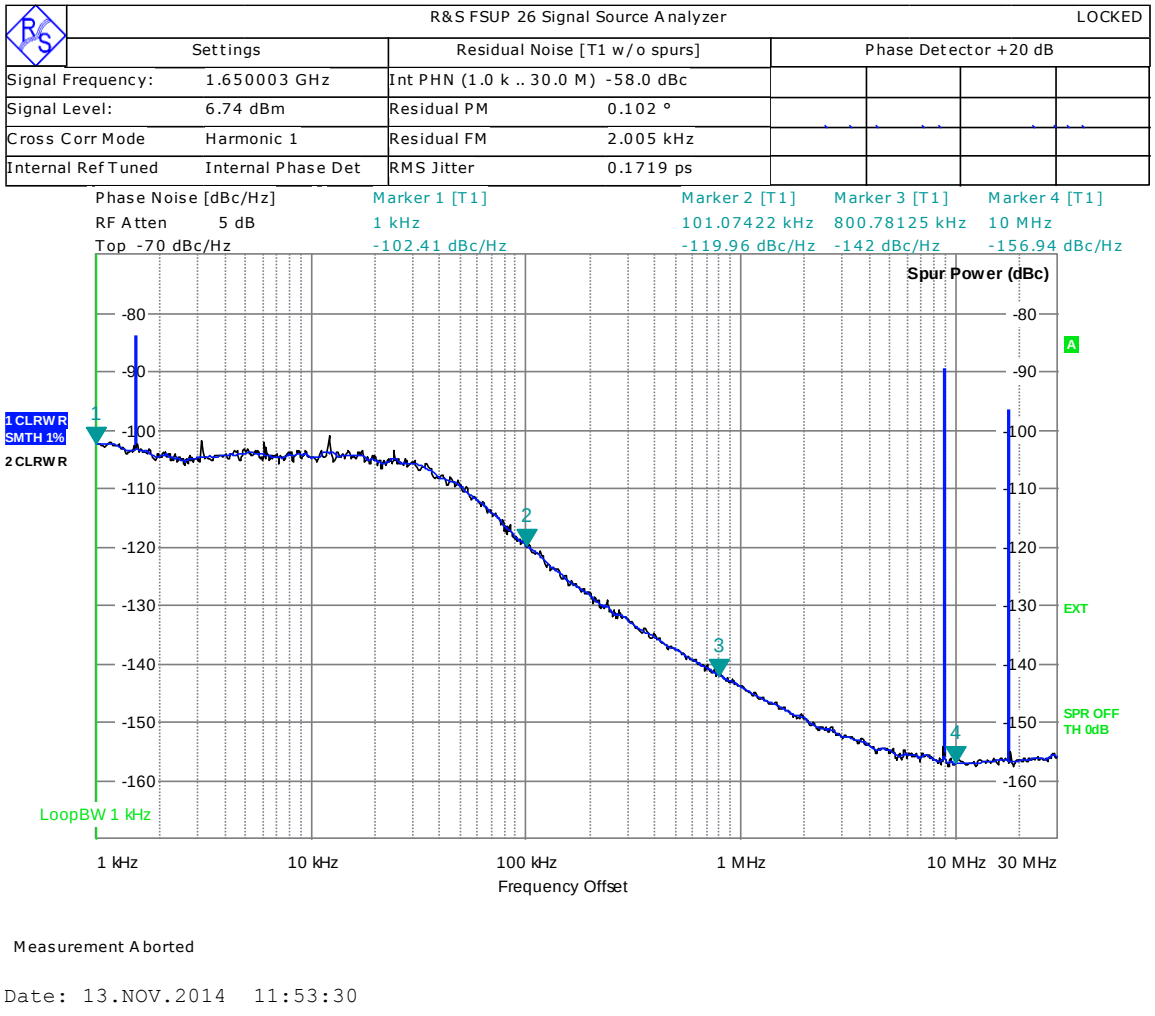


Figure 6. Single Sideband Plot

EVALUATION BOARD SCHEMATICS AND ARTWORK

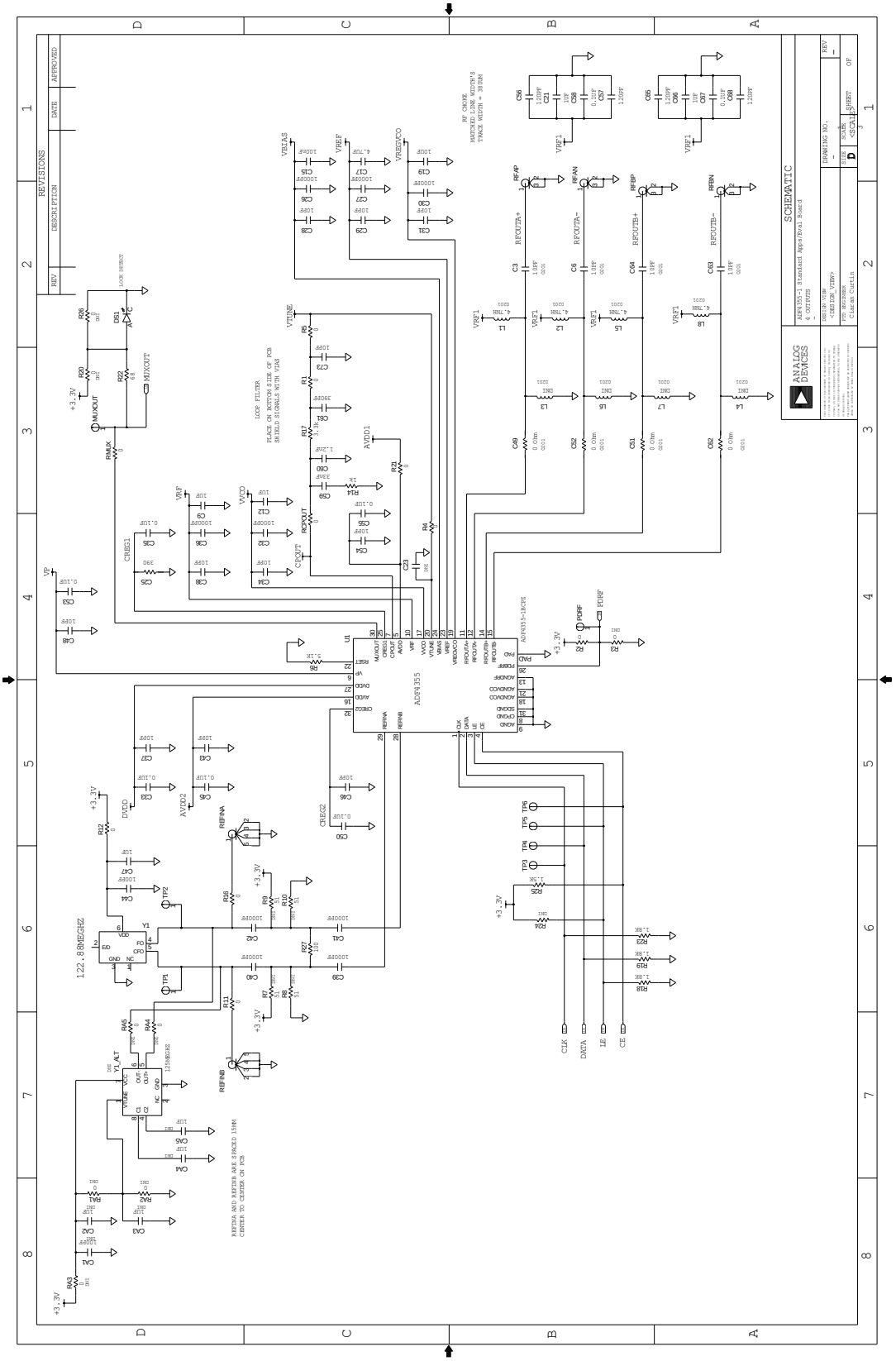


Figure 7. Evaluation Board Schematic (Page 1)

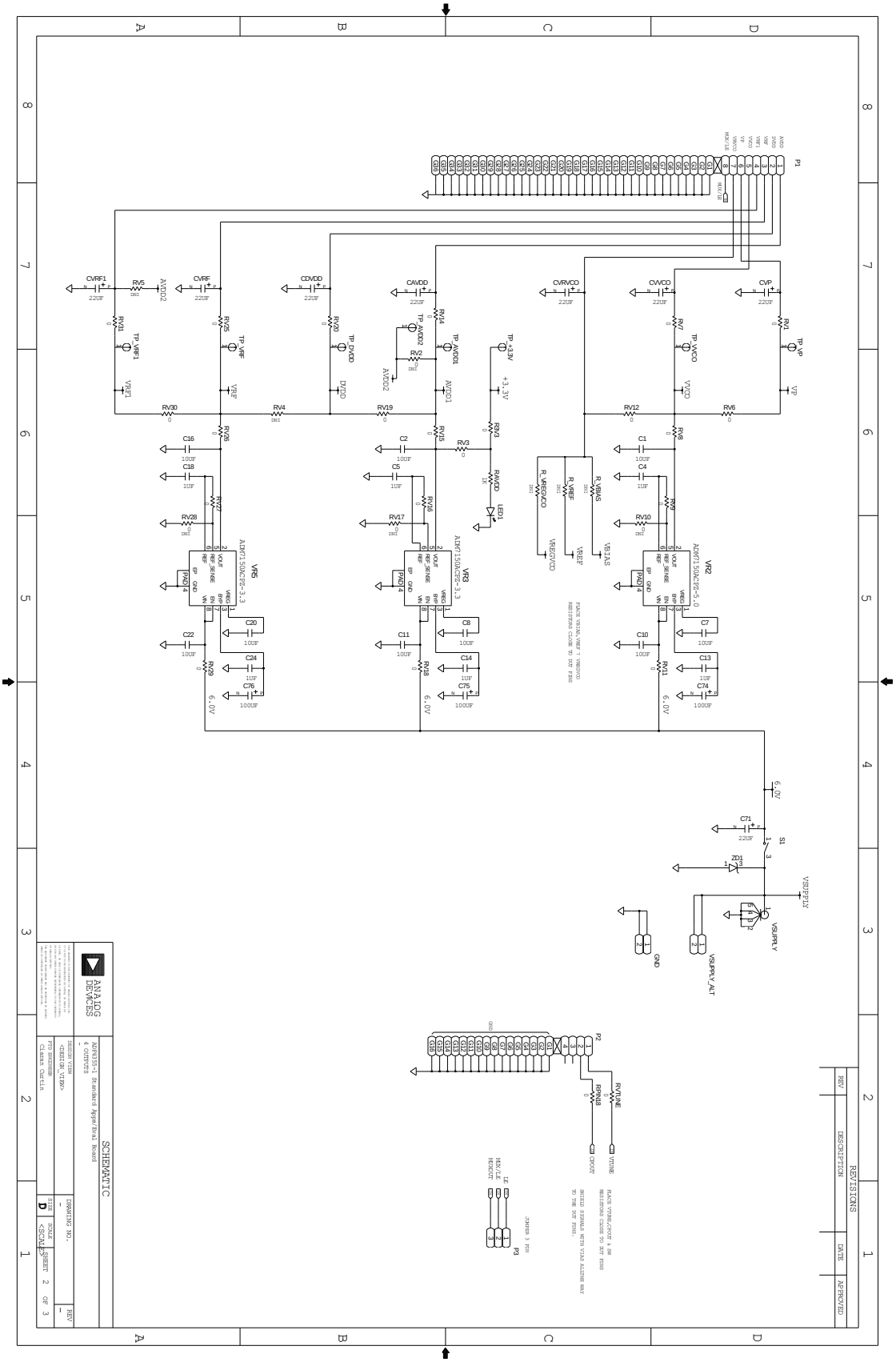


Figure 8. Evaluation Board Schematic (Page 2)

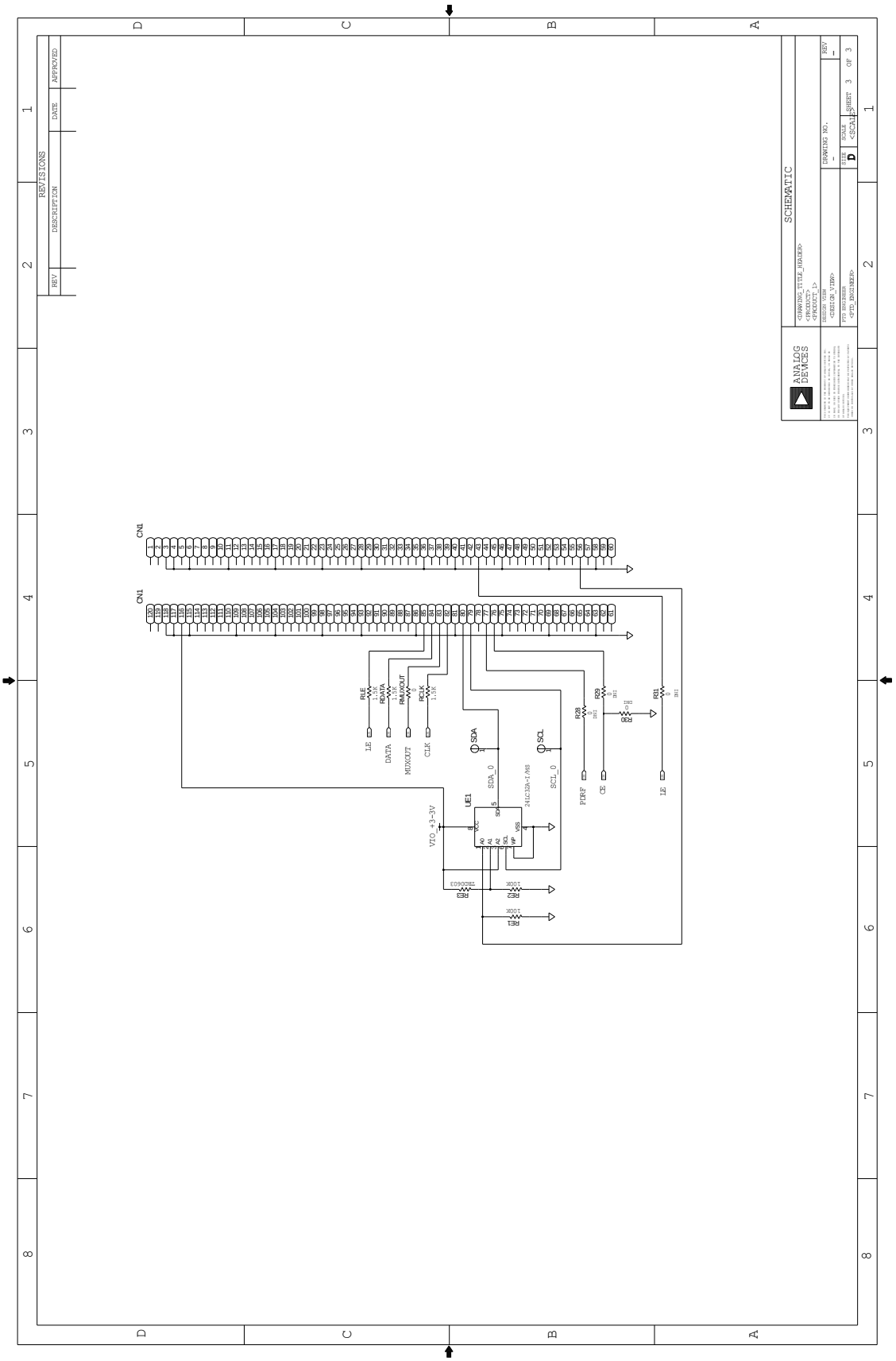
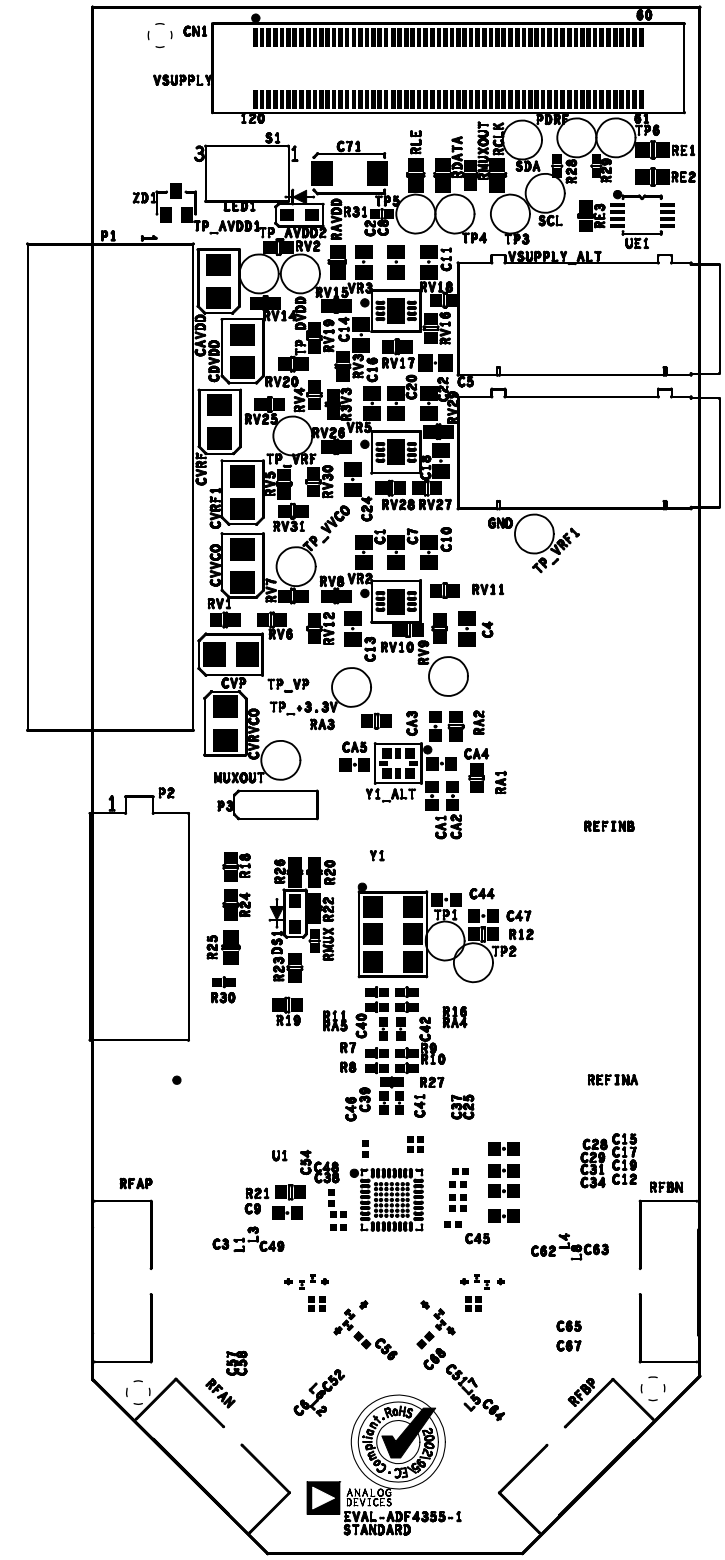


Figure 9. Evaluation Board Schematic (Page 3)



PRIMARY SIDE SILKSCREEN

Figure10. Evaluation Board Silk Screen(Top Side)

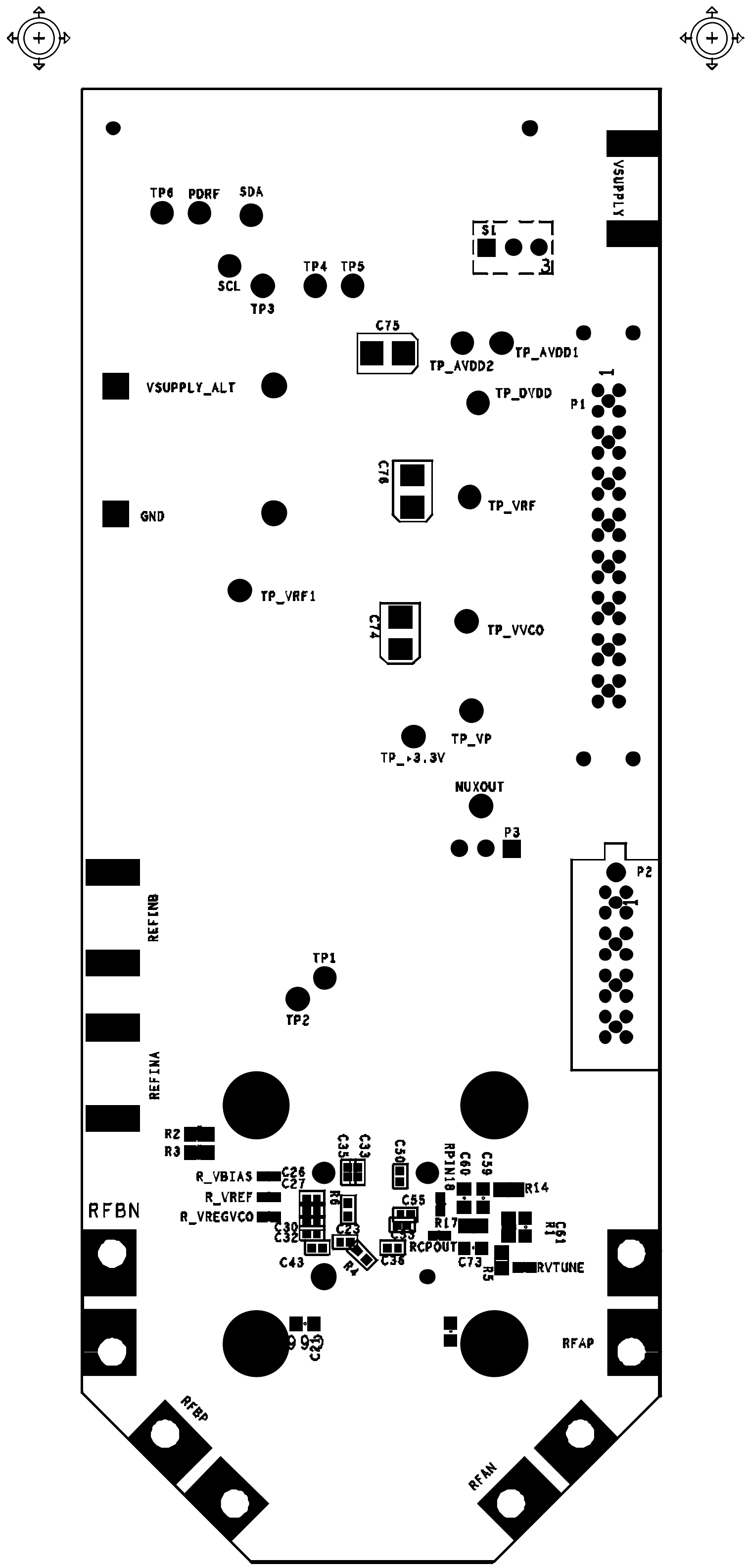


Figure11. Evaluation Board Silk Screen(Bottom Side)

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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