

## Applicable Products

HMC820LP6CE	HMC821LP6CE	HMC822LP6CE	HMC824LP6CE	HMC826LP6CE
HMC828LP6CE	HMC829LP6GE	HMC830LP6GE	HMC831LP6CE	HMC832LP6GE
HMC833LP6GE	HMC834LP6GE	HMC836LP6CE	HMC837LP6CE	HMC838LP6CE
HMC839LP6CE	HMC840LP6CE	HMC1032LP6GE	HMC1033LP6GE	HMC1034LP6GE
HMC1035LP6GE				

## 6 'Must-Knows' about using Hittite's PLL+VCO product family

Hittite's family of PLL+VCO products has, by far, the fewest and lowest level Fractional-N spurious tones and the best phase noise performance available for an integrated PLL and VCO product. No other integrated PLL and VCO product can approach their level of spectral performance.

When designing with these products it is important that the Designer take note of the following considerations:

1. Serial Programming Interface (SPI) Protocol Mode selection – introduced in this note with more details at:  
[https://www.hittite.com/content/documents/application\\_notes/SPI\\_Mode\\_Selection\\_Application\\_Note.pdf](https://www.hittite.com/content/documents/application_notes/SPI_Mode_Selection_Application_Note.pdf)
2. Charge Pump (CP) Offset Current configuration – discussed in this note and datasheet/Operating Guide;
3. Lock Detect (LD) configuration – discussed in this note and datasheet/Operating Guide;
4. VCO Register access protocol – discussed in this note and datasheet/Operating Guide;
5. Power-Up and Brown-Out considerations – discussed in separate note available at:  
[http://www.hittite.com/content/documents/application\\_notes/RF\\_PLL+VCO\\_Power-Up\\_&Brown-Out\\_Design.pdf](http://www.hittite.com/content/documents/application_notes/RF_PLL+VCO_Power-Up_&Brown-Out_Design.pdf)
6. Fast Settling Time considerations – discussed in separate note available at:  
[http://hittite.com/content/documents/application\\_notes/Fast\\_Frequency\\_Hopping\\_Application\\_Note.pdf](http://hittite.com/content/documents/application_notes/Fast_Frequency_Hopping_Application_Note.pdf)

What follows is a list of questions and answers that attempt to address operating concepts to supplement the existing datasheets and operating guides. The intent is to assist the customer to gain operating insight to avoid the most common prototyping obstacles.

## How to select the desired SPI mode?

All PLL+VCO devices have two SPI protocol modes, HMC Mode and Open Mode. Mode selection is determined by which signal edge occurs first after power-up, SEN or SCK. SEN (before SCK) selects HMC Mode. SCK (before SEN) selects Open Mode. For this reason, it is important that SPI signals are well controlled when the PLL+VCO device is being powered up.

To reliably configure the device for the desired serial interface mode it is important to following the recommendations in the Application Note →  
[https://www.hittite.com/content/documents/application\\_notes/SPI\\_Mode\\_Selection\\_Application\\_Note.pdf](https://www.hittite.com/content/documents/application_notes/SPI_Mode_Selection_Application_Note.pdf)

If the wrong serial interface mode is entered, the only way to recover is to remove power from the device and follow the above procedure again.

In multi-device platforms that have more than one PLL or PLL+VCO device and the intended serial interface mode is Hittite Mode, it is critical that all devices be configured for the serial interface mode prior to writing/reading to/from any device.

If this is not done, the access to the first device will also apply SCK to the other non-accessed devices. This will force the non-accessed devices to enter Open Mode unless these devices have had a rising SEN edge applied prior to SCK.

In multi-device platforms that have more than one PLL or PLL+VCO device and the intended serial interface mode is Open Mode, a write to any device will configure all devices for Open Mode because SCK is common to all devices, provided all SEN lines are held low until the first SCK edge occurs.

## How to determine which SPI Mode is active?

Although highly recommended, some customer applications do not implement SPI read capability. In addition, some customer applications cannot guarantee the required start-up conditions to ensure proper SPI Mode selection. A possible work around is to implement both HMC and Open SPI Modes and use the one that is active. Then the question is how to determine which SPI Mode is active. The procedure to determine the active SPI Mode is simple:

Program Reg0Fh = C0h: LD/SDO pin should go logic Low;  
Program Reg0FH = E0h: LD/SDO pin should go logic High;

If the output levels do not correspond to the expected level then either the device is in the other SPI mode or there is another issue with SPI communication. Attempt the same exercise with the other SPI mode to confirm communication.

## How to connect multiple PLL+VCO devices on one SPI bus?

All PLL+VCO's have two SPI protocol modes, described elsewhere in this document and the datasheets. In applications that connect multiple PLL+VCO devices on one SPI bus using Open SPI Mode there are several considerations that need to be addressed.

Open SPI Mode has a 3 bit Chip Address embedded in the serial data transfer. All devices on the SPI bus constantly monitor SDI. If an address match is observed, the data will be latched into the device when SEN transitions to high. Since all PLL+VCO devices have the same (non-user configurable) Chip Address = 000b, all devices will latch data when SEN goes high. As such, a separate SEN signal is required for each PLL+VCO device on the shared SPI bus.

In addition, when moving SPI access from one PLL+VCO device to another PLL+VCO device, a procedure needs to be executed to 'unmatch' the Chip Address in the first device to prevent a contention issue when the other device is accessed. Under normal circumstances all SPI write transfers are also SPI read transfers. Once a device has been accessed with a valid Chip Address after power-up, it activates the serial data output pin (SDO). Data comes out of SDO when data is being clocked into SDI. When a write has been completed to the first device and the microcontroller/FPGA has moved onto access the second device, SCK, being applied to all devices, causes data to come out of SDO of the first device. In order to prevent this, it is necessary to perform a 'dummy' write to the first device using a non-existent Chip Address to 'unmatch' the address. For example, writing Reg00h = 0h with Chip Address 111b tells the device that it is not being accessed so it disables its SDO pin. The access to the second device can now proceed without contention problems.

If HMC SPI Mode is used, the only requirement is to have a separate SEN signal for each device. Beware of the requirements to ensure the correct SPI Mode is selected for each of the devices, described elsewhere in this document.

### What is CP Offset Current? What does it do?

The purpose for using CP Offset current is to improve phase noise performance and reduce spurs when in Fractional Mode (Integer-N mode does not require the use of CP Offset current. CP Offset current should be zero for Integer-N mode).

A primary contributor to spurious signals in a Fractional-N synthesizer is PFD/CP non-linearity. Non-linearity is made more pronounced by the mis-match in the N and P devices in the Up and Down CP current sources. This non-linearity is especially problematic when both the Up and Down CP's are alternatively 'firing' to keep the PLL in lock (operating on both sides of the PFD zero-crossing). A non-linear CP degrades phase noise and increases spur levels. Reducing this non-linear behavior improves phase noise and spurious performance.

Now we need to understand what happens at the PFD in a Fractional-N PLL. The Delta-Sigma Modulator (DSM) dynamically switches the instantaneous VCO divider setting at the comparison frequency rate. In the case of a 50MHz comparison frequency, every 20ns the VCO divider is programmed to a different value. This is how the fractional divide capability works, by dividing by (for example) N, N-2, N+3, N-1.... The pattern is almost random and determined by the DSM. The maximum VCO divider excursion of Hittite Fractional PLL's is from N-4 to N+3 (where N is the integer divider setting). What effect does this have at the PFD? It means the arrival time of the divided VCO signal at the PFD input shifts in time anywhere from -4T<sub>vco</sub> to +3T<sub>vco</sub> periods.

For example, assuming a 50MHz comparison frequency and a 2GHz VCO, the divided VCO edge at the PFD input will vary every 20ns from -2ns (N-4, Down CP on), -1.5ns (N-3, Down CP on), -1ns (N-2, Down CP on), -0.5ns (N-1, Down CP on), 0 (N, Up or Down CP on), +0.5ns (N+1, Up CP on), +1ns (N+2, Up CP on), +1.5ns (N+3, Up CP on) relative to the reference edge at the PFD input. These large time excursions at the PFD straddle the PFD zero crossing giving rise to excessive non-linearity described earlier. The larger the excursions, the larger the effect of the non-linearity.

By sourcing or sinking 'extra' current at the CP pin (CP Offset current), it forces the operating point of the PFD to shift away from the zero crossing. The goal is to inject enough current so that only one side of the CP is pumping (Up or Down) so there are no zero crossings at the PFD. This means we need to time shift the arrival of the divided VCO edge by at least 4xT<sub>vco</sub>.

There are two CP Offset current sources, one between VDD and the CP pin (CP Up Offset) and one between CP pin and ground (CP Down Offset). These current sources have programmable current level. With zero CP Offset current, the divided VCO edge at the PFD and the reference edge at the PFD will

always occur very close to one another and there will be frequent zero crossings at the PFD. When we add CP Offset current, the operating point at the PFD will be shifted by an amount:

$$\text{Toffset} = [\text{Ioffset}/\text{Icp}] \times \text{Tpfd}$$

Toffset = time offset between reference edge and divided VCO edge at PFD input;  
Ioffset = programmed CP Offset Leakage current (uA);  
Icp = programmed CP current (uA);  
Tpfd = 1/comparison frequency;

Re-arranging:

$$\text{Ioffset} = [\text{Toffset}/\text{Tpfd}] \times \text{Icp}$$

or

$$\text{Ioffset} = [4 \times \text{Tvco}/\text{Tpfd}] \times \text{Icp}$$

or

$$\text{Ioffset} = 4 \times \text{Tvco} \times \text{Fpfd} \times \text{Icp}$$

Example: 50MHz comparison, 2GHz VCO, 2000uA CP current. The minimum required Ioffset would be given by:

$$\text{Ioffset} = 4 \times 0.5\text{ns} \times 50\text{E}6\text{Hz} \times 2000\text{uA}$$
$$\text{Ioffset} = 200\text{uA}$$

This is for the ideal perfect PLL. There are extra delays that need to be included so we use (adding 2.5ns):

$$\text{Ioffset} = (2.5\text{E}-9 + 4 \times \text{Tvco}) \times \text{Fpfd} \times \text{Icp}$$

This is the same expression presented in datasheets and operating guides.

Although very effective, this CP Offset Current technique does not completely eliminate spurious signals.

## **Are there CP Offset & Lock Detect (LD) issues to consider?**

CP Offset current is a critical feature to ensure good phase noise and spurious performance. If ill-configured, extremely poor performance can be expected. It is recommended to pay close attention to this configuration.

Details of how to set the proper level of CP Offset current are highlighted elsewhere in this document and in the respective datasheet or operating guide.

Optimum CP Offset current is determined by the following parameters:

1. Comparison frequency;
2. VCO frequency;
3. CP current;

It is not necessary to reconfigure the CP Offset current for each frequency programmed. Instead, perform the calculation using a mid-band frequency. For example, for a device offering a Fundamental VCO frequency range of 1.5GHz to 3GHz, use a VCO frequency of 2.2GHz for the CP Offset current calculation. This setting will be acceptable for all frequencies.

If either the comparison frequency or CP current parameters are changed by a large amount it is important to verify whether the CP Offset current setting needs modifying.

If the CP Offset current is set too high for the comparison frequency and CP current setting, the PLL will not lock. This is frequently observed by customers using the evaluation board, fitted with a 50MHz reference source who manage to get it working with R=1 (50MHz comparison frequency) but when they configure it for R=5 (10MHz comparison frequency), the PLL goes out of lock. All other things being equal, if the comparison frequency is reduced to 10MHz from 50MHz, then the CP Offset current should be reduced to 20% of its 50MHz value. Under no circumstances should the CP Offset current exceed 25% of the programmed CP current.

Although seemingly unrelated, the Lock Detect (LD) configuration is affected by the CP Offset current setting.

The LD circuit operates on the principal that if the device is 'in lock', the reference signal edge and the divided VCO signal edge will occur close to one another in time. The LD circuit generates a small 'timing window' within which the two signals must occur (the start of the timing window is triggered by either edge, reference or divided VCO, whichever occurs first). This 'in-window' event must occur multiple consecutive times before lock is declared. The 'timing window' size must be shorter than the comparison frequency period (Tpd) but long enough to accommodate phase jitter and other effects that cause phase offsets (such as the CP Offset Current setting and the Delta-Sigma Modulator induced jitter on the divided VCO signal).

The effect of the CP Offset current is to induce a fixed phase (time) offset at the Phase-Frequency Detector (PFD). This offset can be as large as 25% of the period, Tpd. The message is that optimum setting of the LD circuit is influenced by the CP Offset current setting. It is important to verify the correct setting.

Further details are found in the datasheet or operating guide documents.

## **Does CP Offset Current affect locking behavior of the PLL?**

Yes, in two ways. First, it has the effect of speeding up the slew time when the frequency hop is in the direction of the CP Offset current, and slowing the slew time when they are opposite. For example, a Down CP Offset current will reduce the slew time when hopping from a high frequency to a low frequency, but increase it when hopping from a low frequency to a high frequency.

In the case of the RF PLL+VCO devices, it is not simple to know from which direction the VCO will be coming because of the switched capacitor VCO architecture and VCO Auto-calibration feature which chooses the best VCO and VCO sub-band for the chosen frequency. When the VCO Auto-calibration finishes execution and relinquishes control of the VCO Vtune to the PLL's CP, the VCO frequency could be above or below the target frequency.

Second, at high comparison frequencies, when out of lock, the imbalance caused by the CP Offset current can prevent the PLL from locking. The following procedure must be followed for comparison frequencies  $\geq 80\text{MHz}$ :

- Disable CP Offset current;
- Execute frequency hop;
- Delay settling time of the PLL;
- Re-enable CP Offset current;

## What is the VCO Register access method?

The VCO sub-system in the PLL+VCO products possess digital control registers that set VCO states such as VCO enable/disable, VCO output enable/disable, VCO output divider setting, VCO output power level.

VCO sub-system registers are accessed using an indirect addressing technique. Data values written to PLL Reg05h are transferred to the specified VCO sub-system register by an internal SPI bus between the PLL sub-system and the VCO sub-system. This bus is unidirectional, only allowing writes to VCO sub-system registers.

Data words written to PLL Reg05h need to be properly assembled to include data bits (9 bits), address bits of the VCO sub-system register (4 bits) and Chip Address of the VCO sub-system (3 bits) totaling 16 bits in all. Transfers to PLL Reg05h need to have a full 24 bits of data so unused upper bits should be set to 0.

If using the built-in VCO Auto-calibration feature, it requires that the lower 7 bits of PLL Reg05h be in a specific state prior to execution (of the VCO Auto-calibration). If not, VCO Auto-calibration will fail. The lower 7 bits (Reg05h[6:0]) should be either '0000 000' or '0000 101' depending on the device (refer to the datasheet or operating guide). Writing PLL Reg05h=0h or 5h will meet this requirement, however, it will also force the VCO and VCO sub-band to 0 or 5 which will force the PLL out of lock if the device was operating on a different VCO setting. As such, configuring Reg05h[6:0] should be done immediately prior to a change in frequency.

It is possible to set the correct value of PLL Reg05h[6:0] without disturbing the VCO setting:

Read PLL Reg10h;

Program PLL Reg05h = 256 x [PLL Reg10h];

(PLL Reg10h provides the last VCO setting chosen by the VCO Auto-calibration)

Further details are found in the datasheet or operating guide documents.

## What is a “Switched Capacitor VCO”?

A “Switched Capacitor VCO” is a VCO that has a bank of capacitors that can be switched in/out of the tank circuit under digital control to effect a change in the nominal resonant frequency.

The benefit of this architecture is that the VCO can be made to have a wide frequency tuning range while maintaining low  $K_{vco}$  and low  $V_{tune}$ , both aids to improved phase noise.

All Hittite PLL+VCO products use this technique with 5 switched capacitors in the tank circuit (offering 32 VCO ‘sub-bands’). Some products have multiple VCO cores. Each VCO core has 32 sub-bands to cover the specified frequency range.

## How does the VCO Auto-calibration circuit function?

All PLL+VCO products have internal VCO’s with digitally controlled center frequency selection/adjust (“switched Capacitor VCO”). Five binary weighted capacitors can be switched in/out circuit allowing a wide VCO tuning range. For any programmed frequency, there will be a preferred VCO capacitor (also known as VCO ‘sub-band’) setting for optimal performance. This optimal capacitor setting is determined by a built-in internal VCO Auto-calibration state machine. Note that some products have multiple VCO cores. However, the VCO Auto-calibration state machine is similar whether one VCO core or multiple VCO cores are present.

When a new frequency is programmed (via Reg03h/Reg04h), VCO Auto-calibration runs. The calibration circuit momentarily forces a fixed voltage on Vtune (but not measurable on the Vtune pin) and, using a combination of frequency counting and successive approximation, switches through the VCO capacitor sub-band settings and identifies the best capacitor setting for the programmed frequency.

To perform the frequency count function, the VCO Divider circuit is dynamically re-configured during the VCO Auto-calibration run time. Once completed, the VCO Divider circuit is returned to its normal function of dividing the VCO signal, the fixed voltage is removed from Vtune and the normal PLL settling behavior completes as the charge pump takes control of the VCO.

The frequency count result is compared with a known expected value which is determined by the device configuration. PLL+VCO device configuration parameters that affect the VCO Auto-calibration result are:  
Reference Frequency applied to device;  
Reg02h Reference Divider Setting;  
Reg03h/Reg04h VCO (Integer & Fractional) Divider Setting;  
Reg0Ah VCO Auto-Calibration Configuration;

The state machine will remember the VCO sub-band setting that offered the closest frequency count to the expected value as it switches through the capacitor settings.

All these activities are automatically performed, not requiring any intervention by the microcontroller/FPGA.

Execution of the VCO Auto-calibration state machine takes a finite time which can be calculated. For a typical configuration using a 50MHz comparison frequency it executes in ~30 to 40us. During this period, it is critical that no writes to Reg05h occur. Writes to Reg05h, engage the internal PLL to VCO SPI which if already being used by the VCO Auto-calibration state machine, will result in an SPI bus contention issue.

A second, less critical timing requirement needs to be observed when writing to Reg05h with high speed SPI rates. Transfers to the VCO via the internal PLL to VCO SPI bus require 20 cycles of the (VCO Auto-calibration) state machine clock which is derived from the reference source and the setting of Reg0Ah[14:13]. This transfer time must be allowed to expire prior to a follow-on write to Reg05h.

For more details, refer to the PLL+VCO Operating Guide

→ [https://www.hittite.com/content/documents/operating\\_guide/pll\\_operating\\_guide\\_rf\\_vcocs.pdf](https://www.hittite.com/content/documents/operating_guide/pll_operating_guide_rf_vcocs.pdf)

## How to Powerdown PLL+VCO?

To fully power down these products, the VCO must be disabled first (by writing to the VCO via Reg05h) and then the PLL can be powered down (either from the CEN pin #23 or by writing SPI Reg01h[1]).

Since a write to the VCO via the SPI is required, it makes sense that the PLL's SPI Chip Enable feature be used (instead of the CEN pin #23 function).

To fully power down:

1. Reg01h[0]=0 (this is the default value for Reg01h, so this does not need to be programmed. However, it is included here to demonstrate how to configure the PLL's Chip Enable control to be from the SPI (Reg01h[0]=0) or via the CEN pin #23 (Reg01h[0]=1);
2. Write Reg05h = F08h (this disables the VCO); Write Reg01h[1]=0 (this disables the PLL assuming Reg01h[0]=0);

To re-enable the device;

1. Write Reg01h[1]=1 (to enable the PLL);
2. Write Reg05h =F88h (to enable the VCO);

Prior to the next frequency programming exercise (via Reg03h & Reg04h), the lower 7 bits of Reg05h must be programmed to 0 (otherwise the VCO Auto-calibration will not execute properly).

### How to disable PLL+VCO output but leave PLL locked (HMC829, HMC830, HMC833, HMC834, HMC1032, HMC1033, HMC1034 devices only)?

The VCO state is configured via Reg05h. A write to this register results in an internal transfer across a separate internal SPI bus between the PLL and the VCO.

Muting of the VCO Output Buffer is accomplished by writing:

Reg05h = E010h (VCO\_Reg02h[5:0]=0)

To enable the output the value written to Reg05h depends on the VCO Output Divider setting and the Output Power Level. Required values to be programmed into Reg05h for different VCO output divider values and output power levels are provided in the table below:

VCO Output Divide-by-	Max O/P Power	Next Lower O/P Power	Next Lower O/P Power	Lowest O/P Power
1	E090	C090	A090	8090
2	E110	C110	A110	8110
4	6210	4210	2210	210
6	6310	4310	2310	310
8	6410	4410	2410	410
10	6510	4510	2510	510
12	6610	4610	2610	610
14	6710	4710	2710	710
16	6810	4810	2810	810
18	6910	4910	2910	910
20	6A10	4A10	2A10	A10
22	6B10	4B10	2B10	B10
24	6C10	4C10	2C10	C10
26	6D10	4D10	2D10	D10
28	6E10	4E10	2E10	E10
30	6F10	4F10	2F10	F10
32	7010	5010	3010	1010
34	7110	5110	3110	1110
36	7210	5210	3210	1210
38	7310	5310	3310	1310
40	7410	5410	3410	1410
42	7510	5510	3510	1510

44	7610	5610	3610	1610
46	7710	5710	3710	1710
48	7810	5810	3810	1810
50	7910	5910	3910	1910
52	7A10	5A10	3A10	1A10
54	7B10	5B10	3B10	1B10
56	7C19	5C19	3C19	1C19
58	7D10	5D10	3D10	1D10
60	7E10	5E10	3E10	1E10
62	7F10	5F10	3F10	1F10

### **Do the PLL+VCO products support ‘Phase Coherent’ Frequency Hopping operation?**

Phase Coherent frequency hopping implies that a device, starting at frequency  $f_1$ , can be sent to a second frequency,  $f_2$ , then returned to frequency,  $f_1$ , exhibiting the exact same phase as if it never left original frequency,  $f_1$ .

This feature has been designed into the HMC835LP6GE, HMC1190LP6GE HMC1197LP7FE products.

However, other PLL+VCO products were not designed with this in mind, so they do not have the required hardware to offer this functionality.

### **How to measure settling time using Hittite’s evaluation software?**

Measurement of settling time can be complicated on these PLL+VCO products because two separate registers need to be programmed to effect a frequency change. The evaluation software exhibits a long delay (~1ms) between register writes which causes erroneous settling time measurements. However, the settling time can still be measured with the evaluation software in the following way:

1. Connect the E5052B’s (or other instrument) External Trigger Input to the SEN signal of the evaluation board and configure it to trigger with the external signal’s negative edge;
2. Program and initialize the PLL+VCO device and get it on frequency, say 2000.000MHz, Fractional mode with 50MHz comparison (standard eval board);
3. Open the ‘SPI Write/Read 1’ window (top left corner of the main software screen). Uncheck the ‘Auto Read Verify’ check box;
4. Write Reg04h = 0h. This will cause the VCO Auto-calibration to execute which will be followed by the normal PLL settling behavior. The E5052 will be triggered on the falling edge of SEN;

### **Why are N/C pins of the device connected on the evaluation board?**

Pins designated N/C in the datasheet are not connected inside the package. These N/C pins can be:

1. Connected to ground;
2. Floating;
3. Used to route signals to provide improved PCB routing (this is what has been done on the evaluation boards);