Configuring the ADV7181C for RGB with external CSync from a camera

Introduction

This document describes how to setup the ADV7181C to process properly a RGB signal from a camera with an external CSync signal.

Setup

The setup is described on the block diagram below:

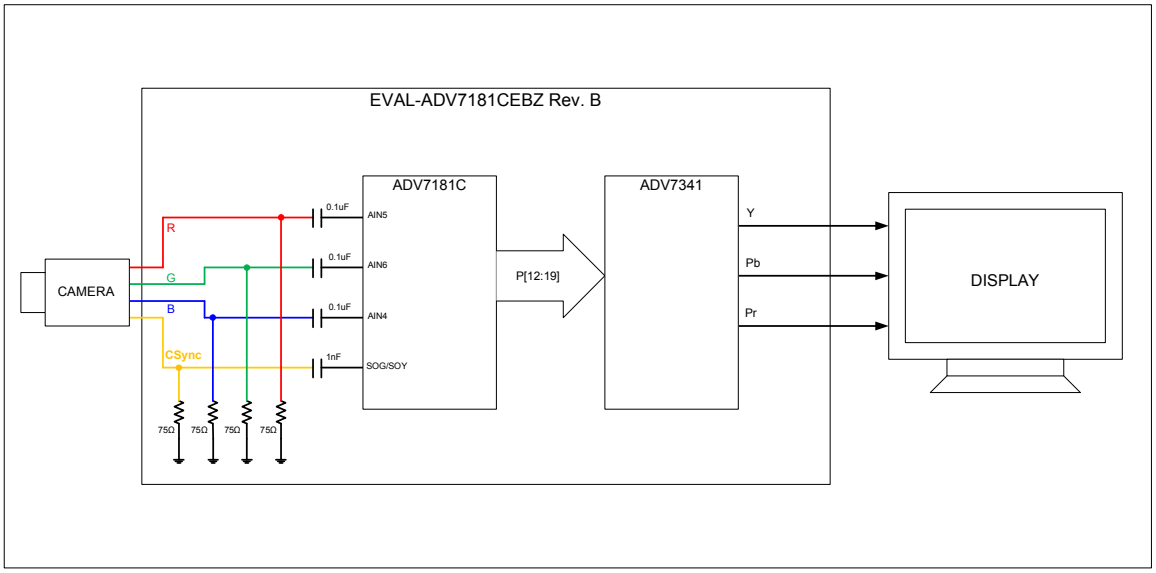

Figure 1: Block diagram of the setup

Please note that the evaluation board had to be modified for this configuration to be possible. Originally the capacitor before AIN6 was connected to the capacitor before SOG/SOY, allowing an embedded timing on Y or G to go to the SOG/SOY input pin. This connection between the two capacitors had to be broken, and a 75Ω termination resistor had to be added to allow an external CSync to go to the SOG/SOY input pin.

Script

The following script can be used to configure the ADV7181C and the ADV7341 for a 525i RGB signal from a camera with external CSync:

```
:525I RGB SOG/SOY In Manual AGC Manual Muxing 8Bit 422:
42 05 00 ; Prim_Mode =000b for SD-M
42 06 0E ; VID_STD=1110b for SD 2x1 525i
```

```
42 1D 47 ; Enable 28MHz Crystal
42 3A 11 ; Set Latch Clock 01b, Power Down ADC3
42 3B 81 ; Enable internal Bias
42 3C 52 ; PLL_QPUMP to 010b
42 C4 85 ; Manual Muxing - ADC2=AIN5(R)
42 C3 46 ; Manual Muxing - ADC0=AIN6(G), ADC1=AIN4(B)
42 52 00 ; Colour Space Conversion from RGB->YCrCb
42 53 00 ; CSC
42 54 12 ; CSC
42 55 90 ; CSC
42 56 38 ; CSC
42 57 69 ; CSC
42 58 48 ; CSC
42 59 08 ; CSC
42 5A 00 ; CSC
42 5B 75 ; CSC
42 5C 21 ; CSC
42 5D 00 ; CSC
42 5E 1A ; CSC
42 5F B8 ; CSC
42 60 08 ; CSC
42 61 00 ; CSC
42 62 20 ; CSC
42 63 03 ; CSC
42 64 D7 ; CSC
42 65 19 ; CSC
42 66 48 ; CSC last
42 67 13 ; DPP Filters
42 6B C3 ; Select 422 8 bit YPrPb out from CP
42 73 CF ; Enable Manual Gain and set CH_A gain
42 74 A3 ; Set CH_A and CH_B Gain - 0FAh
42 75 E8 ; Set CH_B and CH_C Gain
42 76 FA ; Set CH_C Gain
42 7B 06 ; clears the bits CP_DUP_AV and AV_Blank_EN
42 85 19 ; Turn off SSPD and force SOY. For Eval Board.
42 86 1B ; Enable stdi_line_count_mode
42 8F 77 ; FR_LL to 1820 & Enable 28.63MHz LLC
42 90 1C ; FR_LL to 1820
42 BF 06 ; Blue Screen Free Run Colour
42 C0 40 ; default color
42 C1 F0 ; default color
42 C2 80 ; Default color
42 C5 01 ; CP_CLAMP_AVG_FACTOR[1-0] = 00b
42 C9 0C ; Enable DDR Mode
42 F3 07 ; Enable Anti Alias Filters on ADC 0,1,2
42 0E 80 ; ADI Recommended Setting
42 52 46 ; ADI Recommended Setting
42 54 00 ; ADI Recommended Setting
42 F6 3B ; ADI Recommended Setting
42 0E 00 ; ADI Recommended Setting
56 17 02 ; Software Reset
56 00 FC ; Power up all DAcs and PLL
56 01 80 ; SD only mode, Data input on Y-bus
56 80 10 ; SSAF Luma filter enabled, NTSC mode
56 82 C9 ; Step control on, pixel data valid, pedestal on, PrPb SSAF on,CVBS/YC out.
56 84 06 ; RTCO/SFL Enable
```

```
56 88 00 ; 8 bit input enabled
56 87 20 ; Encoder PAL/NTSC auto-detect enabled
End
```

By default, the ADV7181C looks at the embedded sync information on the Y or G channel to determine the gain to be applied. As there is no embedded sync here, the gain must be fixed manually.

The CSC coefficients convert the RGB signal to YCbCr.

Please also note that manual muxing (registers 0xC3 and 0xC4) is enabled in this script. Therefore this script can be adapted to another input muxing configuration by changing the values written to those two registers.