ANALOG DEVICES

ADV7182 & ADV7280
Schematic Check List

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Rev. A

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Legal Terms and Conditions

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1. Introduction

This document is intended as design check list to assist with the design of ADV7182 and ADV7280 systems. This document should be used with the ADV7182 and ADV7280 datasheets and reference schematics.

Please refer to the hardware manual and datasheets for details on all blocks.

2. Check List

2.1 Control and Misc. pins

* Note these pins can operate at the logic level of the DVDDIO voltage supply. Therefore these pins can operate at a 3.3 Volt or 1.8 Volt logic level. Note that if the 1.8V logic level is used then the drive strength for digital outputs and I^2C input/ouptuts need to be set to maximum. See Global Pin Control section of the ADV7182 datasheet and ADV728x hardware manual.

Name	No.	Logic Level	I/O Mode	To Check	✓
SDATA	27	DVDDIO*	Digital Bi-directional	I^2C Data - Connect to CPU/System I2C bus. External pull-up required to DVDDIO for normal I2C operation (Typ: 4.7k ohm)	
SCL	28		Digital Input	I^2C Clock - Connect to CPU/System I2C bus. External pull-up required to DVDDIO for normal I^2C operation (Typ: 4.7k ohm)	
$\overline{\text{RESET}}$	25		Digital Input	Reset (Active Low) – Drive high (to DVDDIO) to take the device out of reset	
$\overline{\text{PWRDWN}}$	31		Digital Input	Powerdown (Active Low) – Drive high (to DVDDIO) to take the device out of powerdown mode.	
ALSB	26		Digital Input	Sets I^2C base address of the ADV7182/ADV7280 - Pull to DVDDIO or ground through a ≥4.7k ohm resistor. Low = Base address 0x40 High = Base address 0x42	
$\overline{\text{INTRQ}}$	24		Digital Output	Interrupt output – connect to downstream CPU/FPGA. Can be pulled to DVDDIO through a ≥4.7k ohm resistor, but this is optional. If not used this pin can be left unconnected.	

2.2 Analog Video Inputs

Name	No.	Logic Level	Description	To Check	✓
$A_{IN}1$	17	n/a	ANALOG Video INPUT	Analog Video Input- A resistor network and an 100 nF AC coupling capacitor are required. A different resistor network is needed for different analog video inputs. See TYPICAL CIRCUIT CONNECTION section of the ADV7182 and ADV7280 datasheets. If not used this pin can be left floating or connected directly to ground.	
$A_{IN}2$	18			Analog Video Input- A resistor network and an 100 nF AC coupling capacitor are required. A different resistor network is needed for different analog video inputs. See TYPICAL CIRCUIT CONNECTION section of the ADV7182 and ADV7280 datasheets. If not used this pin can be left floating or connected directly to ground.	
$A_{IN}3$	22			Analog Video Input- A resistor network and an 100 nF AC coupling capacitor are required. A different resistor network is needed for different analog video inputs. See TYPICAL CIRCUIT CONNECTION section of the ADV7182 and ADV7280 datasheets. If not used this pin can be left floating or connected directly to ground.	
$A_{IN}4$	23			Analog Video Input- A resistor network and an 100 nF AC coupling capacitor are required. A different resistor network is needed for different analog video inputs. See TYPICAL CIRCUIT CONNECTION section of the ADV7182 and ADV7280 datasheets. If not used this pin can be left floating or connected directly to ground.	

2.3 Digital Video Outputs

* Note these pins can operate at the logic level of the DVDDIO voltage supply. Therefore these pins can operate at a 3.3 Volt or 1.8 Volt logic level. Note that if the 1.8V logic level is used then the drive strength for digital outputs and I^2C input/ouptuts need to be set to maximum. See Global Pin Control section of the ADV7182 datasheet and ADV728x hardware manual.

Name	No.	Logic Level	I/O Mode	To Check	✓
P0	12	DVDDIO *	Digital Video Outputs	Digital video output – connect to downstream device. A 33Ω series resistor should be inserted close to the ADV7182/ADV7280.	
P1	11			Digital video output – connect to downstream device. A 33Ω series resistor should be inserted close to the ADV7182/ADV7280.	
P2	10			Digital video output – connect to downstream device. A 33Ω series resistor should be inserted close to the ADV7182/ADV7280.	
P3	9			Digital video output – connect to downstream device. A 33Ω series resistor should be inserted close to the ADV7182/ADV7280.	
P4	8			Digital video output – connect to downstream device. A 33Ω series resistor should be inserted close to the ADV7182/ADV7280.	
P5	7			Digital video output – connect to downstream device. A 33Ω series resistor should be inserted close to the ADV7182/ADV7280.	
P6	6			Digital video output – connect to downstream device. A 33Ω series resistor should be inserted close to the ADV7182/ADV7280.	
P7	5			Digital video output – connect to downstream device. A 33Ω series resistor should be inserted close to the ADV7182/ADV7280.	
LLC	32	DVDDIO*	Digital Output	27 MHz line locked clock – connect to downstream device. A 33Ω series resistor should be inserted close to the ADV7182/ADV7280.	
HS	30	DVDDIO*	Digital Output	Horizontal synchronization signal. A 33Ω series resistor should be inserted close to the ADV7182/ADV7280. This output can be connected to the downstream devices, however this output is optional. If not used this pin can be left floating.	
VS/SFL/FIELD/SFL	29	DVDDIO*	Digital Output	VS/SFL/FIELD/SFL synchronization signal. A 33Ω series resistor should be inserted close to the ADV7182/ADV7280. This output can be connected to the downstream devices, however this output is optional. If not used this pin can be left floating.	

2.4 Voltage Reference Pins

Name	No.	Logic Level	I/O Mode	To Check	✓
VREFP	19	1.8V	Output	Voltage Reference Outputs. A single 100 nF capacitor should be placed between the VREFP and VREFN pins. The 100 nF capacitor should be placed close to the ADV7182 or ADV7180. It should also be located on the same side of the PCB as the ADV7182 or ADV7280.	
VREFN	20	1.8V	Output		

2.5 Clock Pins

Name	No.	Logic Level	Description	To Check	✓
XTALP	14	1.8V	Outputs 1.8V to external crystal.	For Crystal Sources: This pin should be connected to the 1.8V 28.63636 MHz (+/- 50ppm) fundamental crystal. For Oscillator Sources: This pins should be left not connected. Note: The crystal/ oscillator should be located close to, and on the same side of the PCB, as the ADV7182 or ADV7280.	
XTALN	15	1.8V	Input for crystal or clock oscillator	For Crystal Sources: This pin should be connected to the a 1.8V 28.63636 MHz (+/- 50ppm) fundamental crystal. For Oscillator Sources: The output from the 1.8V 28.63636 MHz clock oscillator should be fed into this pin. Note1: The crystal/ oscillator should be located close to, and on the same side of the PCB, as the ADV7182 or ADV7280. Note2: An additional I^2C write is needed in order for the ADV7182 / ADV7280 to operate with a clock oscillator source instead of a crystal source. Write 0x04 to register 0x13 in the User Main Map.	

2.6 Power and Ground

Name	No.	Logic Level	Description	To Check	✓
AVDD	21	1.8V	Power	A 1.8V supply should be connected to the AVDD pin through a filter circuit and a decoupling circuit. Filter Circuit: The filter circuit should be placed close to the supply. The recommended filter circuit consists of these element in this order. • A parallel 220uF capacitor between the supply and ground, • A series ferrite bead, • And another parallel 33uF parallel capacitor to ground. Decoupling Circuit: The decoupling circuit should be placed close to the AVDD pin of the ADV7182/AVD7280. The recommended decoupling circuit consists of these elements in this order. • A parallel 100nF parallel capacitor between the supply and ground. • And another 10nF parallel capacitor between the supply and ground	
PVDD	16	1.8V	Power	A 1.8V supply should be connected to the PVDD pin through a filter circuit and a decoupling circuit. Filter Circuit: The filter circuit should be placed close to the supply. The recommended filter circuit consists of these element in this order. • A parallel 220uF capacitor between the supply and ground, • A series ferrite bead, • And another parallel 33uF parallel capacitor to ground. Decoupling Circuit: The decoupling circuit should be placed close to the PVDD pin of the ADV7182/AVD7280. The recommended decoupling circuit consists of these elements in this order. • A parallel 100nF parallel capacitor between the supply and ground. • And another 10nF parallel capacitor between the supply and ground	

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Name	No.	Logic Level	Description	To Check	✓
DVDD	3, 13	1.8V	Power	A 1.8V supply should be connected to the DVDD pins through a filter circuit and a decoupling circuit. Filter Circuit: The filter circuit should be placed close to the supply. The recommended filter circuit consists of these element in this order. • A parallel 220uF capacitor between the supply and ground, • A series ferrite bead, • And another parallel 33uF parallel capacitor to ground. Decoupling Circuit: Two decoupling circuits are required. One decoupling circuit should be placed close to each DVDD pin of the ADV7182/AVD7280. It is recommended that each decoupling circuit consists of these elements in this order. • A parallel 100nF parallel capacitor between the supply and ground. • And another 10nF parallel capacitor between the supply and ground	
DVDDIO	2	1.8V or 3.3V	Power	The DVDDIO can be set to 1.8V or 3.3V. The 3.3V or 1.8V supply should be connected to the DVDDIO pin after a filter circuit and a decoupling circuit. Filter Circuit: The filter circuit should be placed close to the supply. The recommended filter circuit consists of these element in this order. • A parallel 220uF capacitor between the supply and ground, • A series ferrite bead, • And another parallel 33uF parallel capacitor to ground. Decoupling Circuit: The decoupling circuit should be placed close to the DVDDIO pin of the ADV7182/AVD7280. The recommended decoupling circuit consists of these elements in this order. • A parallel 100nF parallel capacitor between the supply and ground. • And another 10nF parallel capacitor between the supply and ground	
DGND	1,4,		Ground	The DGND pins and the exposed back paddle should be connected together to a common ground plane.	
Exposed Back Paddle	Exposed Back Paddle		Ground	The DGND pins and the exposed back paddle should be connected together to a common ground plane.	