

ADV7850

Register Settings Recommendations

Revision 1.2

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INTRODUCTION

This document describes ADI register setting recommendations and adjustments for the ADV7850 product. This document must be used in conjunction with the latest Hardware Manual and Software Manual.

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REVISION HISTORY

3/13—Rev1.1 to Rev1.2

Updates to pages 1-3

Formatting updated throughout

Storing Internal EDID RAM Contents to SPI EEPROM section moved from section 4 to section 3.

03/12—Rev. 1.0 to Rev. 1.1

Updated section 3.1

Updated section 5.1.1

Added section 3.2.6

12/11—Rev. 1.0 – Initial Version

1 ADV7850 I2C ADDRESSES

The ADV7850 contains 16 I2C register maps which can be accessed through the main I2C port. In previous products all these maps were accessible all the time. In ADV7850 on initial power-up, the IO Map and the HDMI Tx Map are only accessible. To access the other maps, its I2C address should be programmed in the IO Map registers 0xE7 to 0xFE.

These writes are listed below with possible addresses. When referencing to an I2C Map in this document, the sample I2C address values are used throughout this document.

I²C Addresses

40 E7 5C	AUDIO CODEC I ² C address
40 EB A8	MEMORY I ² C address
40 EC A0	VFE I ² C address
40 F1 90	SDP I ² C address
40 F2 94	SDPIO I ² C address
40 F3 84	AVLINK I ² C address
40 F4 80	CEC I ² C address
40 F5 7C	INFOFRAME I ² C address
40 F8 4C	AFE I ² C address
40 F9 64	REPEATER I ² C address
40 FA 6C	EDID I ² C address
40 FB 68	HDMI I ² C address
40 FD 44	CP I ² C address
40 FE 48	VDP I ² C address

2 INITIAL I2C SETTINGS

ADI recommends that these register settings are programmed at initialization to configure the ADV7850 correctly. Subsequent HDMI or Analog settings should be set accordingly.

IO Map

40 E3 92	ADI recommended write
92 24 43	Clock delay adjust
40 E3 00	ADI recommended write

HDMI Map

68 71 05	EDID REG powered of System power
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HDMI Tx Map

B8 41 10	Power up Tx circuitry
B8 BA 70	Configures internal EDID EEPROM
B8 D0 44	Configures output voltage swing
B8 D1 3C	ADI Recommended write
B8 D3 07	ADI Recommended write
B8 D6 02	ADI Recommended write
B8 DB 0B	ADI recommended write
B8 E0 90	ADI Recommended write
B8 E1 FC	ADI Recommended write
B8 E3 D0	ADI Recommended write
B8 E8 F0	ADI Recommended write
B8 E9 1C	ADI Recommended write
B8 EA 85	Normal TMDS Polarity
B8 EC 7C	ADI Recommended write
B8 ED 40	HDMI Output Configuration
B8 EE 40	HDMI Output Configuration
B8 EF 41	HDMI Output Configuration
B8 F3 01	HDMI PLL Configuration
B8 F5 CC	HDMI PLL Configuration
B8 F6 08	HDMI PLL Configuration

3 HDMI RECEIVER REGISTER SETTINGS

3.1 INITIALIZATION SETTINGS FOR HDMI MODE

ADI recommends that these register settings are programmed to setup the ADV7850 correctly in HDMI mode.

IO Map

40 1F 10	HDMI Mux
----------	----------

HDMI Map

68 CB 01	ADI Recommended write
68 6C A2	HPA on automatic mode (user choice)
68 3D 10	TMDS PLL Configuration
68 3E 69	TMDS PLL Configuration
68 3F 46	TMDS PLL Configuration
68 4E FE	TMDS PLL Configuration
68 4F 08	TMDS PLL Configuration
68 02 0F	ALL BG Ports enabled
68 57 A3	TMDS PLL Configuration
68 58 04	TMDS PLL Configuration
68 6F 04	ADI Recommended write
68 75 04	TMDS PLL Configuration
68 83 F0	Enable Termination
68 85 10	Enable Automatic Equalizer

VFE Map

A0 BF 01	Complete CP bypass
----------	--------------------

AFE Map

4C C0 D2	Tri-state CP Core
4C C1 99	PLL power down
4C C2 81	PLL PFD power down
4C C3 80	Bypass video core (for mux mode at 300MHz)

Repeater Map

64 40 81	ADI Recommended write (HDCP 1.0)
64 74 0F	Enable all EDID (internal EDID)
64 7C 80	HPA control Filter

CP Map

44 6C 00	Disable analog clamping
----------	-------------------------

3.2 DYNAMIC SETTINGS FOR HDMI MODE

The following standard register settings are required for the best performance in HDMI mode.

3.2.1 Recommended Equalizer Settings

The ADV7850 contains a dynamic equalizer. This has been optimized for different cable lengths and characteristics; the following write is required for full optimization.

The following writes are required for inputs with a TMDS frequency of 27MHz or below

HDMI Map

68 97 00	Port A
68 93 03	Set Manual EQ value
68 5A 80	Load EQ value
68 97 01	Port B
68 93 03	Set Manual EQ value
68 5A 80	Load EQ value
68 97 02	Port C
68 93 03	Set Manual EQ value
68 5A 80	Load EQ value
68 97 03	Port D
68 93 03	Set Manual EQ value
68 5A 80	Load EQ value
68 85 11	Enable Manual EQ operation

The following writes are required for inputs with a TMDS frequency of 27MHz or below :

HDMI Map	
68 85 10	Enable Automatic EQ operation
68 9C 88	Set Manual Reacquire
68 9C C8	Initialize Reacquire
68 9C 08	Set back to automatic reacquire

The EQ will always carry out an automatically reacquire each time the TMDS frequency is unlocked/locked.

3.2.2 Internal EDID operation in power down mode

The ADV7850 supports EDID read capability even when the system supply is not connected powered up.

It is important that when using/or not using this feature that the ADV7850 is also switched to system supply after power up. The EDID regulator supplies should be switched to system supply even in analog modes.

HDMI Map	
68 71 05	EDID Circuitry powered from System power

In an application where external SPI EEPROM is not used, a 100nF capacitor to ground should be used on each of the regulator outputs Pin C8 and Pin D14.

3.2.3 HDMI Free-Run Operation

For best performance free-run operation in HDMI modes the following should be set.

- Set PRIM_MODE to the desired free-run standard (IO Map 0x01[3:0])
- Set VID_STD to the desired free-run standard (IO Map 0x00[4:0])
- Set VFREQ to desired free-run frequency (IO Map 0x01[6:4])
- Enable free-run based on primary mode and video standard (CP Map 0xC9[0])
- Enable HDMI Free-Run (CP Map 0xBF[0])

3.2.4 Supporting 3D 1080i 50/60Hz Side by Side Full

The following write must be used to support the 1080i 50/60Hz Side by Side Full 3D formats :

IO Map	
40 C1 2F	for 1080i 50/60Hz Side by Side Full 3D formats

3.2.5 Non Fast Switching Application

In a non HDMI fast-switching application, the following I2C writes can be carried out to optimise performance and reduce power consumption.

HDMI Map	
Register 0x00[7:5]	Set to 0x00 for non-fast switching applications

3.2.6 Audio Extraction at Frequencies up to 3 GHz

For Audio Extraction in Non-Mux mode, the following I2C writes should be added to the HDMI script. The Audio data will be output on HA_AP pins.

Audio Extraction at frequencies up to 3GHz

4C C0 C0	Tri-state CP
4C C1 98	PLL power down
4C C2 80	PLL PFD power down
4C C3 B0	Audio and Video

3.3 STORING INTERNAL EDID RAM CONTENTS TO SPI EEPROM

The following software writes are required in order to store the internal EDID RAM contents of the ADV7850 to an external SPI EEPROM.

- Set VGA_EDID_ENABLE = 0
- Set DISABLE_AUTO_EDID to 1

- Set STORE_EDID to 1 (Self Clearing Bit)

- Set VGA_EDID_ENABLE = 1
- Set DISABLE_AUTO_EDID to 0

The above controls are in the following locations:

- VGA_EDID_ENABLE : Repeater Map, Register 0x79, Bit [7]
- DISABLE_AUTO_EDID : Repeater Map, Register 0x77, Bit [5]
- STORE_EDID : Repeater Map, Register 0x7E, Bit [0]

4 COMPONENT PROCESSOR REGISTER SETTINGS

4.1 INITIALIZATION SETTINGS FOR DIGITIZER MODES

ADI recommends that the following register settings are programmed to setup the ADV7850 correctly when digitizing analog component inputs and analog graphics inputs. The following writes are required for the correct optimization of the ADC.

AFE Map

4C 00 01	ADC power Up (3 ADCs)
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For all component and graphics modes manual gain is recommended. The manual gain applied depends on the output quantization range. Based on the CEA-861 and HDMI 1.4 specification the recommended output quantization range is the “Limited Range”.

The recommend manual gain for both “Limited Range” and “Full Range” output quantization ranges are listed below. The values listed below are configured for the Analog Devices evaluation board. Depending on the user’s system these values should be adjusted to user preference.

The recommended manual gain settings when outputting data with the “Limited Range” quantization level are listed below.

CP Map

44 73 EA	Set manual gain of 0x2A8
44 74 8A	Set manual gain of 0x2A8
44 75 A2	Set manual gain of 0x2A8
44 76 A8	Set manual gain of 0x2A8

The following settings should be set on initialization depending on the type of input processed by the part.

Component Mode :

CP Map

44 C3 33	ADI recommended write
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Graphics Mode :

CP Map

44 C3 39	ADI recommended write
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4.2 DYNAMIC SETTINGS FOR DIGITIZER MODES

4.2.1 Sync Filter Clamp Adjustment

The clamp filter on the synchronization channels must be adjusted according to the input resolution:

- If the sync stripper 1 processes a Standard Definition (SD) input then SYNC1_FILTER_SEL [1:0] should be set to 0b11 to filter out pulses that are shorter than 2.5 us. The same applies to the sync stripper 2, i.e. if it processes a SD input then SYNC2_FILTER_SEL [1:0] should be set to 0b11.
- If the sync stripper 1 processes a High Definition (HD) input then SYNC1_FILTER_SEL [1:0] should be set to 0b01 to filter out pulses that are shorter than 250 ns. The same applies to the sync stripper 2, i.e. if it processes a HD input then SYNC2_FILTER_SEL [1:0] should be set to 0b01.

The synchronization stripper filter controls are in the following locations:

- SYNC1_FILTER_SEL[1:0] in AFE Map, Reg 0x15 [3:2]
- SYNC2_FILTER_SEL[1:0] in AFE Map, Reg 0x15 [1:0]

5 SDP REGISTER SETTINGS

5.1 INITIALIZATION SETTINGS FOR SDP MODE

5.1.1 Recommended Writes for All SDP Modes

ADI recommends that these register settings are programmed when the part runs in SDP mode.

External DDR2 Memory is required for correct SD operation

SDP_IO Map

94 04 10	Burst position adjustment
94 08 5A	Peak chroma adjustment
90 11 01	Peak white adjustment
94 97 00	Hsync width Adjustment

SDP Map

90 01 00	Pedestal Off
90 26 CF	CTI Adjustment
90 A7 00	ADI Recommended Write
90 D4 60	ADI Recommended write
90 D5 90	ADI recommended write
90 D7 44	ADI recommended write

VFE Map

A0 D8 00	DDS frequency adjustment
A0 D9 0A	DDS frequency adjustment
A0 DA AA	DDS frequency adjustment
A0 DB A0	DDS frequency adjustment
A0 DC 00	DDS frequency adjustment

Memory Map

A8 2B 08	DDR2 memory enabled
A8 08 D2	Tref clks 3.9us
A8 07 20	Tref clks 3.9us
A8 06 20	TRFC 133ns
A8 05 01	TRFC 133ns
A8 28 C0	Output enable for SDRAM clk pad and other output pads
A8 23 10	Enables Amplifier in charge pump of PLL
A8 24 01	Disable power down of PLL,DLL,bias generator & VCO in the PLL
A8 25 05	Use 5X clock and disable power down of PLL charge pump
A8 26 12	Timing Adjustment
A8 1E 43	Phase_sel look up table
A8 1F 02	Phase_sel look up table
A8 20 80	Phase_sel look up table
A8 21 C1	Phase_sel look up table
A8 27 03	Memory reference on

5.2 SDP DYNAMIC REGISTER SETTINGS**5.2.1 Memory Controller Initialization**

The memory controller must be initialized before use. The memory interface pins should be enabled prior to memory controller initialization and the memory controller must be reset once the appropriate initialization has been implemented. The memory controller is reset by setting MEM_RESET (IO Map, Reg 0xFF [2]) to 1. This bit is self-clearing.

5.2.2 CEA-861 Compliance

For 625i inputs on the ADV7850, it is recommended to set the following writes for CEA-861 compliance. These writes are not required in 525i modes.

SDP_IO Map	Writes required for 625i CEA-861 compliance
94 AA 05	Vsync vertical adjustment
94 B0 CC	Half-Line timing Adjustment

5.2.3 SDP Gain Settings for VCR Type Signals

The SDP automatically analyses the input signal and determines whether or not it is a VCR type signal. It is possible to configure the gain applied when the SDP core detects a VCR type signal to be determined automatically by the automatic gain control (AGC) feature or manually via a user defined gain.

The gain method is selected via SDP_MAN_GAIN_VCR, (SDP Map Register 0x03[5]).

When SDP_MAN_GAIN_VCR is set to 1 the luma gain applied is determined by SDP_Y_GAIN_MAN[12:0] (SDP MAP, 0x03[4:0], 0x04[7:0]) and the chroma gain is determined by SDP_C_GAIN_ACT_MAN[12:0] (SDP MAP, 0x05[4:0], 0x06[7:0]).

It is recommended to select the manual gain option for VCR type signals. The recommended gains for NTSC and PAL VCR type inputs are as follows.

NTSC :

SDP Map	
90 03 E4	Manual gain for VCR input, Manual Luma gain setting 0x40B
90 04 0B	Manual Luma gain setting 0x40B
90 05 C3	Manual Chroma gain setting 0x3FE
90 06 FE	Manual Chroma gain setting 0x3FE

PAL :

SDP Map	
90 03 E3	Manual gain for VCR input, Manual Luma gain setting 0x3E8
90 04 E8	Manual Luma gain setting 0x3E8
90 05 C4	Manual Chroma gain setting 0x4DC
90 06 11	Manual Chroma gain setting 0x4DC

Note : The gain value defined by SDP_Y_GAIN_MAN[12:0] is also used in manual gain mode for non-vcr type signals. However in general the AGC control should be used for standard signals.

5.2.4 DCM Configuration in SDP Modes

The ADV7850 contains decimation filters after the ADC block. These filters are used to filter the output after 2x or 4x sampling.

If 2x oversampling is used the following setting should be used :

VFE Map	
A0 21 80	DCM Manual Configuration
A0 22 2A	DCM Manual Configuration (2x1 modes)

If 4x oversampling is used the following setting should be used :

VFE Map	
A0 21 80	DCM Manual Configuration
A0 22 53	DCM Manual Configuration (4x1 modes)

5.2.5 CGMS Operation in SDP Modes

The following settings should be used if CGMS detection is required on the ADV7850

CGMS Detection

A0 0C 00	Power Up VDP
48 A5 90	CCAP Adjustment
48 A7 00	CCAP Threshold
48 25 06	Delay for TTX
48 F3 02	Detection Window Use
48 F5 F0	Window adjustment
48 C0 FF	Store data in FIFO
48 62 B5	Config for Slave Mode
48 F1 0A	Config for SPI
40 1E 7E	SPI configure
48 09 00	Adjust internal timing for CGMS
48 9C 34	Enable Content Based Update

6 AUDIO CODEC SETTINGS

6.1 POWER DOWN

If the Audio Codec is not used, the following writes should be carried out to minimize the current used by the ADV7850.

Audio Codec Unused

40 E7 5C	Audio Codec Address
5C 33 40	Audio Codec power down
5C 08 10	Audio Codec power down
5C 01 11	Audio Codec power down

LIST OF REGISTERS ACCESSED FOR ADI RECOMMENDED WRITES

This section lists all registers which are used throughout this documentation and for which no description is provided in the SW and/or the HW manuals. The registers listed in the following table should only be configured as per ADI recommendations.

Map	Location	Description
HDMI	0x0D	HDMI Fast Switching optimization
HDMI	0x44	HDMI Fast Switching optimization
HDMI	0x60	HDMI Fast Switching optimization
HDMI	0x57	TMDS PLL Optimization
HDMI	0x58	TMDS PLL Optimization
HDMI	0x67	TMDS PLL Optimization
HDMI	0x61	HDMI Fast Switching optimization
HDMI	0x6C	HDMI Fast Switching optimization
HDMI	0x85	HDMI equalizer setting
HDMI	0x99	HDMI equalizer setting
HDMI	0x9B	HDMI equalizer setting
HDMI	0x9D	HDMI equalizer setting
HDMI	0xC1	HDMI Power control block
HDMI	0xC2	HDMI Power control block
HDMI	0xC3	HDMI Power control block
HDMI	0xC4	HDMI Power control block
HDMI	0xC5	HDMI Power control block
HDMI	0xC6	HDMI Power control block
HDMI	0xFA	ARC transmitter circuitry
CP	0xC3	CP coast control
CP	0xC9	CP Free Run control
AFE	0x00	ADC powerdown controls
AFE	0x01	Analog front end power down controls
SDP	0xA7	FSC Coring filter
SDP	0xD4	Frame TBC Adjustment
SDP	0xD5	Frame TBC Adjustment
SDP	0xD7	Frame TBC Adjustment

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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