AD9981 to AD9984 design conversion considerations

The AD9984 is a pin-for-pin and software compatible upgrade to the AD9981. The AD9984 is capable of higher speeds (170MHz vs. 95MHz) and includes a new Auto Gain Matching feature. Below is a list of considerations to be aware of when converting an AD9981 design to the AD9984. None of these should require PCB or software changes.

1. The VD supply on the AD9984 is now 1.8V (vs. 3.3V on the AD9981). Changing the VD voltage regulator voltage should not require any PCB or software changes.
2. The common mode reference is no longer bonded out. So, pin 19 (REFCM) is now a no connect. The REFCM bypass capacitor is no longer needed. This difference does not require and PCB or software changes.
3. The high reference (REFHI) voltage is now 1.1V, and the low reference (REFLO) voltage is now 0.6V. This difference does not require and PCB or software changes.
4. The clamp voltages (as measured on the outside of the chip), have been changed. The mid-scale clamp voltage is now 1.0V and the ground clamp voltage is now 0.5V. This difference does not require any PCB or software changes.
5. The 50MHz clock output mode has been replaced with a ½ pixel clock mode. In most applications the 50MHz clock mode was not used, so this difference should not require any PCB or software changes.
6. Registers 2F through 3E have been added for test purposes and to control the Auto Gain Matching feature. Since AD9981 applications should not be writing to those registers, this difference requires no PCB or software changes unless the "Auto-Gain" function is to be implemented (software change only).
7. The output drive strength has been updated in order to achieve 170MHz single port data capability. This difference is described below and should not require any PCB or software changes.
8. The default for the new Auto Gain Matching feature is "off", so no PCB or software changes are required. To use the new Auto Gain Matching feature, refer to the section below.

Table 1: AD9984 vs. AD9981 output drive strength comparison (% compared to AD9981 recommended strength).

Register Setting	AD9981	AD9984
00	33%	57%
01	67%	78%
10 (recommended setting)	100%	112%
11	133%	112%

Auto Gain Matching

The AD9984 includes circuitry to match the gains between the three channels to within TBD% of each other. Matching the gains of each channel is necessary in order to achieve good color balance on a display. On products without this feature, gain matching is achieved by writing software which evaluates the output of each channel, calculates gain mismatches, then writes values to the gain registers of each channel to compensate. With the Auto Gain Matching function, this software routine is no longer needed.

To activate Auto Gain Matching, set register 0x3C, bit 2 to 1.

Auto Gain Matching has similar timing requirements to Auto Offset. It requires 16 data clock cycles to perform its function, starting immediately after the end of the clamp pulse. Unlike Auto Offset it does not require that these 16 clock cycles occur during the back porch reference time, although that is what is recommended. During Auto Gain Matching operation, the data outputs of the AD9984 are frozen (held at the value they had just prior to operation). The Auto Gain Matching function can be programmed to run continuously or on a one-time basis (see Auto Gain Matching Hold, register 2Ch, bit 3). In continuous mode, the update frequency can be programmed (register 1Bh, bits 4:3). Continuous operation with updates every 64 Hsyncs is recommended.