Application Note

Auto Graphics Mode for Non Supported Video Formats

1. Introduction

The purpose of this application note is to assist the user to configure the Component Processor (CP) core to process HD, PS, and graphics standards that are not supported by the primary mode and video standard controls. For example, it is possible to program the CP to support other SMPTE HD standards not directly supported using the video standard, such as WXGA, MAC 13 graphics formats, and formats that the CP can support if configured correctly.

In AD9388A/ADV7441A standard operation, the primary mode and video standard controls configure the CP core to process the most common HD, PS, SD, and RGB graphics formats. (To check which modes are supported, refer to the primary mode and video standard selection table in the AD9388A Datasheet Manual or in the ADV7441A Datasheet Manual.)

This application note provides a detailed description and a worked example of how to configure the CP to process non standard video formats.

2. Auto Graphics Mode Configuration

The following steps are performed to correctly configure the CP to process non standard video formats:

1. Enter auto graphics mode.
2. Set the VCO range and charge pump current.
3. Generate the pixel clock.
4. Configure the expected free run line length.
5. Set the expected number of free run lines per field.
6. Configure the interlaced or progressive parameter.
7. Manually adjust the output vertical and horizontal alignment if required.

2.1. Entering Auto Graphics Mode

To process a signal not supported automatically by the primary mode and video standard controls:

1. Program the primary mode to graphics: PRIM_MODE[5:0] = 0b0010
2. Program the video standard to auto graphics: VID_STD[3:0] = 0b00111

2.2. Setting the VCO Range and Charge Pump Current

The VCO range and PLL charge pump current settings can be either calculated automatically or programmed manually. Refer to the ADV7441A or AD9388A Datasheet Manual for details on programming these parameters.

2.3. Generating the Pixel Clock

The AD9388A/ADV7441A uses a PLL to synthesize a pixel clock (TLLC) from the incoming Hsyncs. For a non standard video format, the PLL can be configured manually to derive a pixel clock of any frequency. This is achieved by programming the PLL feedback divider block.

Firstly, PLL_DIV_MAN_EN is set to 1 to enable manual programming of the PLL block. Then, for a non standard mode, PLL_DIV_RATIO[11:0] is set to give the required pixel clock.

Secondly, one of two methods is used to calculate this value of PLL_DIV_RATIO[11:0]. Method one or method two is chosen, depending on the information available about the non standard format.

Equation 1 describes the first method, where the pixel clock frequency is divided by the incoming Hsync frequency. This equation describes the multiplying process of the PLL to generate a pixel clock from the incoming Hsyncs.

$$PLL\_DIV\_RATIO[11:0] = \left[\frac{\int_{pixelclock}}{\int_{Hsync}} \right]$$

Equation 1. Calculating PLL_DIV_RATIO[11:0]

The second method uses the rule that the PLL_DIV_RATIO[11:0] is always equal to the number of luma sample pixel periods per total line.

Note that because the PLL divide ratio is located in multiple registers, it cannot be updated in one I^2C register write. To avoid an instantaneous incorrect value, the circuit is designed so that the full 12 bits must be written to in sequence, one register after the other, with no interruption between the two writes.

2.4. Configuring the Free Run Mode Line Length

The expected line length for non standard formats must be programmed to the CP core. FR_LL[11:0] (free run line length) is the number of system clock cycles in the ideal line length of the video format.

Equation 2 shows that to calculate the FR_LL [11:0] manual parameter, the line period is divided by the system clock period. The numerator in this equation can be calculated either directly from the Hsync period or by using the total number of luma pixel periods per line multiplied by the pixel clock period.

Note that because the free run line length is located in multiple registers, it cannot be updated in one I^2C register write. To avoid an instantaneous incorrect value, the circuit is designed so that the full 12 bits must be written to in sequence, one register after the other, with no interruption between the two writes.

$$FR\_LL[11:0]\left[\frac{T_{line}}{T_{28.6363MHz}}\right]$$

Equation 2. Calculating FR_LL[11:0]

2.5. Setting the Free Run Mode Number of Lines per Field

The expected number of lines per field for non standard formats must be programmed to the CP core. The control LCOUNT_MAX[11:0] is used to set manually the number of lines per field and is programmed with the ideal number of lines per field for the required standard.

Note that because the number of lines per field is located in multiple registers, it cannot be updated in one I^2C register write. To avoid an instantaneous incorrect value, the circuit is designed so that the full 12 bits must be written to in sequence, one register after the other, with no interruption between the two writes

2.6. Configuring the Interlaced or Progressive Parameter

The expected interlaced or progressive configuration must be programmed to the CP core for non standard formats. For progressive modes, the INTERLACED bit (User Map, Address 0x91, [6]) is set to 0b.

For interlaced modes, the INTERLACED bit is set to 1. ADI recommends setting the User Map, register 0xB7 to17 for correct operation in interlaced modes.

2.7. Adjusting the Vertical or Horizontal Alignment

When programming the CP core for a non supported standard, it is possible that the horizontal and vertical alignment of the output video are not aligned as required. If AV codes are required, it is possible to adjust manually the output vertical and horizontal alignment as follows:

- Adjust the horizontal position and width by varying the values in DE_H_START[9:0] and DE_H_END[9:0]
- Adjust the vertical position and height by varying the values in DE_V_START[3:0] and DE_V_END[3:0]
- Adjust the VBI start and end position by varying the values in CP_START_VBI[11:0] and CP_END_VBI[11:0] (and CP_START_VBI_EVEN[11:0] **and** CP_END_VBI_EVEN[11:0] for interlaced standards)
- Adjust the EAV and SAV code position by varying the values in CP_START_EAV[11:0] and CP_START_SAV[11:0]

3. Worked Example

3.1. Interlaced Graphics 1024 x 768 at 43 Hz

```
Timing Name       = "1024 x 768 @ 43Hz";
Hor Pixels        = 1024;       // Pixels
Ver Pixels        = 768;        // Lines
Hor Frequency     = 35.522;     // KHz    =    28.2 usec   / line
Ver Frequency     = 86.957;     // Hz     =    11.5 msec   / field
Pixel Clock       = 44.900;     // MHz    =    22.3 nsec     ± 0.5%
Character Width   = 8;          // Pixels =   178.2 nsec
Scan Type         = INTERLACED;
Hor Sync Polarity = POSITIVE;   // HBlank =  19.0% of HTotal
Ver Sync Polarity = POSITIVE;   // VBlank =   5.9% of VTotal
```

Equation 3. Excerpt from 1024 x 768 at 43 Hz Specification

This example requires that 1024 x 768 at 43 Hz is processed by the CP core.

Follow these steps:

- Calculate the required pixel clock:
  PLL divider ratio = Fpixelclk/Fhsync = 44.9 MHz/35.522 kHz = 1264 (4F0 Hex)

- Calculate the free run line length:
  Free run line length = $F_{system\ -clock}/F_{hsync}$ = 28.636363 MHz/35.522 kHz = 806 (326 Hex)

- Calculate the maximum number of lines per field:
  Frame period/line period = 11.5 ms * 2/28.2 us = 816 (330 Hex)

Using the above calculations, the following script was developed to program the AD9388A/ADV7441A to support interlaced graphics 1024 x 768 at 43 Hz.

```
##CP XGA 1024x768##
:RGB  1024x768 _@ 43 Auto Grapics 44.900MHz Out through DAC:
42 03 0C ; Disable TOD
42 05 02 ; Prim_Mode =010b for automatic graphics mode
42 06 07 ; VID_STD=00111b for automatic graphics mode
42 1D 40 ; Disable TRI_LLC
42 3C A8 ; SOG Sync level for atenuated sync, PLL Qpump to default
42 47 0A ; Enable Automatic PLL_Qpump and VCO Range
42 68 F2 ; Auto CSC , RGB Out
42 7B 1D ; TURN OFF EAV & SAV CODES
42 B7 17 ; ADI Recommended write for Interlaced auto-graphics modes
42 F4 3F ; Max Drive Strength
42 87 E4 ; Enable Manual PLL Divider Ratio
42 88 F0 ; Set PLL Divider Ratio
42 8F 03 ; Set Free Run Line Length(32FHex = 806)
42 90 2F ; Set Free Run Line Length
42 AB 33 ; Set Line Count Max (331Hex = 817)
42 AC 00 ; Set Line Count Max
42 91 50 ; Setup interlacing
50 02 0C ; Setup FPGA 30 Bit;
End
```