ANALOG DEVICES

Application Note

ADV7441A/AD9388A
An Investigation Procedure for Audio Issues

1 Introduction

The purpose of this document is to assist designers investigating the audio issues that can be encountered when integrating the ADV7441A/AD9388A. Sections 2.1 to 2.13 provide a step-by-step procedure to follow in order to investigate and fix audio issues.

2 Investigation Procedure

2.1 Hardware Verification

Check that the hardware is correct and follows the recommendations provided in the Hardware Manual. Verify that the loop filter of the analog audio PLL connected to Pin 102 is configured as shown in Figure 1.

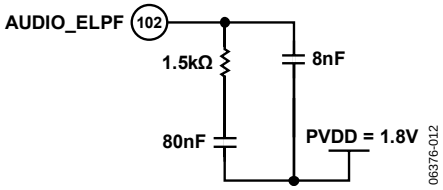

Figure 1. Audio PLL Loop Filter

2.2 EDID

Check that the HDMI transmitter connected to the ADV7441A/AD9388A can access an external EDID or the internal EDID via the DDC bus, as required by the HDMI specifications. Verify that the EDID data image is compliant with the HDMI specifications and indicates audio support.

2.3 Hot Plug Detect

Verify that the Hot Plug Detect (HPD) signal is asserted on the HDMI port used to connect the HDMI source to the ADV7441A/AD9388A.

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2.4 Registers Configuration

Configure the ADV7441A/AD9388A in HDMI mode. For functional verification of the audio, it is possible to configure the ADV7441A/AD9388A with a limited set of settings (see Figure 2) following a hardware or software reset of the ADV7441A/AD9388A. A hardware reset is performed by asserting the RESET pin low for a minimum of 5 ms. A software reset is performed by setting the RES bit (User Map, Address 0x0F[7]) to 1.

```
42 03 0C ; Disable TOD
42 05 06 ; Prim_Mode =0110b HDMI
42 1D 40 ; Disable TRI_LLC
42 37 00 ; Disable PCLK
42 6B E2 ; Setting cp_op_sel = 2 & Enable DE
42 68 F2 ; Auto CSC , RGB Out
42 BA A0 ; Enable HDMI and Analog in
42 C8 08 ; Digital Fine Clamp Start position
42 7B 0D ; Disable AV code Insertion
42 F4 3F ; Max Drive Strength
62 F0 10 ; ADI Recommended Write
62 F1 0F ; ADI Recommended Write
62 F4 20 ; ADI Recommended Write
6A 15 EC ; Disable these mute mask bits
6A 1C 49 ; Set MCLKOUT to output 256fs
6A 1D 04 ;  & Set Unmute Delay to 1_5 sec.
6A 5A 01 ; Reset Audio Pll
```

Figure 2. Register Settings Configuration for Port A With TMDS Clock Less Than 160 MHz

Verify that the ADV7441A/AD9388A outputs valid video data out to the rest of the system, e.g. check that the expected picture is displayed on a panel.

2.5 TMDS PLL

Once the HDMI source has been connected to the ADV7441A/AD9388A, verify that the TMDS PLL of the ADV7441A/AD9388A has locked by reading back the VIDEO_PLL_LCK_RAW flag (User Map 1, Address 0x69[0]). Note that the read-back VIDEO_PLL_LCK_RAW is valid if there is activity on the TMDS clock lines of the HDMI port selected via the HDMI_PORT_SELECT bit (HDMI Map, Address 0x00[1]). The TMDS clock activity status is provided by the following bits:

- TMDS_CLK_A_RAW (User Map 1, Address 0x68[4])
  Set to 1 if the ADV7441A/AD9388A detects TMDS activity on the HDMI port A.
- TMDS_CLK_B_RAW (User Map 1, Address 0x68[3])
  Set to 1 if the ADV7441A/AD9388A detects TMDS activity on the HDMI port B.

The source may not be sending a valid TMDS clock if VIDEO_PLL_LCK_RAW is set to 0. This indicates that the TMDS PLL is not locked.

2.6 HDMI Mode

Verify that the source is sending an HDMI stream to the ADV7441A/AD8388A. This can be done by reading back the HDMI_MODE_RAW bit in User Map 1, Address 0x68[1]. If HDMI_MODE is set to

0, it indicates that the ADV7441A/AD9388A is receiving a DVI stream. If this situation occurs, review the configuration of the source to make sure that it does output an HDMI stream. Verify also the EDID in the ADV7441A/AD9388A, as described in Section 2.2.

2.7 Audio Sample Packets

Verify the ADV7441A/AD9388A is receiving audio data from the source if the source is configured to send audio sample packets. Check that the ADV7441A/AD9388A does receive these packets by reading back the AUDIO_S_PCKT_RAW flag (User Map 1, Address 0x64[0]). If the AUDIO_S_PCKT_RAW bit is set to 0, the ADV7441A/AD9388A is not receiving audio sample packets. If the AUDIO_S_PCKT_RAW bit is set to 0, repeat the instructions in Sections 2.2, 2.5, and 2.6.

2.8 Audio Clock Regeneration Packets

Check that the ADV7441A/AD9388A receives audio clock regeneration (ACR) packets by reading back the AUDIO_C_PCKT_RAW flag (User Map 1, Address 0x64[1]). If the ADV7441A/AD9388A is not receiving ACR packets, AUDIO_C_PCKT_RAW is set to 0, and the ADV7441A/AD9388A cannot generate an internal audio master clock required by the audio processing section. If the bit AUDIO_C_PCKT_RAW is set to 0, repeat the instructions in Sections 2.2, 2.5, and 2.6.

2.9 Audio Clock Regeneration Parameters

Read back the N and CTS parameters and verify that the read back parameters are as per the HDMI specification. The N and CTS parameters are input to the audio synthesiser, which regenerates an internal audio master clock used by the audio processing section. If the N and CTS parameters read back from the HDMI map are not as per the specification, review the HDMI source to verify that it does support audio and sends valid audio clock regeneration packets.

The N and CTS parameters can be read back from the following locations:

- N, HDMI Map, Address 0x7D[3:0], Address 0x7E[7:0], Address 0x7F[7:0]
- CTS, HDMI Map, Address 0x7B[7:0], Address 0x7C[7:0], Address 0x7D[7:4]

2.10 Resetting the Audio Synthesizer

Make sure the audio synthesizer is reset manually at least once after the source has started sending the HMDI stream. There are two conditions for which the audio synthesiser should be reset, i.e. change of CTS and reception of the ACR packet. For investigation purposes, it should be enough to reset manually the audio synthesiser after the source has started sending an HDMI stream to the ADV7441A/AD9388A.

The audio synthesiser of the ADV7441A/AD9388A is reset by setting the self-clearing bit AUDIO_PLL_RESET (HDMI Map, Address 0x5A[0]).

2.11 Audio PLL

Check that the audio PLL is locked by reading back the AUDIO_PLL_LCK _RAW flag (User Map 1, Address 0x64[7]).

If the audio PLL is not locked (i.e. AUDIO_PLL_LCK_RAW is set to 0), repeat the instructions in Sections 2.4, 2.6, 2.8, and 2.9. Verify that the ADV7441A/AD9388A is configured as follows:

- The Audio PLL VCO Range setting (HDMI Map, Address 0x3D[7:6]) is set to 0x1 when the audio sampling frequency is less than 176 kHz.
- The Audio PLL VCO Range setting (HDMI Map, Address 0x3D[7:6]) is set to 0x2 when the audio sampling frequency is equal or more than 176 kHz.
- HDMI Map Address 0x47 is set to 0x00 if the processed TMDS clock is below 147.8 MHz. This setting must be followed by an audio synthesiser reset (see Section 2.10).
- HDMI Map Address 0x47 is set to 0x05 if the processed TMDS clock is higher than 147.8 MHz. This setting must be followed by an audio synthesiser reset (see Section 2.10).

2.12 Internal Mute Status

Check if the ADV7441A/AD9388A is internally muting the audio stream by reading back the internal mute status flag INTERNAL_MUTE_RAW (User Map 1, Address 0x68[5]). If the ADV7441A/AD9388A has not internally muted the audio (i.e. INTERNAL_MUTE_RAW is set to 0), it should output audio data through the I2S and SPIF pins. If no data is output on these pins, repeat the instructions in Sections 2.1 to 2.11.

If the ADV7441A/AD9388A has internally muted the audio (i.e. INTERNAL_MUTE_RAW is set to 1), continue with Section 2.13.

Note that it is also possible to output the audio mute status on the interrupt pins INT0 and INT1 as follows:

- Set INTERNAL_MUTE_INT (User Map 1, Address 0x40[3]) to 1 to output the audio internal mute signal on INT1. The polarity of the internal mute signal on INT1 is controlled by INTRQ_OP_SEL[1:0] (User Map 1, Address 0x40[1:0]).
- Set INTERNAL_MUTE_INT2 (User Map 1, Address 0x41[3]) to 1 to output the audio internal mute signal on INT2. The polarity of the internal mute signal on INT1 is controlled by INTRQ2_OP_SEL[1:0] (User Map 1, Address 0x41[1:0]).

2.13 Internal Mute Investigation

If the ADV7441A/AD9388A internally mutes the audio, it is possible to identify the cause of the internal mute. This can be done by disabling one mute mask at a time and checking if the ADV7441A/AD9388A starts to output audio (see Table 1).

For example, set MT_COMPRS_AUD (HDMI Map, Address 0x14[5] to 0 and check if the ADV7441A/AD9388A unmutes the audio. If the ADV7441A/AD9388A starts to output audio, it means that the ADV7441A/AD9388A was internally muting the audio output through both the I2S and the SPDIF because it was compressed.

Table 1. Audio Mute Masks

Item	Bit Name	HDMI Map Address	Description
1	MT_MSK_COMPRS_AUD	Address 0x14[5]	Causes audio mute if audio is compressed
2	MT_MSK_CHNG_DSD_PCM	Address 0x14[4]	Causes audio mute if audio changes from PCM to DSD and vice versa
3	MT_MSK_PARITY_ERR	Address 0x14[1]	Causes audio mute if parity bits in audio samples are not correct
4	MT_MSK_VCLK_CHNG	Address 0x14[0]	Causes audio mute if TMDS clock has irregular/missing pulses
5	MT_MSK_APLL_UNLOCK	Address 0x15[7]	Causes audio mute if audio PLL goes unlock
6	MT_MSK_VPLL_UNLOCK	Address 0x15[6]	Causes audio mute if TMDS PLL goes unlock
7	MT_MSK_ACR_NOT_DET	Address 0x15[5]	Causes audio mute if ACR packets are not received within one Vsync
8	MT_MSK_SAMP_RT_CHNG	Address 0x15[4]	Causes audio mute if audio sampling frequency in channel status bits changes
9	MT_MSK_FLATLINE_DET	Address 0x15[3]	Causes audio mute if flat line bit in audio packets is set
10	MT_MSK_VFREQ_CHNG	Address 0x15[2]	Causes audio mute if TMDS frequency changes by more than specified threshold in FREQTOLERANCE, HDMI Map, Address 0x0D[3:0]
11	MT_MSK_AVMUTE	Address 0x16[7]	Causes audio mute if AVMute is set to be a general control packet
12	MT_MSK_NOT_HDMIMODE	Address 0x16[6]	Causes audio mute if HDMI bit goes low
13	MT_MSK_NEW_CTS	Address 0x16[5]	Causes audio mute if CTS changes by more than threshold set in CTS_CHANGE_THRESHOLD, HDMI Map, Address 0x10[5:0]
14	MT_MSK_NEW_N	Address 0x16[4]	Causes audio mute if N changes
15	MT_MSK_CHMODE_CHNG	Address 0x16[3]	Causes audio to mute if channel mode changes from stereo to multichannel or visa versa
16	MT_MSK_APCKT_ECC_ERR	Address 0x16[2]	Causes audio to mute if uncorrectable error is detected in audio packets by ECC block
17	MT_MSK_CHNG_PORT	Address 0x16[1]	Causes audio mute if HDMI port is changed
18	MT_MSK_VCLK_DET	Address 0x16[0]	Causes audio mute if TMDS clock is not detected