ADV7842

Register Settings Recommendations

Revision 2.0

October 2013

TABLE OF CONTENTS

INTRODUCTION

This document describes ADI register setting recommendations and adjustments for the ADV7842 product. This document must be used in conjunction with the latest Hardware Manual and Software Manual.

LEGAL TERMS AND CONDITIONS

REVISION HISTORY

10/13—Rev. 1.9 to Rev. 2.0
Updated Sections 3.1 and 3.3.

04/13—Rev. 1.8 to Rev. 1.9
Updates to pages 1-3
Formatting updated throughout
Component Processor section renumbered to section 3
SDP Register Settings section renumbered to section 4

11/10—Rev. 1.7 to Rev. 1.8
Updated sections 2.3 and 2.2.6

11/10—Rev. 1.6 to Rev. 1.7
Updated sections 2.1 and 2.3

10/10—Rev. 1.5 to Rev. 1.6
Updated section 3.1.1

9/10—Rev. 1.4 to Rev. 1.5
Updated section 2.1, 2.2.1.

8/10—Rev. 1.3 to Rev. 1.4
Added section 2.5

6/10—Rev. 1.2 to Rev. 1.3
Removed previous 2.2.7., 2.2.8
Updated section 2.1, 2.2.1, 2.2.10

5/10—Rev. 1.1 to Rev. 1.2
Added sections 2.2.6, 2.2.7, 2.2.8, 2.2.9, 2.2.10, 2.2.11
Updated sections 2.1, 2.2.1, 2.2.4, 2.3, 3.11, 3.25

1/10—Rev. 1.0 to Rev. 1.1
Updated HDMI Initialization settings

1/10—Revision 1.0: Initial Version

1 INITIAL I2C SETTINGS

The ADV7842 contains 12 x I²C register maps which can be accessed through the main I²C port. In previous products all these maps were accessible all the time. In ADV7842. on initial power-up, only the IO Map is accessible. To access the other maps, its I²C address should be programmed in the IO Map registers 0xF1 to 0xFE.

These writes are listed below with possible addresses. The I²C addresses used here are used throughout this document.

I²C Addresses	
40 F1 90	SDP I²C address
40 F2 94	SDPIO I²C address
40 F3 84	AVLINK I²C address
40 F4 80	CEC I²C address
40 F5 7C	INFOFRAME I²C address
40 F8 4C	AFE I²C address
40 F9 64	REPEATER I²C address
40 FA 6C	EDID I²C address
40 FB 68	HDMI I²C address
40 FD 44	CP I²C address
40 FE 48	VDP I²C address

For correct VDP I²C operation, the ADV7842 should be powered up (40 0C 40) and either an SD or CP Primary mode selected.

2 HDMI RECEIVER REGISTER SETTINGS

2.1 INITIALIZATION SETTINGS FOR HDMI MODE

ADI recommends that these register settings are programmed to setup the ADV7842 correctly in HDMI mode.

HDMI Map	
68 C0 00	ADI recommended write
68 0D 34	ADI recommended write
68 3D 10	ADI recommended write
68 44 85	ADI recommended write
68 46 1F	ADI recommended write
68 57 B6	ADI recommended writes
68 58 03	ADI recommended write
68 60 88	ADI recommended write
68 61 88	ADI recommended write
68 6C 18	ADI recommended write
68 75 10	ADI recommended write
68 85 1F	ADI recommended write
68 87 70	ADI recommended write
68 89 04	ADI recommended write
68 99 A1	ADI recommended write
68 9B 09	ADI recommended write

AFE Map	
4C 00 FF	Power down ADC's and their associated clocks
4C 01 FE	Power down ADC circuitry

CP Map	
44 3E 00	Pre gain block disabled

2.2 DYNAMIC SETTINGS FOR HDMI MODE

The following standard register settings are required for the best performance in HDMI mode.

2.2.1 Recommended Equalizer Settings

The ADV7842 contains a dynamic equalizer. This has been optimized for different cable lengths and characteristics; the following writes are required for full optimization. All other settings must remain at default.

HDMI Map	
68 8A 1E	Recommended EQ setting
68 93 04	Recommended EQ setting
68 94 1E	Recommended EQ setting
68 9D 02	Recommended EQ setting

2.2.2 HDMI Audio Switching (HBR and DSD Audio Modes)

When switching between HDMI modes, it is recommended that the audio is muted when switching between HDMI Ports. Before switching port, the Audio should be muted.

- Set manual mute HDMI Map 0x1A[4]= 1 prior to HDMI port change.
- Clear manual mute HDMI Map 0x1A [4] = 0 after HDMI port change.

This procedure is only required if supporting HBR or DSD audio formats.

2.2.3 Internal EDID operation in power down mode

When accessing the internal EDID with the main system power removed from ADV7842, the following circuit design precautions must be strictly adhered to:

- Each of the power supplies must be powered from the cable. All 3.3V, 2.5V and 1.8V supplies must be powered up.
- Power supply sequencing must be adhered to when powering from HDMI cable.
- As the HDMI specification limits the HDMI cable to 50mA, when using this supply to provide power to the ADV7842 in this mode, we do not recommend any other circuitry is powered from the cable other than the ADV7842 and the SPI EEPROM.

When switching from full power mode to powering the ADV7842 from the HDMI cable the following requirement must be met :

- Reset must go low before or at the same time as the main system supply is removed.
- RESET pin must go low, before or at the same time as PWRDWN pin goes low. To ensure this occurs the circuitry in Figure 1 is recommended. It is important to note that this requirement must be met even if the main supply is removed without notice. (For example, if a TV is abruptly disconnected from the wall socket).

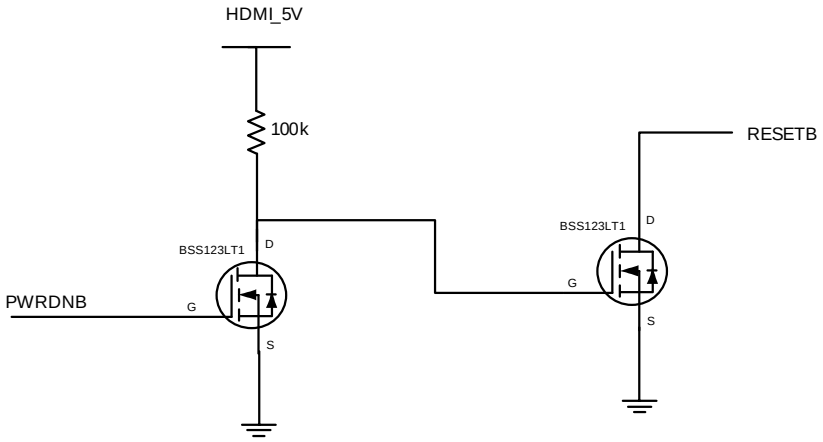

Figure 1: EDID Power-Down Functional Circuitry

The recommendation above must be followed to ensure the ADV7842 is correctly setup for internal EDID read capability in power-down mode and the correct amount of current is drawn from the HDMI cable.

Notes

- The above recommendations only apply to internal EDID in power-down mode.
- If this EDID feature is not required, the PWRDWN pin can be permanently connected to 3.3V.
- This circuitry and procedure are not required if internal EDID is used in normal operation.

2.2.4 HDMI Free-Run Operation

For best performance free-run operation in HDMI modes the following should be set :

- Set PRIM_MODE to the desired free-run standard (IO Map 0x01[3:0])
- Set VID_STD to the desired free-run standard (IO Map 0x00[4:0])
- Set VFREQ to desired free-run frequency (IO Map 0x01[6:4])
- Enable free-run based on primary mode and video standard (CP Map 0xC9[0])
- Enable HDMI Free-Run (CP Map 0xBF[0])

2.2.5 Infoframe Checksum Calculation

The ADV7842 calculates incorrect checksums for Infoframes that have a length of 14 or 15 bytes. By default the ADV7842 does not store any Infoframes which show a checksum error. However, these Infoframes can be stored regardless of checksum error if the following bit is set :

HDMI Map	
Register 0x47[0]	Set = 1, ALWAYS_STORE_INF

When this bit is set to 1, the processor controlling the ADV7842 should verify the validity of the Infoframes received by the ADV7842.

2.2.6 Low Frequency 720p and 108p Format Support

To process the low frame rate video formats 720p24, 720p25, 720p30, 1080p24, 1080p25, 1080p30, the following write should be employed :

HDMI Map	
Register 0x4C[2]	Set = 1 for low frame rate video formats

For all other formats, this bit should be cleared. An algorithm to define when this bit should be set is as follows: If the total horizontal blanking length (hsync front porch + hsync pulse width + hsync back porch) is greater than half the total line length, set HDMI Map, 0x4C[2]. If the total horizontal blanking length (hsync front porch + hsync pulse width + hsync back porch) is less than half the total line length, clear HDMI Map, 0x4C[2].

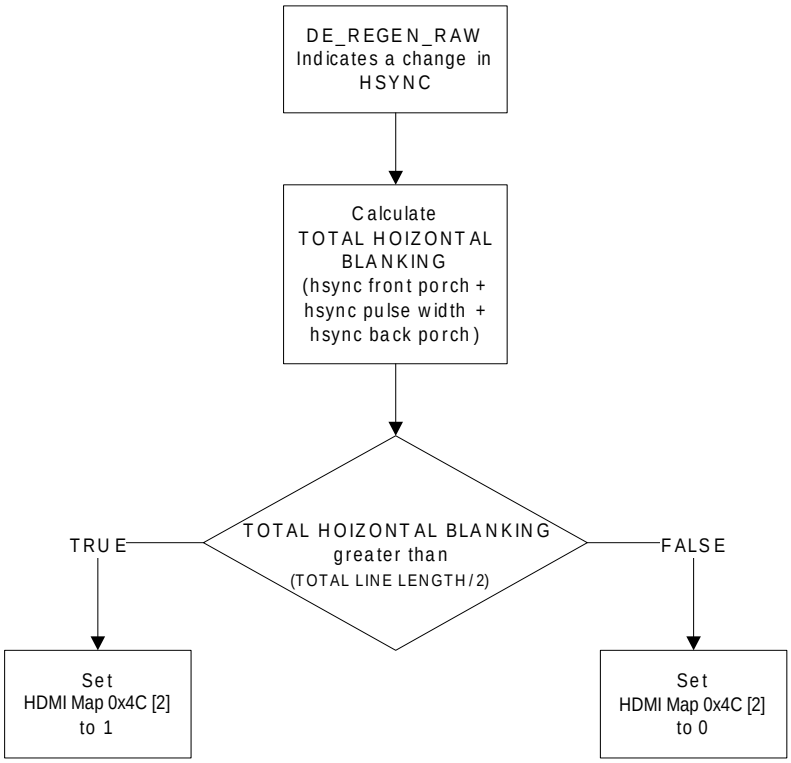

Figure 2. Low Frame Rate Formats Algorithm

2.2.7 Supporting 3D 1080i 50/60Hz Side by Side Full

The following write must be used to support the following 3D formats: 1080i 50/60Hz Side by Side Full

IO Map	
40 C1 2F	for 1080i 50/60Hz Side by Side Full 3D formats

2.2.8 TMDS PLL Lock

This procedure is only required in a fast switching application.

Each time the TMDS PLL locks on the active port, the following steps should be employed :

- If TMDS PLL on the active port changes to unlocked (IO Map, 0x6B[5:4])
  - Wait until TMDSPLL_LCK_X_ST indicates that the TMDS PLL has locked (IO Map, 0x6B[5:4])
  - Clear the TMDS PLL Lock interrupt (IO Map, 0x6C[5:4])
  - Toggle the following bit depending on which port is active (change to 1 and back to 0)
    - Port A – HDMI Map, 0x61[4]
    - Port B – HDMI Map, 0x61[0]
  - Wait until TMDSPLL_LCK_X_ST indicates that the TMDS PLL has locked (IO Map, 0x6B[5:4])
  - Clear the TMDS PLL Lock interrupt (IO Map, 0x6C[5:4])

Each time the TMDS PLL locks on a background port, the following steps should be employed :

- If TMDS PLL on a background port changes to unlocked (IO Map, 0x6B[5:4])
  - Wait until TMDSPLL_LCK_X_ST indicates that the TMDS PLL has locked (IO Map, 0x6B[7:4])
  - Clear the TMDS PLL Lock interrupt (IO Map, 0x6C[5:4])
  - Toggle the following bit depending on which port has just become locked (change to 1 and back to 0)
    - Port A – HDMI Map, 0x61[4]
    - Port B – HDMI Map, 0x61[0]
  - Wait until TMDSPLL_LCK_X_ST indicates that the TMDS PLL has locked (IO Map, 0x6B[5:4])
  - Clear the TMDS PLL Lock interrupt (IO Map, 0x6C[5:4])

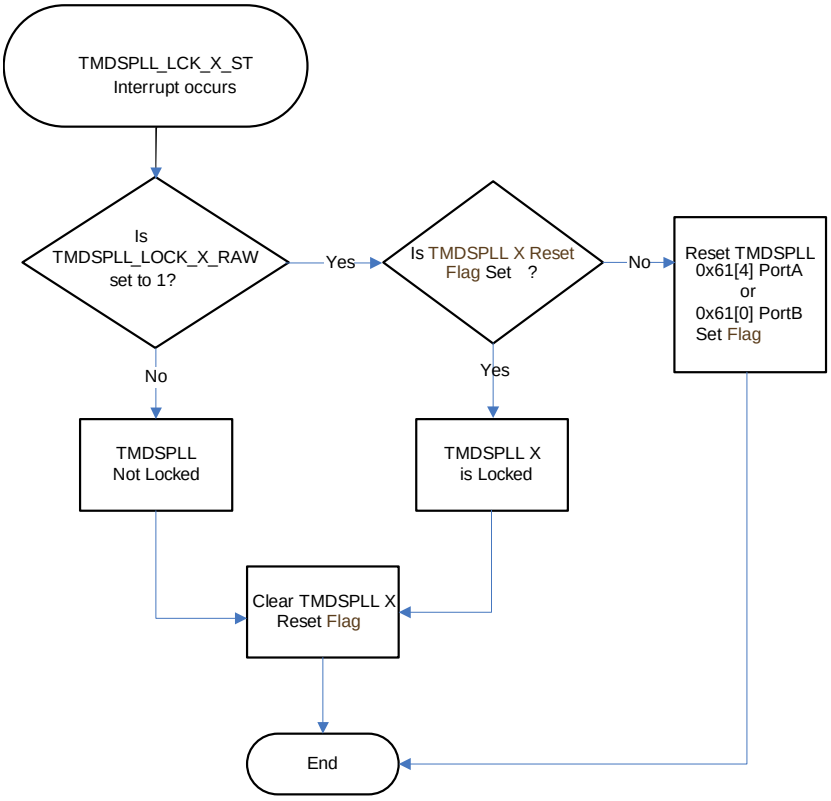

Figure 3. TMDS PLL Algorithm

2.2.9 Non-Fast Switching Application

In a non-fast switching application, the following I²C writes can be carried out to optimise performance and reduce power consumption :

HDMI Map	
Register 0x00[7:5]	Set to 0x00 for non-fast switching applications
Register 0x44[7]	Set to 0x0 for non-fast switching applications

3 COMPONENT PROCESSOR REGISTER SETTINGS

3.1 INITIALIZATION SETTINGS FOR DIGITIZER MODES

ADI recommends that following register settings are programmed to setup the ADV7842 correctly when digitizing analog component inputs and analog graphics inputs. The following writes are required for the correct optimization of the ADC.

AFE Map	
4C 0C 1F	ADI Recommended Write (ADC Range improvement)
4C 12 63	ADI Recommended Write (ADC Range improvement)

For all component and graphics modes manual gain is recommended. The manual gain applied depends on the output quantization range. Based on the CEA-861 and HDMI 1.4 specification the recommended output quantization range is the "Limited Range".

The recommend manual gain for both "Limited Range" and "Full Range" output quantization ranges are listed below. The values listed below are configured for the Analog Devices evaluation board. Depending on the user's system, these values should be adjusted to user preference.

The recommended manual gain settings when outputting data with the "Limited Range" quantization level are listed below :

CP Map	
44 73 EA	Set manual gain of 0x2A8
44 74 8A	Set manual gain of 0x2A8
44 75 A2	Set manual gain of 0x2A8
44 76 A8	Set manual gain of 0x2A8

The recommended manual gain settings when outputting data with the "Full Range" quantization levels are listed below :

CP Map	
44 73 F2	Set manual gain of 0x320
44 74 0C	Set manual gain of 0x320
44 75 83	Set manual gain of 0x320
44 76 20	Set manual gain of 0x320

The following settings should be set on initialization depending on the type of input processed by the part :

Component Mode :

CP Map	
44 C3 33	ADI recommended write

Graphics Mode:

CP Map	
44 C3 39	ADI recommended write (default value)

3.2 DYNAMIC SETTINGS FOR DIGITIZER MODES

3.2.1 Sync Filter Clamp Adjustment

The clamp filter on the synchronization channels must be adjusted according to the input resolution:

- If the sync stripper 1 processes a Standard Definition (SD) input then SYNC1_FILTER_SEL [1:0] should be set to 0b11 to filter out pulses that are shorter than 2.5 us. The same applies to the sync stripper 2, i.e. if it processes a SD input then SYNC2_FILTER_SEL [1:0] should be set to 0b11.

- If the sync stripper 1 processes a High Definition (HD) input then SYNC1_FILTER_SEL [1:0] should be set to 0b01 to filter out pulses that are shorter than 250 ns. The same applies to the sync stripper 2, i.e. if it processes a HD input then SYNC2_FILTER_SEL [1:0] should be set to 0b01.

The synchronization stripper filter controls are in the following locations:

- SYNC1_FILTER_SEL[1:0] in AFE Map, Reg 0x15 [3:2]
- SYNC2_FILTER_SEL[1:0] in AFE Map, Reg 0x15 [1:0]

3.3 STORING INTERNAL EDID RAM CONTENTS TO SPI EEPROM

The following software writes are required in order to store the internal EDID RAM contents of the ADV7842 to an external SPI EEPROM.

- Set VGA_EDID_ENABLE = 0 (Repeater Map, Register 0x7F, Bit [7])
- Set DISABLE_AUTO_EDID to 1 (Repeater Map, Register 0x77, Bit [5])
-
- Set STORE_EDID to 1 (Self Clearing Bit) (Repeater Map, Register 0x7E, Bit [0])

- Set VGA_EDID_ENABLE = 1
- Set DISABLE_AUTO_EDID to 0

4 SDP REGISTER SETTINGS

4.1 INITIALIZATION SETTINGS FOR SDP MODE

4.1.1 Recommended Writes for All SDP Modes

ADI recommends that these register settings are programmed when the part runs in SDP mode.

SDP_IO Map	
94 97 00	Hsync width Adjustment

SDP Map	
90 01 00	Pedestal Off
90 A7 00	ADI Recommended Write

AFE Map	
4C 0C 1F	ADI Recommended Write (ADC Range improvement)
4C 12 63	ADI Recommended Write (ADC Range improvement)

4.2 SDP DYNAMIC REGISTER SETTINGS

4.2.1 Recommended Writes for 3D Comb and 2D Comb

The part should be initialized with the following writes when the 3D Comb feature is used :

- Set 0x12[0](SDP Map) to 1 to enable 3D comb (default value= 1)

No additional writes are needed to be carried out when using 3D comb.

When in 2D Comb mode it is recommended that the following write is carried out :

- Set 0x0E[4](SDP Map) to 0 to disable Y_2D_PK_EN comb (default value= 1)

4.2.2 Recommended Writes for 240p input and 240p output

By default, the ADV7842 decoder outputs 525i/625i timing for 240p/288p inputs. This allows the support of a wide variety of backend devices. To output 240p timing for 240p input the following should be set:

- Set 0xB2[6] (IO Map) ALWAYS_FLIP_F _BIT to 0
- Set 0x7A[2] (SDP Map) to 0 to disable the field signal for 525i timing for 240p input
- Set 0x12[2](SDP Map) to 0 to disable Frame TBC
- Set 0xB0[7:0](SDP_IO Map) to 0xCA to adjust Hsync for 240p
- Set 0xA9[7:0](SDP_IO Map) to 0x05 to adjust Vsync for 240p
- Set 0xAB[7:0](SDP_IO Map) to 0x05 to adjust Vsync for 240p

This will give progressive output timing for the HSync and VSync signals. The VSync signal will also be aligned to the HSync signal.

4.2.3 Memory Controller Initialization

The memory controller must be initialized according to the type of memory used in the application, SDR SDRAM or DDR SDRAM. The memory interface pins should be enabled prior to memory controller initialization and the memory controller must be reset once the appropriate initialization has been implemented. The memory controller is reset by setting SDP_MEM_RESET (SDP_IO Map, Reg 0x60 [0]) to 1.

The DDR SDRAM is automatically configured by default.

When using external DDR or SDR SDRAM the following writes are recommended for optimal performance

SDP_IO Map	
94 7A A5	SDRAM Timing Adjustment
94 7B 8F	SDRAM Timing Adjustment

The following initialization is recommended when SDR SRAM memory is used:

SDP_IO Map	
94 74 00	Reserved in SDR mode
94 75 E6	Set 64Mbit memory size & Exit Refresh Time for SDR SDRAM memory
94 79 33	Sets CAS latency to 3
94 6F 01	Sets up memory controller for SDRAM

The memory controller must be initialized and reset during initialization before enabling any SD core features that use the external memory.

4.2.4 CEA-861 compliance

For 625i inputs on the ADV7842, it is recommended to set the following writes for CEA-861 compliance. These writes are not required in 525i modes.

SDP_IO Map	
94 AA 05	Vsync vertical adjustment
94 B0 CC	Half-Line timing Adjustment

4.2.5 SDP Gain Settings for VCR Type Signals

The SDP automatically analyses the input signal and determines whether or not it is a VCR type signal. It is possible to configure the gain applied when the SDP core detects a VCR type signal to be determined automatically by the automatic gain control (AGC) feature or manually via a user defined gain.

The gain method is selected via SDP_MAN_GAIN_VCR, (SDP Map Register 0x03[5]).

When SDP_MAN_GAIN_VCR is set to 1, the luma gain applied is determined by SDP_Y_GAIN_MAN[12:0] (SDP MAP, 0x03[4:0], 0x04[7:0]) and the chroma gain is determined by SDP_C_GAIN_ACT_MAN[12:0] (SDP MAP, 0x05[4:0], 0x06[7:0]).

It is recommended to select the manual gain option for VCR type signals. The recommended gains for NTSC and PAL VCR type inputs are as follows :

NTSC

SDP Map	
90 03 E4	Manual gain for VCR input, Manual Luma gain setting 0x40B
90 04 0B	Manual Luma gain setting 0x40B
90 05 C3	Manual Chroma gain setting 0x3FE
90 06 FE	Manual Chroma gain setting 0x3FE

PAL

SDP Map	
90 03 E3	Manual gain for VCR input, Manual Luma gain setting 0x3E8
90 04 E8	Manual Luma gain setting 0x3E8
90 05 C4	Manual Chroma gain setting 0x4DC
90 06 11	Manual Chroma gain setting 0x4DC

Note: The gain value defined by SDP_Y_GAIN_MAN[12:0] is also used in manual gain mode for non-vcr type signals. However in general the AGC control should be used for standard signals.

LIST OF REGISTERS ACCESSED FOR ADI RECOMMENDED WRITES

This section lists all registers which are used throughout this documentat and for which no description is provided in the Software and/or Hardware Manuals. The registers listed in the following table should only be configured as per ADI recommendations.

Map	Location	Description
HDMI	0x0D	HDMI Fast Switching optimization
HDMI	0x44	HDMI Fast Switching optimization
HDMI	0x60	HDMI Fast Switching optimization
HDMI	0x57	TMDS PLL Optimization
HDMI	0x58	TMDS PLL Optimization
HDMI	0x67	TMDS PLL Optimization
HDMI	0x61	HDMI Fast Switching optimization
HDMI	0x6C	HDMI Fast Switching optimization
HDMI	0x85	HDMI equalizer setting
HDMI	0x87	HDMI equalizer setting
HDMI	0x99	HDMI equalizer setting
HDMI	0x9B	HDMI equalizer setting
HDMI	0x9D	HDMI equalizer setting
HDMI	0xC1	HDMI Power control block
HDMI	0xC2	HDMI Power control block
HDMI	0xC3	HDMI Power control block
HDMI	0xC4	HDMI Power control block
HDMI	0xC5	HDMI Power control block
HDMI	0xC6	HDMI Power control block
CP	0xC3	CP coast control
CP	0xC9	CP Free Run control
AFE	0x00	ADC powerdown controls
AFE	0x01	Analog front end power down controls
AFE	0x0C	CP Core Gain controls
SDP_IO	0x6F	Memory arbiter control
SDP_IO	0x74	Memory controller control
SDP_IO	0x75	Memory controller control
SDP_IO	0x79	Memory controller control
SDP_IO	0x7A	DDR Pad delay
SDP	0xA7	Coring control

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

HDMI, the HDMI Logo, and High-Definition Multimedia Interface are trademarks or registered trademarks of HDMI Licensing LLC in the United States and other countries.