ADV7619 Required Settings Manual

INTRODUCTION

This document describes the ADI register settings and adjustments required for the ADV7619. This document must be used in conjunction with the latest versions of UG-237: ADV7619 Reference Manual, the ADV7619 Software Manual and the ADV7619 scripts file.

LEGAL TERMS AND CONDITIONS

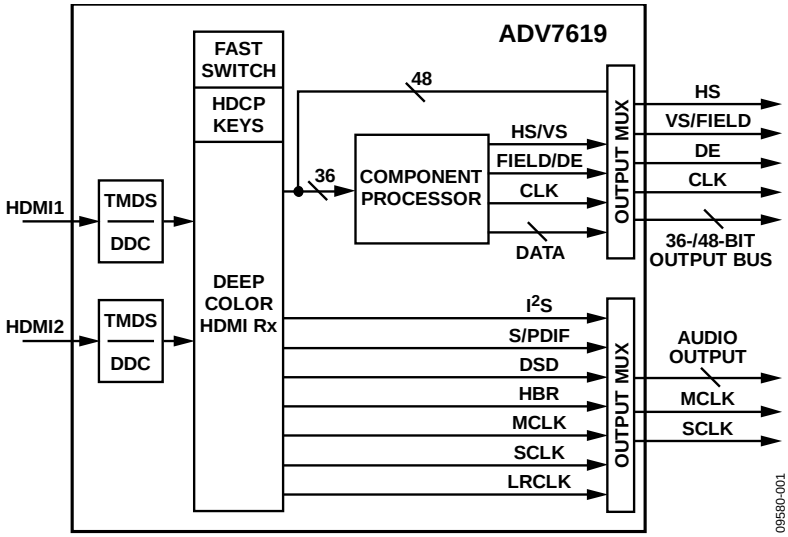

Figure 1. ADV7619 Block Diagram

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REVISION HISTORY

7/10—Revision 1.0: Initial Version

11/11—Revision 1.0 to 1.1:

Sections 1.2 modified (added: 44 6C 00, 68 10 A5, 68 45 04)
Section 1.3.6 modified equalizer writes
Section 1.4 updated with procedure of unsetting 4x2k mode
Figure 3 added

12/11—Revision 1.1 to 1.2:

Section 1.2. Write 68 50 C0 changed to 68 50 00,
Section 1.2. Write added: 68 3D 10
Section 1.3.3 updated (minor edits)
Secion 1.3.4 updated (minor edits)
Figure 1 updated (minor edits)

8/12—Revision 1.2 to 1.3:

Section 1.2 updated – added 68 97 C0.
Section 1.3.6 updated: Added new register writes when changing frequency from 27MHz to above 27MHz (68 85 10; 68 9C 80; 68 9C C0; 68 9C 00)
Section 1.2: Write 68 4C 44 removed (NEW_VS_PARAM)
Section 1.3.7 added outlining usage of NEW_VS_PARAM register.

10/12—Revision 1.3 to 1.4:

Section 1.4 updated – added 68 1B 00 and 08 writes with 1ms delay

12/13—Revision 1.4 to 1.5:

68 6F 0C changed to 68 6F 08 – relaxes restrictions of packet filtering increasing acceptance of some not fully compliant players
Secion 1.3.6 updated – settings for "TMDS frequencies switching to above 27MHz" consolidated wit h "TMDS frequencies above 27MHZ".

Figure 4. updated – TOTAL_LINE_LENGTH changed to TOTAL_LINE_LENGTH/2.

12/14—Revision 1.5 to 1.6:

Updated overall format of the document
Section 1.1 Recommended I2C Addresses renamed Section 1 ADV7619 I2C addresses and content updated
Section 1.2 Recommended Initialization Settings renamed Section 2 HDMI Receiver Register Settings and content updated
Section 1.3.6 Equalizer Settings renamed Section 3 TMDS Equalizer Settings and content updated
Section 1.3.7 Low Frequency Formats renamed Section 4 Low Vertical Frequency Formats and content updated.
Added Section 5 New TMDS Frequency Detection based on what was in Section 1.3.6 previously
Section 1.3.1 Hot Plug Assert renamed Section 6 Manual Hot Plug Assert and content updated
Section 1.3.2 Clock Termination renamed Section 7 Clock Termination and content updated
Section 1.3.3 Free-run Operation renamed Section 8 Free-run Operation and content updated
Section 1.3.4 Power Down Modes renamed Section 9 Power Down Modes and content updated
Section 1.3.5 Packet Detection renamed Section 10 Packet Detection and content updated

09/15—Revision 1.6 to 1.7:

Refined modes listed in Section 2 to input pixel clock frequency ≤ 170 MHz and input pixel clock frequency > 170 MHz
New writes added to Section 2.2
Refined modes listed in Section 3 to input pixel clock frequency ≤ 170 MHz and input pixel clock frequency > 170 MHz
Added clarification on operation of freerun to Section 8

10/15—Revision 1.7 to 1.8:

New write added to Section 2.2

1 ADV7619 I²C ADRESSES

The ADV7619 includes the following programmable I2C map addresses:

I²C Addresses	
98 F4 80	CEC Map Address set to 0x80
98 F5 7C	Infoframe Map Address set to 0x7C
98 F8 4C	DPLL Map Address set to 0x4C
98 F9 64	Repeater Map Address set to 0x64
98 FA 6C	EDID Map Address set to 0x6C
98 FB 68	HDMI Map Address set to 0x68
98 FD 44	CP Map Address set to 0x44

The I²C addresses are programmed in the IO Map at the registers shown above.

The ADV7619 IO I²C Map address is non-programmable and its address is fixed to 0x98. This address can be changed by pulling up the VS/ALSB/FIELD pin with a 10k resistor and sending the SAMPLE_ALSB command (IO Map, Register 0x1B[0]). Refer to UG-237: ADV7619 Reference Manual for further information.

The I²C map addresses listed above are used throughout this document.

2 HDMI RECEIVER REGISTER SETTINGS

Different register settings are required to configure the HDMI Receiver depending on the resolution it receives. These required settings are listed below for the respective resolutions. Note that these settings do not include the TMDS Equalizer settings, which are described in Section 3. Also note that these required settings are not the only settings needed to configure the ADV7619.

Please refer to the latest ADV7619 scripts file revision for all the settings required to configure the ADV7619 for a specific mode, and for the sequence in which these writes must be done.

2.1 INPUT VIDEO PIXEL CLOCK FREQUENCY ≤ 170MHZ

The following two categories of settings are required for input video resolutions with a pixel clock of less than or equal to 170 MHz.

2.1.1 480i, 576i, 480p and 576p Resolutions up to a 36-bit color depth

The following settings are required for the 480i, 576i, 480p and 576p resolutions with color depths between 24-bit and 36-bit. For these resolutions, the data is processed through the CP core.

CP Map and HDMI Map	
44 6C 00	ADI Required Write
68 C0 03	ADI Required Write
68 03 98	ADI Required Write
68 10 A5	ADI Required Write
68 1B 08	ADI Required Write
68 45 04	ADI Required Write
68 97 C0	ADI Required Write
68 3D 10	ADI Required Write
68 3E 69	ADI Required Write
68 3F 46	ADI Required Write
68 4E FE	ADI Required Write
68 4F 08	ADI Required Write
68 50 00	ADI Required Write
68 57 A3	ADI Required Write
68 58 07	ADI Required Write
68 6F 08	ADI Required Write
68 84 03	ADI Required Write

2.1.2 720p, 1080i and 1080p Resolutions up to a 36-bit color depth

The following settings are required for the 720p, 1080i, 1080p resolutions with color depths between 24-bit and 36-bit. For these resolutions, the data is processed through the CP core.

CP Map and HDMI Map	
44 6C 00	ADI Required Write
68 C0 03	ADI Required Write
68 03 98	ADI Required Write
68 10 A5	ADI Required Write
68 1B 08	ADI Required Write
68 45 04	ADI Required Write
68 97 C0	ADI Required Write
68 3D 10	ADI Required Write
68 3E 69	ADI Required Write
68 3F 46	ADI Required Write
68 4E FE	ADI Required Write
68 4F 08	ADI Required Write
68 50 00	ADI Required Write
68 57 A3	ADI Required Write
68 58 07	ADI Required Write
68 6F 08	ADI Required Write
68 84 03	ADI Required Write

2.2 INPUT VIDEO PIXEL CLOCK FREQUENCY > 170MHZ

The following settings are required for input video resolutions with a pixel clock of greater than170 MHz. For these resolutions, the CP core of ADV7619 is bypassed and the clock divider and the double wide (48-bit) output interface are employed.

IO Map, DPLL Map and HDMI Map	
98 00 19	Set VID_STD for 2x1 mode
98 01 05	Set PRIM_MODE for HDMI Comp
98 DD 00	ADI Required Write
98 E7 04	ADI Required Write
4C C3 80	ADI Required Write
4C CF 03	ADI Required Write
4C DB 80	ADI Required Write
68 C0 03	ADI Required Write
68 03 98	ADI Required Write
68 10 A5	ADI Required Write
68 1B 00	ADI Required Write
68 45 04	ADI Required Write
68 97 C0	ADI Required Write
68 3E 69	ADI Required Write
68 3F 46	ADI Required Write
68 4E FE	ADI Required Write
68 4F 08	ADI Required Write
68 50 00	ADI Required Write
68 57 A3	ADI Required Write
68 58 07	ADI Required Write
68 6F 08	ADI Required Write
68 84 03	ADI Required Write

3 TMDS EQUALIZER SETTINGS

Different register settings are required to configure the TMDS Equalizer depending on the resolution received. These required settings are listed below for the respective resolutions.

3.1 INPUT VIDEO PIXEL CLOCK FREQUENCY ≤ 170MHZ

The following two categories of settings are required for input video resolutions with a pixel clock of less than or equal to 170 MHz.

3.1.1 480i, 576i, 480p and 576p Resolutions up to a 36-bit color depth

The following settings are required to configure the TMDS Equalizer for the 480i, 576i, 480p and 576p resolutions with color depths between 24-bit and 36-bit.

HDMI Map	
68 85 11	ADI Required Write
68 86 9B	ADI Required Write
68 89 03	ADI Required Write
68 9B 03	ADI Required Write
68 93 03	ADI Required Write
68 5A 80	ADI Required Write
68 9C 80	ADI Required Write
68 9C C0	ADI Required Write
68 9C 00	ADI Required Write

3.1.2 720p, 1080i and 1080p Resolutions up to a 36-bit color depth

The following settings are required to configure the TMDS Equalizer for the 720p, 1080i, 1080p resolutions with color depths between 24-bit and 36-bit.

HDMI Map	
68 85 10	ADI Required Write
68 86 9B	ADI Required Write
68 89 03	ADI Required Write
68 9B 03	ADI Required Write
68 93 03	ADI Required Write
68 5A 80	ADI Required Write
68 9C 80	ADI Required Write
68 9C C0	ADI Required Write
68 9C 00	ADI Required Write

3.2 INPUT VIDEO PIXEL CLOCK FREQUENCY > 170MHZ

The following settings are required for input video resolutions with a pixel clock of greater than170 MHz.

HDMI Map	
68 85 10	ADI Required Write
68 86 9B	ADI Required Write
68 89 03	ADI Required Write
68 9B 03	ADI Required Write
68 93 03	ADI Required Write
68 5A 80	ADI Required Write
68 9C 80	ADI Required Write
68 9C C0	ADI Required Write
68 9C 00	ADI Required Write

4 LOW VERTICAL FREQUENCY FORMATS

To process low frame rate video formats such as 720p24, 720p25 and 720p30, the NEW_VS_PARAM bit should be set. Figure 2 illustrates how to proceed to detect if this bit must be set.

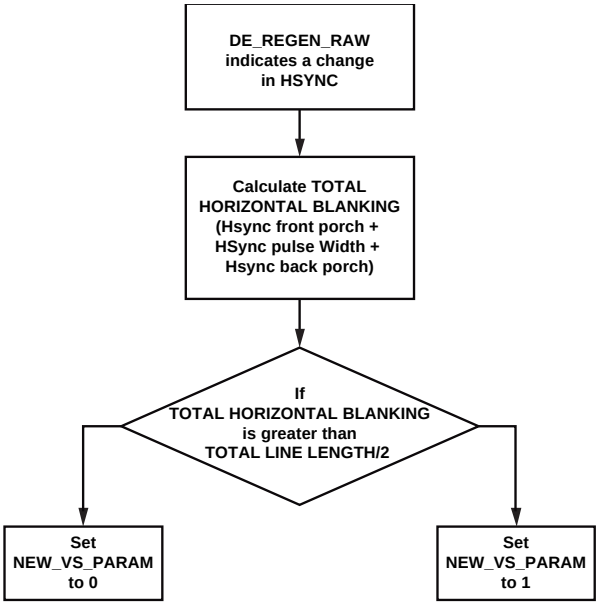


Figure 2. Low frame rate algorithm

NEW_VS_PARAM, HDMI, Address 0x4C[2]

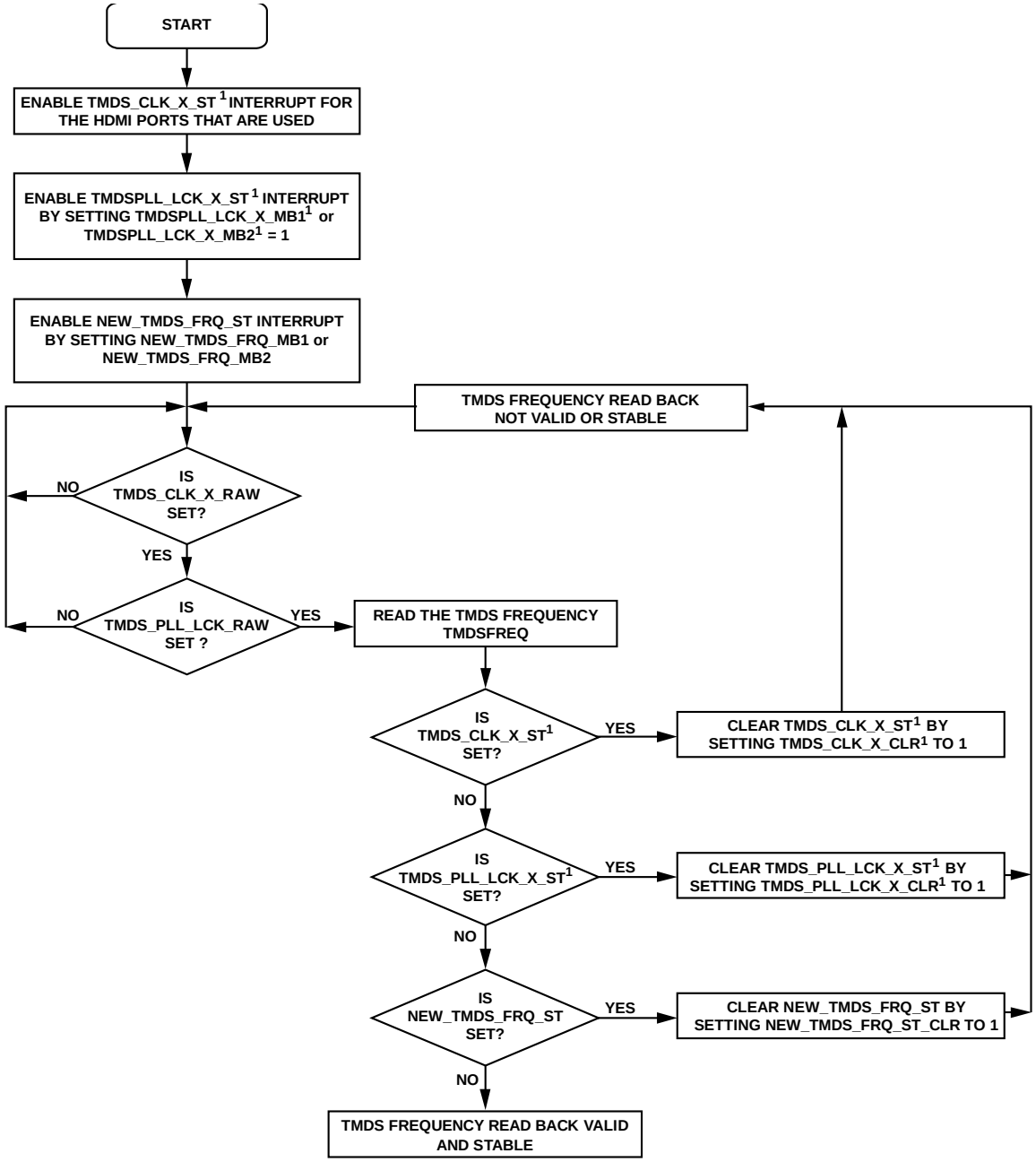
Enables a new version of vertical parameter extraction.

Function

NEW_VS_PARAM	Description
0	NEW_VS_PARAM disabled
1	NEW_VS_PARAM enabled

5 NEW TMDS FREQUENCY DETECTION

A change in TMDS frequency can be detected using the flow illustrated on Figure 3.



[1] Where X = An active port selected by HDMI_PORT_SELECT (HDMI Map, REG 0x00 bits [3:0])

Figure 3: Example algorithm to monitor changes of TMDS frequency.

Refer to Hardware User Guide UG-237 (TMDS Measurement section) for details on register addresses.

6 MANUAL HOT PLUG ASSERT

To manually assert a hot plug, to replicate a downstream hot plug in a repeater application for example, the writes below should be used.

- Port A:

To manually assert hot plug on port A, the following writes should be used.

HDMI Map and IO Map	
68 6C A3	Hot plug assert controlled manually
98 20 B0	Manually assert hot plug on port A

- Port B:

To manually assert hot plug on port A, the following writes should be used.

HDMI Map and IO Map	
68 6C A3	Hot plug assert controlled manually
98 20 70	Manually assert hot plug on port B

When a hot plug was asserted manually, it must also be de-asserted manually.

7 CLOCK TERMINATION

The clock termination on both Port A and Port B can be enabled manually by the following writes:

HDMI Map	
68 01 00	TERM_AUTO set to 0. Automatic clock termination control disabled (default)
68 83 FC	Enable clock termination manually on both part A and port B

The clock termination can also be enabled automatically. This can be done by setting TERM_AUTO (HDMI Map, Register 0x01[0]) to 1.

8 FREE-RUN OPERATION

For better control in free-run mode, the free-run resolution can be set manually. This can be achieved by following the steps below:

- Set PRIM_MODE[3:0] to the desired free-run standard (IO Map, Register 0x01[3:0])
- Set VID_STD[5:0] to the desired free-run standard (IO Map, Register 0x00[5:0])
- Set V_FREQ[2:0] to the desired free-run frame rate (IO Map, Register 0x01[6:4])
- Set DIS_AUTO_PARAM_BUFF to 1 (CP Map, Register 0xC9[0]) for the free-run resolution to be defined by PRIM_MODE[3:0], VID_STD[5:0] and V_FREQ[2:0]

The free-run output defined by PRIM_MODE[3:0], VID_STD[5:0] and V_FREQ[2:0] is generated by the CP core. It is possible to force the CP core to free-run. This can be done by setting CP_FORCE_FREERUN to 1 (CP Map, Register 0xBF[0]).

Note: It is not possible to set the free-run resolution manually for input video resolutions with a pixel clock of greater than170 MHz. For these modes, the CP core is bypassed.

9 POWER DOWN MODES

The ADV7619 has two power down modes, power down mode 0 and power down mode 1. In power down mode 0 and power down mode 1, chassis supply is available. In power down Mode 1, CEC is powered up. In power down Mode 0, CEC is powered down.

To correctly power down the ADV7619, the steps below should be followed:

- Set POWER_DOWN bit to 1 to power down the chip (98 0C 62)
- In case of power down mode 0: power down CEC (80 2A 3E)
- In case of power down mode 1: power up CEC (80 2A 3F)

When returning from low power mode, to correctly power up the ADV7619, the steps below should be followed:

- Set POWER_DOWN to 0 to power up the chip (98 0C 42)
- If CEC should be powered up, set CEC_POWER_UP to 1 (80 2A 3F)
- If CEC should be powered down, set CEC_POWER_UP to 0 (80 2A 3E)

Note: In power down modes, additional power-savings can be achieved by using the following writes:

- Disable ring oscillator (68 48 01)
- Power down DDC pads (68 73 03)

10 PACKET DETECTION

The ADV7619 does not generate an interrupt when a source stops sending the following infoframes:

- Audio infoframe
- Source Prod infoframe
- MPEG Source infoframe
- Vendor Specific infoframe
- ACP infoframe
- ISRC1 infoframe
- ISRC2 infoframe
- Gamut infoframe

To detect when a source has stopped sending an infoframe, the steps below should be followed:

- Clear infoframe interrupt RAW bit
- If RAW bit does not get set during max allowed packet repeat time, the source has stopped sending the infoframe

For example, 3D content is indicated using the Vendor Specific (VS) infoframe. It has been observed that some 3D sources stop sending the VS infoframe should their output be switched from 3D to 2D. For this reason, the application must detect when the VS infoframe stops being received.

Figure 4 and Figure 5 below provide an Interrupt Service Routine (ISR) example that could be used to detect if the VS infoframe is no longer received.

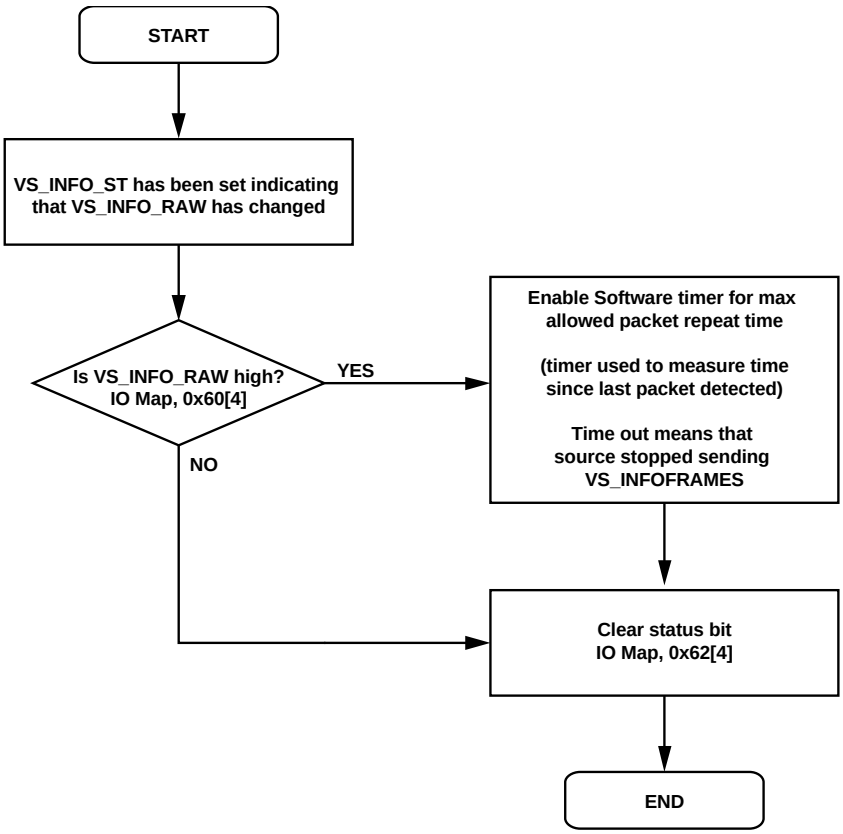


Figure 4. ISR Routine

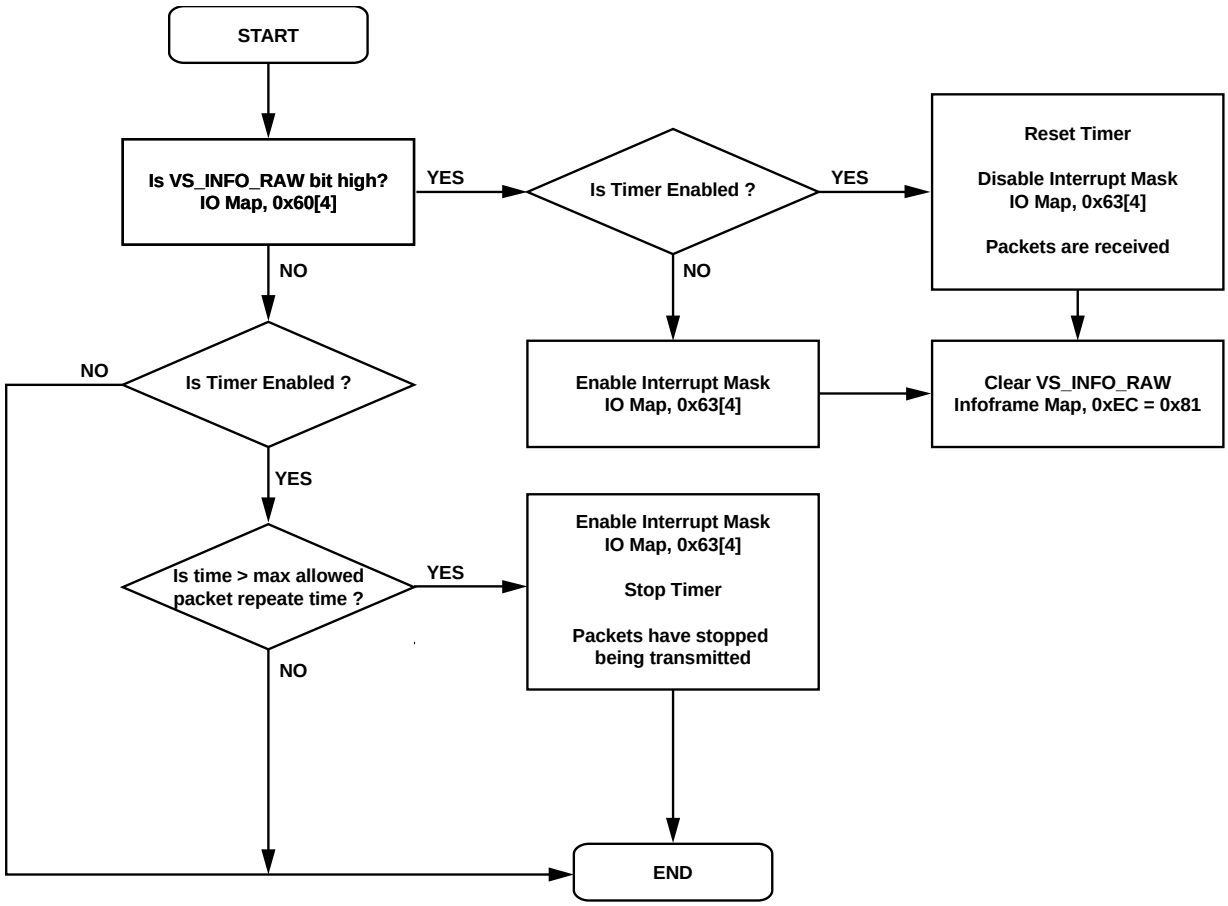


Figure 5. Infoframe Task

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).