AD9985A

Analog Flat Panel Interface Board

Evaluation Board
Documentation
For the AD9985A

Rev 0 9/1/2000

Purpose

The purpose of the AD9985A Evaluation Board is both to demonstrate the performance of the AD9985A and to serve as an implementation example for design and layout. To aid in real-world evaluation, it was designed so that it could be connected as easily as possible into another pc board, (such as a graphics controller board).

Requirements

The requirements to use the AD9985A Evaluation Board are a 5V power supply, graphics signals (through the 15 pin VGA connector), and a means to program the internal chip registers. (Hardware and software for programming the internal chip register are provided.)

Typical Configuration

In most cases, this Evaluation Board will be used to digitize analog RGB graphics signals and pass the data on to another board. To do this, connect the graphics signals to the 15 pin VGA connector, supply 5V to the board, and program the internal serial register. (Supplying power and programming the chip are described later in this document). The digitized data, generated clock signals, and control signals are passed off the board through the right hand side connector.

Power

The AD9985A Evaluation Board contains three 3.3V voltage regulators. These regulators supply power to the AD9985. The three regulators provide power to the three power supplies on the AD9985A (refer to the AD9985A Data Sheet). The best performance can be obtained from the AD9985A when the analog supply (Vd) and the PLL (PVd) supply have their own regulators separate from the primary 3.3 volt supply (Vdd). The three regulators work nominally when supplied with 5V, but will work with a range of voltages. Power is applied to the board through the right hand side connector (pins 1, 2, 41, & 42 of J3). Typically, power is supplied from another board. (As is the case using the XGA Panel Driver Board).

Chip Register Convention

This document frequently refers to specific control registers in the AD9985. The convention used in this document is to specify the register number in hex first, then an "h", and finally the bit number within the register. For example, [12h7] means register 12, bit 7.

Programming the Internal Chip Registers

Hardware and software for programming the AD9985A internal registers are provided. The hardware consists of a standard printer cable and a receiver chip located on the Panel Driver Board. The programming signals come onto the AD9985A Evaluation Board through pins 38 & 39 on connector J3. The software is included on the installation CD and is described below:

Setup Software

The Display Electronics Product Line (DEPL) Evaluation Software is a Visual Basic program requiring Windows 95, or newer. It is on a self-installing CD package included with the Evaluation Board. **When performing the software install, always use the most recent Windows files (DLL or OCX for example) if prompted by the install software (these files may already be on your system).** The AD9985A register setup screen output shown in Figure 1 should be displayed at program execution after a successful installation. The DEPL Evaluation Software can be used to control any of the DEPL AD988X devices. It also includes the Display Interface Board configuration software and a PLL Divisor calculator..

AD9985A Software Control

To select the AD9985A as the target device for the DEPL Evaluation Software, click on the "Device" pull-down menu and select "AD9985". The AD9985A register setup screen is shown in Figure 1. From this screen the user can control every bit within the AD9985. A detailed, bit-by-bit functional description is provided in the AD9985A Data Sheet. In order to update the registers in the AD9985A the "Load" button at the top of the window must be clicked. This is true unless the "Load Register on Change" box next to the "Read" button is checked. In this case, the appropriate register is updated as soon as any change is made in the window. There are 3 tabs within this control window that enables the selection of groups of registers to be displayed. The selections are: 00-0F, 10-14, or 15. Click on the appropriate tab to view/control the register desired.

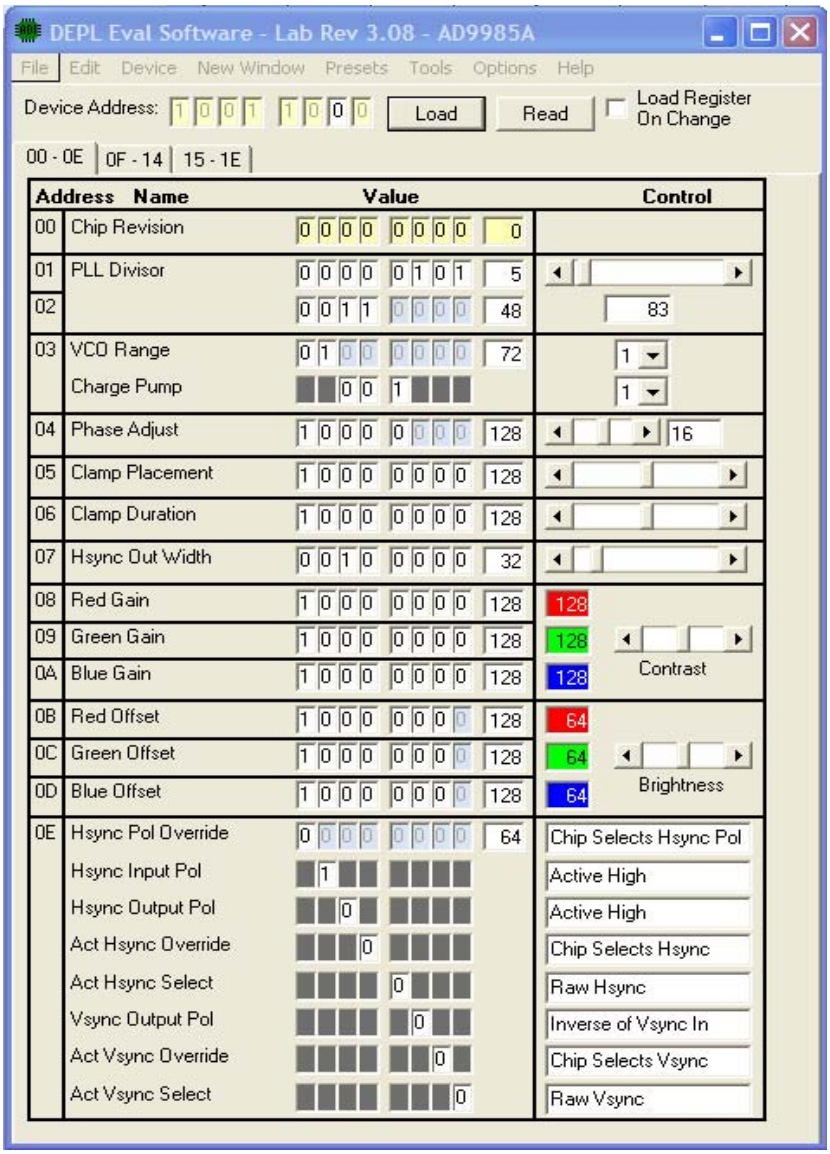

Figure 1: AD9985A Register Setup Screens

PLL Settings

The PLL settings are contained in registers 01 – 04. The **PLL Divisor** setting (12 bits) can be set bit-by-bit (the value toggles when clicking on the bit), by setting a value for registers 01 and 02 (decimal value), by setting the 12-bit value (decimal value), or by moving the control bar left (to decrease) or right (to increase). When changing the value using one of these methods, the change is reflected in the other three. The values are not written to the AD9985A until the LOAD button is clicked. The **VCO Range** and **Charge Pump** settings in register 03 can be set by individual bit, by register, or by pull-down menu selection. The 5-bit **Phase Adjust** in register 04 can be altered in the some manner as the PLL Divisor.

Clamp and Hsync Out Settings

Clamp Placement, **Clamp Duration**, and **Hsync Output Width** controls are contained in registers 05 – 07 and can be changed bit-by-bit, by setting a value for the registers (decimal value), or by moving the control bar left (to decrease) or right (to increase). When changing the value using one of these methods, the change is reflected in the other two. Again, these value changes are not loaded into the AD9985A until the LOAD button is clicked unless the "Load Register on Change" box is checked

Gain and Offset Settings

Gain for the **Red**, **Green**, and **Blue** video channels are controlled via all eight bits of registers 08 –0Ah and can be changed bit-by-bit, by setting a value for the registers (decimal value), or by moving the control bar left (to decrease) or right (to increase). The 7-bit **Offset** control for the **Red**, **Green**, and **Blue** are contained in registers 0Bh – 0Dh. These can be set in the same manner as Gain, with the additional option of setting the 7-bit decimal value. Note that using the gain and offset control bars will change all 3 channels by the same amount, regardless of their setting. In other words, if, in order to achieve color balance, your offset settings are 60, 70 and 80 for R, G, and B, respectively, then the minimum settings are 0, 10, and 20. The maximum offset settings would then be 107, 117, and 127.

Sync Control

Register 0Eh contains bits for controlling input and output **Hsync** and **Vsync** signals. You can toggle each bit by clicking on it. The resulting state of the bit is reflected in the box to the right of each bit. Refer to the AD9985A Data Sheet for a functional description of these bits.

Clamp, Coast, and Power Management

Register 0Fh contains bits for controlling the **Clamp** and **Coast** functions, as well as **Power Management** functions. You can toggle each bit by clicking on it. The resulting state of the bit is reflected in the box to the right of each bit. Refer to the AD9985A Data Sheet for a functional description of these bits.

SOG and Clamp Control

Register 10h contains bits for controlling the **SOG Threshold** and **Clamp** selection functions.

Register 11h contains bits for adjusting the **Sync Seperator Threshold.** The 5-bit (7:3) SOG Threshold can be modified bit by bit or by changing the 5-bit (decimal) value. You can toggle each of the Clamp Selection bits by clicking on it. The resulting state of the bit is reflected in the box to the right of each bit. The Sync Separator Threshold can be changed bit-by-bit, by setting a value for the register (decimal value), or by moving the control bar left (to decrease) or right (to increase). Refer to the AD9985A Data Sheet for a functional description of these bits.

Pre and Post Coast

Registers 12h and 13h contain the bits for controlling **Pre-Coast** and **Post Coast**. The 8-bit Pre-Coast and 8-bit Post-Coast can be modified bit by bit or by changing the 8-bit (decimal) value. The resolution of this adjustment is in Hsync periods. These adjustments apply to the internal Coast function of the AD9985A and do not alter an external Coast signal. Refer to the AD9985A Data Sheet for a functional description of these bits.

Sync and Coast Status (Read Only)

Register 14h is a read only register that provides status for Hsync, Vsync, SOG, and Coast polarity. Performing a read (by clicking the "READ" button at the bottom of the window) allows the user to see the status of each of these bits. The status is also reflected in the text to the right of each of these bits. Refer to the AD9985A Data Sheet for a functional description of these bits.

Sample Settings for Evaluation Board

PLL Timing Chart							
		Horizontal[2]					
Mode	**Resolution**	**Nominal Frequency Hs (KHz)**	**Sync Polarity**	**PLL Divider[1] N+1**	**Nominal Pixel Clock (MHz)**	**VCO Range[2]**	**Charge Pump Current[2]**
VGA	640x480 @ 60 Hz	31.469	N	800	25.175	00	110
	640x480 @ 72 Hz	37.861	N	832	31.500	00	110
	640x480 @ 75 Hz	37.500	N	840	31.500	00	110
	640x480 @ 85 Hz	43.269	N	832	36.000	01	100
SVGA	800x600 @ 56 Hz	35.156	N/P	1024	36.000	01	100
	800x600 @ 60 Hz	37.879	P	1056	40.000	01	100
	800x600 @ 72 Hz	48.077	P	1040	50.000	01	101
	800x600 @ 75 Hz	46.875	P	1056	49.500	01	101
	800x600 @ 85 Hz	53.674	P	1048	56.250	01	101
XGA	1024x768 @ 60 Hz	48.363	N	1344	65.000	10	101
	1024x768 @ 70 Hz	56.476	N	1328	75.000	10	100
	1024x768 @ 75 Hz	60.023	P	1312	78.750	10	100
	1024x768 @ 80 Hz	64.000	P	1336	85.500	10	101
	1024x768 @ 85 Hz	68.677	P	1376	94.50	10	101
SXGA	1280x1024 @ 60 Hz	60.020	P	1688	108.000	10	110
	1280x1024 @ 75 Hz	80.000	P	1688	135.000	11	110

Note 1: (PLL divisor to chip should be odd integer - Chip Divide ratio = Input N + offset of 1)
Note 2: The VCO Range and Charge Pump Current settings are preliminary and may need slight adjustments.

Schematics and Layout

The schematics and layout for this board are included in separate files. They can be found on the CD.

Contact Information

Questions? Please email us directly at flatpanel_apps@analog.com, visit our web site at http://www.analog.com/flatpanel, or call the Analog Devices help line at 1-800-AnalogD.