

ADV8003 Advantiv (TM) Video Evaluation Board

This PCB design was originally designed to allow evaluation of ADV8003:

- * EVAL-ADV8003-SMZ (HDCP)
- * EVAL-ADV8003-SMZ-P (non-HDCP)

We also used this PCB initially to allow evaluation of ADV8005:

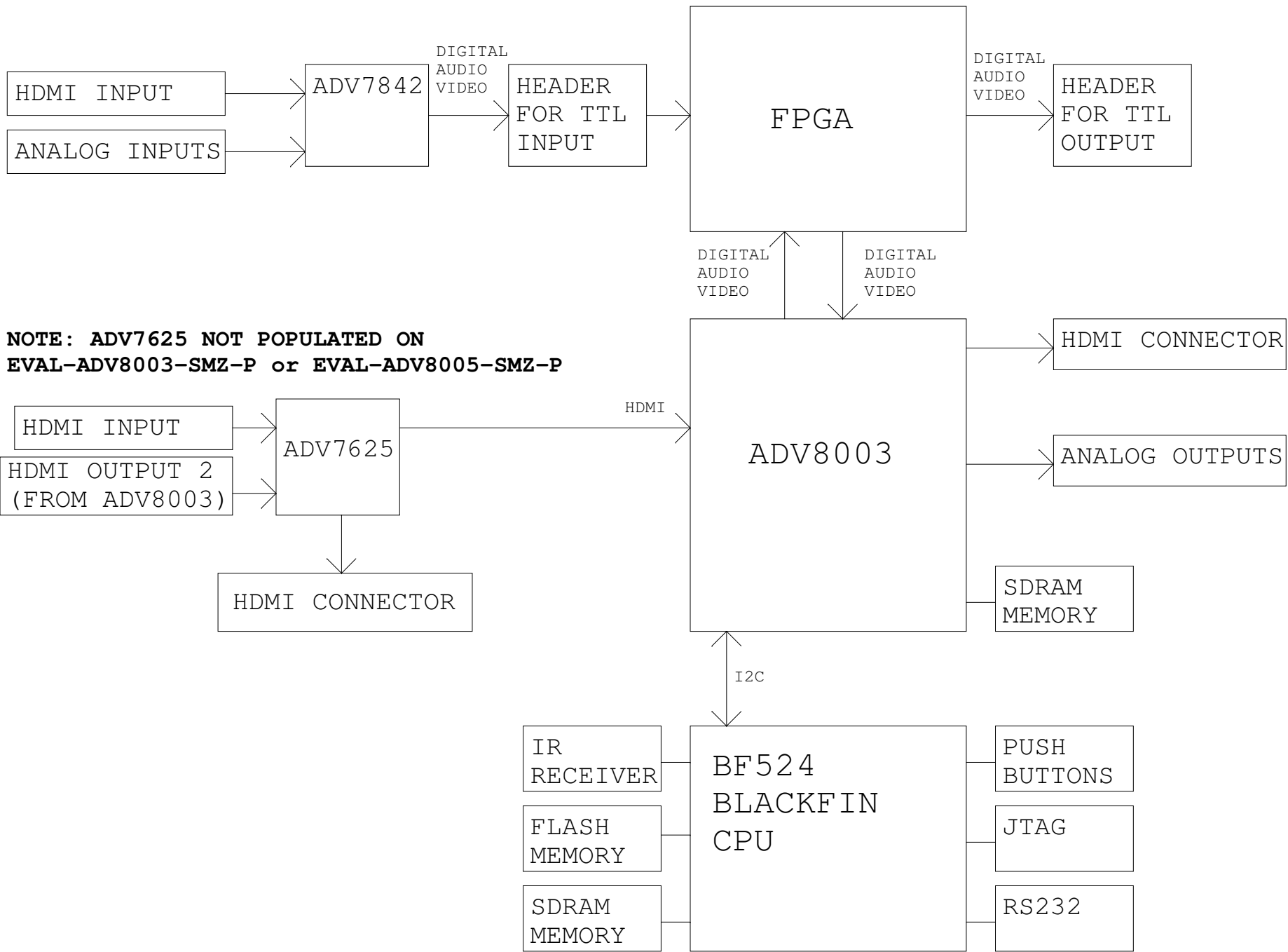
- * EVAL-ADV8005-SMZ (HDCP)
- * EVAL-ADV8005-SMZ-P (non-HDCP)

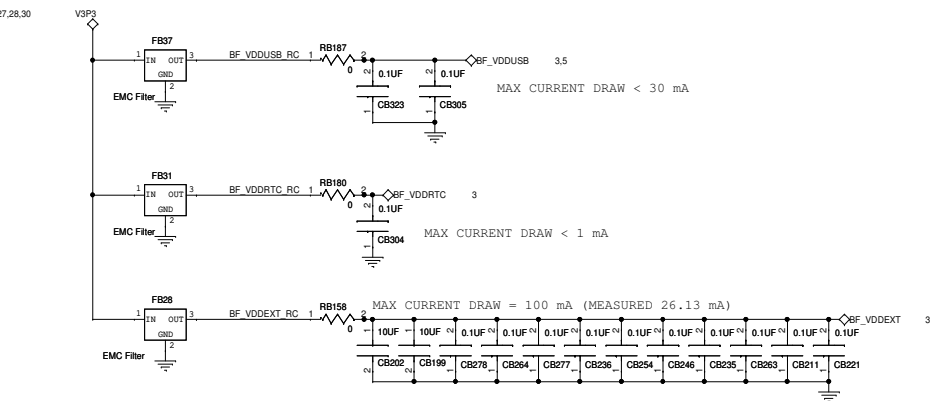
We plan to design a new PCB for EVAL-ADV8005-SMZ and EVAL-ADV8005-SMZ-P in 2015.

Change Log

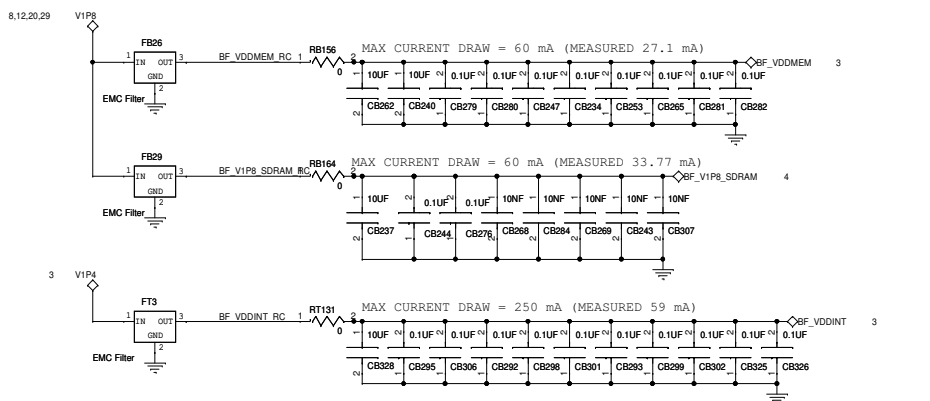
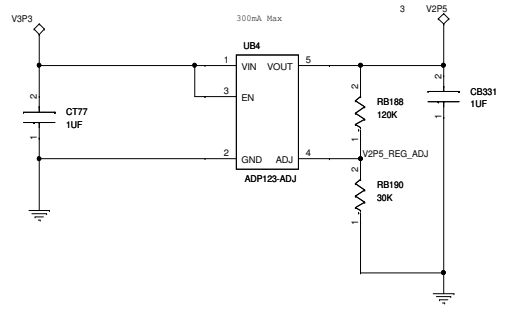
Revision	Date	Description
0.1	2013/02/04	Initial Release
0.2	2013/06/12	<ul style="list-style-type: none">* Added 500 ohm resistor to GND for ADV8003 R_TX1* Added 500 ohm resistor to GND for ADV8003 R_TX2* Added 1K resistor between 7842_RXA_DDC_5V and 7842_RXA_HPD* Added 1K resistor between 5V and 7625_TXA_HPD* Routed ADV7842_LLC_T to TTL-IN connector and then into FPGA (rather than ADV7842_SYNC_T)* Routed IR_RECEIVER_VOUT to to BF524 pin B17 and pin F2 (through resistors)* Removed LED circuitry between ADV7625 and ADV8003 (UT31, CT66, RB162, DT6)
0.2	2015/01/16	<ul style="list-style-type: none">* Added reference to EVAL-ADV8005-SMZ-P* Added note on page 20 (ADV8003 Power) about N23 and W23 being different on ADV8003 and ADV8005.* Added note on page 23 (ADV8003 SDRAM) about AA8 being different on ADV8003 and ADV8005.

Title		
Cover Page		
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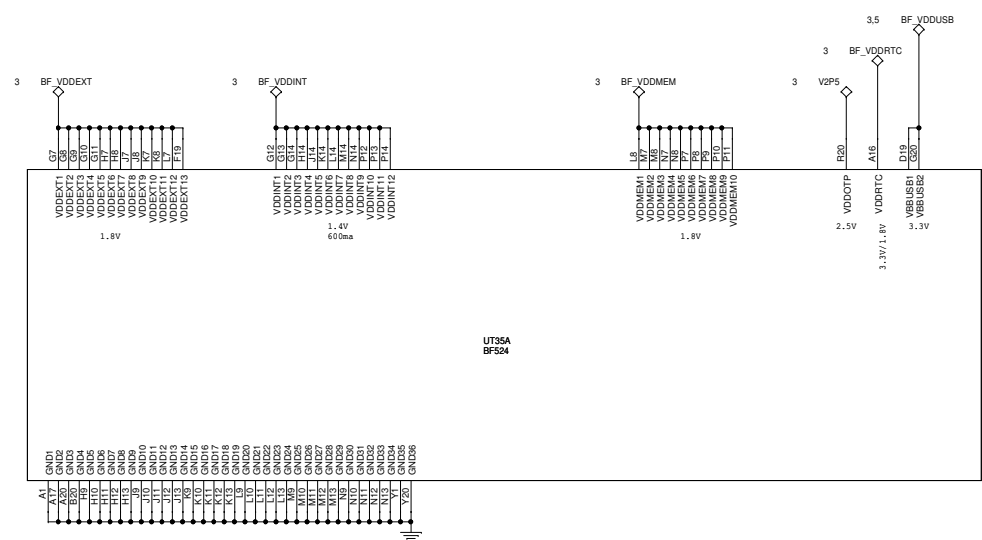
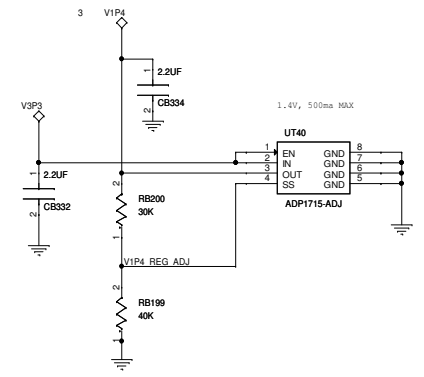




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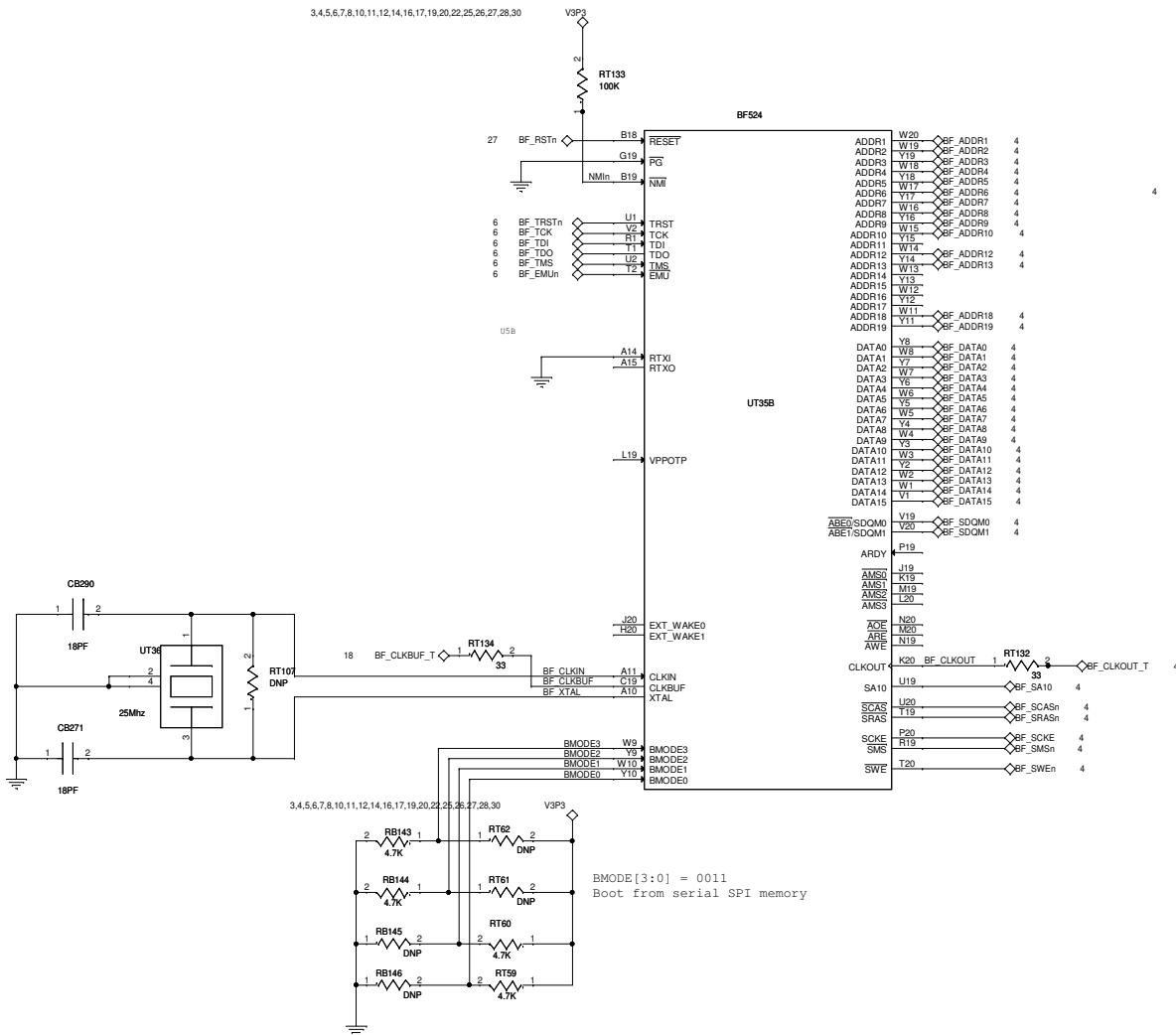


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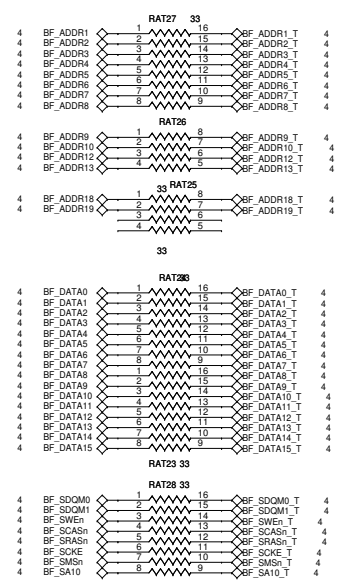
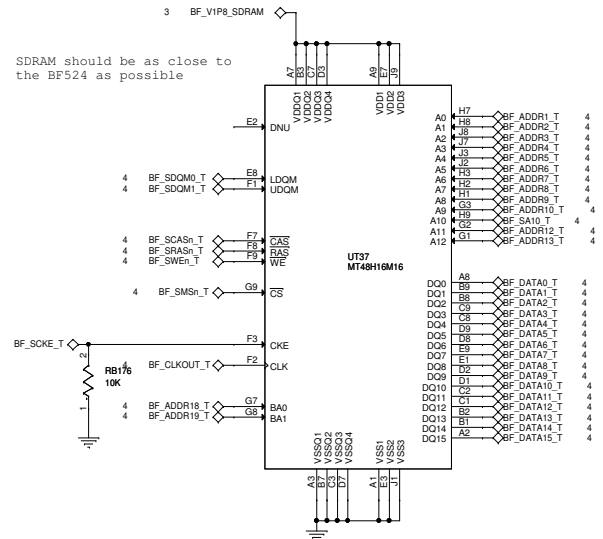


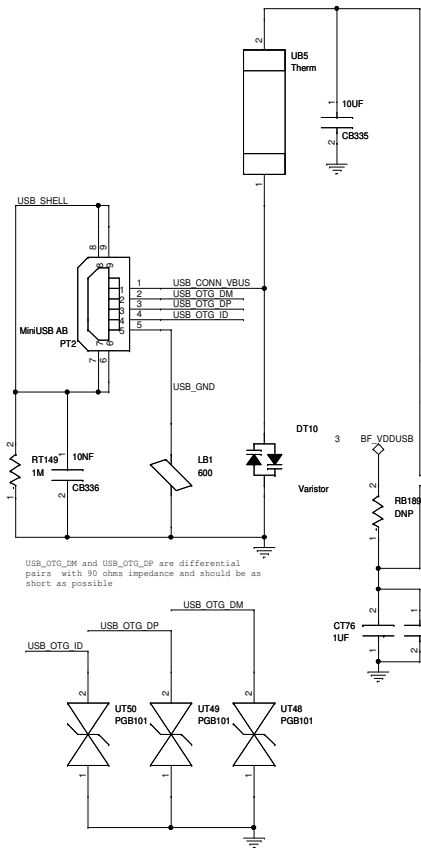
Title			BF524 POWER		
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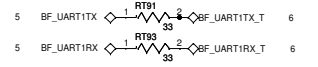
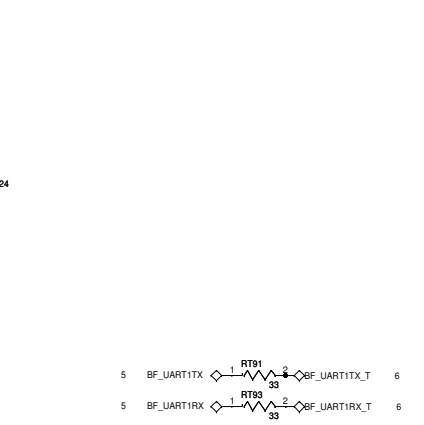
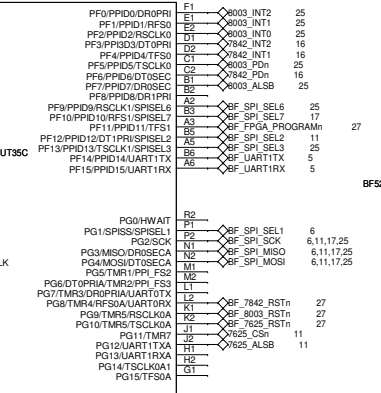
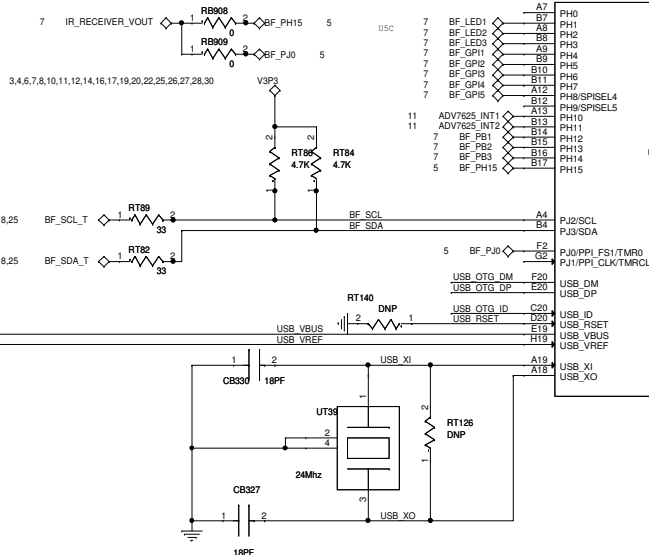


SDRAM should be as close to the BF524 as possible

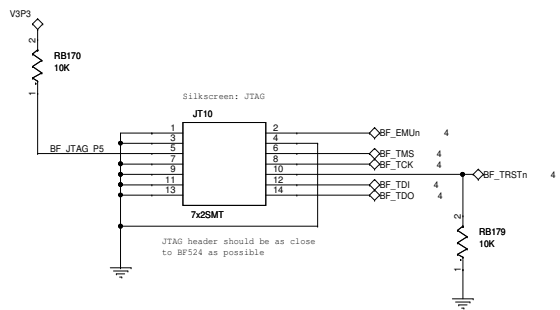




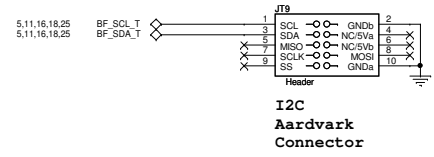
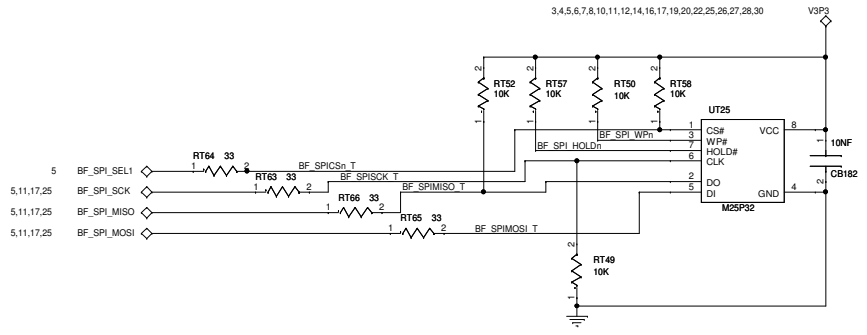
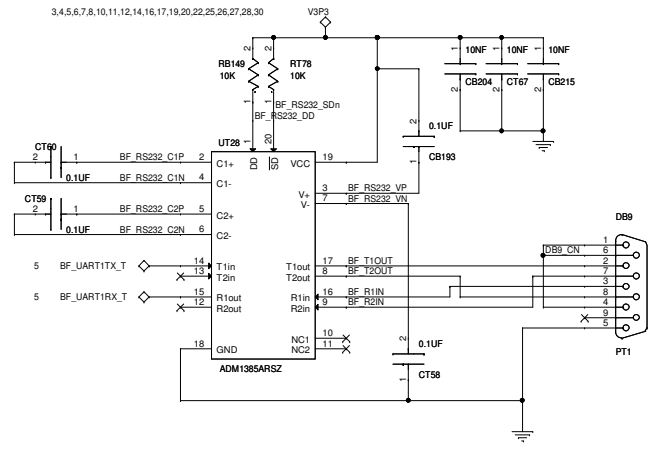
USB_OTG_DM and USB_OTG_DP are differential pairs with 90 ohms impedance and should be as short as possible



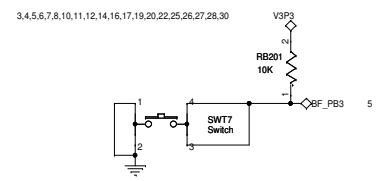
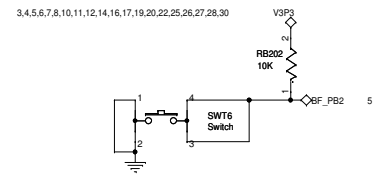
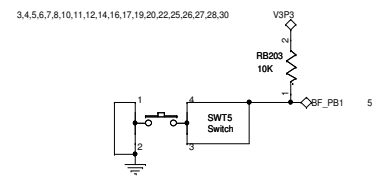
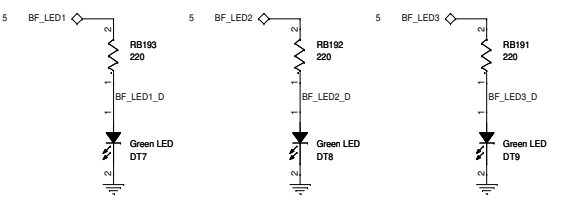
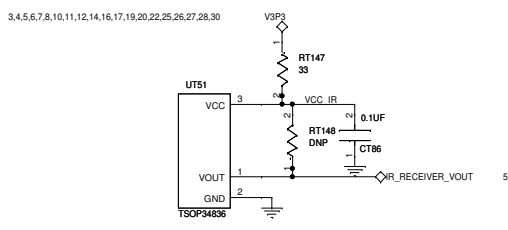
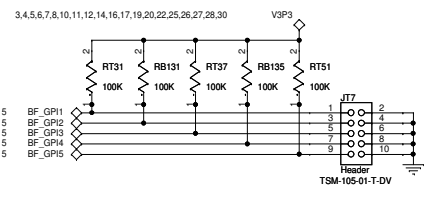
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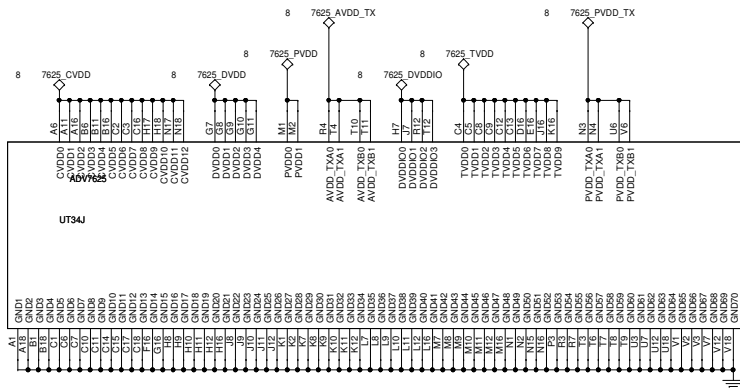
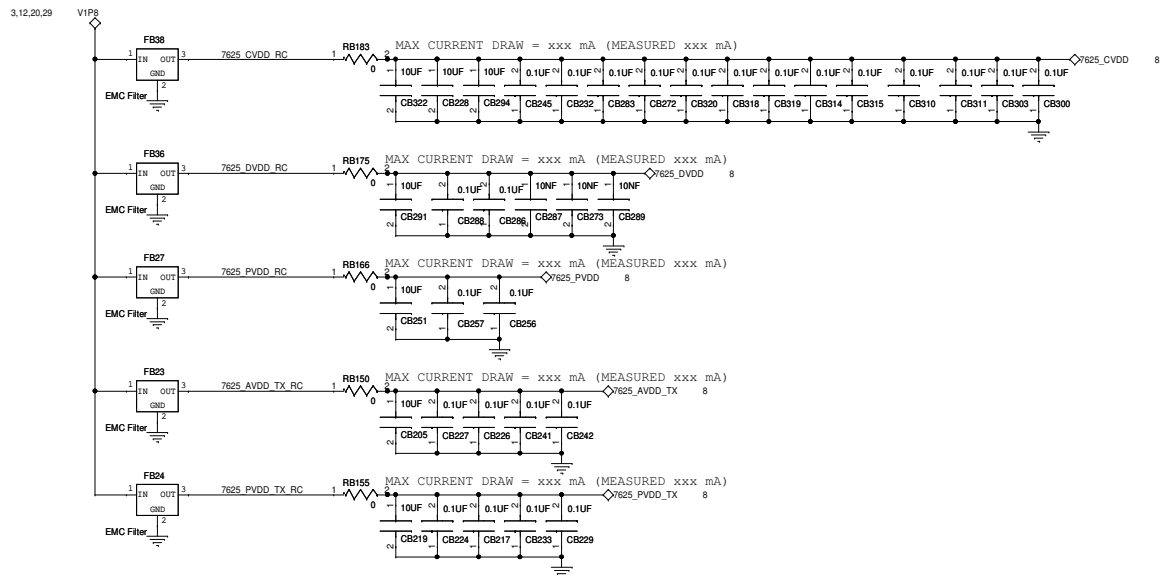
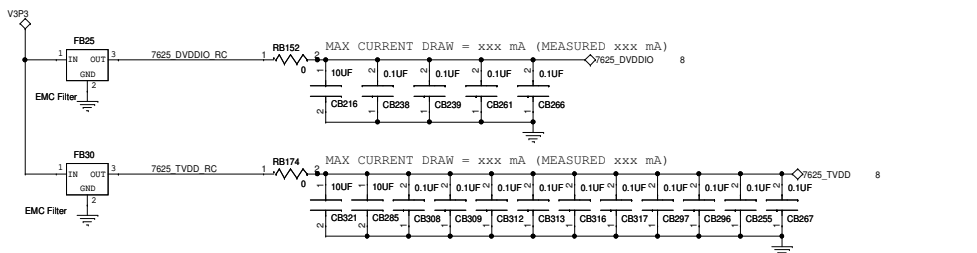
Title		BF524 FLASH / JTAG / RS232	
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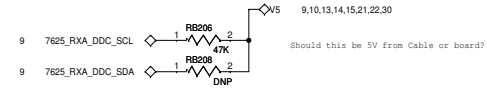
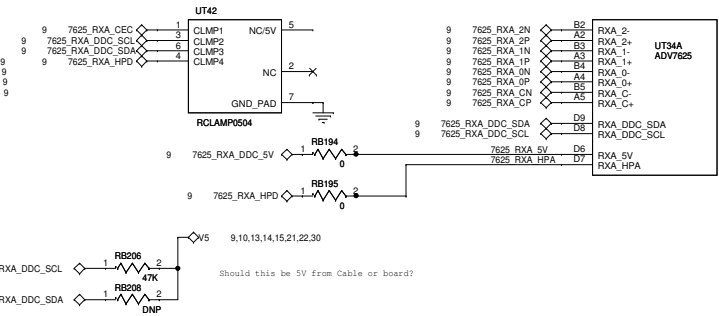
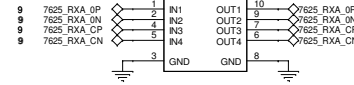
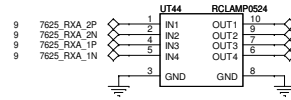
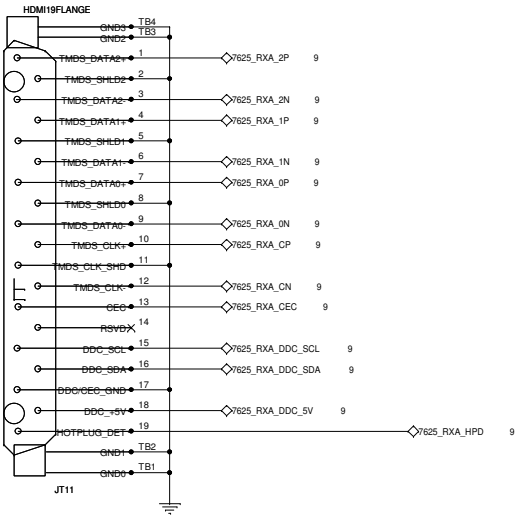
Title		
BF524 GP INPUTS / OUTPUTS		
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NOTE: ADV7625 NOT POPULATED ON EVAL-ADV8003-SMZ-P OR EVAL-ADV8005-SMZ-P

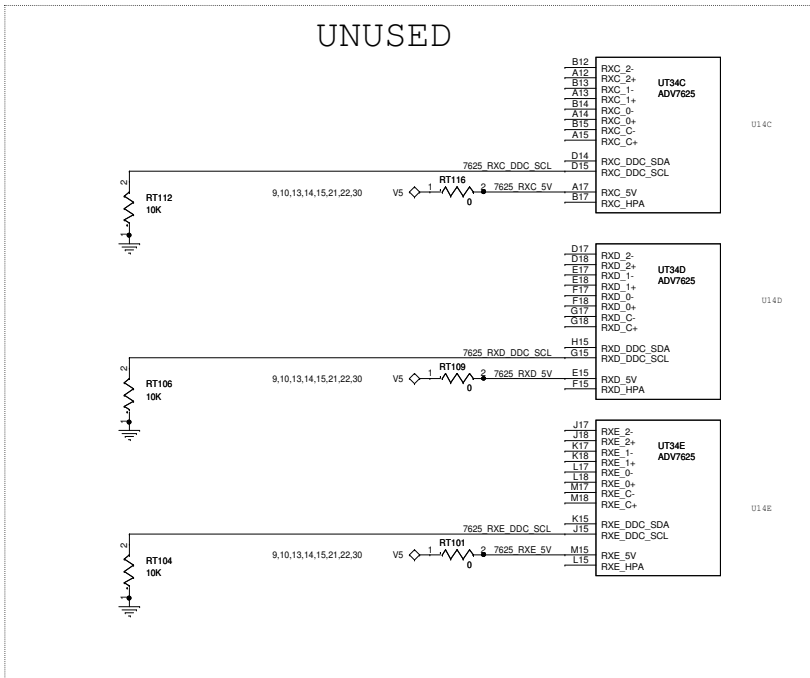
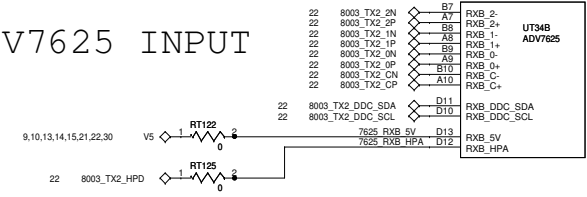
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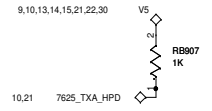
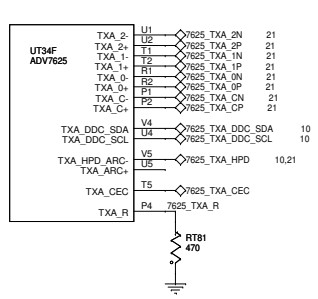
NOTE: ADV7625 NOT POPULATED ON EVAL-ADV8003-SMZ-P OR EVAL-ADV8005-SMZ-P



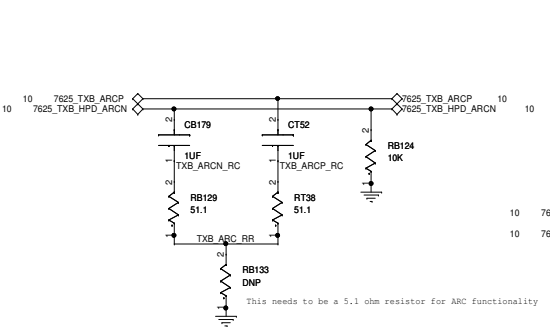
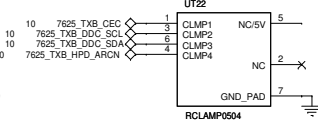
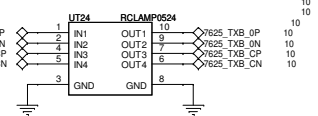
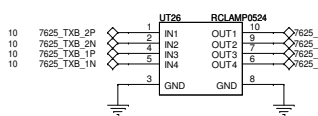
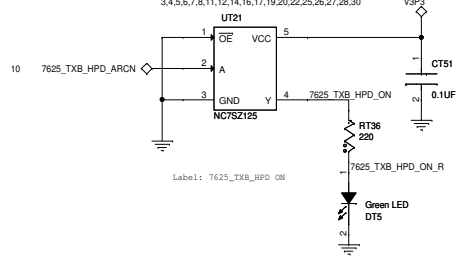
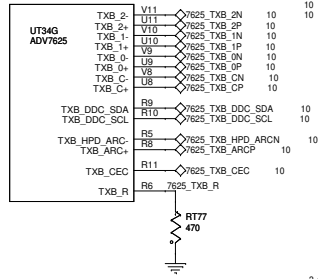
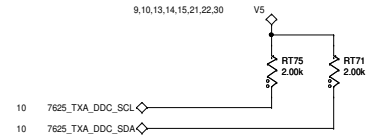
ADV8003 OUTPUT CONNECTED TO ADV7625 INPUT



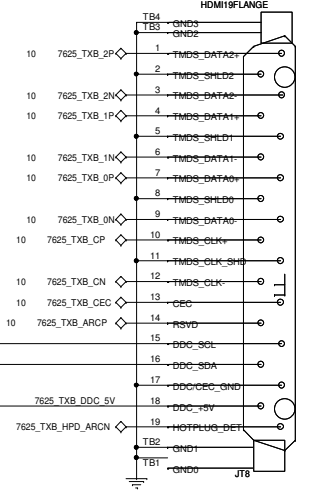
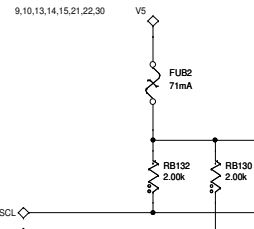
NOTE: ADV7625 NOT POPULATED ON EVAL-ADV8003-SMZ-P or EVAL-ADV8005-SMZ-P



THIS GOES TO ADV8003 HDMI INPUT ON-BOARD SO HPD NEEDS TO BE PULLED UP. CAN BYPASS BUT MIGHT CAUSE CONFUSION WHEN EXISTING SCRIPTS ARE USED.



This needs to be a 5.1 ohm resistor for ARC functionality

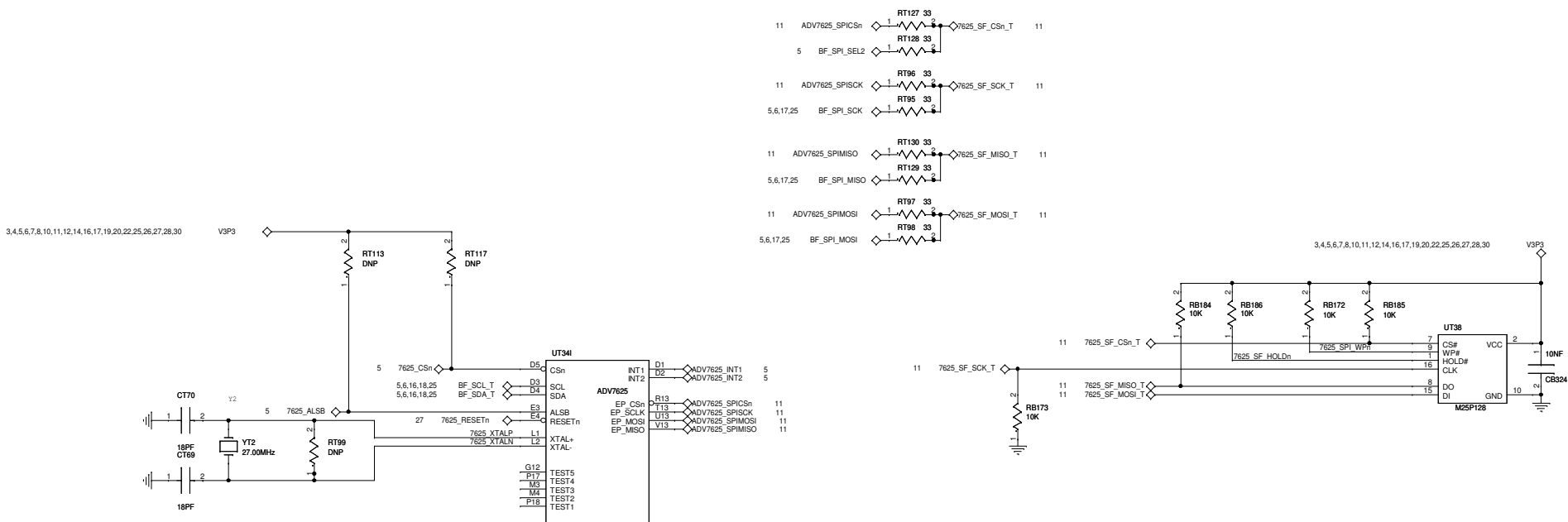


HDMI OUTPUT B

Title			ADV7625 HDMI OUTPUTS
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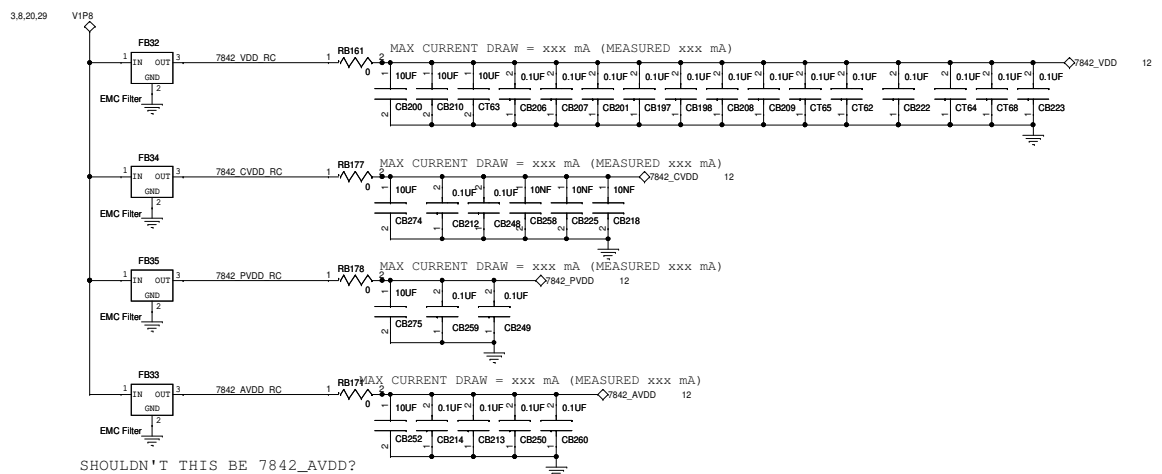
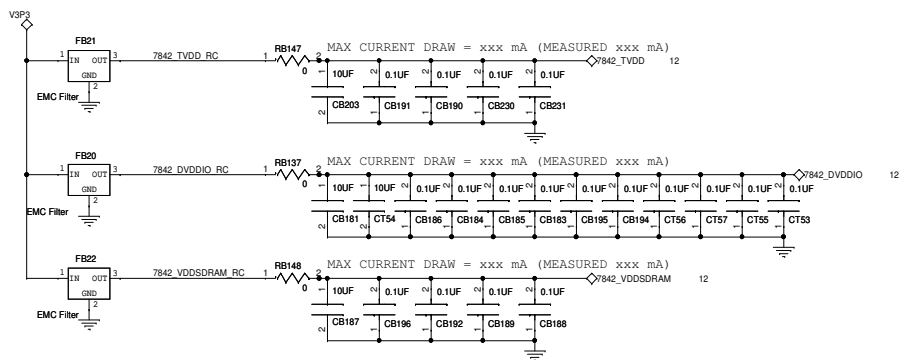
NOTE: ADV7625 NOT POPULATED ON EVAL-ADV8003-SMZ-P OR EVAL-ADV8005-SMZ-P

UT34H		
HOME - PRO	ADV7625	
U14	P0 - AP1_IN_MCLK	AP1_OUT_MCLK
U15	P1 - AP1_IN_SCLK	AP1_OUT_SCLK
U16	P2 - AP1_IN_IN5	AP1_OUT5
U15	P3 - AP1_IN_IN4	AP1_OUT4
U16	P4 - AP1_IN_IN3	AP1_OUT3
U17	P5 - AP1_IN_IN2	AP1_OUT2
U17	P6 - AP1_IN_IN1	AP1_OUT1
U17	P7 - AP1_IN_IN0	AP1_OUT0
T14	P8 - AP2_IN_MCLK	AP2_OUT_MCLK
T15	P9 - AP2_IN_SCLK	AP2_OUT_SCLK
T16	P10 - AP2_IN_IN5	AP2_OUT5
T16	P11 - AP2_IN_IN4	AP2_OUT4
T16	P12 - AP2_IN_IN3	AP2_OUT3
T17	P13 - AP2_IN_IN2	AP2_OUT2
T17	P14 - AP2_IN_IN1	AP2_OUT1
T17	P15 - AP2_IN_IN0	AP2_OUT0
P16	HS	
P16	VS	
T18	DE	
R18	PCLK	
J3	AUD1_IN - NC	
K3	AUD1_SCLK - NC	
K4	AUD1_LRCLK - NC	
K4	AUD2_IN - NC	
L3	AUD2_SCLK - NC	
L4	AUD2_LRCLK - NC	

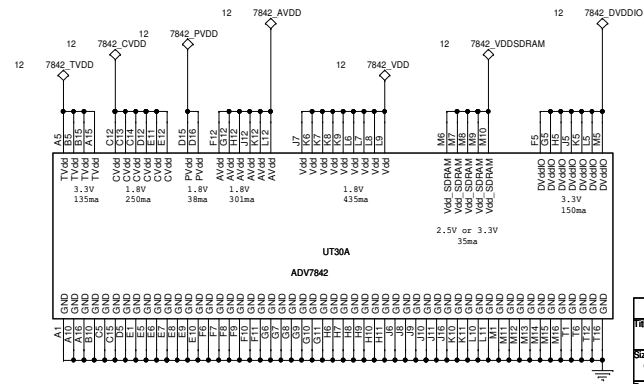


ADV7625 I2C ADDRESS:
 ALSB Low : IO Map address is 0xB0 (default)
 ALSB High : IO Map address is 0xB2

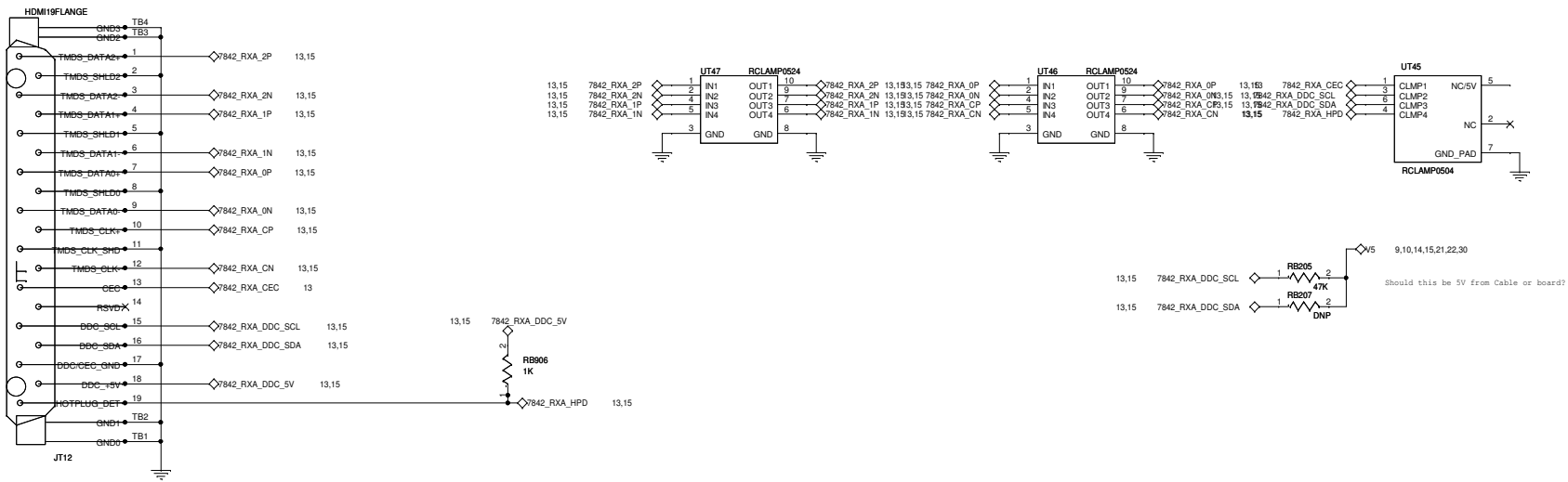
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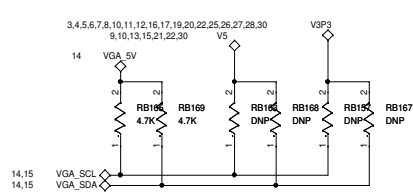
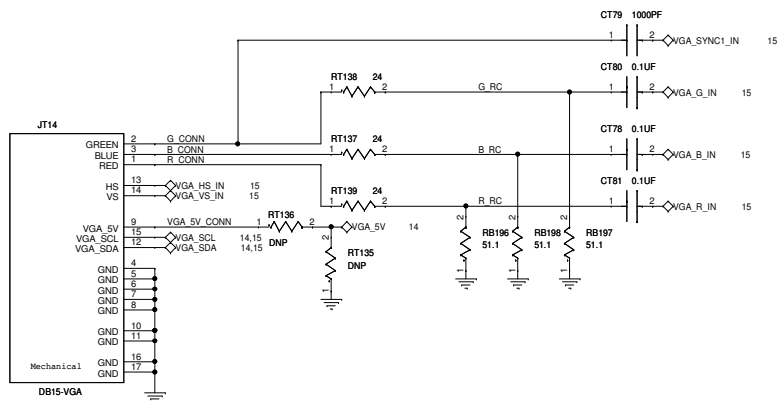
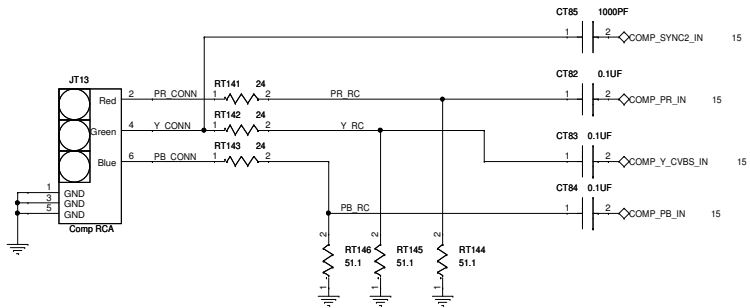


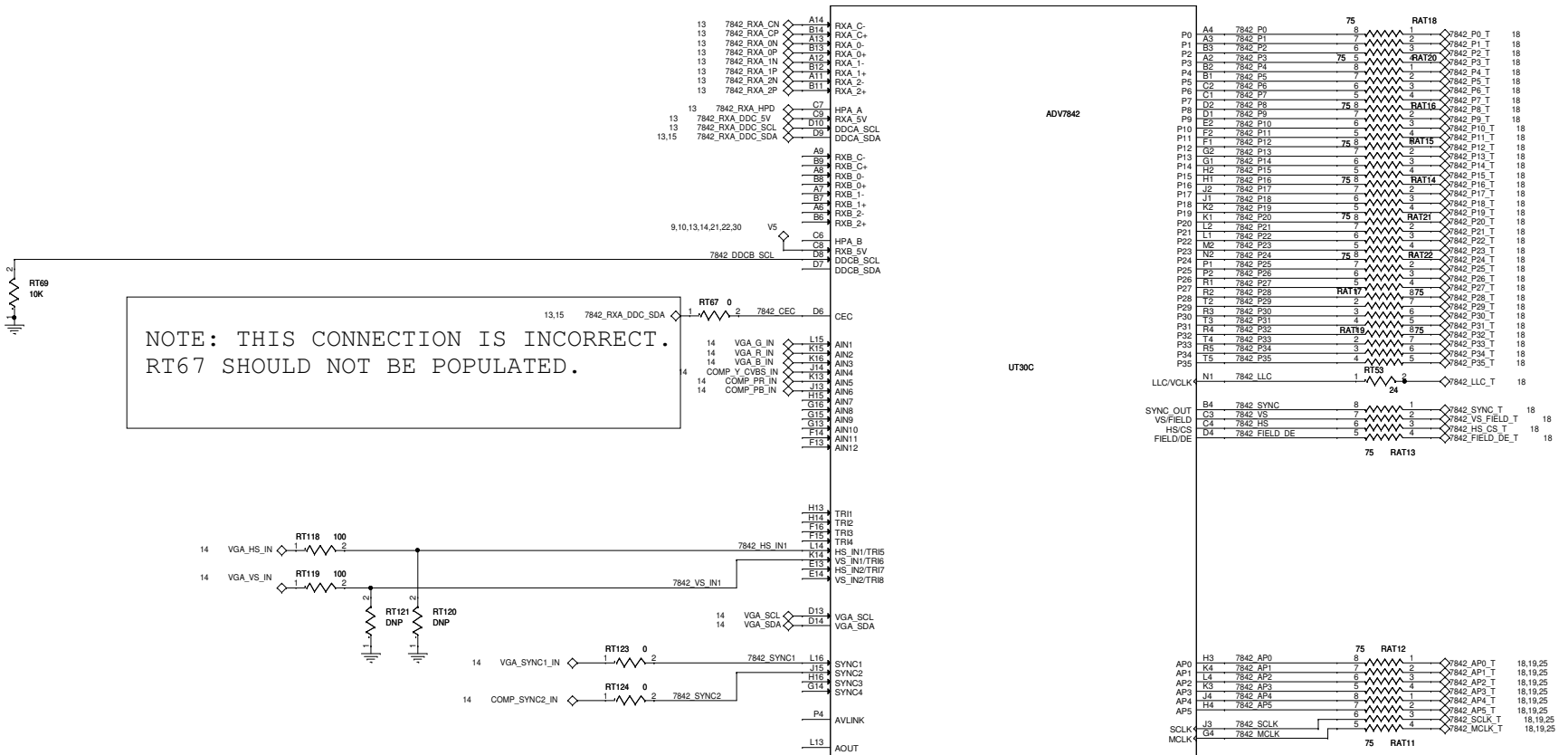
SHOULDN'T THIS BE 7842_AVDD?



Title			ADV7842 POWER
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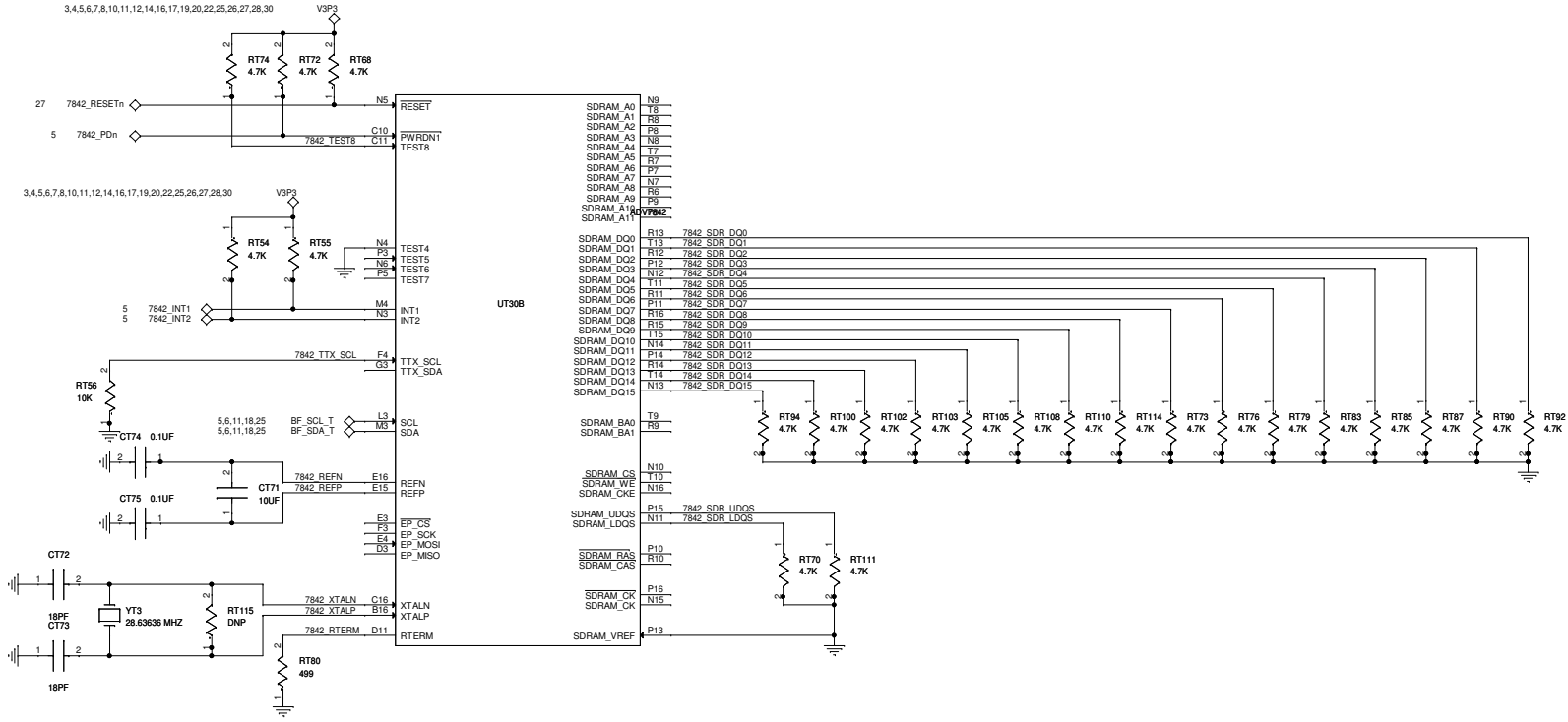






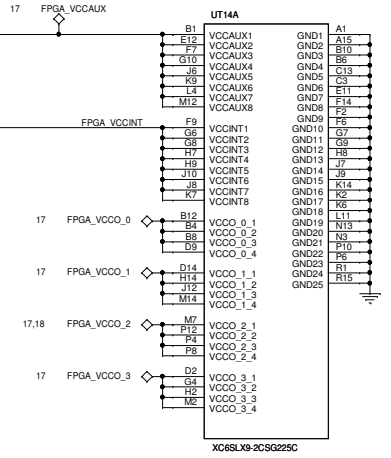
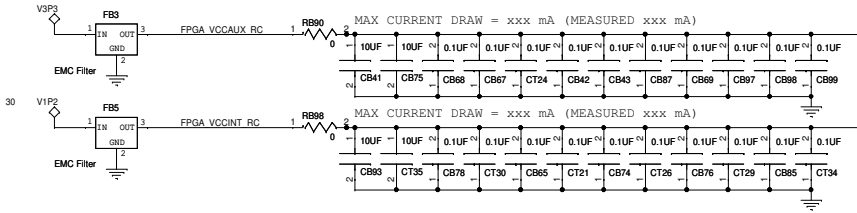
NOTE: THIS CONNECTION IS INCORRECT.
RT67 SHOULD NOT BE POPULATED.

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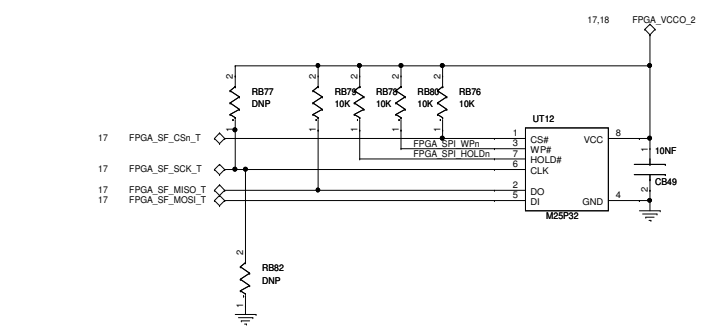
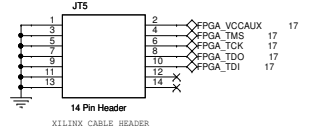
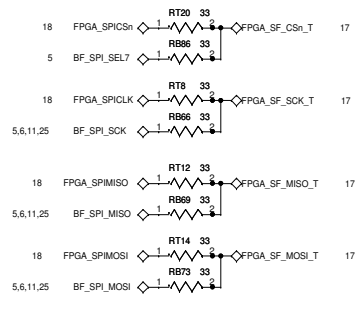
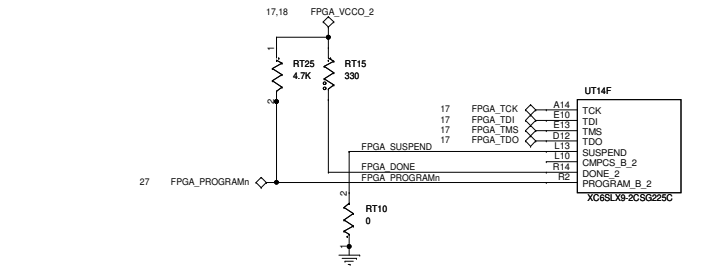
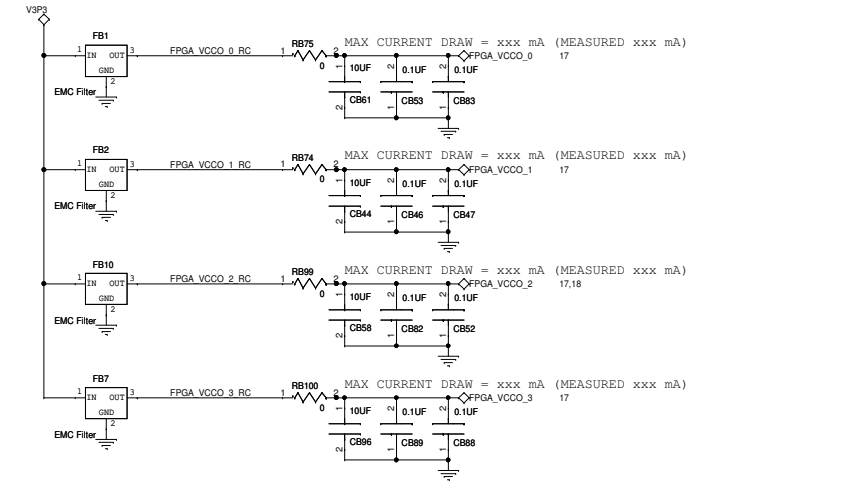


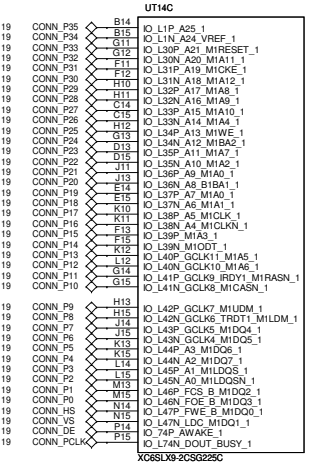
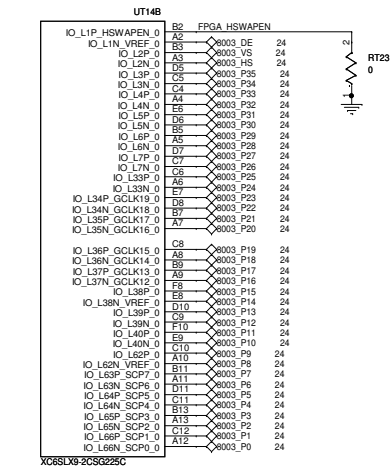
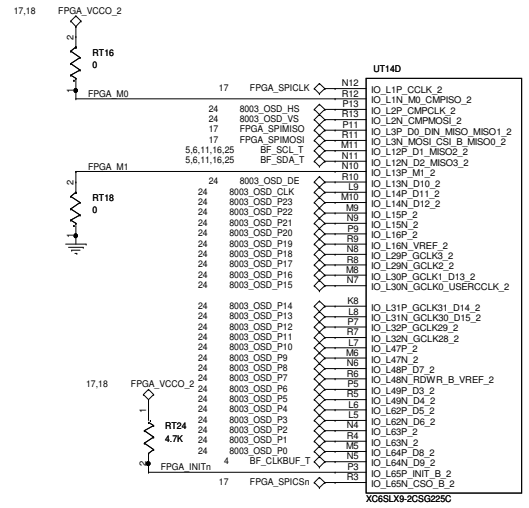
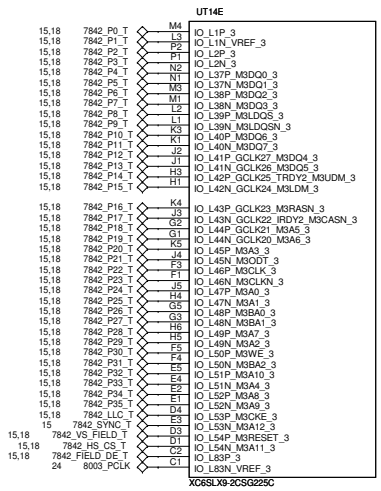
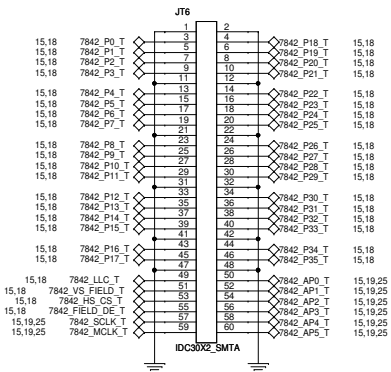
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ADV7842 SDRAM		
Size	Document Number	Rev
C	ADV9003 Advantiv™ Video Evaluation Board	0.2
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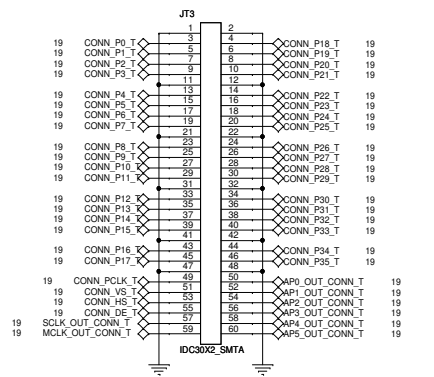
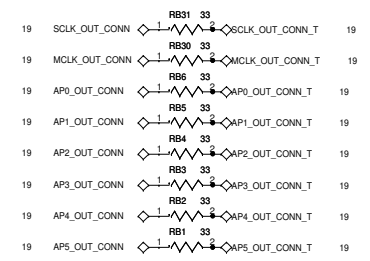
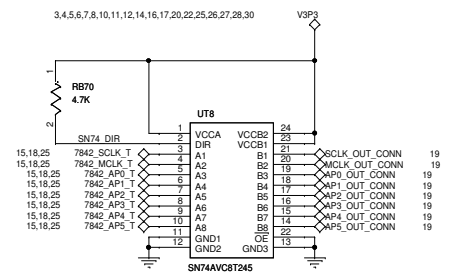
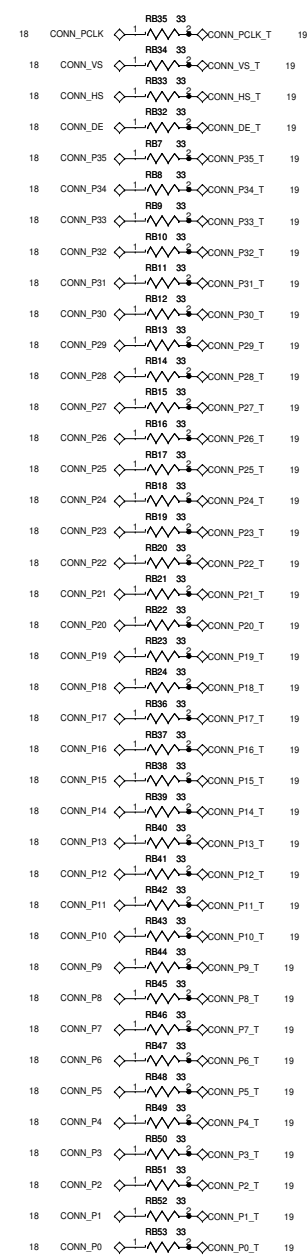
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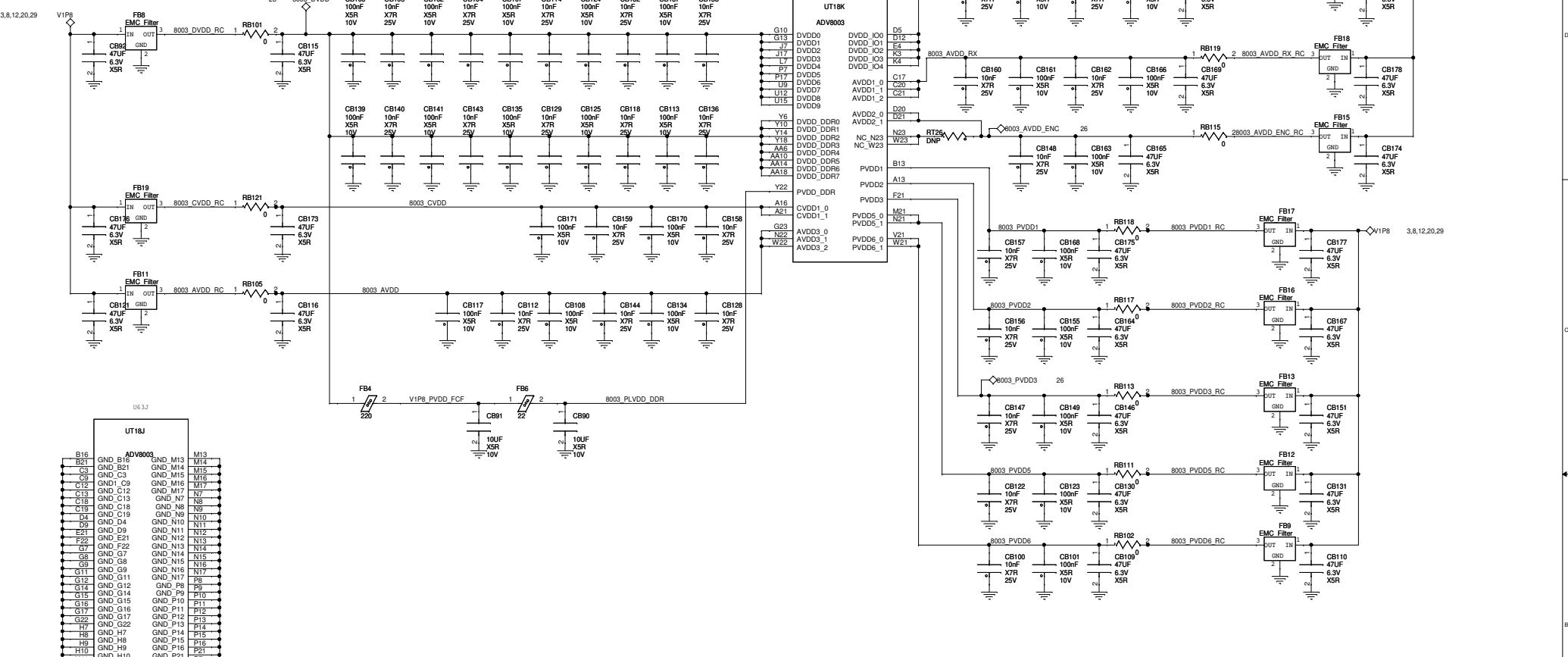


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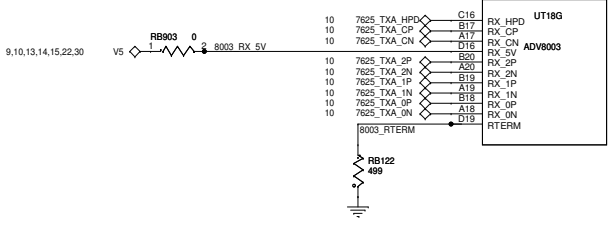
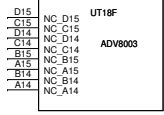


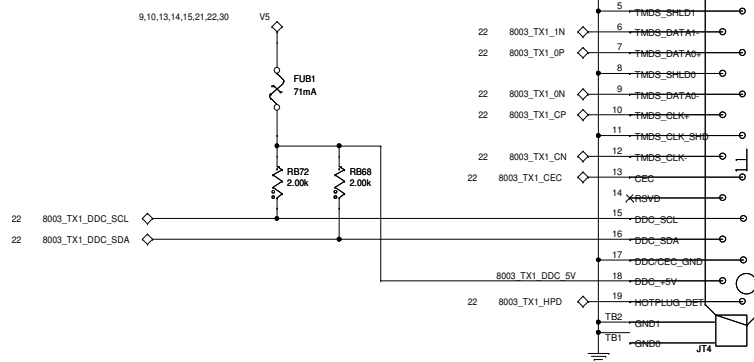
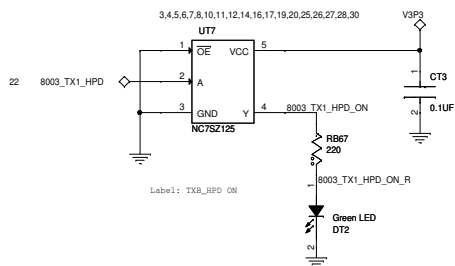
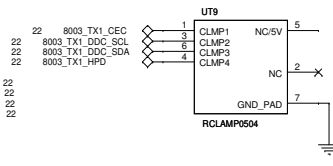
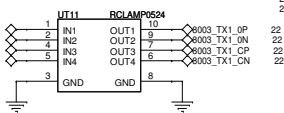
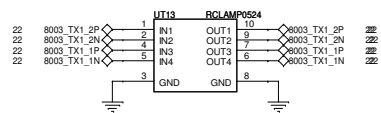
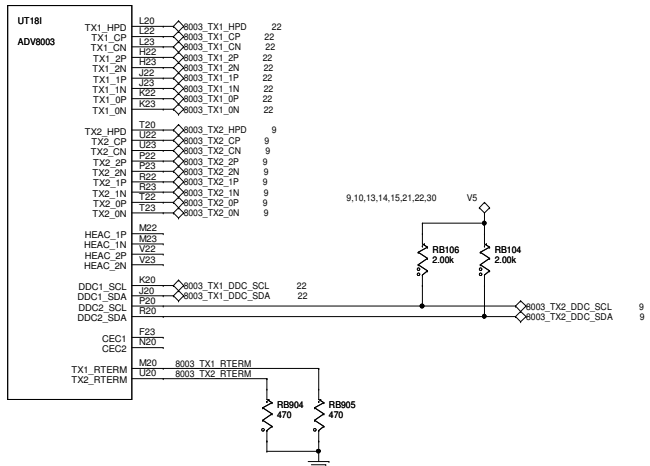


UT18J		
B16	ADV8003	M13
B21	GND_B1	GND_M13
C3	GND_B21	GND_M14
C9	GND_C3	GND_M15
C12	GND_C9	GND_M16
C13	GND_C12	GND_M17
C18	GND_C13	GND_N7
C19	GND_C18	GND_N8
D4	GND_C19	GND_N9
D9	GND_D4	GND_N10
E21	GND_D9	GND_N11
F22	GND_E21	GND_N12
G7	GND_F22	GND_N13
G8	GND_G7	GND_N14
G9	GND_G8	GND_N15
G11	GND_G9	GND_N16
G12	GND_G11	GND_N17
G14	GND_G12	GND_P8
G15	GND_G14	GND_P9
G16	GND_G15	GND_P10
G17	GND_G16	GND_P11
G22	GND_G17	GND_P12
H8	GND_G22	GND_P13
H9	GND_H8	GND_P14
H10	GND_H9	GND_P15
H11	GND_H10	GND_P16
H12	GND_H11	GND_P17
H13	GND_H12	GND_P18
H14	GND_H13	GND_P19
H15	GND_H14	GND_P20
H16	GND_H15	GND_R11
H17	GND_H16	GND_R12
H20	GND_H17	GND_R13
H21	GND_H20	GND_R14
J8	GND_H21	GND_R15
J9	GND_J8	GND_R16
J10	GND_J9	GND_R17
J11	GND_J10	GND_R18
J12	GND_J11	GND_T3
J13	GND_J12	GND_T4
J14	GND_J13	GND_T5
J15	GND_J14	GND_T8
J16	GND_J15	GND_T9
J21	GND_J16	GND_T10
K7	GND_J21	GND_T11
K8	GND_K7	GND_T12
K9	GND_K8	GND_T13
K10	GND_K9	GND_T14
K11	GND_K10	GND_T15
K12	GND_K11	GND_T16
K13	GND_K12	GND_T17
K14	GND_K13	GND_T21
K15	GND_K14	GND_U7
K16	GND_K15	GND_U8
K17	GND_K16	GND_U10
K21	GND_K17	GND_U11
L8	GND_K21	GND_U14
L9	GND_L8	GND_U16
L10	GND_L9	GND_U17
L11	GND_L10	GND_U21
L12	GND_L11	GND_V20
L13	GND_L12	GND_V20
L14	GND_L13	GND_V8
L15	GND_L14	GND_V8
L16	GND_L15	GND_Y12
L17	GND_L16	GND_Y16
L21	GND_L17	GND_Y20
M7	GND_M7	GND_Y23
M8	GND_M8	GND_AA2
M9	GND_M9	GND_AA3
M10	GND_M9	GND_AA12
M11	GND_M10	GND_AA16
M12	GND_M11	GND_AA21
	GND_M12	GND_AA22

WARNING ABOUT ADV8003/ADV8005 N23/W23:
 * In ADV8003, N23 and W23 pins are No Connect
 * In ADV8005, N23 is AVDD3 (1.8V) and W23 is AVDD4 (1.8V)
 * Therefore, it is important to ensure that RT26 is not populated
 * We plan to design a new PCB for ADV8005 in 2015.

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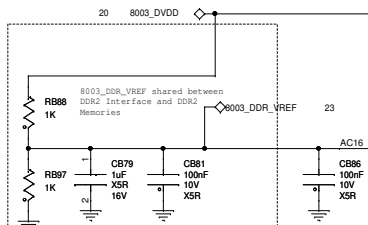
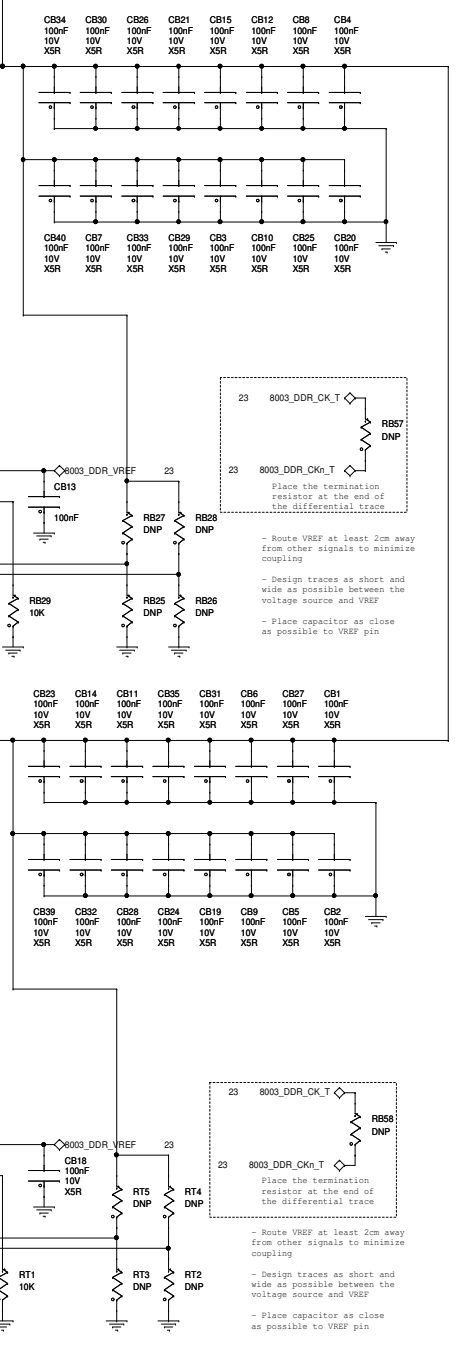
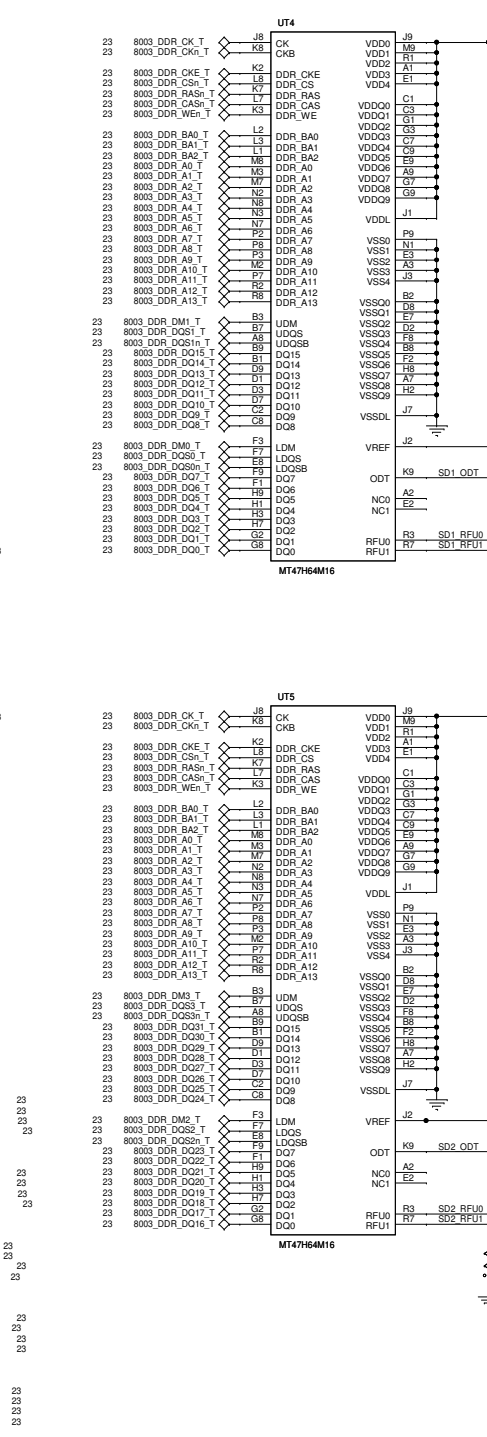
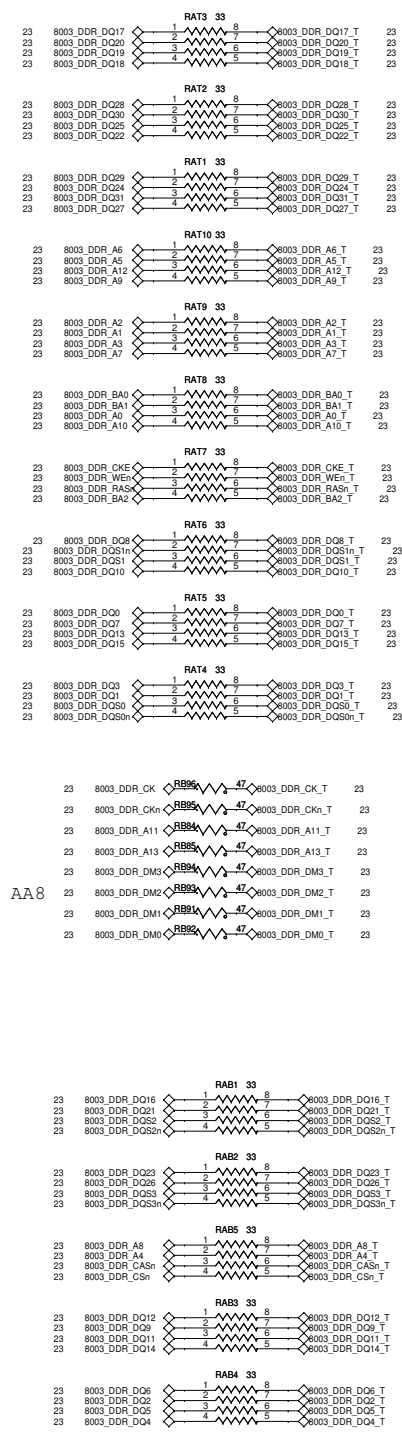
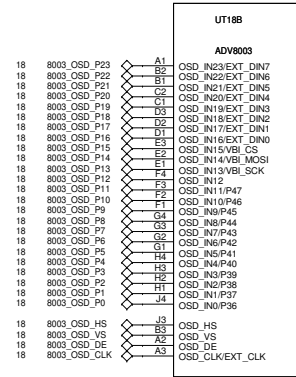
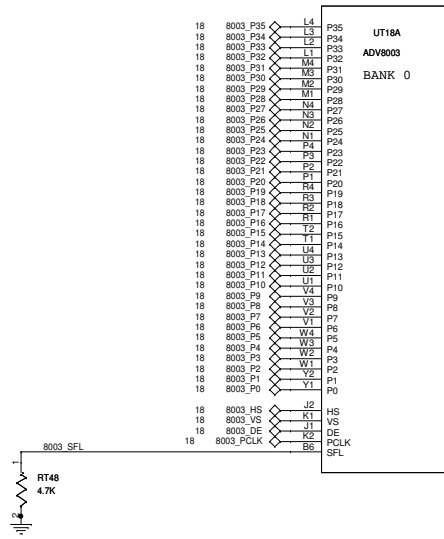


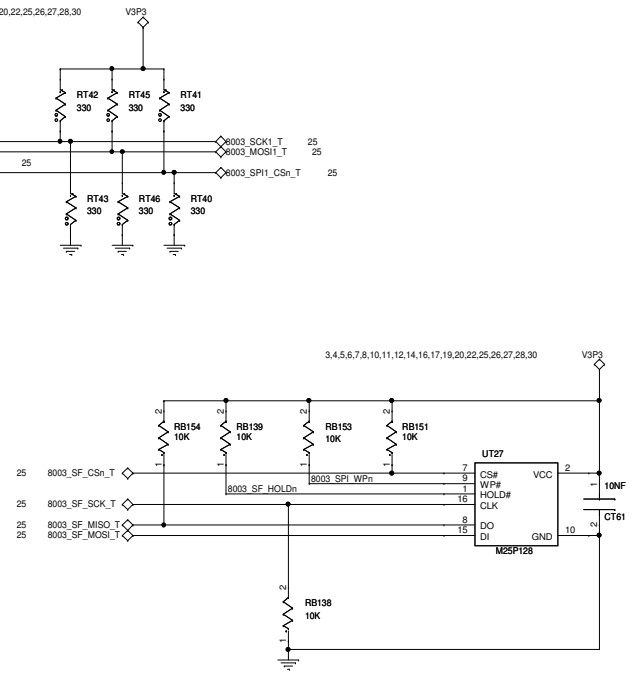
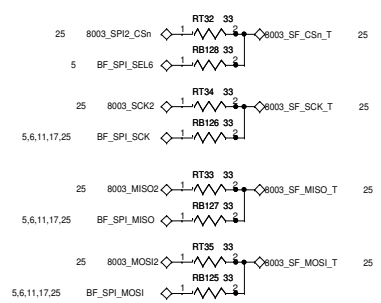
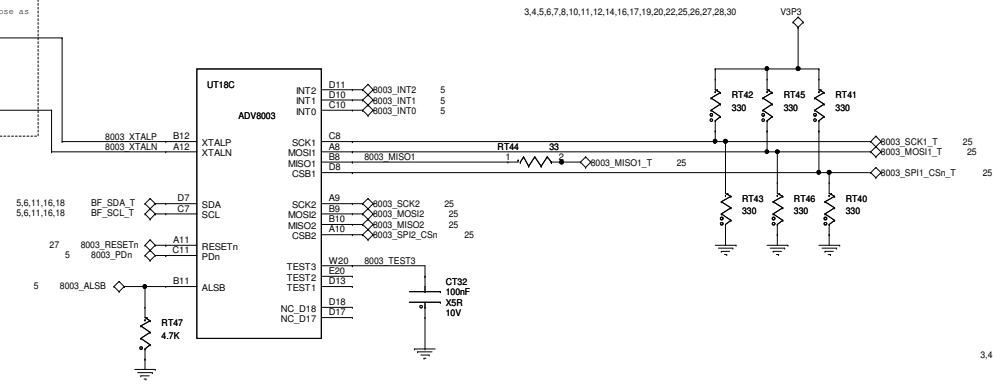
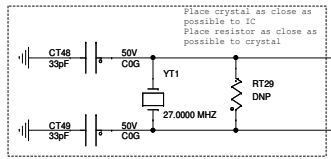
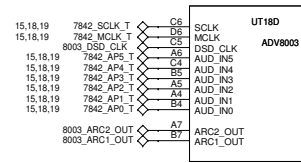
Table listing pin connections for UT18E and ADV8003, including signals like DDR_CK, DDR_CKE, DDR_CSB, DDR_RASn, DDR_CASn, DDR_WEn, and data bus signals.

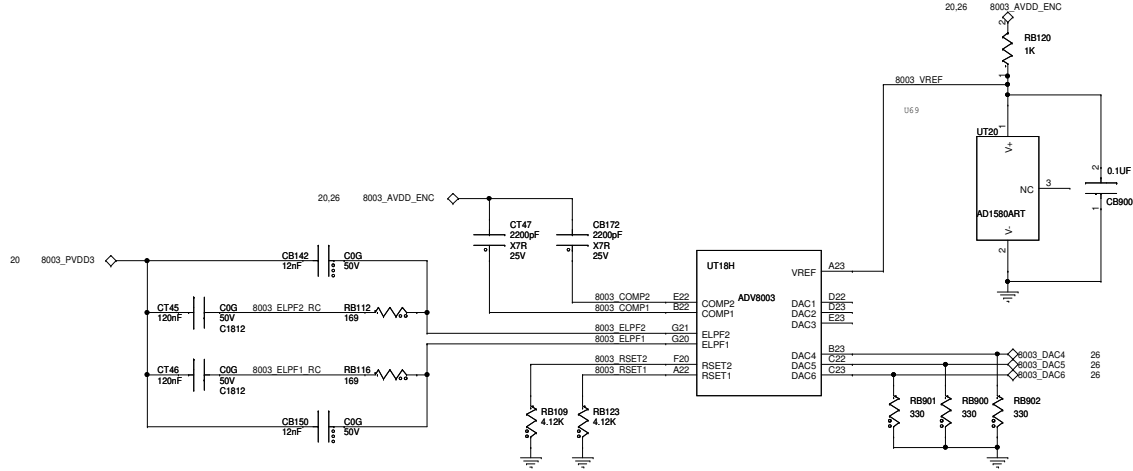


NOTE ABOUT ADV8003/ADV8005 AA8:
* In ADV8003, AA8 is No Connect
* In ADV8005, AA8 is DDR_A[13]
* If designing a board for ADV8003, we recommend to leave AA8 as No Connect rather than what we did here.

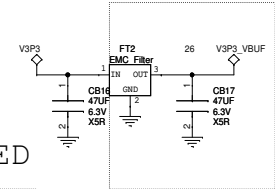
- DDR2 Memory Layout Guidelines:
1. DRS2 Modules and ADV8003 to be placed as close together as possible.
2. Balanced T-routing if possible for all shared connections between ADV8003 and DRS2 Memories
3. All traces to be impedance matched.
4. All traces to be routed on the same layer(s) - outer layer(s) if possible
5. CK and CS, DDR_DQ33 and DDR_DQ35, DDR_DQ37, DDR_DQ39, DDR_DQ41, DDR_DQ43, DDR_DQ45, DDR_DQ47, DDR_DQ49, DDR_DQ51, DDR_DQ53, DDR_DQ55, DDR_DQ57, DDR_DQ59, DDR_DQ61, DDR_DQ63, DDR_DQ65, DDR_DQ67, DDR_DQ69, DDR_DQ71, DDR_DQ73, DDR_DQ75, DDR_DQ77, DDR_DQ79, DDR_DQ81, DDR_DQ83, DDR_DQ85, DDR_DQ87, DDR_DQ89, DDR_DQ91, DDR_DQ93, DDR_DQ95, DDR_DQ97, DDR_DQ99
6. Match CK trace length to CK trace length to 20mil (0.5mm)
7. There are 4 x byte-wide data lines on the DDR2 interface
8. DDR_DMS, DDR_DQ03, DDR_DQ05, DDR_DQ07, DDR_DQ09, DDR_DQ11, DDR_DQ13, DDR_DQ15, DDR_DQ17, DDR_DQ19, DDR_DQ21, DDR_DQ23, DDR_DQ25, DDR_DQ27, DDR_DQ29, DDR_DQ31, DDR_DQ33, DDR_DQ35, DDR_DQ37, DDR_DQ39, DDR_DQ41, DDR_DQ43, DDR_DQ45, DDR_DQ47, DDR_DQ49, DDR_DQ51, DDR_DQ53, DDR_DQ55, DDR_DQ57, DDR_DQ59, DDR_DQ61, DDR_DQ63, DDR_DQ65, DDR_DQ67, DDR_DQ69, DDR_DQ71, DDR_DQ73, DDR_DQ75, DDR_DQ77, DDR_DQ79, DDR_DQ81, DDR_DQ83, DDR_DQ85, DDR_DQ87, DDR_DQ89, DDR_DQ91, DDR_DQ93, DDR_DQ95, DDR_DQ97, DDR_DQ99
9. Isolate data and address/control traces to each other by at least 20mil
10. Place 47-ohm series termination resistors as close to source (ADV8003) as possible on the following signals
11. Keep stubs short on CK or CS lines
12. Do not share a DQS signal resistor pack with a non-data-group signal
13. Route VREF as far away from other signals as possible



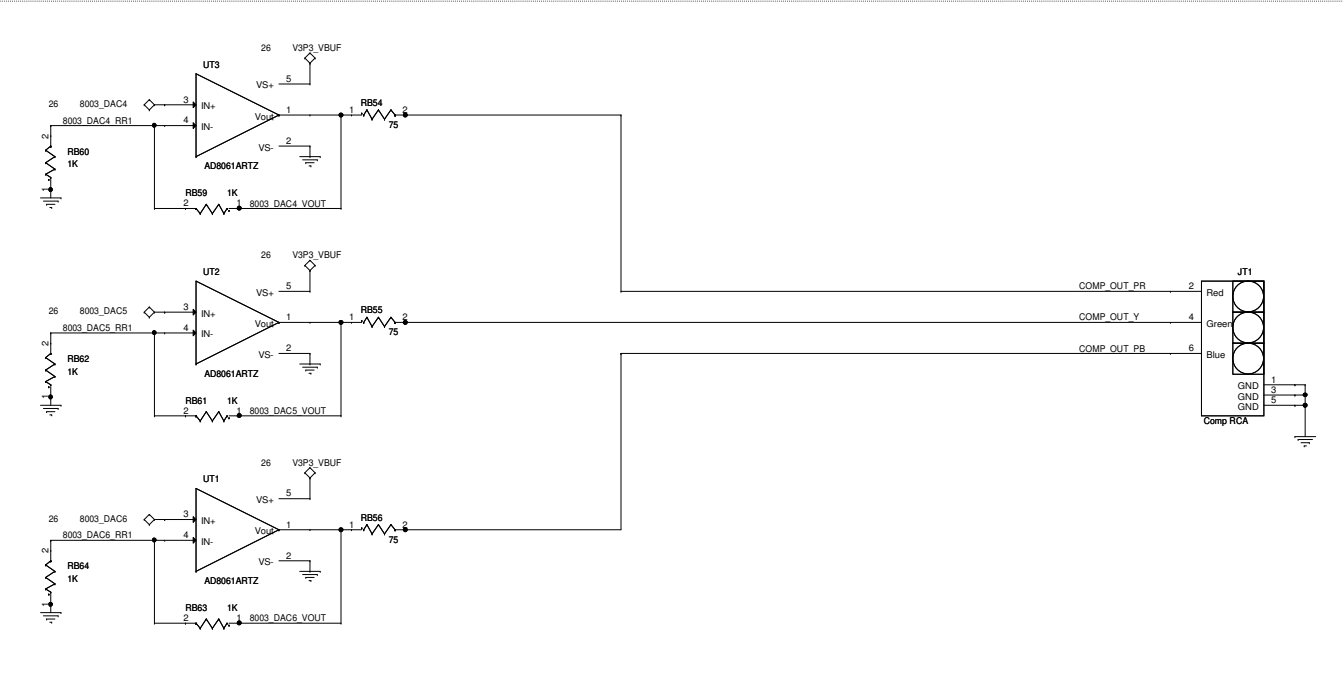




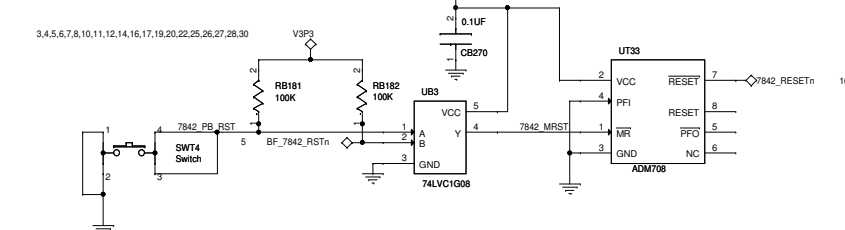
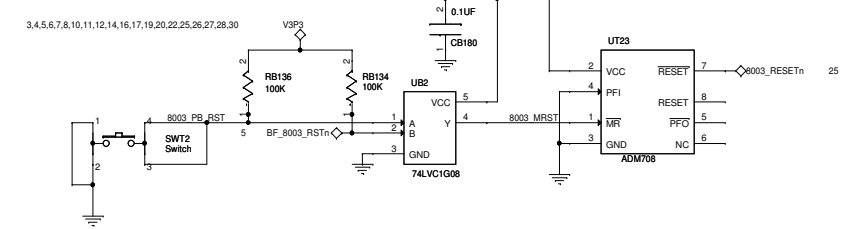
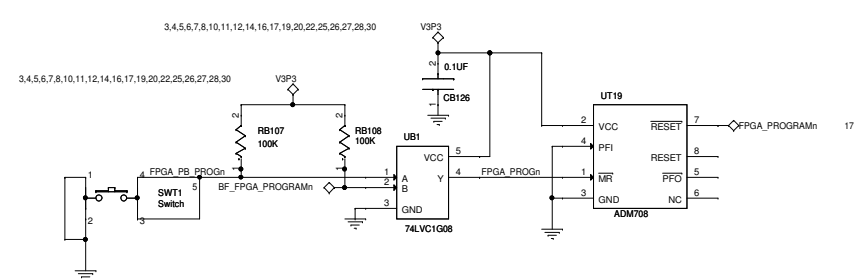
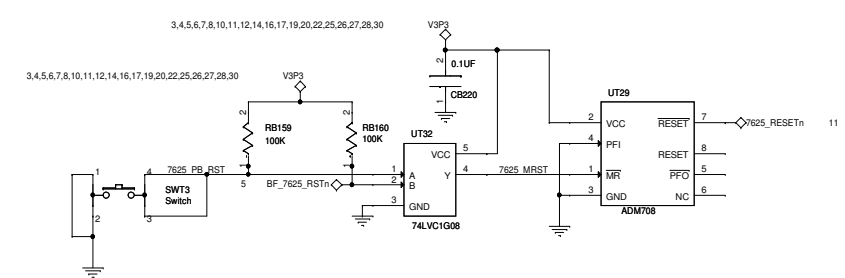
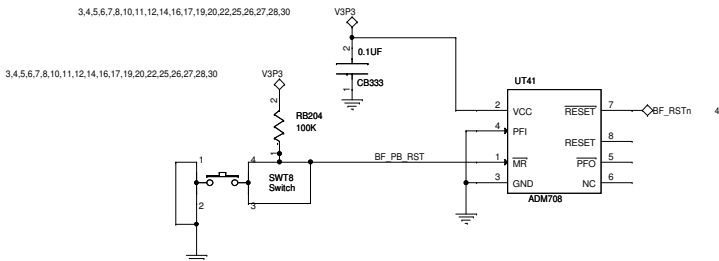
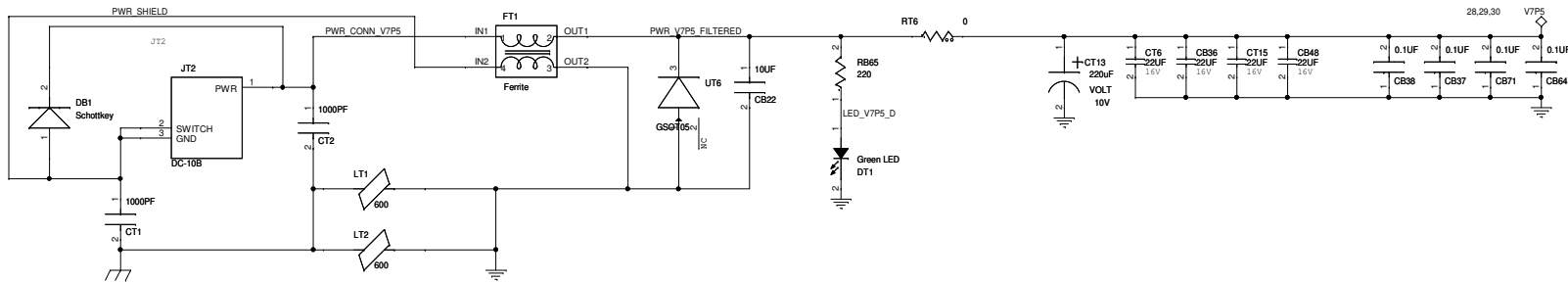
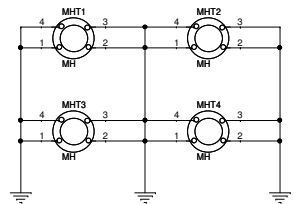
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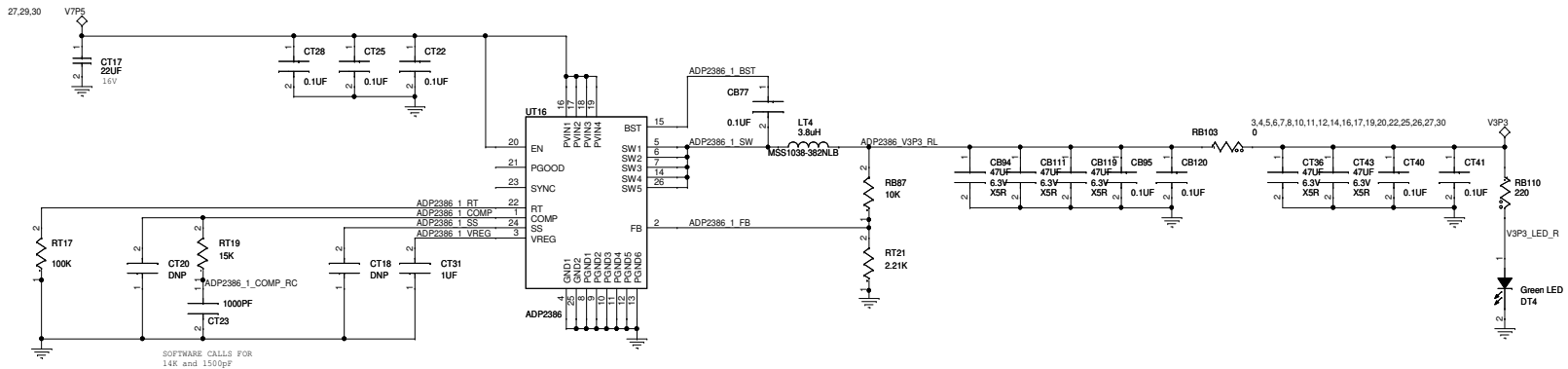
BOXED COMPONENTS NOT POPULATED



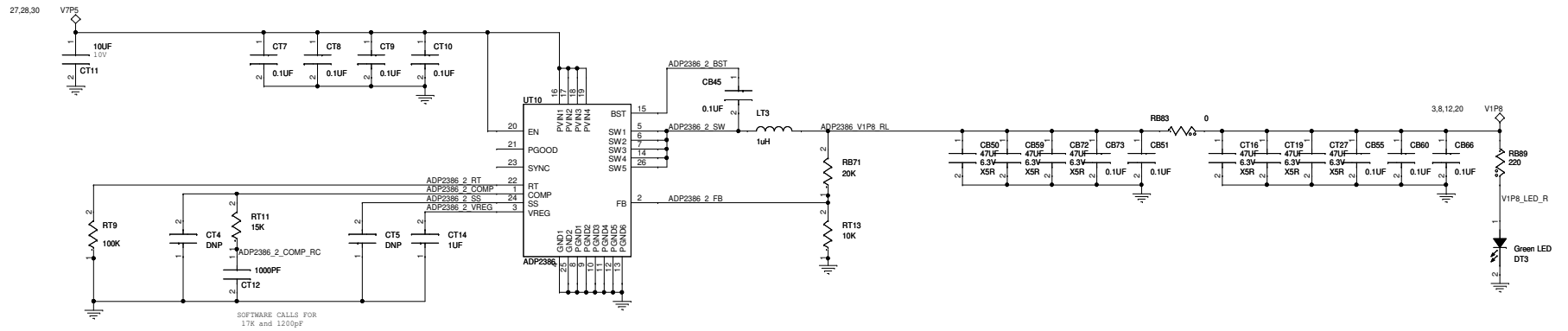
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SWITCHING REGULATOR FOR 3.3V		
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SWITCHING REGULATOR FOR 1.8V		
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