Application Note

Crystal Design Considerations for ADV740x Video Decoders

Objective

Design guide for the external circuitry of the oscillator in order to achieve frequency stability and accuracy.

We will use, as an example, the oscillator circuit of the video decoder chips such as the ADV7403. These chips typically require a crystal with nominal frequency of 28.63636MHz[1] and 50ppm of frequency stability in fundamental mode. The specifications of the crystal used are given in Table I.

1. Oscillator Description

In this part we briefly describe the typical crystal oscillators that are used in Analog Devices decoders video chips.

Table I. Specifications of crystal oscillator used on ADV7403 evaluation boards [2]

Characteristics	Value	Unit
Holder type	HC49	
Nominal frequency	28.63636	MHz
Mode of oscillation	Fund	
Frequency calibration (at 25°C)	+/-0.0030	%
Frequency temperature stability tolerance	+/-0.0050	%
Operating Temperature range	-10 ~ +60	°C
Equivalent Resistance (max)	30	Ω
Load capacitance	30	pF
Drive level	100	μW
Shunt capacitance (max)	7.0	pF
Aging for year	+/-0.0003	%

[1]The 27MHz frequency for previous decoders was changed to 28.63636MHz to avoid intermodulation noise between the sampling clock and the line lock clock.

1.1. Circuitry

Figure 1 shows the block description of the oscillator used in the video decoders. The equivalent circuit of the quartz crystal is shown on Figure 2. C_0 is the shunt or static capacitance of the crystal. R_1 is the motional resistance, L_1 is the motional inductance and C_1 is the motional capacitance. R_1, L_1 and C_1 are determined by the mechanical properties of the crystal (i.e. they are in the motional arm of the crystal and their effect only exists when the crystal is oscillating) [1]. R is an external shunt resistance with a recommended value of 1MΩ for the ADV740x's.

1.2. Series and parallel resonances

The effective reactance curve of the crystal is shown in Figure 3. The range of frequency in area 1 and 2 is called the fundamental mode.

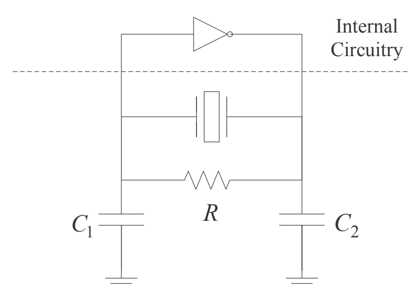

Figure 1. Oscillator block diagram.

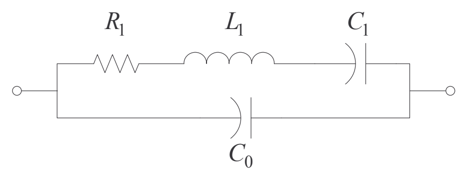

Figure 2. Crystal representation.

There are two cases of resonance in the fundamental mode:

- *Series resonance*: Series resonance occurs when the motional inductance L_1 is resonating with the motional capacitance C_1. The series resonant frequency is given by (approximately)

$$f_s = \frac{1}{2\pi\sqrt{L_1 C_1}}$$

- *Parallel resonance*: This type of resonance is the one we consider in this note. It occurs when a load capacitance C_L is connected between the crystal pins. The oscillating frequency of the crystal in parallel resonance is given by (approximately):

$$f_{\text{XTAL}} = f_s\left(\frac{C_1}{2(C_0 + C_L)} + 1\right)$$

Note that the parallel resonance is located within the region 2 of Figure 3 i.e.

$$f_s < f_{\text{XTAL}} < f_a$$

Where f_a is the anti-resonant frequency given by

$$f_a = \frac{1}{2\pi\sqrt{L_1 C_1 (C_1 C_0)/(C_1 + C_0)}}$$

The crystals used for the ADV740x decoders oscillate in parallel resonance mode which we consider in the remainder of this guide. The operating frequency will be referred as the frequency of the crystal in the range of region 2 (Figure 3).

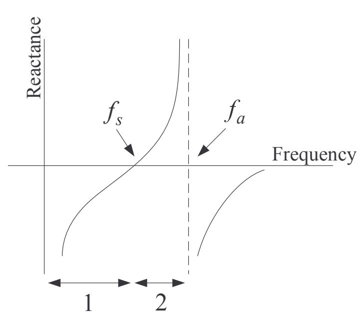

Figure 3. Reactance of the crystal oscillator.

2. Crystal Specifications

This section intends to help designers using the specification given by crystal manufacturers.

2.1. Frequency tolerance

The frequency tolerance refers to the ability of the crystal to oscillate within a limited range of frequency for proper tuning. The manufacturers generally give two specifications related to frequency tolerance:

Frequency calibration tolerance: It corresponds to the maximum deviation from nominal frequency usually at 25°C.

Frequency temperature stability tolerance: It stands for the maximum deviation from nominal frequency when the temperature fluctuates within the operating temperature range.

Application: The frequency calibration tolerance in Table I equals ±0.0030%. The maximum frequency deviation Δf is therefore given by:

$$\Delta f = 26.63636\text{MHz} \cdot 0.0030 \cong 79.909\text{kHz}$$

The unit 'ppm' is often used and refers to 'part per million'. Therefore

$$0.0030\% = \frac{0.0030}{10^2} = \frac{30}{10^6} = 30\text{ppm}$$

2.2. Load capacitance

The load capacitance given in a crystal data sheet specifies the parallel resonance frequency within the tolerance at 25°C. It is therefore important to design a circuit that matches the load capacitance in order to achieve the frequency stipulated by the manufacturer. The load can be calculated based on Figure 4:

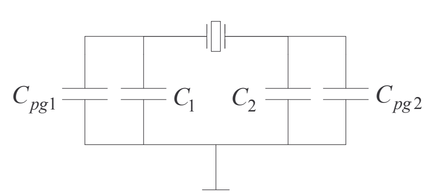

Figure 4. Calculating crystal load capacitance.

$$C_L = \frac{\left(C_{pg1} + C_1\right)\left(C_{pg2} + C_2\right)}{C_{pg1} + C_1 + C_{pg2} + C_2} + C_s$$

C_{pg1} and C_{pg2} are the pin to ground capacitances and C_s the pcb strays capacitance. A good rule of thumb is to approximate C_{pg1} and C_{pg2} to 5pF-10pF and C_s to 2-3pF.

Application: Let $C_{pg1} = C_{pg2} = C_{pg} = 4\text{pF}$ and $C_1 = C_2 = C$. We want to find what should be the value C in order to get a load capacitance $C_L = 30\text{pF}$ (refer to Table I). C is derived from the previous equation:

$$\begin{aligned} C &= 2\left(C_L - C_s\right) - C_{pg} \\ &= 2\left(30 - 3\right) - 4 \\ &= 50\text{pF} \end{aligned}$$

Therefore two capacitors of 47pF can be chosen for C_1 and C_2. The circuit can be later optimized by changing the stating values of C_1 and C_2.

2.3. Equivalent Series Resistance

The equivalent series resistance (ESR) is usually specified by the manufacturer. The ESR is the real part of the crystal impedance assuming that the oscillator is matched to the load capacitance C_L :

$$\text{ESR} = R1\left(1 + \frac{C_0}{C_L}\right)^2$$

Application: $\text{ESR} = 30\Omega$ for crystal specified in Table I with $C_L = 30\text{pF}$[2].

2.4. Drive level

The drive level refers to the power dissipated in the crystal. It is important to limit the dissipated power to the value specified by the specifications in order to prevent the crystal from any damage. If the peak voltage across the crystal is approximated as its DC supply, the power dissipation can be approximated as [1]:

$$P = 2R_1\left[\pi f_{XTAL}\left(C_L + C_0\right)V_{cc}\right]^2$$

2.5. Quality factor

The quality factor (Q) is not usually specified in the crystal data sheets. Q is the ratio of stored energy in reactive form to the sum total of all energy losses. Hence the Q factor equals infinity in an ideal oscillator where there are no losses. Q standard crystals fall between values of 20,000 and 200,000. Very high Q of a crystal contribute will contribute to high frequency stability of crystal oscillator.

Appendix A

Calibration of external oscillator using debug mode

It is possible to derive the on-board crystal oscillator output to the LLC pin (pin 37) of ADV740x decoders when in Standard definition mode. In order to do so, the following bit have to be set up:

- Register 0x06 bit[3:0] set up to '0000' (Standard Definition in double sampling)
- Register 0x28 bit[7] set up to '0' (Enabling 27MHz clock frequency on pin 37)

References

[1] Intel Application Note AP-155, Oscillator for Microcontrollers, 1983.

[2] Product Specification, Part Number MA01377, Golledge.

[2] We recommend ESR≤30Ω for the ADV740x decoders.