I²C Specification Interpretation for $t_{HD;DAT}$

Understanding and Handling Borderline Cases
Applies to: AD9889B, ADV7523A, ADV7524A, ADV7526, ADV7527, ADV7510, ADV7511, ADV7511W
The following information is from the I²C Specification

- $t_{HD:DAT} = 0\mu s$
- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.

For timing purposes, an ACK should be considered a data bit.
I2C Requirement

◆ The I²C slave is required to have $0\mu s \ t_{\text{HD:DAT}}$

◆ The HDMI Tx has 0ns hold time
  ● SDA is clocked on the SCL falling edge to distinguish between a data byte and START condition
  ● Exact threshold between START and data conditions varies with process and temperature
  ● +/- 10ns of margin is recommended to avoid a borderline condition

◆ If the hold time is violated, then the signal will be interpreted as an I²C START condition.

◆ The following two slides show the boundary condition between a START condition and a data byte for the HDMI Tx
Behavior of the HDMI Tx: Case 1

- **START Condition**
- If the falling edge of SDA is before the falling edge of SCL, then the HDMI Tx will consider it a START condition
Behavior of the HDMI Tx: Case 2

- Data bit
- If the falling edge of SDA > the falling edge of SCL, then the HDMI Tx will consider it a data bit
Borderline Cases

- There are 2 cases where care must be taken to meet the hold time requirement when using the HDMI Tx
  - I²C Master pulls down SDA on falling edge of SCL after a logic 1 bit
  - I²C Slave or Master ACKS immediately on the 9th bit, when the eight bit was a logic 1

- Ideally these cases should be avoided
  - In an ideal case there will be 300ns of hold time provided from the master or ACKing device as stated in the t_{HD;DAT} note in the I²C Specification
Method to Handle Border Line Case

To ensure that these cases are handled correctly, care needs to be taken that the SDA line is slower than the SCL line.

- The pull-up resistor on the SDA can be decreased to slow the falling edge.
- The pull-up resistor on the SCL can be increased to speed up the falling edge.
- If the data transition of the I²C master has margin, but another device is producing a fast ACK, try separating the I²C bus for the individual devices.
- If the device pulling the SDA low at the falling SCL edge has drive current or time delay adjustment, modify these settings to delay the SDA.