ADV7182

Register Settings Recommendations

Revision C

December 2014

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INTRODUCTION

This document describes ADI register setting recommendations and adjustments for the ADV7182. This document must be used in conjunction with the latest Datasheet. A detailed description of the script changes are available in the ADV7182 Script Update Document.

LEGAL TERMS AND CONDITIONS

REVISION HISTORY

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09/13—Revision 1.0: Initial Version

1 ADV7182 I²C ADDRESSES

The ADV7182 has one I²C address. This address can be set to two values depending on the voltage on the ALSB pin of the ADV7182. When the ALSB is at 0 volts then the I²C write main map address of the ADV7182 is 0x40. When the ALSB is pulled up to the DVDDIO supply, then the I²C write main map address of the ADV7182 is 0x42 (see Table 1).

Throughout this document it will be assumed that the I²C write map address is 0x42.

Table 1. I²C write slave map address of the ADV7182

ALSB Pin	R/$\overline{W}$ Bit	Slave Address
0	0	0x40 (write)
0	1	0x41 (read)
1	0	0x42 (write)
1	1	0x43 (read)

The ADV7182 however contains three I²C sub maps: the user sub map, user sub map 2, and the interrupt/VDP sub map (see Figure 1).

The User sub map is available by default. The other two maps are accessed using the SUB_USR_EN bits (Address 0x0E bits [6:5]). When programming of these maps is completed, it is necessary to write to the SUB_USR_EN bit to return to the main register map.

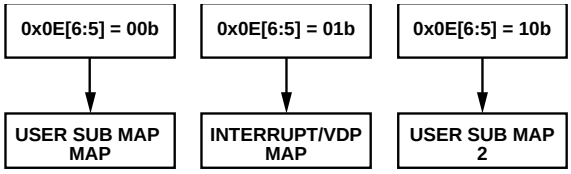

Figure 1. ADV7182 I²C Sub maps

1.1 USER SUB MAP

The User sub map is available by default. The user sub map contains registers that program the analog front end and digital core of the ADV7182. The user sub map has the same I²C slave address as the main map. To access the user sub map, set the SUB_USR_EN bits in the main map (Address 0x0E[6:5]) to 00.

1.2 INTERRUPT/VDP SUB MAP

The interrupt/VDP sub map contains registers that can be used to program internal interrupts, control the $\overline{\text{INTRQ}}$ pin, and decode vertical blanking interval (VBI) data. The interrupt/VDP sub map has the same I²C slave address as the main map. To access the interrupt/VDP sub map, set the SUB_USR_EN bits in the main map (Address 0x0E[6:5]) to 01.

1.3 USER SUB MAP 2

User Sub Map 2 contains registers that control the ACE, down dither, and fast lock functions. It also contains controls that set the acceptable input luma and chroma limits before the ADV7182 enters free-run and color kill modes.

User Sub Map 2 has the same I²C slave address as the main map. To access User Sub Map 2, set the SUB_USR_EN bits in the main map (Address 0x0E[6:5]) to 10.

Table 2. Accessing I²C Sub Map Addresses of the ADV7182

ALSB Pin	R/$\overline{W}$ Bit	Slave Address	SUB_USR_EN Bits (Address 0x0E[6:5])	Sub Map
0	0 (write)	0x40	00	User sub map
0	1 (read)	0x41	00	User sub map
0	0 (write)	0x40	01	Interrupt/VDP sub map
0	1 (read)	0x41	01	Interrupt/VDP Sub map
0	0 (write)	0x40	10	User Sub Map 2
0	1 (read)	0x41	10	User Sub Map 2
1	0 (write)	0x42	00	User sub map
1	1 (read)	0x43	00	User sub map
1	0 (write)	0x42	01	Interrupt/VDP sub map
1	1 (read)	0x43	01	Interrupt/VDP sub map
1	0 (write)	0x42	10	User Sub Map 2
1	1 (read)	0x43	10	User Sub Map 2

2 DESCRIPTION OF I²C WRITES

A number of script tables are provided in this recommended settings document. These script tables detail the I²C register writes that are required to configure the ADV7182. Each row of a script table details one I²C write to the ADV7182 followed by a description. Each I²C write to the ADV7182 consists of three groups of two hexadecimal numbers.

- The first two hexadecimal numbers state the slave address of the ADV7182 for I²C writing . This can either be 0x40 or 0x42 (see ADV7182 I²C Addresses section for more information). Throughout this document we will assume that the slave address of the ADV7182 for I²C writing is set to 0x42.
- The second two hexadecimal numbers state which register in the ADV7182 is being written to.
- The last two hexadecimal numbers state what value is being written to the register.

2.1 EXAMPLE SCRIPT TABLE

This subsection provides an example of a script table followed by a description.

The writes below force the ADV7182 into free-run mode. (See Section 4.5 Free-Run Mode for more information.)

User Sub Map	
42 00 05	Adjust INSEL
42 0C 37	Force Free-Run mode
42 14 XX	Set Free-Run Pattern
42 02 YY	Force Video Standard

In this example:

- Each row consists of an I²C write. These four I²C writes need to be performed to put the ADV7182 into free-run mode. The writes should be performed in the sequence shown above.
- The '**User Sub Map**' at the top of the table indicates that, before the first write, the ADV7182 is in the User Sub Map. See ADV7182 I²C Addresses section for more information.
- The first row indicates that the value 0x05 is being written to register 0x00 in the ADV7182.
    - The device address 0x42 indicates that the ADV7182 is being written to.
    - The register address 0x00 indicates that register 0x00 within the ADV7182 is being written to.
    - The value 0x05 indicates that the value 0x05 is being written to register 0x00 within the ADV7182.
- The comment on the right of the first row indicates that this write adjusts the INSEL register in the ADV7182.
- Similarly the second row shows that the value 0x37 is being written to register 0x0C in the ADV7182. This write activates the Free-Run mode on the ADV7182.
- The third and fourth rows show how to program the Free-Run Pattern and the Output Video Standard. Note the XX and YY values indicates that many different values are possible. The possible values are indicated in separate tables.

3 PROGRAMMING THE ADV7182

Programming the ADV7182 consists of the following stages:

- Setup the ADV7182
- Configure the input to the ADV7182
- Differential CVBS writes (differential CVBS mode only)
- Fast Switch mode (optional mode)
- Configure digital output from the ADV7182

Each of these stages is discussed in the following sections.

3.1 SETUP THE ADV7182

This section describes how to reset and power-up the ADV7182.

3.1.1 RESET THE ADV7182

It is recommended that the ADV7182 be reset when switching from one input mode to another input mode (for example switching from differential CVBS mode to single ended CVBS mode, or switching from YC mode to YPbYr mode).

Note that it is not necessary to perform a reset when switching from one analog input pin to another analog input pin (for example switching from single ended CVBS on Ain1 to single ended CVBS on Ain2).

After a software reset, a 10 ms wait is needed before I²C communication can be started with the ADV7182. See 'Power-up Sequence' section of the ADV7182 datasheet for more information.

User Sub Map	
42 0F 80	Reset ADV7182
delay 10	Wait 10 ms

3.1.2 EXITING POWER DOWN MODE

The following write makes the ADV7182 exit the reset/power down state. This write should be performed only after the 10 ms wait described in Section 3.1.1.

User Sub Map	
42 0F 00	Exit Power Down Mode

3.1.3 CONFIGURE FOR CRYSTAL OR OSCILLATOR INPUT

The ADV7182 requires a 28.63636 MHz clock input in order to operate correctly. This clock input can be supplied from either an external crystal or an external oscillator device.

The ADV7182 needs to be configured for either a 28.63636 MHz crystal or 28.63636 MHz oscillator clock input.

User Sub Map register 0x13 is used to configure the ADV7182 for either a 28.63636 MHz crystal or 28.63636 MHz oscillator clock input. See Table 3 below.

Note that if a 28.63636 MHz oscillator is used, then the write to user Sub Map register 0x13 must be made directly after the ADV7182 exits power down mode.

User Sub Map	
42 13 XX	Enable ADV7182 for 28.63636 MHz Crystal or Oscillator[1]

[1] The 'XX' term indicates that a number of different options are available to the user. These options are listed in Table 3 below.

Table 3. Configure for Crystal or Oscillator Clock Input

User Sub Map, Register 0x13	Comment
00	Enable ADV7182 for 28.63636 MHz Crystal Clock Input
04	Enable ADV7182 for 28.63636 MHz Oscillator Clock Input

See Section 4.4 below for more information on using an oscillator to clock the ADV7182.

3.2 INPUT CONFIGURATION

This section describes how to configure the analog front end (AFE) of the ADV7182 for analog video.

3.2.1 Set Analog Front End IBIAS Settings

Different bias current (IBIAS) settings are needed for the analog front end (AFE) of the ADV7182, depending on the input video format. These settings optimize the performance of the ADV7182. The following table shows the required IBIAS settings for each video input format.

Table 4. List of IBIAS Settings

Input Format	User Sub Map	Comment
Single Ended CVBS	42 52 CD	Set optimized IBIAS for the AFE
Differential CVBS	42 52 C0	Set optimized IBIAS for the AFE
YC	42 53 CE	Set optimized IBIAS for the AFE
YPbPr	42 54 C0	Set optimized IBIAS for the AFE

3.2.2 Input Select

Resister 0x00 in the User Sub Map contains the INSEL[4:0] bits. The INSEL[4:0] bits are used to program the ADV7182 for each analog video input format (e.g. single ended CVBS, differential CVBS, YC and YPbPr). The INSEL[4:0] bits also indicates to the ADV7182 on which analog input pins the analog video input is being applied.

Note for differential CVBS inputs, an INSEL Switch write should be performed. The INSEL switch write sets the INSEL bits to an intermediate value before setting the INSEL bits to the desired value. Doing this optimizes the lock time of the ADV7182 in differential CVBS mode.

User Sub Map	
42 00 10	INSEL Switch[1]
42 00 XX[2]	Set INSEL Register

[1] The INSEL Switch write should be performed only for differential CVBS inputs.

[2] XX indicates that many different values are possible, Table 4 lists these possible values.

Table 5. List of INSEL Values

User Sub Map	Video Format	Comment
42 00 00	Single Ended CVBS	CVBS input on AIN1
42 00 01	Single Ended CVBS	CVBS input on AIN2
42 00 02	Single Ended CVBS	CVBS input on AIN3
42 00 03	Single Ended CVBS	CVBS input on AIN4
42 00 08	Y/C (S-Video)	Y input on AIN1 C input on AIN2
42 00 09	Y/C (S-Video)	Y input on AIN3 C input on AIN4
42 00 0C	YPbPr	Y input on AIN1 Pb input on AIN2 Pr input on AIN3
42 00 0E	Differential CVBS	Positive on AIN1 Negative on AIN2
42 00 0F	Differential CVBS	Positive on AIN3 Negative on AIN4

3.2.3 Current clamp reset

Once the INSEL register is set, four writes are needed to reset the current clamp circuitry. These writes need to be performed directly after the INSEL write(s) and in the order shown below. These four writes reset the current clamp circuitry to improve the lock time of the ADV7182.

See Clamp Operation section of ADV7182 datasheet for more information about the clamp circuitry of the ADV7182.

User Sub Map	
42 0E 80	ADI Required Write; Reset Current Clamp Circuitry (step1)
42 9C 00	ADI Required Write; Reset Current Clamp Circuitry (step2)
42 9C FF	ADI Required Write; Reset Current Clamp Circuitry (step3)
42 0E 00	ADI Required Write; Reset Current Clamp Circuitry (step4)

3.3 DIFFERENTIAL CVBS WRITES

The writes in this section should only be used for differential CVBS inputs. The writes below modify the analog front end of the ADV7182 to enable it to accept differential CVBS video sources. These writes must be performed after the Input configuration writes described in Section 3.2.

3.3.1 Common Mode Clamp Setup

The following writes setup the common mode clamps of the ADV7182. The common mode clamps are used only in differential mode. The common mode clamps bring the positive and negative differential CVBS inputs to a common voltage level.

The writes shown in the following table optimize the common mode clamp circuitry and enable the ADV7182 to lock to incoming differential CVBS signals quickly.

The common mode clamp setup writes are recommended for new product designs to offer optimal performance. These writes are not required for existing designs which have already been quality approved and released.

User Sub Map	
42 5A90	ADI Required Write [common mode clamp setup]
42 60 A0	ADI Required Write [common mode clamp setup]
delay 25	Wait 25 ms
42 60 B0	ADI Required Writes [common mode clamp setup]

3.3.2 Differential Analog Front End Setup

The following writes setup the analog front end (AFE) of the ADV7182 for differential CVBS inputs.

User Sub Map	
42 5F A8	Compensates for the External Divide by 4 Resistor Divider Circuit
42 0E 80	ADI Required Writes
42 B6 08	ADI Required Writes [differential CVBS required write]
42 C0 A0	ADI Required Writes [differential CVBS required write]
42 0E 00	Enter User Sub Map

3.4 FAST SWITCH MODE

Fast switch mode is an optional mode that allows the ADV7182 to lock to single ended CVBS or differential CVBS signals more quickly. Fast switch mode is recommended for automotive applications.

In fast switch mode the ADV7182 will not be as robust to poor sources and will not be able to process sources with Rovi®/Macrovision copyright protection. In fast switch mode the ADV7182 will only be able to lock to NTSC-M, NTSC 4.43 and PAL-I video standards.

The following writes should be performed when the user requires fast switch mode. Note that fast switch mode is optional.

User Sub Map	
42 0E 80	ADI Required Write [Fast Switch]
42 D9 44	ADI Required Write [Fast Switch]
42 0E 40	Enter User Sub Map 2 [Fast Switch]
42 E0 01	Enable Fast Switch Mode [Fast Switch]
42 0E 00	Enter User Sub Map [Fast Switch]

3.5 CONFIGURE DIGITAL CORE

This section describes the writes needed to configure the digital output from the ADV7182.

3.5.1 Select Chroma Shaping Filter Mode

This write applies only to single ended CVBS and Differential CVBS inputs (i.e. this does not apply to YC or YPbPr inputs). The following write sets the chroma shaping filter response. See 'Chroma Filter' section of the ADV7182 datasheet for more information.

User Sub Map	
42 17 41	Select SH1 Chroma Shaping Filter[1]

[1] The chroma shaping filter write should be applied only to single ended CVBS and Differential CVBS inputs.

3.5.2 Power Up Digital Output Pads

The following writes are needed to power up the Pixel output pads (P0:P7), the line locked clock (LLC), synchronization pins (HS and VS/FIELD/SFL) as well as the interrupt output pin INTRQ.

User Sub Map	
42 03 0C	Enable Pixel & Sync output drivers
42 04 07	Power-up INTRQ, HS and VS/FIELD/SFL pad
42 1D 40	Enable LLC Output Driver

4 ADDITIONAL FEATURES OF THE ADV7182

4.1 ADAPTIVE CONTRAST ENHANCEMENT (ACE)

The ADV7182 ACE feature enables the contrast within dark areas of an image to be increased without significantly affecting bright areas. This is particularly useful in automotive applications where the ability to discern objects in shaded areas can be critical.

The writes below are needed to enable the ACE feature of the ADV7182. These writes should be performed in the order listed below.

User Sub Map	
42 0E 40	Enter User Sub Map 2
42 84 00	Optimize ACE Performance[1]
42 80 80	Enable ACE Feature
42 0E 00	Re-enter User Sub Map

[1] Setting the ACE chroma gain to zero optimizes the performance of the ACE circuit.

4.2 ITU-R BT.656-4 MODE

By default the ADV7182 outputs in the ITU-R BT.656-3 video standard. If the receiving device is expecting ITU-R BT.656-4 video then ten dark lines of video may appear at the top of the resulting image in NTSC mode.

It is possible to program the ADV7182 to output in the ITU-R BT.656-4 video standard. This will prevent the appearance of the dark lines of video at the top of the resulting image. See "AV Code Insertion and Controls" section of ADV7182 datasheet for more information.

Set User Map register 0x04 bit [7] to 0 (default) to use ITU-R BT.656-3 video standard.

Set User Map register 0x04 bit [7] to 1 to use ITU-R BT.656-4 video standard.

4.3 CONFIGURE VS/FIELD/SFL PIN OUTPUT

By default the VS/FIELD/SFL pin on the ADV7182 outputs field synchronization information. The VS/FIELD/SFL can be programmed to output vertical synchronization information instead. See the Global Pin Control section of ADV7182 datasheet.

Set User Map register 0x6B bits [2:0] to 0b'010 (default) for the VS/FIELD/SFL pin to output field synchronization information.

Set User Map register 0x6B bits [2:0] to 0b'001 for the VS/FIELD/SFL pin to output vertical synchronization information.

4.4 OSCILLATOR CLOCK INPUT

The standard ADV7182 scripts assume that the ADV7182 is being clocked by an external 28.63636 MHz crystal. With the standard scripts, the ADV7182 outputs 1.8 V between the XTALP and XTALN pins. However, if an oscillator is used, a software write is needed to disable this voltage (between the XTALP and XTALN pins).

4.4.1 Oscillator Specifications

An oscillator with an output of 1.8 Vpp must be used. The oscillator must output a 28.63636 MHz clock with a tolerance of +/- 50 ppm.

4.4.2 Physical setup

Connect the output of the oscillator to the XTALN pin of the ADV7182. Leave the XTALP pin of the ADV7182 floating.

4.4.3 Software Write

The following write is needed to disable the voltage output on the XTALP pin and allow the ADV7182 to be clocked by a 28.63636 MHz oscillator.

User Sub Map	
42 13 04	Enable Oscillator Clock Input

4.4.4 Note on Software Write

The ADV7182 datasheet states that register 0x13 is a read only register (status register 3). Actually, two registers share the register address 0x13.
When a read is performed on register 0x13, Status Register 3 (which is read only) data is read. When a write command is performed on register 0x13, an internal control register (which is write only) is written to.

4.5 FREE-RUN MODE

Free-run mode is a useful function that allows the ADV7182 to output a number of test patterns (for example 100% color bars) without the need for a video source to be connected to the ADV7182. See the 'Free-Run Operation' section of ADV7182 datasheet for more information.

The following writes force the ADV7182 into free-run mode. They must be written in order shown below.

User Sub Map	
42 00 05	Adjust INSEL
42 0C 37	Force Free-Run mode
42 14 XX	Set Free-Run Pattern[1]
42 02 YY	Force Video Standard [2]

[1] The 'XX' term indicates that a number of different options are available to the user. This register write is discussed in section 4.5.2 Free-Run Video Output Standard

[2] The 'XX' and 'YY' terms indicate that a number of different options are available to the user. These options are discussed in Sections Free-Run Pattern Selection and Free-Run Video Output Standard respectively.

4.5.1 Free-Run Pattern Selection

The following table shows all the possible free-run output patterns. See 'Free-Run Operation' section of the ADV7182 datasheet for more information.

User Sub Map	Free-Run Pattern
42 14 10	Outputs a Blue Screen. The output color can be changed by setting the DEF_C and DEF_Y controls; see 'Color Controls' section of ADV7182 datasheet.
42 14 11	Outputs 100% Color Bars Test Pattern.
42 14 12 42 0D 88	Outputs a Luma Ramp Test Pattern. Note that in order to display properly, the DEF_C register must be set to 0x88. See 'Color Controls' section of ADV7182 datasheet.
42 14 15	Outputs a Boundary Box Test Pattern

4.5.2 Free-Run Video Output Standard

Under normal conditions if free-run mode is forced then the ADV7182 outputs in the format of the last valid video input. For example: If an NTSC source was connected to the ADV7182 before the ADV7182 was programmed into free-run mode, the ADV7182 will output in 480i format in free-run mode.

Writes to user sub-map registers 0x00 and 0x02, in the free-run script, allow the user to control which video format is output in free-run mode.

The following table lists the values for user sub-map register 0x02 in order for the ADV7182 to output in PAL(576i) or NTSC (480i) modes. A full list of output modes can be found in 'Video Standard Selection' section of the ADV7182 datasheet.

User Sub Map	Output Video Standard
42 02 84	Force standard to PAL
42 02 54	Force standard to NTSC-M

5 Example How to Program the ADV7182 to Output an Interrupt on the INTRQ Pin

The INTRQ interrupt pin on the ADV7182 can be programmed to change state under a number of different conditions. This can be useful to detect issues with the inputted analog video.

The INTRQ pin can be programmed to drive high or low when activated. It can drive high/low for a set period of time or can drive high/low until the interrupt is cleared. See the 'Interrupt/VDP Map Descriptions' table in the ADV7182 datasheet for more information.

The following example will describe how to set the interrupt pin to go from a high state to a low state when the ADV7182 has locked or lost lock to the inputted video. The interrupt will remain low until cleared.

5.1 PROGRAMMING THE INTERRUPT

These writes should be performed in the order listed below, after an ADI recommended script has been performed.

User Sub Map	
42 0E 20	Enter Interrupt/VDP Sub-Map
42 40 D1	INTRQ pin drives low when active and remains low until interrupt is cleared
42 44 03	Enable SD_LOCK and SD_UNLOCK interrupts
42 43 03	Clear SD_LOCK and SD_UNLOCK interrupts
42 0E 00	Re-enter User Sub-Map

The ADV7182 has now been programmed to drive the INTRQ pin high under normal operation. When the ADV7182 locked to a video source or loses video lock, the INTRQ pin will drive low and remain low until the interrupt has been cleared.

5.2 CLEARING THE INTERRUPT

The writes listed below must be performed after the interrupt is triggered (i.e. INTRQ pin drives low).

User Sub Map	
42 0E 20	Enter Interrupt/VDP Sub-Map
42 43 03	Clear SD_LOCK and SD_UNLOCK interrupts
42 0E 00	Re-enter User Sub-Map

The interrupt is now un-triggered (i.e. INTRQ pin drives high). The INTRQ will not drive low until the ADV7182 has locked or lost lock to a video source.

5.3 NOTE ON LOST_LOCK AND IN_LOCK BITS

The LOST_LOCK (User Map, register 0x10[bit 1]) and IN_LOCK bits (User Map, register 0x10[bit 0]) can be used to determine if a lock or loss of lock event has occurred. Note in order for the LOST_LOCK and IN_LOCK bits to work correctly, the ADV7182 must be programmed with an Analog Devices recommended script.

The following table shows the operation of the LOST_LOCK and IN_LOCK bits as the active video source is connected or disconnected.

Source Connected/Disconnected	LOST_LOCK Bit	IN_LOCK Bit
When the video source is connected to the ADV7182	0	1
When the video source is disconnected from the ADV7182	1	0
When the video source is reconnected to the ADV7182(the first read of register 0x10 after reconnection)	1	1
Second and subsequent reads of register 0x10 after the video source is reconnected	0	1

See the "Global Status Register" section of the ADV7182 datasheet for more information.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).