ADV7441A

SD/HDTV Video Decoder, Component and Graphics Digitizer with 2:1 Multiplexed HDMI Receiver

SOFTWARE MANUAL

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Advantiv™ Analog Devices

NSV® Analog Devices

ANALOG DEVICES

1 I²C Global Register Map

1.1 User Map

Table 1: User Map Register 0x00 to 0x7F

Address		Register Name	rw	7	6	5	4	3	2	1	0	Reset Value	(Hex)
0	00h	Input Control	rw	VID_SEL.3	VID_SEL.2	VID_SEL.1	VID_SEL.0	INSEL.3	INSEL.2	INSEL.1	INSEL.0	00000000	00
1	01h	Video Selection	rw		ENHSPLL	BETACAM		ENVSPROC				11001000	C8
3	03h	Output Control	rw	VBI_EN	TOD	OF_SEL.3	OF_SEL.2	OF_SEL.1	OF_SEL.0		SD_DUP_AV	01001100	4C
4	04h	Extended Output Control	rw	BT656-4			INT2_EN	TIM_OE	BL_C_VBI	EN_SFL_PIN	RANGE	01x00111	47
5	05h	Primary Mode	rw					PRIM_MODE.3	PRIM_MODE.2	PRIM_MODE.1	PRIM_MODE.0	00000000	00
6	06h	Video Standard	rw	CP_V_FREQ.2	CP_V_FREQ.1	CP_V_FREQ.0	VID_STD.4	VID_STD.3	VID_STD.2	VID_STD.1	VID_STD.0	00000010	02
7	07h	Autodetect Enable	rw	AD_SECS25_EN	AD_SECAM_EN	AD_N443_EN	AD_P60_EN	AD_PALN_EN	AD_PALM_EN	AD_NTSC_EN	AD_PAL_EN	01111111	7F
8	08h	Contrast	rw	CON.7	CON.6	CON.5	CON.4	CON.3	CON.2	CON.1	CON.0	10000000	80
10	0Ah	Brightness	rw	BRI.7	BRI.6	BRI.5	BRI.4	BRI.3	BRI.2	BRI.1	BRI.0	00000000	00
11	0Bh	Hue	rw	HUE.7	HUE.6	HUE.5	HUE.4	HUE.3	HUE.2	HUE.1	HUE.0	00000000	00
12	0Ch	Default Value Y	rw	DEF_Y.5	DEF_Y.4	DEF_Y.3	DEF_Y.2	DEF_Y.1	DEF_Y.0	DEF_VAL_AUTO_EN	DEF_VAL_EN	00110110	36
13	0Dh	Default Value C	rw	DEF_C.7	DEF_C.6	DEF_C.5	DEF_C.4	DEF_C.3	DEF_C.2	DEF_C.1	DEF_C.0	01111100	7C
14	0Eh	uss2_slave_address	rw	USS2_ADDR.7	USS2_ADDR.6	USS2_ADDR.5	USS2_ADDR.4	USS2_ADDR.3	USS2_ADDR.2	USS2_ADDR.1	USS2_ADDR.0	01100000	60
15	0Fh	Power Management	rw	RES	TRAQ	PWRDN	PWRSAV	CP_PWRDN		FB_PWRDN		00000000	00
16	10h	Status 1	r	COL_KILL	AD_RESULT.2	AD_RESULT.1	AD_RESULT.0	FOLLOW_PW	FSC_LOCK	LOST_LOCK	IN_LOCK	---	---
17	11h	Ident	r	IDENT.7	IDENT.6	IDENT.5	IDENT.4	IDENT.3	IDENT.2	IDENT.1	IDENT.0	---	---
18	12h	Status 2	r	TLLC PLL LOCK	CP FREE RUN	FSC NSTD	LL NSTD	MV AGC DET	MV PS DET	MVCS T3	MVCS DET	---	---
19	13h	Status 3	r	PAL SW LOCK	INTERLACE	STD FLD LEN	FREE_RUN_ACT	CVBS	SD_OP_50Hz	GEMD	INST_HLOCK	---	---
19	13h	Analogue Control Internal	w							AA_FILT_HIGH_BW_EN		00000000	00
20	14h	Analogue Clamp Control	rw				CCLEN					00010010	12
21	15h	Digital Clamp Control 1	rw		DCT.1	DCT.0						0000xxxx	00
23	17h	Shaping Filter Control	rw	CSFM.2	CSFM.1	CSFM.0	YSFM.4	YSFM.3	YSFM.2	YSFM.1	YSFM.0	00000001	01
24	18h	Shaping Filter Control 2	rw	WYSFMOVR			WYSFM.4	WYSFM.3	WYSFM.2	WYSFM.1	WYSFM.0	10010011	93
25	19h	Comb Filter Control	rw					NSFSEL.1	NSFSEL.0	PSFSEL.1	PSFSEL.0	11110001	F1
29	1Dh	Vertical Scale Value 1	rw	TRI_LLC	EN28XTAL							11000xxx	C0
39	27h	Pixel Delay Control	rw	SWPC	AUTO_PDC_EN	CTA.2	CTA.1	CTA.0		LTA.1	LTA.0	01011000	58
43	2Bh	Misc Gain Control	rw		CKE						PW_UPD	11100001	E1
44	2Ch	AGC Mode Control	rw		LAGC.2	LAGC.1	LAGC.0			CAGC.1	CAGC.0	10101110	AE
45	2Dh	Chroma Gain Control 1	w	CAGT.1	CAGT.0			CMG.11	CMG.10	CMG.9	CMG.8	11110100	F4
46	2Eh	Chroma Gain Control 2	w	CMG.7	CMG.6	CMG.5	CMG.4	CMG.3	CMG.2	CMG.1	CMG.0	00000000	00
47	2Fh	Luma Gain Control 1	w	LAGT.1	LGAT.0			LMG.11	LMG.10	LMG.9	LMG.8	1111xxxx	F0
48	30h	Luma Gain Control 2	w	LMG.7	LMG.6	LMG.5	LMG.4	LMG.3	LMG.2	LMG.1	LMG.0	xxxxxxxx	00
49	31h	VSync Field Control 1	rw				NEWAVMODE	HVSTIM				00010010	12
50	32h	VSync Field Control 2	rw	VSBHO	VSBHE							01000001	41
51	33h	VSync Field Control 3	rw	VSEHO	VSEHE							10000100	84
52	34h	HSync Position Control 1	rw		HSB.10	HSB.9	HSB.8		HSE.10	HSE.9	HSE.8	00000000	00
53	35h	HSync Position Control 2	rw	HSB.7	HSB.6	HSB.5	HSB.4	HSB.3	HSB.2	HSB.1	HSB.0	00000010	02
54	36h	HSync Position Control 3	rw	HSE.7	HSE.6	HSE.5	HSE.4	HSE.3	HSE.2	HSE.1	HSE.0	00000000	00
55	37h	Polarity	rw	PHS		PVS		PF			PCLK	00000001	01
56	38h	NTSC Comb Control	rw	CTAPSN.1	CTAPSN.0	CCMN.2	CCMN.1	CCMN.0	YCMN.2	YCMN.1	YCMN.0	10000000	80
57	39h	PAL Comb Control	rw	CTAPSP.1	CTAPSP.0	CCMP.2	CCMP.1	CCMP.0	YCMP.2	YCMP.1	YCMP.0	11000000	C0
58	3Ah	ADC Control	rw					PDN_ADC0	PDN_ADC1	PDN_ADC2	PDN_ADC3	00000001	01
60	3Ch	TLLC Control Analogue	rw	SOG_SYNC_LEV.4	SOG_SYNC_LEV.3	SOG_SYNC_LEV.2	SOG_SYNC_LEV.1	SOG_SYNC_LEV.0	PLL_QPUMP.2	PLL_QPUMP.1	PLL_QPUMP.0	01011000	58
61	3Dh	Manual Window Control	rw		CKILLTHR.2	CKILLTHR.1	CKILLTHR.0					10100010	A2
65	41h	Resample Control	rw		SFL_INV							00000001	01
71	47h	AutoPLL Parm Ctrl	rw					CALC_VCO_RANGE_EN		CALC_PLL_QPUMP_EN		xxx00000	00
72	48h	GemStar Ctrl 1	rw	GDECEL.15	GDECEL.14	GDECEL.13	GDECEL.12	GDECEL.11	GDECEL.10	GDECEL.9	GDECEL.8	00000000	00
73	49h	GemStar Ctrl 2	rw	GDECEL.7	GDECEL.6	GDECEL.5	GDECEL.4	GDECEL.3	GDECEL.2	GDECEL.1	GDECEL.0	00000000	00
74	4Ah	GemStar Ctrl 3	rw	GDECOL.15	GDECOL.14	GDECOL.13	GDECOL.12	GDECOL.11	GDECOL.10	GDECOL.9	GDECOL.8	00000000	00
75	4Bh	GemStar Ctrl 4	rw	GDECOL.7	GDECOL.6	GDECOL.5	GDECOL.4	GDECOL.3	GDECOL.2	GDECOL.1	GDECOL.0	00000000	00
76	4Ch	GemStar Ctrl 5	rw								GDECAD	xxxx0000	00
77	4Dh	CTI DNR Ctrl 1	rw			DNR_EN		CTI_AB.1	CTI_AB.0	CTI_AB_EN	CTI_EN	11101111	EF
78	4Eh	CTI DNR Ctrl 2	rw	CTI_C_TH.7	CTI_C_TH.6	CTI_C_TH.5	CTI_C_TH.4	CTI_C_TH.3	CTI_C_TH.2	CTI_C_TH.1	CTI_C_TH.0	00001000	08
80	50h	CTI DNR Ctrl 4	rw	DNR_TH.7	DNR_TH.6	DNR_TH.5	DNR_TH.4	DNR_TH.3	DNR_TH.2	DNR_TH.1	DNR_TH.0	00001000	08
81	51h	Lock Count	rw	FSCLE	SRLS	COL.2	COL.1	COL.0	CIL.2	CIL.1	CIL.0	00100100	24
82	52h	CSC_1	rw	CSC_scale.1	CSC_scale.0		A4.12	A4.11	A4.10	A4.9	A4.8	01000000	40
83	53h	CSC_2	rw	A4.7	A4.6	A4.5	A4.4	A4.3	A4.2	A4.1	A4.0	00000000	00
84	54h	CSC_3	rw		A3.12	A3.11	A3.10	A3.9	A3.8	A3.7	A3.6	00000000	00
85	55h	CSC_4	rw	A3.5	A3.4	A3.3	A3.2	A3.1	A3.0	A2.12	A2.11	00000000	00
86	56h	CSC_5	rw	A2.10	A2.9	A2.8	A2.7	A2.6	A2.5	A2.4	A2.3	00000000	00
87	57h	CSC_6	rw	A2.2	A2.1	A2.0	A1.12	A1.11	A1.10	A1.9	A1.8	00001000	08
88	58h	CSC_7	rw	A1.7	A1.6	A1.5	A1.4	A1.3	A1.2	A1.1	A1.0	00000000	00
89	59h	CSC_8	rw				B4.12	B4.11	B4.10	B4.9	B4.8	00000000	00
90	5Ah	CSC_9	rw	B4.7	B4.6	B4.5	B4.4	B4.3	B4.2	B4.1	B4.0	00000000	00
91	5Bh	CSC_10	rw		B3.12	B3.11	B3.10	B3.9	B3.8	B3.7	B3.6	00000000	00
92	5Ch	CSC_11	rw	B3.5	B3.4	B3.3	B3.2	B3.1	B3.0	B2.12	B2.11	00000001	01
93	5Dh	CSC_12	rw	B2.10	B2.9	B2.8	B2.7	B2.6	B2.5	B2.4	B2.3	00000000	00
94	5Eh	CSC_13	rw	B2.2	B2.1	B2.0	B1.12	B1.11	B1.10	B1.9	B1.8	00000000	00
95	5Fh	CSC_14	rw	B1.7	B1.6	B1.5	B1.4	B1.3	B1.2	B1.1	B1.0	00000000	00
96	60h	CSC_15	rw				C4.12	C4.11	C4.10	C4.9	C4.8	00000000	00
97	61h	CSC_16	rw	C4.7	C4.6	C4.5	C4.4	C4.3	C4.2	C4.1	C4.0	00000000	00
98	62h	CSC_17	rw		C3.12	C3.11	C3.10	C3.9	C3.8	C3.7	C3.6	00100000	20
99	63h	CSC_18	rw	C3.5	C3.4	C3.3	C3.2	C3.1	C3.0	C2.12	C2.11	00000000	00
100	64h	CSC_19	rw	C2.10	C2.9	C2.8	C2.7	C2.6	C2.5	C2.4	C2.3	00000000	00
101	65h	CSC_20	rw	C2.2	C2.1	C2.0	C1.12	C1.11	C1.10	C1.9	C1.8	00000000	00
102	66h	CSC_21	rw	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0	00000000	00
103	67h	CSC_22	rw			EmbSyncOnAll	SOFT_FILT	DS_ONLY	INP_CSPACE.2	INP_CSPACE.1	INP_CSPACE.0	00000111	07
104	68h	CSC_23	rw	CSC_COEFF_SEL.3	CSC_COEFF_SEL.2	CSC_COEFF_SEL.1	CSC_COEFF_SEL.0		ALT_DATA_SAT	RGB_OUT	CSC_ALT_GAMMA	1111x000	F0
105	69h	Config 1	rw	TRI_LEVEL	SYN_LOTRIG	INV_DINCLK	BACK_END_CSC_EN	INT_COEFF_FOR_FRONT_END_CSC	EIA_861B_COMPLIANCE	SDM_SEL.1	SDM_SEL.0	00000000	00
106	6Ah	TLLC Phase Adjust	rw		PLL_DLL_UPD_VS_EN	BYP_DLL	DLL_PH.4	DLL_PH.3	DLL_PH.2	DLL_PH.1	DLL_PH.0	01000000	40
107	6Bh	CP Output Selection	rw	HS_OUT_SEL	VS_OUT_SEL	DE_OUT_SEL	OP_656_RANGE	CPOP_SEL.3	CPOP_SEL.2	CPOP_SEL.1	CPOP_SEL.0	11000010	C2
108	6Ch	CP Clamp 1	rw	CLMP_A_MAN	CLMP_BC_MAN	CLMP_FREEZE		CLMP_A.11	CLMP_A.10	CLMP_A.9	CLMP_A.8	00010000	10
109	6Dh	CP Clamp 2	rw	CLMP_A.7	CLMP_A.6	CLMP_A.5	CLMP_A.4	CLMP_A.3	CLMP_A.2	CLMP_A.1	CLMP_A.0	00000000	00
110	6Eh	CP Clamp 3	rw	CLMP_B.11	CLMP_B.10	CLMP_B.9	CLMP_B.8	CLMP_B.7	CLMP_B.6	CLMP_B.5	CLMP_B.4	00000000	00
111	6Fh	CP Clamp 4	rw	CLMP_B.3	CLMP_B.2	CLMP_B.1	CLMP_B.0	CLMP_C.11	CLMP_C.10	CLMP_C.9	CLMP_C.8	00000000	00
112	70h	CP Clamp 5	rw	CLMP_C.7	CLMP_C.6	CLMP_C.5	CLMP_C.4	CLMP_C.3	CLMP_C.2	CLMP_C.1	CLMP_C.0	00000000	00
113	71h	CP AGC 1	rw	AGC_TAR.9	AGC_TAR.8	AGC_TAR_MAN	AGC_FREEZE	HS_NORM	AGC_TIM.2	AGC_TIM.1	AGC_TIM.0	00000000	00
114	72h	CP AGC 2	rw	AGC_TAR.7	AGC_TAR.6	AGC_TAR.5	AGC_TAR.4	AGC_TAR.3	AGC_TAR.2	AGC_TAR.1	AGC_TAR.0	00000000	00
115	73h	CP AGC 3	rw	GAIN_MAN	AGC_MODE_MAN	A_GAIN.9	A_GAIN.8	A_GAIN.7	A_GAIN.6	A_GAIN.5	A_GAIN.4	00010000	10
116	74h	CP AGC 4	rw	A_GAIN.3	A_GAIN.2	A_GAIN.1	A_GAIN.0	B_GAIN.9	B_GAIN.8	B_GAIN.7	B_GAIN.6	00000100	04
117	75h	CP AGC 5	rw	B_GAIN.5	B_GAIN.4	B_GAIN.3	B_GAIN.2	B_GAIN.1	B_GAIN.0	C_GAIN.9	C_GAIN.8	00000001	01
118	76h	CP AGC 6	rw	C_GAIN.7	C_GAIN.6	C_GAIN.5	C_GAIN.4	C_GAIN.3	C_GAIN.2	C_GAIN.1	C_GAIN.0	00000000	00
119	77h	CP Offset 1	rw	CP_PREC.1	CP_PREC.0	A_OFFSET.9	A_OFFSET.8	A_OFFSET.7	A_OFFSET.6	A_OFFSET.5	A_OFFSET.4	11111111	FF
120	78h	CP Offset 2	rw	A_OFFSET.3	A_OFFSET.2	A_OFFSET.1	A_OFFSET.0	B_OFFSET.9	B_OFFSET.8	B_OFFSET.7	B_OFFSET.6	11111111	FF
121	79h	CP Offset 3	rw	B_OFFSET.5	B_OFFSET.4	B_OFFSET.3	B_OFFSET.2	B_OFFSET.1	B_OFFSET.0	C_OFFSET.9	C_OFFSET.8	11111111	FF
122	7Ah	CP Offset 4	rw	C_OFFSET.7	C_OFFSET.6	C_OFFSET.5	C_OFFSET.4	C_OFFSET.3	C_OFFSET.2	C_OFFSET.1	C_OFFSET.0	11111111	FF
123	7Bh	CP AV Control	rw	AV_inv_F	AV_inv_V			AV_BLANK_EN	AV_POS_SEL	AV_CODE_EN	DE_WITH_AVCODE	00001111	0F
124	7Ch	CP HVF Control 1	rw	PIN_inv_HS	PIN_inv_VS	PIN_inv_F	PIN_inv_DE	START_HS.9	START_HS.8	END_HS.9	END_HS.8	11000000	C0
125	7Dh	CP HVF Control 2	rw	END_HS.7	END_HS.6	END_HS.5	END_HS.4	END_HS.3	END_HS.2	END_HS.1	END_HS.0	00000000	00
126	7Eh	CP HVF Control 3	rw	START_HS.7	START_HS.6	START_HS.5	START_HS.4	START_HS.3	START_HS.2	START_HS.1	START_HS.0	00000000	00
127	7Fh	CP HVF Control 4	rw	START_VS.3	START_VS.2	START_VS.1	START_VS.0	END_VS.3	END_VS.2	END_VS.1	END_VS.0	00000000	00

Table 2: User Map Register 0x80 to 0xFE

Address		Register Name	rw	7	6	5	4	3	2	1	0	Reset Value	(Hex)
128	80h	CP HVF Control 5	rw	START_FE .3	START_FE .2	START_FE .1	START_FE .0	START_F O.3	START_F O.2	START_F O.1	START_F O.0	00000000	00
129	81h	CP Measure Control 1	rw	MEAS_WL.1	MEAS_WL.0		GR_AV_BL_E N	MEAS_WS.11	MEAS_WS.10	MEAS_WS.9	MEAS_WS.8	11000000	C0
130	82h	CP Measure Control 2	rw	MEAS_WS.7	MEAS_WS.6	MEAS_WS.5	MEAS_WS.4	MEAS_WS.3	MEAS_WS.2	MEAS_WS.1	MEAS_WS.0	00000100	04
131	83h	CP Measure Control 3	rw	ISD_THR .7	ISD_THR .6	ISD_THR .5	ISD_THR .4	ISD_THR .3	ISD_THR .2	ISD_THR .1	ISD_THR .0	00000000	00
132	84h	CP Measure Control 4	rw	CP_GAIN_F ILT.3	CP_GAIN_F ILT.2	CP_GAIN_F ILT.1	CP_GAIN_F ILT.0				IFSD_AV G	00001100	0C
133	85h	CP Detection Control 1	rw	POL_MAN_E N	POL_VS	POL_HSC S	SYN_SRC .1	SYN_SRC .0	TRIG_SSPD	SSPD_C ONT	DS_OUT	0xx00011	03
134	86h	CP Misc Control 1	rw				CPOP_INV_PrPb	stdi_line_count_mode	TRIG_STDI	STDI_CONT		00x01011	0B
135	87h	CP TLLC Control 1	rw	PLL_DIV_MAN_EN				PLL_DIV_RATIO.11	PLL_DIV_RATIO.10	PLL_DIV_RATIO.9	PLL_DIV_RATIO.8	01100011	63
136	88h	CP TLLC Control 2	rw	PLL_DIV_RATIO.7	PLL_DIV_RATIO.6	PLL_DIV_RATIO.5	PLL_DIV_RATIO.4	PLL_DIV_RATIO.3	PLL_DIV_RATIO.2	PLL_DIV_RATIO.1	PLL_DIV_RATIO.0	01011010	5A
137	89h	CP TLLC Control 3	rw				SWP_CR_CB_ WB					00001000	08
138	8Ah	CP TLLC Control 4	rw	VCO_RANGE_MAN	VCO_RANGE.1	VCO_RANGE.0						00010000	10
139	8Bh	CP DE Ctrl 1 58	rw	IGNR_CL MP_VS_MAR.3	IGNR_CL MP_VS_MAR.2	IGNR_CL MP_VS_MAR.1	IGNR_CL MP_VS_MAR.0	DE_H_START .9	DE_H_START .8	DE_H_END .9	DE_H_END .8	01000000	40
140	8Ch	CP DE Ctrl 2 59	rw	DE_H_END .7	DE_H_END .6	DE_H_END .5	DE_H_END .4	DE_H_END .3	DE_H_END .2	DE_H_END .1	DE_H_END .0	00000000	00
141	8Dh	CP DE Ctrl 3 60	rw	DE_H_START .7	DE_H_START .6	DE_H_START .5	DE_H_START .4	DE_H_START .3	DE_H_START .2	DE_H_START .1	DE_H_START .0	00000000	20
142	8Eh	CP DE Ctrl 4 61	rw	DE_V_START .3	DE_V_START .2	DE_V_START .1	DE_V_START .0	DE_V_END .3	DE_V_END .2	DE_V_END .1	DE_V_END .0	00000000	00
143	8Fh	Free Run Line Length 1	w		LLC_PAD_SEL _MAN	LLC_PAD_SEL .1	LLC_PAD_SEL .0		FR_LL .10	FR_LL .9	FR_LL .8	00000000	00
144	90h	VBI Info	r					CGMSD	EDTVD	CCAP D	WSSD	---	---
144	90h	Free Run Line Lengh 2	w	FR_LL.7	FR_LL.6	FR_LL.5	FR_LL.4	FR_LL.3	FR_LL.2	FR_LL.1	FR_LL.0	00000000	00
145	91h	WSS 1	r	WSS1.7	WSS1.6	WSS1.5	WSS1.4	WSS1.3	WSS1.2	WSS1.1	WSS1.0	---	---
145	91h	DPP_CP_64	w		interlaced							0101xxxx	50
146	92h	WSS 2	r	WSS2.7	WSS2.6	WSS2.5	WSS2.4	WSS2.3	WSS2.2	WSS2.1	WSS2.0	---	---
147	93h	EDTV 1	r	EDTV1.7	EDTV1.6	EDTV1.5	EDTV1.4	EDTV1.3	EDTV1.2	EDTV1.1	EDTV1.0	---	---
148	94h	EDTV 2	r	EDTV2.7	EDTV2.6	EDTV2.5	EDTV2.4	EDTV2.3	EDTV2.2	EDTV2.1	EDTV2.0	---	---
149	95h	EDTV 3	r	EDTV3.7	EDTV3.6	EDTV3.5	EDTV3.4	EDTV3.3	EDTV3.2	EDTV3.1	EDTV3.0	---	---
150	96h	CGMS 1	r	CGMS1.7	CGMS1.6	CGMS1.5	CGMS1.4	CGMS1.3	CGMS1.2	CGMS1.1	CGMS1.0	---	---
151	97h	CGMS 2	r	CGMS2.7	CGMS2.6	CGMS2.5	CGMS2.4	CGMS2.3	CGMS2.2	CGMS2.1	CGMS2.0	---	---
152	98h	CGMS 3	r	CGMS3.7	CGMS3.6	CGMS3.5	CGMS3.4	CGMS3.3	CGMS3.2	CGMS3.1	CGMS3.0	---	---
153	99h	CCAP 1	r	CCAP1 .7	CCAP1 .6	CCAP1 .5	CCAP1 .4	CCAP1 .3	CCAP1 .2	CCAP1 .1	CCAP1 .0	---	---
154	9Ah	CCAP 2	r	CCAP2 .7	CCAP2 .6	CCAP2 .5	CCAP2 .4	CCAP2 .3	CCAP2 .2	CCAP2 .1	CCAP2 .0	---	---
155	9Bh	Letterbox 1	r	LB_LCT.7	LB_LCT.6	LB_LCT.5	LB_LCT.4	LB_LCT.3	LB_LCT.2	LB_LCT.1	LB_LCT.0	---	---
156	9Ch	Letterbox 2	r	LB_LCM.7	LB_LCM.6	LB_LCM.5	LB_LCM.4	LB_LCM.3	LB_LCM.2	LB_LCM.1	LB_LCM.0	---	---
157	9Dh	Letterbox 3	r	LB_LCB .7	LB_LCB .6	LB_LCB .5	LB_LCB .4	LB_LCB .3	LB_LCB .2	LB_LCB .1	LB_LCB .0	---	---
160	A0h	RB CP AGC 1	r		0	0	0	0	0	CP_AGC_GAIN.9	CP_AGC_GAIN.8	---	---
161	A1h	RB CP AGC 2	r	CP_AGC_GAIN.7	CP_AGC_GAIN.6	CP_AGC_GAIN.5	CP_AGC_GAIN.4	CP_AGC_GAIN.3	CP_AGC_GAIN.2	CP_AGC_GAIN.1	CP_AGC_GAIN.0	---	---
162	A2h	RB CP Measure 1	r	NOISE.7	NOISE.6	NOISE.5	NOISE.4	NOISE.3	NOISE.2	NOISE.1	NOISE.0	---	---
162	A2h	DPP_CP_81	w	cp_start_sav.11	cp_start_sav.10	cp_start_sav.9	cp_start_sav.8	cp_start_sav.7	cp_start_sav.6	cp_start_sav.5	cp_start_sav.4	00000000	00
163	A3h	RB CP Measure 2	r	0	0	0	CALIB.10	CALIB.9	CALIB.8	IFSD.8	ISD.8	---	---
163	A3h	DPP_CP_82	w	cp_start_sav.3	cp_start_sav.2	cp_start_sav.1	cp_start_sav.0	cp_start_eav.11	cp_start_eav.10	cp_start_eav.9	cp_start_eav.8	00000000	00
164	A4h	RB CP Measure 3	r	ISD.7	ISD.6	ISD.5	ISD.4	ISD.3	ISD.2	ISD.1	ISD.0	---	---
164	A4h	DPP_CP_83	w	cp_start_eav.7	cp_start_eav.6	cp_start_eav.5	cp_start_eav.4	cp_start_eav.3	cp_start_eav.2	cp_start_eav.1	cp_start_eav.0	00000000	00
165	A5h	RB CP Measure 4	r	IFSD.7	IFSD.6	IFSD.5	IFSD.4	IFSD.3	IFSD.2	IFSD.1	IFSD.0	---	---
165	A5h	DPP_CP_84	w	cp_start_vbi.11	cp_start_vbi.10	cp_start_vbi.9	cp_start_vbi.8	cp_start_vbi.7	cp_start_vbi.6	cp_start_vbi.5	cp_start_vbi.4	00000000	00
166	A6h	RB CP Measure 5	r	CALIB.7	CALIB.6	CALIB.5	CALIB.4	CALIB.3	CALIB.2	CALIB.1	CALIB.0	---	---
166	A6h	DPP_CP_85	w	cp_start_vbi.3	cp_start_vbi.2	cp_start_vbi.1	cp_start_vbi.0	cp_end_vbi.11	cp_end_vbi.10	cp_end_vbi.9	cp_end_vbi.8	00000000	00
167	A7h	RB CP HSync Depth 1	r	0	0	HSD_CHC .9	HSD_CHC .8	HSD_CHB .9	HSD_CHB .8	HSD_CHA .9	HSD_CHA .8	---	---
167	A7h	DPP_CP_86	w	cp_end_vbi.7	cp_end_vbi.6	cp_end_vbi.5	cp_end_vbi.4	cp_end_vbi.3	cp_end_vbi.2	cp_end_vbi.1	cp_end_vbi.0	00000000	00
168	A8h	RB CP HSync Depth 2	r	HSD_CHA .7	HSD_CHA .6	HSD_CHA .5	HSD_CHA .4	HSD_CHA .3	HSD_CHA .2	HSD_CHA .1	HSD_CHA .0	---	---
168	A8h	DPP_CP_87	w	cp_start_vbi_even.11	cp_start_vbi_even.10	cp_start_vbi_even.9	cp_start_vbi_even.8	cp_start_vbi_even.7	cp_start_vbi_even.6	cp_start_vbi_even.5	cp_start_vbi_even.4	00000000	00
169	A9h	RB CP HSync Depth 3	r	HSD_CHB .7	HSD_CHB .6	HSD_CHB .5	HSD_CHB .4	HSD_CHB .3	HSD_CHB .2	HSD_CHB .1	HSD_CHB .0	---	---
169	A9h	DPP_CP_88	w	cp_start_vbi_even.3	cp_start_vbi_even.2	cp_start_vbi_even.1	cp_start_vbi_even.0	cp_end_vbi_even.11	cp_end_vbi_even.10	cp_end_vbi_even.9	cp_end_vbi_even.8	00000000	00
170	AAh	RB CP HSync Depth 4	r	HSD_CHC .7	HSD_CHC .6	HSD_CHC .5	HSD_CHC .4	HSD_CHC .3	HSD_CHC .2	HSD_CHC .1	HSD_CHC .0	---	---
170	AAh	DPP_CP_89	w	Cp_end_vbi_even.7	cp_end_vbi_even.6	cp_end_vbi_even.5	cp_end_vbi_even.4	cp_end_vbi_even.3	cp_end_vbi_even.2	cp_end_vbi_even.1	cp_end_vbi_even.0	00000000	00
171	ABh	RB CP HSync Depth 5	r	0	0	0	0	HSD_FB .11	HSD_FB .10	HSD_FB .9	HSD_FB .8	---	---
171	ABh	DPP_CP_90	w	cp_lcount_max.11	cp_lcount_max.10	cp_lcount_max.9	cp_lcount_max.8	cp_lcount_max.7	cp_lcount_max.6	cp_lcount_max.5	cp_lcount_max.4	00000000	00
172	ACh	RB CP HSync Depth 6	r	HSD_FB .7	HSD_FB .6	HSD_FB .5	HSD_FB .4	HSD_FB .3	HSD_FB .2	HSD_FB .1	HSD_FB .0	---	---
172	ACh	DPP_CP_91	w	cp_lcount_max.3	cp_lcount_max.2	cp_lcount_max.1	cp_lcount_max.0					0000xxxx	00
173	ADh	RB CP Peak Video 1	r	0	0	PKV_CHA .9	PKV_CHA .8	PKV_CHB .9	PKV_CHB .8	PKV_CHC .9	PKV_CHC .8	---	---
174	AEh	RB CP Peak Video 2	r	PKV_CHA .7	PKV_CHA .6	PKV_CHA .5	PKV_CHA .4	PKV_CHA .3	PKV_CHA .2	PKV_CHA .1	PKV_CHA .0	---	---
175	AFh	RB CP Peak Video 3	r	PKV_CHB .7	PKV_CHB .6	PKV_CHB .5	PKV_CHB .4	PKV_CHB .3	PKV_CHB .2	PKV_CHB .1	PKV_CHB .0	---	---
176	B0h	RB CP Peak Video 4	r	PKV_CHC .7	PKV_CHC .6	PKV_CHC .5	PKV_CHC .4	PKV_CHC .3	PKV_CHC .2	PKV_CHC .1	PKV_CHC .0	---	---
177	B1h	RB Standard Ident 1	r	STDI_DVAL ID	STDI_INTLC D	BL.13	BL.12	BL.11	BL.10	BL.9	BL.8	---	---
178	B2h	RB Standard Ident 2	r	BL.7	BL.6	BL.5	BL.4	BL.3	BL.2	BL.1	BL.0	---	---
178	B2h	DPP_CP_97	w						CRC_ENABL E			00011100	1C
179	B3h	RB Standard Ident 3	r	SCVS.4	SCVS.3	SCVS.2	SCVS.1	SCVS.0	SCF.10	SCF.9	SCF.8	---	---
179	B3h	DPP_CP_98	w				CP_FL_FR_THRESH OLD.1	CP_FL_FR_THRESH OLD.0	cp_f_run_th.2	cp_f_run_th.1	cp_f_run_th.0	01110100	74
180	B4h	RB Standard Ident 4	r	SCF.7	SCF.6	SCF.5	SCF.4	SCF.3	SCF.2	SCF.1	SCF.0	---	---
181	B5h	RB Standard Ident 5	r	SSPD_DVAL ID	VS_ACT	CUR_P OL_VS	HS_ACT	CUR_P OL_HS		CUR_SYNC_SRC .1	CUR_SYNC_SRC .0	---	---
186	BAh	DPP_CP_105	rw	ADC_HD MI_SIMULTANE OUS_MODE						HDMI_FRUN_ MODE	HDMI_FRUN_E N	00100x00	20
188	BCh	DPP_CP_107	r	CSC_C OEFF_SEL_RB .3	CSC_C OEFF_SEL_RB .2	CSC_C OEFF_SEL_RB .1	CSC_C OEFF_SEL_RB .0					---	---
189	BDh	Cp Debug 0	w				DPP_BYPASS_E N					00001011	0B
191	BFh	CP DEF COL 1	rw				EXT_VCL MP_POS_EDGE_SEL		CP_DEF_C OL_MAN_VAL	CP_DEF_C OL_AUT O	CP_FORCE_FREERU N	0001x010	12
192	C0h	CP DEF COL 2	rw	DEF_C OL_CHA .7	DEF_C OL_CHA .6	DEF_C OL_CHA .5	DEF_C OL_CHA .4	DEF_C OL_CHA .3	DEF_C OL_CHA .2	DEF_C OL_CHA .1	DEF_C OL_CHA .0	xxxxxxxx	00
193	C1h	CP DEF COL 3	rw	DEF_C OL_CHB .7	DEF_C OL_CHB .6	DEF_C OL_CHB .5	DEF_C OL_CHB .4	DEF_C OL_CHB .3	DEF_C OL_CHB .2	DEF_C OL_CHB .1	DEF_C OL_CHB .0	xxxxxxxx	00
194	C2h	CP DEF COL 4	rw	DEF_C OL_CHC .7	DEF_C OL_CHC .6	DEF_C OL_CHC .5	DEF_C OL_CHC .4	DEF_C OL_CHC .3	DEF_C OL_CHC .2	DEF_C OL_CHC .1	DEF_C OL_CHC .0	xxxxxxxx	00
195	C3h	ADC Switch 1	rw	ADC1_S W.3	ADC1_S W.2	ADC1_S W.1	ADC1_S W.0	ADC0_S W.3	ADC0_S W.2	ADC0_S W.1	ADC0_S W.0	xxxxxxxx	00
196	C4h	ADC Switch 2	rw	ADC_S W_MAN	SOG_SEL			ADC2_S W.3	ADC2_S W.2	ADC2_S W.1	ADC2_S W.0	0xxxxxxx	00
197	C5h	CP Clamp Pos HS Ctrl 1	rw	CP_CLA MP_AVG_FCTR .1	CP_CLA MP_AVG_FCTR .0		EXT_VCL MP_REGEN					10010001	91
198	C6h	CP Clamp Pos HS Ctrl 2	rw									00000000	00
199	C7h	CP Clamp Pos HS Ctrl 3	rw									00000000	00
200	C8h	CP Clamp Pos HS Ctrl 4	rw									00000000	00
201	C9h	DPP_CP_118	rw				DDR_2X_CL K	DDR_E N	DDR_I2C_RC_F IRST	EXT_CLK_E N	DPP_CP_BYPAS S	00x00100	04
202	CAh	Field Length Count 1	r				FCL.12	FCL.11	FCL.10	FCL.9	FCL.8	---	---
203	CBh	Field Length Count 2	r	FCL.7	FCL.6	FCL.5	FCL.4	FCL.3	FCL.2	FCL.1	FCL.0	---	---
220	DCh	Letterbox Control 1	rw				LB_TH.4	LB_TH.3	LB_TH.2	LB_TH.1	LB_TH.0	10101100	AC
221	DDh	Letterbox Control 2	rw	LB_SL.3	LB_SL.2	LB_SL.1	LB_SL.0	LB_EL.3	LB_EL.2	LB_EL.1	LB_EL.0	01001100	4C
222	DEh	ST Noise Readback 1	r					ST_NOISE_VLD	ST_NOISE.10	ST_NOISE.9	ST_NOISE.8	---	---
223	DFh	ST Noise Readback 2	r	ST_NOISE.7	ST_NOISE.6	ST_NOISE.5	ST_NOISE.4	ST_NOISE.3	ST_NOISE.2	ST_NOISE.1	ST_NOISE.0	---	---
225	E1h	SD Offset U	rw	SD_OFF_U.7	SD_OFF_U.6	SD_OFF_U.5	SD_OFF_U.4	SD_OFF_U.3	SD_OFF_U.2	SD_OFF_U.1	SD_OFF_U.0	10000000	80
226	E2h	SD Offset V	rw	SD_OFF_V.7	SD_OFF_V.6	SD_OFF_V.5	SD_OFF_V.4	SD_OFF_V.3	SD_OFF_V.2	SD_OFF_V.1	SD_OFF_V.0	10000000	80
227	E3h	SD Saturation U	rw	SD_SAT_U.7	SD_SAT_U.6	SD_SAT_U.5	SD_SAT_U.4	SD_SAT_U.3	SD_SAT_U.2	SD_SAT_U.1	SD_SAT_U.0	10000000	80
228	E4h	SD Saturation V	rw	SD_SAT_V.7	SD_SAT_V.6	SD_SAT_V.5	SD_SAT_V.4	SD_SAT_V.3	SD_SAT_V.2	SD_SAT_V.1	SD_SAT_V.0	10000000	80
229	E5h	NTSC V bit begin	rw	NVBEGDEL O	NVBEGDEL E	NVBEGSIGN	NVBEG.4	NVBEG.3	NVBEG.2	NVBEG.1	NVBEG.0	00100101	25
230	E6h	NTSC V bit end	rw	NVENDDEL O	NVENDDEL E	NVENDS IGN	NVEND .4	NVEND .3	NVEND .2	NVEND .1	NVEND .0	00000100	04
231	E7h	NTSC F bit toggle	rw	NFTOGDEL O	NFTOGDEL E	NFTOGSIGN	NFTOG.4	NFTOG.3	NFTOG.2	NFTOG.1	NFTOG.0	01100111	63
232	E8h	PAL V bit begin	rw	PVBEGDEL O	PVBEGDEL E	PVBEGSIGN	PVBEG.4	PVBEG.3	PVBEG.2	PVBEG.1	PVBEG.0	01100101	65
233	E9h	PAL V bit end	rw	PVENDDEL O	PVENDDEL E	PVENDS IGN	PVEND .4	PVEND .3	PVEND .2	PVEND .1	PVEND .0	00010100	14
234	EAh	PAL F bit toggle	rw	PFTOGDEL O	PFTOGDEL E	PFTOGSIGN	PFTOG.4	PFTOG.3	PFTOG.2	PFTOG.1	PFTOG.0	01100111	63
235	EBh	Vblank Control 1	rw	NVBIOLCM.1	NVBIOLCM.0	NVBIELCM.1	NVBIELCM.0	PVBIOLCM.1	PVBIOLCM.0	PVBIELCM.1	PVBIELCM.0	01010101	55
236	ECh	Vblank Control 2	rw	NVBIOCCM.1	NVBIOCCM.0	NVBIECCM.1	NVBIECCM.0	PVBIOCCM.1	PVBIOCCM.0	PVBIECCM.1	PVBIECCM.0	01010101	55
237	EDh	FB_STATUS	r	FB_STATUS .3	FB_STATUS .2	FB_STATUS .1	FB_STATUS .0					---	---
237	EDh	FB_CONTROL1	w					FB_INV	CVBS_R GB_SEL	FB_MODE.1	FB_MODE.0	00010000	10
238	EEh	FB_CONTROL 2	rw	FB_CSC_ MAN	MAN_ALPHA_VAL .6	MAN_ALPHA_VAL .5	MAN_ALPHA_VAL .4	MAN_ALPHA_VAL .3	MAN_ALPHA_VAL .2	MAN_ALPHA_VAL .1	MAN_ALPHA_VAL .0	00000000	00
239	EFh	FB_CONTROL 3	rw	FB_SP_AD JUST.3	FB_SP_AD JUST.2	FB_SP_AD JUST.1	FB_SP_AD JUST.0	CNTR_ENABL E	FB_EDGE_SHAPE .2	FB_EDGE_SHAPE .1	FB_EDGE_SHAPE .0	01001010	4A
240	F0h	FB_CONTROL 4	rw					FB_DELAY .3	FB_DELAY .2	FB_DELAY .1	FB_DELAY .0	01000011	43
241	F1h	FB_CONTROL 5	rw	CNTR_LEVEL .1	CNTR_LEVEL .0	FB_LEVEL .2	FB_LEVEL .1	FB_LEVEL .0	CNTR_ MODE.1	CNTR_ MODE.0	RGB_IP_SEL	00001110	0E
243	F3h	AFE_CONTROL 1	rw	ADC3_S W.3	ADC3_S W.2	ADC3_S W.1	ADC3_S W.0	AA_FILT_EN.3	AA_FILT_EN.2	AA_FILT_EN.1	AA_FILT_EN.0	00000000	00
244	F4h	Drive Strength	rw	AA_FILT_PR OG_BW.1	AA_FILT_PR OG_BW.0	DR_ST R	DR_STR .0	DR_STR_ C	DR_STR_C .0	DR_STR_ S	DR_STR_S .0	00010101	15
248	F8h	IF Comp Control	rw						IFFILTSEL .2	IFFILTSEL .1	IFFILTSEL .0	00000000	00
249	F9h	VS Mode Control	rw					VS_COAST_MODE.1	VS_COAST_MODE.0	EXTEND_VS_ MIN_FRE Q	EXTEND_VS_ MAX_FRE Q	00000011	03
251	FBh	Peaking Control	rw	PEAKING_GAIN.7	PEAKING_GAIN.6	PEAKING_GAIN.5	PEAKING_GAIN.4	PEAKING_GAIN.3	PEAKING_GAIN.2	PEAKING_GAIN.1	PEAKING_GAIN.0	01000000	40
252	FCh	Coring Threshold 2	rw	DNR_TH_2 .7	DNR_TH_2 .6	DNR_TH_2 .5	DNR_TH_2 .4	DNR_TH_2 .3	DNR_TH_2 .2	DNR_TH_2 .1	DNR_TH_2 .0	00000100	04
253	FDh	general_chip_ctl	rw								PIN_CHECKER_E N	00000000	00
254	FEh	Pin_Checker_Op	rw	PIN_CHECKER_ OP.7	PIN_CHECKER_ OP.6	PIN_CHECKER_ OP.5	PIN_CHECKER_ OP.4	PIN_CHECKER_ OP.3	PIN_CHECKER_ OP.2	PIN_CHECKER_ OP.1	PIN_CHECKER_ OP.0	10101010	AA

1.2 User Map 1

Table 3: User Map 1 Register 0x40 to 0x9E

Address		Register Name	rw	7	6	5	4	3	2	1	0	Reset Value	(Hex)
64	40h	Interrupt Configuration 0	rw	INTRQ_DUR_SEL.1	INTRQ_DUR_SEL.0	MV_INTRQ_SEL.1	MV_INTRQ_SEL.0	INTERNAL_MUTE_INT	MPU_STIM_INTRQ	INTRQ_OP_SEL.1	INTRQ_OP_SEL.0	00010000	10
65	41h	Interrupt Configuration 1	rw	INTRQ2_DUR_SEL.1	INTRQ2_DUR_SEL.0			INTERNAL_MUTE_INT2		INTRQ2_OP_SEL.1	INTRQ2_OP_SEL.0	00000000	00
66	42h	Interrupt Status 1	r	SSPD_RESULT_Q	MV_PS_CS_Q	SD_FR_CHNG_Q	STDI_DVALID_Q	CP_UNLOCK_Q	CP_LOCK_Q	SD_UNLOCK_Q	SD_LOCK_Q	---	---
66	42h	Interrupt Clear 1	w	SSPD_RESULT_CLR	MV_PS_CS_CLR	SD_FR_CHNG_CLR	STDI_DVALID_CLR	CP_UNLOCK_CLR	CP_LOCK_CLR	SD_UNLOCK_CLR	SD_LOCK_CLR	00000000	00
67	43h	Interrupt 2 Maskb 1	rw	SSPD_RESULT_MSKB2	MV_PS_CS_MSKB2	SD_FR_CHNG_MSKB2	STDI_DVALID_MSKB2	CP_UNLOCK_MSKB2	CP_LOCK_MSKB2	SD_UNLOCK_MSKB2	SD_LOCK_MSKB2	00000000	00
68	44h	Interrupt Maskb 1	rw	SSPD_RESULT_MSKB	MV_PS_CS_MSKB	SD_FR_CHNG_MSKB	STDI_DVALID_MSKB	CP_UNLOCK_MSKB	CP_LOCK_MSKB	SD_UNLOCK_MSKB	SD_LOCK_MSKB	00000000	00
69	45h	Raw Status 2	r	MPU_STIM_INTRQ			EVEN_FIELD				CCAPD	---	---
70	46h	Interrupt Status 2	r	MPU_STIM_INTRQ_Q			SD_FIELD_CHNGD_Q	WSS_CHNGD_Q	CGMS_CHNGD_Q	GEMD_Q	CCAPD_Q	---	---
70	46h	Interrupt Clear 2	w	MPU_STIM_INTRQ_CLR			SD_FIELD_CHNGD_CLR	WSS_CHNGD_CLR	CGMS_CHNGD_CLR	GEMD_CLR	CCAPD_CLR	0xx00000	00
71	47h	Interrupt 2 Maskb 2	rw	MPU_STIM_INT2_MSKB2			SD_FIELD_CHN_MSKB2	WSS_CHNGD_MSKB2	CGMS_CHN_MSKB2	GEMD_CLR_MSKB2	CCAPD_CLR_MSKB2	0xx00000	00
72	48h	Interrupt Maskb 2	rw	MPU_STIM_INTRQ_MSKB			SD_FIELD_CHNGD_MSKB	WSS_CHNGD_MSKB	CGMS_CHNGD_MSKB	GEMD_MSKB	CCAPD_MSKB	0xx00000	00
73	49h	Raw Status 3	r	FL_PLL_LOCKED			SCM_LOCK		SD_H_LOCK	SD_V_LOCK	SD_OP_50Hz	---	---
74	4Ah	Interrupt Status 3	r	FL_PLL_LOCKED_Q		PAL_SW_LK_CHNG_Q	SCM_LOCK_CHNG_Q	SD_AD_CHNG_Q	SD_H_LOCK_CHNG_Q	SD_V_LOCK_CHNG_Q	SD_OP_CHNG_Q	---	---
74	4Ah	Interrupt Clear 3	w	FL_PLL_LOCKED_MASKB2		PAL_SW_LK_CHNG_CLR	SCM_LOCK_CHNG_CLR	SD_AD_CHNG_CLR	SD_H_LOCK_CHNG_CLR	SD_V_LOCK_CHNG_CLR	SD_OP_CHNG_CLR	xx000000	00
75	4Bh	Interrupt 2 Maskb 3	rw	FL_PLL_LOCKED_MASKB		PAL_SW_LK_CHNG_MSKB2	SCM_LOCK_CHNG_MSKB2	SD_AD_CHNG_MSKB2	SD_H_LOCK_CHNG_MSKB2	SD_V_LOCK_CHNG_MSKB2	SD_OP_CHNG_MSKB2	xx000000	00
76	4Ch	Interrupt Maskb 3	rw	FL_PLL_LOCKED		PAL_SW_LK_CHNG_MSKB	SCM_LOCK_CHNG_MSKB	SD_AD_CHNG_MSKB	SD_H_LOCK_CHNG_MSKB	SD_V_LOCK_CHNG_MSKB	SD_OP_CHNG_MSKB	xx000000	00
77	4Dh	Raw Status 4	r	VDP_TTX_AVL	VDP_VITC_AVL		VDP_GS_PDC_VPS_UTC_AVL		VDP_CGMS_WSS_AVL		VDP_CC_AVL	---	---
78	4Eh	Interrupt Status 4	r	VDP_TTX_AVL_Q	VDP_VITC_Q		VDP_GS_VPS_PDC_UTC_CHG		VDP_CGMS_WSS_CHNGD_Q		VDP_CCAPD_Q	---	---
78	4Eh	Interrupt Clear 4	w	VDP_TTX_AVL	VDP_VITC_CLR							00x0x0x0	00
79	4Fh	Interrupt 2 Maskb 4	rw	VDP_TTX_AVL_MSKB2	VDP_VITC_MSKB2		VDP_GS_VPS_PDC_UTC_CHG		VDP_CGMS_WSS_CHNGD_M		VDP_CCAPD_MSKB2	00x0x0x0	00
80	50h	Interrupt Maskb 4	rw	VDP_TTX_AVL_MSKB	VDP_VITC_MSKB		VDP_GS_VPS_PDC_UTC_CHG		VDP_CGMS_WSS_CHNGD_M		VDP_CCAPD_MSKB	00x0x0x0	00
96	60h	HDMI Raw Status 1	r	DSD_PCKT_RAW	ISRC2_PCKT_RAW	ISRC1_PCKT_RAW	ACP_PCKT_RAW	MS_INFO_RAW	SPD_INFO_RAW	AUDIO_INFO_RAW	AVI_INFO_RAW	---	---
97	61h	HDMI Int Status 1	r	DSD_PCKT_ST	ISRC2_PCKT_ST	ISRC1_PCKT_ST	ACP_PCKT_ST	MS_INFO_ST	SPD_INFO_ST	AUDIO_INFO_ST	AVI_INFO_ST	---	---
97	61h	HDMI Int Clr 1	w	DSD_PCKT_CLR	ISRC2_PCKT_CLR	ISRC1_PCKT_CLR	ACP_PCKT_CLR	MS_INFO_CLR	SPD_INFO_CLR	AUDIO_INFO_CLR	AVI_INFO_CLR	00000000	00
98	62h	HDMI Int2 Maskb 1	rw	DSD_PCKT_MB2	ISRC2_PCKT_MB2	ISRC1_PCKT_MB2	ACP_PCKT_MB2	MS_INFO_MB2	SPD_INFO_MB2	AUDIO_INFO_MB2	AVI_INFO_MB2	00000000	00
99	63h	HDMI Int Maskb 1	rw	DSD_PCKT_MB1	ISRC2_PCKT_MB1	ISRC1_PCKT_MB1	ACP_PCKT_MB1	MS_INFO_MB1	SPD_INFO_MB1	AUDIO_INFO_MB1	AVI_INFO_MB1	00000000	00
100	64h	HDMI Raw Status 2	r	AUDIO_PLL_LCK_RAW	HDMI_ENCRPT_RAW	DE_REGEN_LCK_RAW	AV_MUTE_RAW	INFO_FR_PCKT_RAW	GEN_CTL_PCKT_RAW	AUDIO_C_PCKT_RAW	AUDIO_S_PCKT_RAW	---	---
101	65h	HDMI Int Status 2	r	AUDIO_PLL_LCK_ST	HDMI_ENCRPT_ST	DE_REGEN_LCK_ST	AV_MUTE_ST	INFO_FR_PCKT_ST	GEN_CTL_PCKT_ST	AUDIO_C_PCKT_ST	AUDIO_S_PCKT_ST	---	---
101	65h	HDMI Int Clr 2	w	AUDIO_PLL_LCK_CLR	HDMI_ENCRPT_CLR	DE_REGEN_LCK_CLR	AV_MUTE_CLR	INFO_FR_PCKT_CLR	GEN_CTL_PCKT_CLR	AUDIO_C_PCKT_CLR	AUDIO_S_PCKT_CLR	00000000	00
102	66h	HDMI Int2 Maskb 2	rw	AUDIO_PLL_LCK_MB2	HDMI_ENCRPT_MB2	DE_REGEN_LCK_MB2	AV_MUTE_MB2	INFO_FR_PCKT_MB2	GEN_CTL_PCKT_MB2	AUDIO_C_PCKT_MB2	AUDIO_S_PCKT_MB2	00000000	00
103	67h	HDMI Int Maskb 2	rw	AUDIO_PLL_LCK_MB1	HDMI_ENCRPT_MB1	DE_REGEN_LCK_MB1	AV_MUTE_MB1	INFO_FR_PCKT_MB1	GEN_CTL_PCKT_MB1	AUDIO_C_PCKT_MB1	AUDIO_S_PCKT_MB1	00000000	00
104	68h	HDMI Raw Status 3	r	V_LOCKED_RAW	GAMUT_MDATA_RAW	INTERNAL_MUTE_RAW	TMDS_CLK_A_RAW	TMDS_CLK_B_RAW	AUDIO_CH_MODE_R	HDMI_MODE_RAW	VIDEO_PLL_LCK_RAW	---	---
105	69h	HDMI Int Status 3	r	V_LOCKED_ST	GAMUT_MDATA_ST	INTERNAL_MUTE_ST	TMDS_CLK_A_ST	TMDS_CLK_B_ST	AUDIO_CH_MD_ST	HDMI_MODE_ST	VIDEO_PLL_LCK_ST	---	---
105	69h	HDMI Int Clr 3	w	V_LOCKED_CL	GAMUT_MDATA_CLR	INTERNAL_MUTE_CLR	TMDS_CLK_A_CLR	TMDS_CLK_B_CLR	AUDIO_CH_MD_CLR	HDMI_MODE_CLR	VIDEO_PLL_LCK_CLR	00000000	00
106	6Ah	HDMI Int2 Maskb 3	rw	V_LOCKED_MB2	GAMUT_MDATA_MB2	INTERNAL_MUTE_MB2	TMDS_CLK_A_MB2	TMDS_CLK_B_MB2	AUDIO_CH_MD_MB2	HDMI_MODE_MB2	VIDEO_PLL_LCK_MB2	00000000	00
107	6Bh	HDMI Int Maskb 3	rw	V_LOCKED_MB1	GAMUT_MDATA_MB1	INTERNAL_MUTE_MB1	TMDS_CLK_A_MB1	TMDS_CLK_B_MB1	AUDIO_CH_MD_MB1	HDMI_MODE_MB1	VIDEO_PLL_LCK_MB1	00000000	00
108	6Ch	HDMI Int Status 4	r	NEW_GAMUT_MDATA_ST	NEW_ISRC2_PCKT_ST	NEW_ISRC1_PCKT_ST	NEW_ACP_PCKT_ST	NEW_MS_INFO_ST	NEW_SPD_INFO_ST	NEW_AUDIO_INFO_ST	NEW_AVI_INFO_ST	---	---
108	6Ch	HDMI Int Clr 4	w	NEW_GAMUT_MDATA_CLR	NEW_ISRC2_PCKT_CL	NEW_ISRC1_PCKT_CL	NEW_ACP_PCKT_CLR	NEW_MS_INFO_CLR	NEW_SPD_INFO_CLR	NEW_AUDIO_INFO_CL	NEW_AVI_INFO_CLR	00000000	00
109	6Dh	HDMI Int2 Maskb 4	rw	NEW_GAMUT_MDATA_MB2	NEW_ISRC2_PKT_M2	NEW_ISRC1_PKT_M2	NEW_ACP_PKT_MB2	NEW_MS_INFO_MB2	NEW_SPD_INFO_MB2	NEW_AUDIO_INF_M2	NEW_AVI_INFO_MB2	00000000	00
110	6Eh	HDMI Int Maskb 4	rw	NEW_GAMUT_MDATA_MB1	NEW_ISRC2_PKT_M1	NEW_ISRC1_PKT_M1	NEW_ACP_PKT_MB1	NEW_MS_INFO_MB1	NEW_SPD_INFO_MB1	NEW_AUDIO_IN_M1	NEW_AVI_INFO_MB1	00000000	00
111	6Fh	HDMI Int Status 5	r				CTS_PASS_THRSH_ST	CHANGE_N_ST	INFOFRAME_ERR_ST	PACKET_ERROR_ST	AUDIO_PCKT_ERR_ST	---	---
111	6Fh	HDMI Int Clr 5	w				CTS_PASS_THRSH_CL	CHANGE_N_CLR	INFOFRAME_ERR_CL	PACKET_ERROR_CLR	AUDIO_PCKT_ERR_CL	00000000	00
112	70h	HDMI Int2 Maskb 5	rw				CTS_PASS_THRS_M2	CHANGE_N_MB2	INFOFRAME_ERR_M2	PACKET_ERROR_MB2	AUDIO_PKT_ERR_M2	00000000	00
113	71h	HDMI Int Maskb 5	rw				CTS_PASS_THRS_M1	CHANGE_N_MB1	INFOFRAME_ERR_M1	PACKET_ERROR_MB1	AUDIO_PKT_ERR_M1	00000000	00
114	72h	HDMI Status 6	r	DEEP_COLOR_CHNG_ST	VCLK_CHNG_ST	AKSV_UPDATE_ST	PARRITY_ERROR_ST	NEW_SAMP_RT_ST	AUDIO_FLT_LINE_ST	NEW_TMDS_FRQ_ST	FIFO_NEAR_UFLO_ST	---	---
114	72h	HDMI Int Clr 6	w	DEEP_COLOR_CHNG_CLR	VCLK_CHNG_CL	AKSV_UPDATE_CL	PARRITY_ERROR_CL	NEW_SAMP_RT_CL	AUDIO_FLT_LINE_CL	NEW_TMDS_FRQ_CL	FIFO_NEAR_UFLO_CLR	00000000	00
115	73h	HDMI Int2 Maskb 6	rw	DEEP_COLOR_CHNG_MB2	VCLK_CHNG_MB2	AKSV_UPDATE_M2	PARRITY_ERROR_M2	NEW_SAMP_RT_MB2	AUDIO_FLT_LINE_M2	NEW_TMDS_FRQ_M2	FIFO_NEAR_UFLO_M2	00000000	00
116	74h	HDMI Int Maskb 6	rw	DEEP_COLOR_CHNG_MB1	VCLK_CHNG_MB1	AKSV_UPDATE_M1	PARRITY_ERROR_M1	NEW_SAMP_RT_MB1	AUDIO_FLT_LINE_M1	NEW_TMDS_FRQ_M1	FIFO_NEAR_UFLO_M1	00000000	00
117	75h	DLL on LLC path	rw		DLL_on_LLC_en	DLL_on_LLC_mux	DLL_on_LLC_Phase4	DLL_on_LLC_Phase3	DLL_on_LLC_Phase2	DLL_on_LLC_Phase1	DLL_on_LLC_Phase0	00000000	00
154	9Ah	CP CONTRAST	rw	CP_CONTRAST.7	CP_CONTRAST.6	CP_CONTRAST.5	CP_CONTRAST.4	CP_CONTRAST.3	CP_CONTRAST.2	CP_CONTRAST.1	CP_CONTRAST.0	10000000	80
155	9Bh	CP SATURATION	rw	CP_SATURATION.7	CP_SATURATION.6	CP_SATURATION.5	CP_SATURATION.4	CP_SATURATION.3	CP_SATURATION.2	CP_SATURATION.1	CP_SATURATION.0	10000000	80
156	9Ch	CP BRIGHTNESS	rw	CP_BRIGHTNESS7	CP_BRIGHTNESS6	CP_BRIGHTNESS5	CP_BRIGHTNESS4	CP_BRIGHTNESS3	CP_BRIGHTNESS2	CP_BRIGHTNESS1	CP_BRIGHTNESS0	00000000	00
157	9Dh	CP HUE	rw	CP_HUE.7	CP_HUE.6	CP_HUE.5	CP_HUE.4	CP_HUE.3	CP_HUE.2	CP_HUE.1	CP_HUE.0	00000000	00
158	9Eh	VID_ADJ_BLANK_CTRL	rw	VID_ADJ_EN								10000000	80

1.3 User Map 2

Table 4: User Map 2 Register 0xEA to 0xEF

Address		Register Name	rw	7	6	5	4	3	2	1	0	Reset Value	(Hex)
234	EAh	rsv_slave_address	rw	RSV_ADDR.7	RSV_ADDR.6	RSV_ADDR.5	RSV_ADDR.4	RSV_ADDR.3	RSV_ADDR.2	RSV_ADDR.1	RSV_ADDR.0	01001100	4C
235	EBh	uss1_slave_address	rw	USS1_ADDR.7	USS1_ADDR.6	USS1_ADDR.5	USS1_ADDR.4	USS1_ADDR.3	USS1_ADDR.2	USS1_ADDR.1	USS1_ADDR.0	01000100	44
236	ECh	vdp_slave_address	rw	VDP_ADDR.7	VDP_ADDR.6	VDP_ADDR.5	VDP_ADDR.4	VDP_ADDR.3	VDP_ADDR.2	VDP_ADDR.1	VDP_ADDR.0	01001000	48
237	EDh	ksv_slave_address	rw	KSV_ADDR.7	KSV_ADDR.6	KSV_ADDR.5	KSV_ADDR.4	KSV_ADDR.3	KSV_ADDR.2	KSV_ADDR.1	KSV_ADDR.0	01100100	64
238	EEh	edid_slave_address	rw	EDID_ADDR.7	EDID_ADDR.6	EDID_ADDR.5	EDID_ADDR.4	EDID_ADDR.3	EDID_ADDR.2	EDID_ADDR.1	EDID_ADDR.0	01101100	6C
239	EFh	hdmi_slave_address	rw	HDMI_ADDR.7	HDMI_ADDR.6	HDMI_ADDR.5	HDMI_ADDR.4	HDMI_ADDR.3	HDMI_ADDR.2	HDMI_ADDR.1	HDMI_ADDR.0	01101000	68

1.4 User Map 3 (VDP Map)

Table 5: User Map 3 Register 0x3C to 0x9C

Address		Register Name	rw	7	6	5	4	3	2	1	0	Reset Value	(Hex)
60	3Ch	vdp_cgms_typeb_data_1	b	vdp_cgms_typeb_data[7]	vdp_cgms_typeb_data[6]	vdp_cgms_typeb_data[5]	vdp_cgms_typeb_data[4]	vdp_cgms_typeb_data[3]	vdp_cgms_typeb_data[2]	vdp_cgms_typeb_data[1]	vdp_cgms_typeb_data[0]	---	---
61	3Dh	vdp_cgms_typeb_data_2	b	vdp_cgms_typeb_data[15]	vdp_cgms_typeb_data[14]	vdp_cgms_typeb_data[13]	vdp_cgms_typeb_data[12]	vdp_cgms_typeb_data[11]	vdp_cgms_typeb_data[10]	vdp_cgms_typeb_data[9]	vdp_cgms_typeb_data[8]	---	---
62	3Eh	vdp_cgms_typeb_data_3	b	vdp_cgms_typeb_data[23]	vdp_cgms_typeb_data[22]	vdp_cgms_typeb_data[21]	vdp_cgms_typeb_data[20]	vdp_cgms_typeb_data[19]	vdp_cgms_typeb_data[18]	vdp_cgms_typeb_data[17]	vdp_cgms_typeb_data[16]	---	---
63	3Fh	vdp_cgms_typeb_data_4	b	vdp_cgms_typeb_data[31]	vdp_cgms_typeb_data[30]	vdp_cgms_typeb_data[29]	vdp_cgms_typeb_data[28]	vdp_cgms_typeb_data[27]	vdp_cgms_typeb_data[26]	vdp_cgms_typeb_data[25]	vdp_cgms_typeb_data[24]	---	---
64	40h	vdp_status	r	status_tbd	status_vitc	status_gems_type	status_gems_vps		status_wss_cgms	status_ccap_even_field	status_ccap	---	---
65	41h	vdp_ccap_data_0	r	vdp_ccap_data[7]	vdp_ccap_data[6]	vdp_ccap_data[5]	vdp_ccap_data[4]	vdp_ccap_data[3]	vdp_ccap_data[2]	vdp_ccap_data[1]	vdp_ccap_data[0]	---	---
66	42h	vdp_ccap_data_1	r	vdp_ccap_data[15]	vdp_ccap_data[14]	vdp_ccap_data[13]	vdp_ccap_data[12]	vdp_ccap_data[11]	vdp_ccap_data[10]	vdp_ccap_data[9]	vdp_ccap_data[8]	---	---
67	43h	vdp_cgms_wss_data_0	r	vdp_cgms_wss_data[23]	vdp_cgms_wss_data[22]	vdp_cgms_wss_data[21]	vdp_cgms_wss_data[20]	vdp_cgms_wss_data[19]	vdp_cgms_wss_data[18]	vdp_cgms_wss_data[17]	vdp_cgms_wss_data[16]	---	---
68	44h	vdp_cgms_wss_data_1	r	vdp_cgms_wss_data[15]	vdp_cgms_wss_data[14]	vdp_cgms_wss_data[13]	vdp_cgms_wss_data[12]	vdp_cgms_wss_data[11]	vdp_cgms_wss_data[10]	vdp_cgms_wss_data[9]	vdp_cgms_wss_data[8]	---	---
69	45h	vdp_cgms_wss_data_2	r	vdp_cgms_wss_data[7]	vdp_cgms_wss_data[6]	vdp_cgms_wss_data[5]	vdp_cgms_wss_data[4]	vdp_cgms_wss_data[3]	vdp_cgms_wss_data[2]	vdp_cgms_wss_data[1]	vdp_cgms_wss_data[0]	---	---
70	46h	vdp_wss_biphase_error_count	r					vdp_wss_biphase_error_count[3]	vdp_wss_biphase_error_count[2]	vdp_wss_biphase_error_count[1]	vdp_wss_biphase_error_count[0]	---	---
71	47h	vdp_gs_vps_pdc_utc_cgmstb	r	vdp_gs_vps_pdc_utc_cgmstb_data[7]	vdp_gs_vps_pdc_utc_cgmstb_data[6]	vdp_gs_vps_pdc_utc_cgmstb_data[5]	vdp_gs_vps_pdc_utc_cgmstb_data[4]	vdp_gs_vps_pdc_utc_cgmstb_data[3]	vdp_gs_vps_pdc_utc_cgmstb_data[2]	vdp_gs_vps_pdc_utc_cgmstb_data[1]	vdp_gs_vps_pdc_utc_cgmstb_data[0]	---	---
72	48h	vdp_gs_vps_pdc_utc_cgmstb	r	vdp_gs_vps_pdc_utc_cgmstb_data[15]	vdp_gs_vps_pdc_utc_cgmstb_data[14]	vdp_gs_vps_pdc_utc_cgmstb_data[13]	vdp_gs_vps_pdc_utc_cgmstb_data[12]	vdp_gs_vps_pdc_utc_cgmstb_data[11]	vdp_gs_vps_pdc_utc_cgmstb_data[10]	vdp_gs_vps_pdc_utc_cgmstb_data[9]	vdp_gs_vps_pdc_utc_cgmstb_data[8]	---	---
73	49h	vdp_gs_vps_pdc_utc_cgmstb	r	vdp_gs_vps_pdc_utc_cgmstb_data[23]	vdp_gs_vps_pdc_utc_cgmstb_data[22]	vdp_gs_vps_pdc_utc_cgmstb_data[21]	vdp_gs_vps_pdc_utc_cgmstb_data[20]	vdp_gs_vps_pdc_utc_cgmstb_data[19]	vdp_gs_vps_pdc_utc_cgmstb_data[18]	vdp_gs_vps_pdc_utc_cgmstb_data[17]	vdp_gs_vps_pdc_utc_cgmstb_data[16]	---	---
74	4Ah	vdp_gs_vps_pdc_utc_cgmstb	r	vdp_gs_vps_pdc_utc_cgmstb_data[31]	vdp_gs_vps_pdc_utc_cgmstb_data[30]	vdp_gs_vps_pdc_utc_cgmstb_data[29]	vdp_gs_vps_pdc_utc_cgmstb_data[28]	vdp_gs_vps_pdc_utc_cgmstb_data[27]	vdp_gs_vps_pdc_utc_cgmstb_data[26]	vdp_gs_vps_pdc_utc_cgmstb_data[25]	vdp_gs_vps_pdc_utc_cgmstb_data[24]	---	---
75	4Bh	vdp_vps_pdc_utc_cgmstb_data	r	vdp_gs_vps_pdc_utc_cgmstb_data[39]	vdp_gs_vps_pdc_utc_cgmstb_data[38]	vdp_gs_vps_pdc_utc_cgmstb_data[37]	vdp_gs_vps_pdc_utc_cgmstb_data[36]	vdp_gs_vps_pdc_utc_cgmstb_data[35]	vdp_gs_vps_pdc_utc_cgmstb_data[34]	vdp_gs_vps_pdc_utc_cgmstb_data[33]	vdp_gs_vps_pdc_utc_cgmstb_data[32]	---	---
76	4Ch.	vdp_vps_pdc_utc_cgmstb_data	r	vdp_gs_vps_pdc_utc_cgmstb_data[47]	vdp_gs_vps_pdc_utc_cgmstb_data[46]	vdp_gs_vps_pdc_utc_cgmstb_data[45]	vdp_gs_vps_pdc_utc_cgmstb_data[44]	vdp_gs_vps_pdc_utc_cgmstb_data[43]	vdp_gs_vps_pdc_utc_cgmstb_data[42]	vdp_gs_vps_pdc_utc_cgmstb_data[41]	vdp_gs_vps_pdc_utc_cgmstb_data[40]	---	---
77	4Dh	vdp_vps_pdc_utc_cgmstb_data	r	vdp_gs_vps_pdc_utc_cgmstb_data[55]	vdp_gs_vps_pdc_utc_cgmstb_data[54]	vdp_gs_vps_pdc_utc_cgmstb_data[53]	vdp_gs_vps_pdc_utc_cgmstb_data[52]	vdp_gs_vps_pdc_utc_cgmstb_data[51]	vdp_gs_vps_pdc_utc_cgmstb_data[50]	vdp_gs_vps_pdc_utc_cgmstb_data[49]	vdp_gs_vps_pdc_utc_cgmstb_data[48]	---	---
78	4Eh	vdp_vps_pdc_utc_cgmstb_data	r	vdp_gs_vps_pdc_utc_cgmstb_data[63]	vdp_gs_vps_pdc_utc_cgmstb_data[62]	vdp_gs_vps_pdc_utc_cgmstb_data[61]	vdp_gs_vps_pdc_utc_cgmstb_data[60]	vdp_gs_vps_pdc_utc_cgmstb_data[59]	vdp_gs_vps_pdc_utc_cgmstb_data[58]	vdp_gs_vps_pdc_utc_cgmstb_data[57]	vdp_gs_vps_pdc_utc_cgmstb_data[56]	---	---
79	4Fh	vdp_vps_pdc_utc_cgmstb_data	r	vdp_gs_vps_pdc_utc_cgmstb_data[71]	vdp_gs_vps_pdc_utc_cgmstb_data[70]	vdp_gs_vps_pdc_utc_cgmstb_data[69]	vdp_gs_vps_pdc_utc_cgmstb_data[68]	vdp_gs_vps_pdc_utc_cgmstb_data[67]	vdp_gs_vps_pdc_utc_cgmstb_data[66]	vdp_gs_vps_pdc_utc_cgmstb_data[65]	vdp_gs_vps_pdc_utc_cgmstb_data[64]	---	---
80	50h	vdp_vps_pdc_utc_cgmstb_data	r	vdp_gs_vps_pdc_utc_cgmstb_data[79]	vdp_gs_vps_pdc_utc_cgmstb_data[78]	vdp_gs_vps_pdc_utc_cgmstb_data[77]	vdp_gs_vps_pdc_utc_cgmstb_data[76]	vdp_gs_vps_pdc_utc_cgmstb_data[75]	vdp_gs_vps_pdc_utc_cgmstb_data[74]	vdp_gs_vps_pdc_utc_cgmstb_data[73]	vdp_gs_vps_pdc_utc_cgmstb_data[72]	---	---
81	51h	vdp_vps_pdc_utc_cgmstb_data	r	vdp_gs_vps_pdc_utc_cgmstb_data[87]	vdp_gs_vps_pdc_utc_cgmstb_data[86]	vdp_gs_vps_pdc_utc_cgmstb_data[85]	vdp_gs_vps_pdc_utc_cgmstb_data[84]	vdp_gs_vps_pdc_utc_cgmstb_data[83]	vdp_gs_vps_pdc_utc_cgmstb_data[82]	vdp_gs_vps_pdc_utc_cgmstb_data[81]	vdp_gs_vps_pdc_utc_cgmstb_data[80]	---	---
82	52h	vdp_vps_pdc_utc_cgmstb_data	r	vdp_gs_vps_pdc_utc_cgmstb_data[95]	vdp_gs_vps_pdc_utc_cgmstb_data[94]	vdp_gs_vps_pdc_utc_cgmstb_data[93]	vdp_gs_vps_pdc_utc_cgmstb_data[92]	vdp_gs_vps_pdc_utc_cgmstb_data[91]	vdp_gs_vps_pdc_utc_cgmstb_data[90]	vdp_gs_vps_pdc_utc_cgmstb_data[89]	vdp_gs_vps_pdc_utc_cgmstb_data[88]	---	---
83	53h	vdp_vps_pdc_utc_cgmstb_data	r	vdp_gs_vps_pdc_utc_cgmstb_data[103]	vdp_gs_vps_pdc_utc_cgmstb_data[102]	vdp_gs_vps_pdc_utc_cgmstb_data[101]	vdp_gs_vps_pdc_utc_cgmstb_data[100]	vdp_gs_vps_pdc_utc_cgmstb_data[99]	vdp_gs_vps_pdc_utc_cgmstb_data[98]	vdp_gs_vps_pdc_utc_cgmstb_data[97]	vdp_gs_vps_pdc_utc_cgmstb_data[96]	---	---
84	54h	vdp_vps_biphase_error_count	r	vdp_vps_biphase_error_count[7]	vdp_vps_biphase_error_count[6]	vdp_vps_biphase_error_count[5]	vdp_vps_biphase_error_count[4]	vdp_vps_biphase_error_count[3]	vdp_vps_biphase_error_count[2]	vdp_vps_biphase_error_count[1]	vdp_vps_biphase_error_count[0]	---	---
85	55h	vdp_vitc_data_0	r	vdp_vitc_data[7]	vdp_vitc_data[6]	vdp_vitc_data[5]	vdp_vitc_data[4]	vdp_vitc_data[3]	vdp_vitc_data[2]	vdp_vitc_data[1]	vdp_vitc_data[0]	---	---
86	56h	vdp_vitc_data_1	r	vdp_vitc_data[15]	vdp_vitc_data[14]	vdp_vitc_data[13]	vdp_vitc_data[12]	vdp_vitc_data[11]	vdp_vitc_data[10]	vdp_vitc_data[9]	vdp_vitc_data[8]	---	---
87	57h	vdp_vitc_data_2	r	vdp_vitc_data[23]	vdp_vitc_data[22]	vdp_vitc_data[21]	vdp_vitc_data[20]	vdp_vitc_data[19]	vdp_vitc_data[18]	vdp_vitc_data[17]	vdp_vitc_data[16]	---	---
88	58h	vdp_vitc_data_3	r	vdp_vitc_data[31]	vdp_vitc_data[30]	vdp_vitc_data[29]	vdp_vitc_data[28]	vdp_vitc_data[27]	vdp_vitc_data[26]	vdp_vitc_data[25]	vdp_vitc_data[24]	---	---
89	59h	vdp_vitc_data_4	r	vdp_vitc_data[39]	vdp_vitc_data[38]	vdp_vitc_data[37]	vdp_vitc_data[36]	vdp_vitc_data[35]	vdp_vitc_data[34]	vdp_vitc_data[33]	vdp_vitc_data[32]	---	---
90	5Ah	vdp_vitc_data_5	r	vdp_vitc_data[47]	vdp_vitc_data[46]	vdp_vitc_data[45]	vdp_vitc_data[44]	vdp_vitc_data[43]	vdp_vitc_data[42]	vdp_vitc_data[41]	vdp_vitc_data[40]	---	---
91	5Bh	vdp_vitc_data_6	r	vdp_vitc_data[55]	vdp_vitc_data[54]	vdp_vitc_data[53]	vdp_vitc_data[52]	vdp_vitc_data[51]	vdp_vitc_data[50]	vdp_vitc_data[49]	vdp_vitc_data[48]	---	---
92	5Ch	vdp_vitc_data_7	r	vdp_vitc_data[63]	vdp_vitc_data[62]	vdp_vitc_data[61]	vdp_vitc_data[60]	vdp_vitc_data[59]	vdp_vitc_data[58]	vdp_vitc_data[57]	vdp_vitc_data[56]	---	---
93	5Dh	vdp_vitc_data_8	r	vdp_vitc_data[71]	vdp_vitc_data[70]	vdp_vitc_data[69]	vdp_vitc_data[68]	vdp_vitc_data[67]	vdp_vitc_data[66]	vdp_vitc_data[65]	vdp_vitc_data[64]	---	---
94	5Eh	vdp_vitc_calc_crc	r	vdp_vitc_calc_crc[7]	vdp_vitc_calc_crc[6]	vdp_vitc_calc_crc[5]	vdp_vitc_calc_crc[4]	vdp_vitc_calc_crc[3]	vdp_vitc_calc_crc[2]	vdp_vitc_calc_crc[1]	vdp_vitc_calc_crc[0]	---	---
96	60h	vdp_config_1	rw	ham_err_op_en				en_fc_window_after_crl_det	vdp_tbd_type_man_en	vdp_tbd_type[1]	vdp_tbd_type[0]	00001000	08
97	61h	vdp_config_2	rw	vdp_cp_clmp_avg		noise_clk_disable						00011000	18
98	62h	vdp_adf_config_1	rw	adf_en	adf_mode[1]	adf_mode[0]	did5_2[4]	did5_2[3]	did5_2[2]	did5_2[1]	did5_2[0]	00010101	15
99	63h	vdp_adf_config_2	rw	toggle_adf	sys2_dup_adf	sdid7_2[5]	sdid7_2[4]	sdid7_2[3]	sdid7_2[2]	sdid7_2[1]	sdid7_2[0]	00101010	2A
100	64h	vdp_man_line_1_21	rw	vdp_man_line_1_21[7]	vdp_man_line_1_21[6]	vdp_man_line_1_21[5]	vdp_man_line_1_21[4]	vdp_man_line_1_21[3]	vdp_man_line_1_21[2]	vdp_man_line_1_21[1]	vdp_man_line_1_21[0]	00000000	00
101	65h	vdp_man_line_2_22	rw	vdp_man_line_2_22[7]	vdp_man_line_2_22[6]	vdp_man_line_2_22[5]	vdp_man_line_2_22[4]	vdp_man_line_2_22[3]	vdp_man_line_2_22[2]	vdp_man_line_2_22[1]	vdp_man_line_2_22[0]	00000000	00
102	66h	vdp_man_line_3_23	rw	vdp_man_line_3_23[7]	vdp_man_line_3_23[6]	vdp_man_line_3_23[5]	vdp_man_line_3_23[4]	vdp_man_line_3_23[3]	vdp_man_line_3_23[2]	vdp_man_line_3_23[1]	vdp_man_line_3_23[0]	00000000	00
103	67h	vdp_man_line_4_24	rw	vdp_man_line_4_24[7]	vdp_man_line_4_24[6]	vdp_man_line_4_24[5]	vdp_man_line_4_24[4]	vdp_man_line_4_24[3]	vdp_man_line_4_24[2]	vdp_man_line_4_24[1]	vdp_man_line_4_24[0]	00000000	00
104	68h	vdp_man_line_5_25	rw	vdp_man_line_5_25[7]	vdp_man_line_5_25[6]	vdp_man_line_5_25[5]	vdp_man_line_5_25[4]	vdp_man_line_5_25[3]	vdp_man_line_5_25[2]	vdp_man_line_5_25[1]	vdp_man_line_5_25[0]	00000000	00
105	69h	vdp_man_line_6_26	rw	vdp_man_line_6_26[7]	vdp_man_line_6_26[6]	vdp_man_line_6_26[5]	vdp_man_line_6_26[4]	vdp_man_line_6_26[3]	vdp_man_line_6_26[2]	vdp_man_line_6_26[1]	vdp_man_line_6_26[0]	00000000	00
106	6Ah	vdp_man_line_7_27	rw	vdp_man_line_7_27[7]	vdp_man_line_7_27[6]	vdp_man_line_7_27[5]	vdp_man_line_7_27[4]	vdp_man_line_7_27[3]	vdp_man_line_7_27[2]	vdp_man_line_7_27[1]	vdp_man_line_7_27[0]	00000000	00
107	6Bh	vdp_man_line_8_28	rw	vdp_man_line_8_28[7]	vdp_man_line_8_28[6]	vdp_man_line_8_28[5]	vdp_man_line_8_28[4]	vdp_man_line_8_28[3]	vdp_man_line_8_28[2]	vdp_man_line_8_28[1]	vdp_man_line_8_28[0]	00000000	00
108	6Ch	vdp_man_line_9_29	rw	vdp_man_line_9_29[7]	vdp_man_line_9_29[6]	vdp_man_line_9_29[5]	vdp_man_line_9_29[4]	vdp_man_line_9_29[3]	vdp_man_line_9_29[2]	vdp_man_line_9_29[1]	vdp_man_line_9_29[0]	00000000	00
109	6Dh	vdp_man_line_10_30	rw	vdp_man_line_10_30[7]	vdp_man_line_10_30[6]	vdp_man_line_10_30[5]	vdp_man_line_10_30[4]	vdp_man_line_10_30[3]	vdp_man_line_10_30[2]	vdp_man_line_10_30[1]	vdp_man_line_10_30[0]	00000000	00
110	6Eh	vdp_man_line_11_31	rw	vdp_man_line_11_31[7]	vdp_man_line_11_31[6]	vdp_man_line_11_31[5]	vdp_man_line_11_31[4]	vdp_man_line_11_31[3]	vdp_man_line_11_31[2]	vdp_man_line_11_31[1]	vdp_man_line_11_31[0]	00000000	00
111	6Fh	vdp_man_line_12_32	rw	vdp_man_line_12_32[7]	vdp_man_line_12_32[6]	vdp_man_line_12_32[5]	vdp_man_line_12_32[4]	vdp_man_line_12_32[3]	vdp_man_line_12_32[2]	vdp_man_line_12_32[1]	vdp_man_line_12_32[0]	00000000	00
112	70h	vdp_man_line_13_33	rw	vdp_man_line_13_33[7]	vdp_man_line_13_33[6]	vdp_man_line_13_33[5]	vdp_man_line_13_33[4]	vdp_man_line_13_33[3]	vdp_man_line_13_33[2]	vdp_man_line_13_33[1]	vdp_man_line_13_33[0]	00000000	00
113	71h	vdp_man_line_14_34	rw	vdp_man_line_14_34[7]	vdp_man_line_14_34[6]	vdp_man_line_14_34[5]	vdp_man_line_14_34[4]	vdp_man_line_14_34[3]	vdp_man_line_14_34[2]	vdp_man_line_14_34[1]	vdp_man_line_14_34[0]	00000000	00
114	72h	vdp_man_line_15_35	rw	vdp_man_line_15_35[7]	vdp_man_line_15_35[6]	vdp_man_line_15_35[5]	vdp_man_line_15_35[4]	vdp_man_line_15_35[3]	vdp_man_line_15_35[2]	vdp_man_line_15_35[1]	vdp_man_line_15_35[0]	00000000	00
115	73h	vdp_man_line_16_36	rw	vdp_man_line_16_36[7]	vdp_man_line_16_36[6]	vdp_man_line_16_36[5]	vdp_man_line_16_36[4]	vdp_man_line_16_36[3]	vdp_man_line_16_36[2]	vdp_man_line_16_36[1]	vdp_man_line_16_36[0]	00000000	00
116	74h	vdp_man_line_17_37	rw	vdp_man_line_17_37[7]	vdp_man_line_17_37[6]	vdp_man_line_17_37[5]	vdp_man_line_17_37[4]	vdp_man_line_17_37[3]	vdp_man_line_17_37[2]	vdp_man_line_17_37[1]	vdp_man_line_17_37[0]	00000000	00
117	75h	vdp_man_line_18_38	rw	vdp_man_line_18_38[7]	vdp_man_line_18_38[6]	vdp_man_line_18_38[5]	vdp_man_line_18_38[4]	vdp_man_line_18_38[3]	vdp_man_line_18_38[2]	vdp_man_line_18_38[1]	vdp_man_line_18_38[0]	00000000	00
118	76h	vdp_man_line_19_39	rw	vdp_man_line_19_39[7]	vdp_man_line_19_39[6]	vdp_man_line_19_39[5]	vdp_man_line_19_39[4]	vdp_man_line_19_39[3]	vdp_man_line_19_39[2]	vdp_man_line_19_39[1]	vdp_man_line_19_39[0]	00000000	00
119	77h	vdp_man_line_20_40	rw	vdp_man_line_20_40[7]	vdp_man_line_20_40[6]	vdp_man_line_20_40[5]	vdp_man_line_20_40[4]	vdp_man_line_20_40[3]	vdp_man_line_20_40[2]	vdp_man_line_20_40[1]	vdp_man_line_20_40[0]	00000000	00
120	78h	vdp_status_clear	rw	status_clear_tbd	status_clear_vitc		status_clear_gemss_vps		status_clear_wss_cgms		status_clear_ccap	00000000	00
156	9Ch	vdp_status_config	rw			gs_vps_pdc_utc_cb_change	wss_cgms_cb_change	raw_status_ena	gs_vps_pdc_utc_cgmstb[2]	gs_vps_pdc_utc_cgmstb[1]	gs_vps_pdc_utc_cgmstb[0]	00100000	20

1.5 HDMI Map

Table 6: HDMI Map Register 0x00 to 0x7E

Address		Register Name	rw	7	6	5	4	3	2	1	0	Reset Value	(Hex)
0	00h	REGISTER_00H	rw							HDCP_ONLY_MODE	HDMI_PORT_SELECT	00000000	00
1	01h	REGISTER_01H	rw	AUDIOPLL_PDN	CLOCK_TERM_PORT_A	CLOCK_TERM_PORT_B						00001000	08
2	02h	REGISTER_02H	rw			SPDIF_TRISTATE	I2S_TRISTATE	HDCP_A0		OVR_AUTO_MUX_DSD_OUT	MUX_DSD_OUT	00000000	00
3	03h	REGISTER_03H	rw		I2SOUTMODE.1	I2SOUTMODE.0	I2SBITWIDTH.4	I2SBITWIDTH.3	I2SBITWIDTH.2	I2SBITWIDTH.1	I2SBITWIDTH.0	00011000	18
4	04h	REGISTER_04H	r		AV_MUTE	HDCP_KEYS_READ	HDCP_KEY_ERROR	TMDS_PORT_A_ACTIVE	TMDS_PORT_B_ACTIVE	VIDEO_PLL_LOCKED	AUDIO_PLL_LOCKED	---	---
5	05h	REGISTER_05H	r	HDMI_MODE	HDMI_CONTENT_ENCRYPTED	DVI_HSYNC_POLARITY	DVI_VSYNC_POLARITY	HDMI_PIXEL_REPETITION.3	HDMI_PIXEL_REPETITION.2	HDMI_PIXEL_REPETITION.1	HDMI_PIXEL_REPETITION.0	---	---
6	06h	TMDSFREQ	r	TMDSFREQ.7	TMDSFREQ.6	TMDSFREQ.5	TMDSFREQ.4	TMDSFREQ.3	TMDSFREQ.2	TMDSFREQ.1	TMDSFREQ.0	---	---
7	07h	REGISTER_07H	r		VERT_FILTER_LOCKED	AUDIO_CHANNEL_MODE	DE_REGEN_FILTER_LOCKED	LINE_WIDTH.11	LINE_WIDTH.10	LINE_WIDTH.9	LINE_WIDTH.8	---	---
8	08h	LINE WIDTH	r	LINE_WIDTH.7	LINE_WIDTH.6	LINE_WIDTH.5	LINE_WIDTH.4	LINE_WIDTH.3	LINE_WIDTH.2	LINE_WIDTH.1	LINE_WIDTH.0	---	---
9	09h	FIELD 0 HEIGHT MSB	r					FIELD_0_HEIGHT.11	FIELD_0_HEIGHT.10	FIELD_0_HEIGHT.9	FIELD_0_HEIGHT.8	---	---
10	0Ah	FIELD 0 HEIGHT	r	FIELD_0_HEIGHT.7	FIELD_0_HEIGHT.6	FIELD_0_HEIGHT.5	FIELD_0_HEIGHT.4	FIELD_0_HEIGHT.3	FIELD_0_HEIGHT.2	FIELD_0_HEIGHT.1	FIELD_0_HEIGHT.0	---	---
11	0Bh	REGISTER_0BH	r		DEEP_COLOR_MODE.1	DEEP_COLOR_MODE.0	HDMI_INTERLACED	FIELD_1_HEIGHT.11	FIELD_1_HEIGHT.10	FIELD_1_HEIGHT.9	FIELD_1_HEIGHT.8	---	---
12	0Ch	FIELD 1 HEIGHT	r	FIELD_1_HEIGHT.7	FIELD_1_HEIGHT.6	FIELD_1_HEIGHT.5	FIELD_1_HEIGHT.4	FIELD_1_HEIGHT.3	FIELD_1_HEIGHT.2	FIELD_1_HEIGHT.1	FIELD_1_HEIGHT.0	---	---
13	0Dh	REGISTER_0DH	rw					FREQTOLERANCE.3	FREQTOLERANCE.2	FREQTOLERANCE.1	FREQTOLERANCE.0	00000100	04
15	0Fh	AUDIO MUTE SPEED	rw	MAN_AUDIO_DL_BYPASS	AUDIO_DELAY_LINE_BYPASS	AUDIO_MUTE_SPEED.5	AUDIO_MUTE_SPEED.4	AUDIO_MUTE_SPEED.3	AUDIO_MUTE_SPEED.2	AUDIO_MUTE_SPEED.1	AUDIO_MUTE_SPEED.0	00111111	3F
16	10h	REGISTER_10H	rw			CTS_CHANGE_THRESHOLD.5	CTS_CHANGE_THRESHOLD.4	CTS_CHANGE_THRESHOLD.3	CTS_CHANGE_THRESHOLD.2	CTS_CHANGE_THRESHOLD.1	CTS_CHANGE_THRESHOLD.0	00000111	07
19	13h	AUDIO COAST MASK	rw		AC_MSK_VCLK_CHNG	AC_MSK_VPLL_UNLOCK	AC_MSK_VFREQ_CHNG	AC_MSK_NEW_CTS	AC_MSK_NEW_N	AC_MSK_CHNG_PORT	AC_MSK_VCLK_DET	01111111	7F
20	14h	MUTE MASK 19_16	rw			MT_MSK_COMPRS_AUD	MT_MSK_CHNG_DSD_PCM			MT_MSK_PARITY_ERR	MT_MSK_VCLK_CHNG	00111111	3F
21	15h	MUTE MASK 15_8	rw	MT_MSK_APLL_UNLOCK	MT_MSK_VPLL_UNLOCK	MT_MSK_ACR_NOT_DET	MT_MSK_SAMP_RT_CHNG	MT_MSK_FLATLINE_DET	MT_MSK_VFREQ_CHNG			11111111	FF
22	16h	MUTE MASK 7_0	rw	MT_MSK_AVMUTE	MT_MSK_NOT_HDMIMODE	MT_MSK_NEW_CTS	MT_MSK_NEW_N	MT_MSK_CHMODE_CHNG	MT_MSK_APCKT_ECC_ERR	MT_MSK_CHNG_PORT	MT_MSK_VCLK_DET	11111111	FF
23	17h	PACKETS DETECTED MSB	r		DST_AUDIO_PCKT_DET	HBR_AUDIO_PCKT_DET	GAMUT_MDATA_PCKT_DET	INFOFRAME_PCKT_DET	GC_PACKET_DET	ACR_PACKET_DET	AUDIO_SAMPLE_PCKT_DET	---	---
24	18h	PACKETS DETECTED	r	DSD_PACKET_DET	ISRC2_PACKET_DET	ISRC1_PACKET_DET	ACP_PACKET_DET	MS_INFOFRAME_DET	SPD_INFOFRAME_DET	AUDIO_INFOFRAME_DET	AVI_INFOFRAME_DET	---	---
25	19h	PACKET STATUS FLAGS 20_16	r				AUDIO_PARITY_ERR	SAMP_RT_CHNG	FLATLINE_BIT_SET	NEW_TMDS_FREQ		---	---
26	1Ah	PACKET STATUS FLAGS 15_8	r				NEW_CTS	NEW_N	ERR_IN_INFOFRAME_PCKT	ERR_IN_UNKNOWN_PCKT	ERR_IN_AUDIO_PCKT	---	---
27	1Bh	PACKET STATUS FLAGS 7_0	r	NEW_GAMUT_MDATA_PCKT	NEW_ISRC2_PCKT	NEW_ISRC1_PCKT	NEW_ACP_PCKT	NEW_MS_INFOFRAME	NEW_SPD_INFOFRAME	NEW_AUDIO_INFOFRAME	NEW_AVI_INFOFRAME	---	---
28	1Ch	REGISTER_1CH	rw		MCLKPLLEN		MCLKPLL_N.2	MCLKPLL_N.1	MCLKPLL_N.0	MCLKFS_N.2	MCLKFS_N.1	MCLKFS_N.0	01011000	58
29	1Dh	REGISTER_1DH	rw				UP_CONVERSION_MODE		MUTE_AUDIO	WAIT_UNMUTE.1	WAIT_UNMUTE.0	NOT_AUTO_UNMUTE	00000000	00
30	1Eh	TOTAL_LINE_WIDTH_MSB	r						TOTAL_LINE_WIDTH.11	TOTAL_LINE_WIDTH.10	TOTAL_LINE_WIDTH.9	TOTAL_LINE_WIDTH.8	---	---
31	1Fh	TOTAL_LINE_WIDTH	r	TOTAL_LINE_WIDTH.7	TOTAL_LINE_WIDTH.6	TOTAL_LINE_WIDTH.5	TOTAL_LINE_WIDTH.4	TOTAL_LINE_WIDTH.3	TOTAL_LINE_WIDTH.2	TOTAL_LINE_WIDTH.1	TOTAL_LINE_WIDTH.0	---	---
32	20h	HSYNC_FRONT_PORCH_MSB	r							HSYNC_FRONT_PORCH.9	HSYNC_FRONT_PORCH.8	---	---
33	21h	HSYNC_FRONT_PORCH	r	HSYNC_FRONT_PORCH.7	HSYNC_FRONT_PORCH.6	HSYNC_FRONT_PORCH.5	HSYNC_FRONT_PORCH.4	HSYNC_FRONT_PORCH.3	HSYNC_FRONT_PORCH.2	HSYNC_FRONT_PORCH.1	HSYNC_FRONT_PORCH.0	---	---
34	22h	HSYNC_PULSE_WIDTH_MSB	r							HSYNC_PULSE_WIDTH.9	HSYNC_PULSE_WIDTH.8	---	---
35	23h	HSYNC_PULSE_WIDTH	r	HSYNC_PULSE_WIDTH.7	HSYNC_PULSE_WIDTH.6	HSYNC_PULSE_WIDTH.5	HSYNC_PULSE_WIDTH.4	HSYNC_PULSE_WIDTH.3	HSYNC_PULSE_WIDTH.2	HSYNC_PULSE_WIDTH.1	HSYNC_PULSE_WIDTH.0	---	---
36	24h	HSYNC_BACK_PORCH_MSB	r							HSYNC_BACK_PORCH.9	HSYNC_BACK_PORCH.8	---	---
37	25h	HSYNC_BACK_PORCH	r	HSYNC_BACK_PORCH.7	HSYNC_BACK_PORCH.6	HSYNC_BACK_PORCH.5	HSYNC_BACK_PORCH.4	HSYNC_BACK_PORCH.3	HSYNC_BACK_PORCH.2	HSYNC_BACK_PORCH.1	HSYNC_BACK_PORCH.0	---	---
38	26h	FIELD0_TOTAL_HEIGHT_MSB	r				FIELD0_TOTAL_HEIGHT.12	FIELD0_TOTAL_HEIGHT.11	FIELD0_TOTAL_HEIGHT.10	FIELD0_TOTAL_HEIGHT.9	FIELD0_TOTAL_HEIGHT.8	---	---
39	27h	FIELD0_TOTAL_HEIGHT	r	FIELD0_TOTAL_HEIGHT.7	FIELD0_TOTAL_HEIGHT.6	FIELD0_TOTAL_HEIGHT.5	FIELD0_TOTAL_HEIGHT.4	FIELD0_TOTAL_HEIGHT.3	FIELD0_TOTAL_HEIGHT.2	FIELD0_TOTAL_HEIGHT.1	FIELD0_TOTAL_HEIGHT.0	---	---
40	28h	FIELD1_TOTAL_HEIGHT_MSB	r				FIELD1_TOTAL_HEIGHT.12	FIELD1_TOTAL_HEIGHT.11	FIELD1_TOTAL_HEIGHT.10	FIELD1_TOTAL_HEIGHT.9	FIELD1_TOTAL_HEIGHT.8	---	---
41	29h	FIELD1_TOTAL_HEIGHT	r	FIELD1_TOTAL_HEIGHT.7	FIELD1_TOTAL_HEIGHT.6	FIELD1_TOTAL_HEIGHT.5	FIELD1_TOTAL_HEIGHT.4	FIELD1_TOTAL_HEIGHT.3	FIELD1_TOTAL_HEIGHT.2	FIELD1_TOTAL_HEIGHT.1	FIELD1_TOTAL_HEIGHT.0	---	---
42	2Ah	FIELD0_VS_FRONT_PORCH_MSB	r				FIELD0_VS_FRONT_PORCH.12	FIELD0_VS_FRONT_PORCH.11	FIELD0_VS_FRONT_PORCH.10	FIELD0_VS_FRONT_PORCH.9	FIELD0_VS_FRONT_PORCH.8	---	---
43	2Bh	FIELD0_VS_FRONT_PORCH	r	FIELD0_VS_FRONT_PORCH.7	FIELD0_VS_FRONT_PORCH.6	FIELD0_VS_FRONT_PORCH.5	FIELD0_VS_FRONT_PORCH.4	FIELD0_VS_FRONT_PORCH.3	FIELD0_VS_FRONT_PORCH.2	FIELD0_VS_FRONT_PORCH.1	FIELD0_VS_FRONT_PORCH.0	---	---
44	2Ch	FIELD1_VS_FRONT_PORCH_MSB	r				FIELD1_VS_FRONT_PORCH.12	FIELD1_VS_FRONT_PORCH.11	FIELD1_VS_FRONT_PORCH.10	FIELD1_VS_FRONT_PORCH.9	FIELD1_VS_FRONT_PORCH.8	---	---
45	2Dh	FIELD1_VS_FRONT_PORCH	r	FIELD1_VS_FRONT_PORCH.7	FIELD1_VS_FRONT_PORCH.6	FIELD1_VS_FRONT_PORCH.5	FIELD1_VS_FRONT_PORCH.4	FIELD1_VS_FRONT_PORCH.3	FIELD1_VS_FRONT_PORCH.2	FIELD1_VS_FRONT_PORCH.1	FIELD1_VS_FRONT_PORCH.0	---	---
46	2Eh	FIELD0_VS_PULSE_WIDTH_MSB	r				FIELD0_VS_PULSE_WIDTH.12	FIELD0_VS_PULSE_WIDTH.11	FIELD0_VS_PULSE_WIDTH.10	FIELD0_VS_PULSE_WIDTH.9	FIELD0_VS_PULSE_WIDTH.8	---	---
47	2Fh	FIELD0_VS_PULSE_WIDTH	r	FIELD0_VS_PULSE_WIDTH.7	FIELD0_VS_PULSE_WIDTH.6	FIELD0_VS_PULSE_WIDTH.5	FIELD0_VS_PULSE_WIDTH.4	FIELD0_VS_PULSE_WIDTH.3	FIELD0_VS_PULSE_WIDTH.2	FIELD0_VS_PULSE_WIDTH.1	FIELD0_VS_PULSE_WIDTH.0	---	---
48	30h	FIELD1_VS_PULSE_WIDTH_MSB	r				FIELD1_VS_PULSE_WIDTH.12	FIELD1_VS_PULSE_WIDTH.11	FIELD1_VS_PULSE_WIDTH.10	FIELD1_VS_PULSE_WIDTH.9	FIELD1_VS_PULSE_WIDTH.8	---	---
49	31h	FIELD1_VS_PULSE_WIDTH	r	FIELD1_VS_PULSE_WIDTH.7	FIELD1_VS_PULSE_WIDTH.6	FIELD1_VS_PULSE_WIDTH.5	FIELD1_VS_PULSE_WIDTH.4	FIELD1_VS_PULSE_WIDTH.3	FIELD1_VS_PULSE_WIDTH.2	FIELD1_VS_PULSE_WIDTH.1	FIELD1_VS_PULSE_WIDTH.0	---	---
50	32h	FIELD0_VS_BACK_PORCH_MSB	r				FIELD0_VS_BACK_PORCH.12	FIELD0_VS_BACK_PORCH.11	FIELD0_VS_BACK_PORCH.10	FIELD0_VS_BACK_PORCH.9	FIELD0_VS_BACK_PORCH.8	---	---
51	33h	FIELD0_VS_BACK_PORCH	r	FIELD0_VS_BACK_PORCH.7	FIELD0_VS_BACK_PORCH.6	FIELD0_VS_BACK_PORCH.5	FIELD0_VS_BACK_PORCH.4	FIELD0_VS_BACK_PORCH.3	FIELD0_VS_BACK_PORCH.2	FIELD0_VS_BACK_PORCH.1	FIELD0_VS_BACK_PORCH.0	---	---
52	34h	FIELD1_VS_BACK_PORCH_MSB	r				FIELD1_VS_BACK_PORCH.12	FIELD1_VS_BACK_PORCH.11	FIELD1_VS_BACK_PORCH.10	FIELD1_VS_BACK_PORCH.9	FIELD1_VS_BACK_PORCH.8	---	---
53	35h	FIELD1_VS_BACK_PORCH	r	FIELD1_VS_BACK_PORCH.7	FIELD1_VS_BACK_PORCH.6	FIELD1_VS_BACK_PORCH.5	FIELD1_VS_BACK_PORCH.4	FIELD1_VS_BACK_PORCH.3	FIELD1_VS_BACK_PORCH.2	FIELD1_VS_BACK_PORCH.1	FIELD1_VS_BACK_PORCH.0	---	---
54	36h	CHANNEL STATUS DATA 0	r	CHANNEL_STATUS_DATA_0.7	CHANNEL_STATUS_DATA_0.6	CHANNEL_STATUS_DATA_0.5	CHANNEL_STATUS_DATA_0.4	CHANNEL_STATUS_DATA_0.3	CHANNEL_STATUS_DATA_0.2	CHANNEL_STATUS_DATA_0.1	CHANNEL_STATUS_DATA_0.0	---	---
55	37h	CHANNEL STATUS DATA 1	r	CHANNEL_STATUS_DATA_1.7	CHANNEL_STATUS_DATA_1.6	CHANNEL_STATUS_DATA_1.5	CHANNEL_STATUS_DATA_1.4	CHANNEL_STATUS_DATA_1.3	CHANNEL_STATUS_DATA_1.2	CHANNEL_STATUS_DATA_1.1	CHANNEL_STATUS_DATA_1.0	---	---
56	38h	CHANNEL STATUS DATA 2	r	CHANNEL_STATUS_DATA_2.7	CHANNEL_STATUS_DATA_2.6	CHANNEL_STATUS_DATA_2.5	CHANNEL_STATUS_DATA_2.4	CHANNEL_STATUS_DATA_2.3	CHANNEL_STATUS_DATA_2.2	CHANNEL_STATUS_DATA_2.1	CHANNEL_STATUS_DATA_2.0	---	---
57	39h	CHANNEL STATUS DATA 3	r	CHANNEL_STATUS_DATA_3.7	CHANNEL_STATUS_DATA_3.6	CHANNEL_STATUS_DATA_3.5	CHANNEL_STATUS_DATA_3.4	CHANNEL_STATUS_DATA_3.3	CHANNEL_STATUS_DATA_3.2	CHANNEL_STATUS_DATA_3.1	CHANNEL_STATUS_DATA_3.0	---	---
58	3Ah	CHANNEL STATUS DATA 4	r					CHANNEL_STATUS_DATA_4.3	CHANNEL_STATUS_DATA_4.2	CHANNEL_STATUS_DATA_4.1	CHANNEL_STATUS_DATA_4.0	---	---
60	3Ch	PLL DIVIDER	rw	PLL_DIVIDER.3	PLL_DIVIDER.2	PLL_DIVIDER.1	PLL_DIVIDER.0					01000010	42
65	41h	REGISTER_41H	rw				DEREP_N_OVERRIDE	DEREP_N.3	DEREP_N.2	DEREP_N.1	DEREP_N.0	01000000	40
80	50h	REGISTER_50	rw							CS_COPYRIGHT_FORCE		00000000	00
90	5Ah	REGISTER_5A	w							PACKET_DET_RESET	AUDIO_PLL_RESET	00000000	00
91	5Bh	CTS_REG1	r	CTS.19	CTS.18	CTS.17	CTS.16	CTS.15	CTS.14	CTS.13	CTS.12	---	---
92	5Ch	CTS_REG2	r	CTS.11	CTS.10	CTS.9	CTS.8	CTS.7	CTS.6	CTS.5	CTS.4	---	---
93	5Dh	CTS_REG3_N_REG1	r	CTS.3	CTS.2	CTS.1	CTS.0	N.19	N.18	N.17	N.16	---	---
94	5Eh	N_REG2	r	N.15	N.14	N.13	N.12	N.11	N.10	N.9	N.8	---	---
95	5Fh	N_REG3	r	N.7	N.6	N.5	N.4	N.3	N.2	N.1	N.0	---	---
96	60h	GAMUT_MDATA_BODY_0	r	GBD_0.7	GBD_0.6	GBD_0.5	GBD_0.4	GBD_0.3	GBD_0.2	GBD_0.1	GBD_0.0	---	---
97	61h	GAMUT_MDATA_BODY_1	r	GBD_1.7	GBD_1.6	GBD_1.5	GBD_1.4	GBD_1.3	GBD_1.2	GBD_1.1	GBD_1.0	---	---
98	62h	GAMUT_MDATA_BODY_2	r	GBD_2.7	GBD_2.6	GBD_2.5	GBD_2.4	GBD_2.3	GBD_2.2	GBD_2.1	GBD_2.0	---	---
99	63h	GAMUT_MDATA_BODY_3	r	GBD_3.7	GBD_3.6	GBD_3.5	GBD_3.4	GBD_3.3	GBD_3.2	GBD_3.1	GBD_3.0	---	---
100	64h	GAMUT_MDATA_BODY_4	r	GBD_4.7	GBD_4.6	GBD_4.5	GBD_4.4	GBD_4.3	GBD_4.2	GBD_4.1	GBD_4.0	---	---
101	65h	GAMUT_MDATA_BODY_5	r	GBD_5.7	GBD_5.6	GBD_5.5	GBD_5.4	GBD_5.3	GBD_5.2	GBD_5.1	GBD_5.0	---	---
102	66h	GAMUT_MDATA_BODY_6	r	GBD_6.7	GBD_6.6	GBD_6.5	GBD_6.4	GBD_6.3	GBD_6.2	GBD_6.1	GBD_6.0	---	---
104	68h	GAMUT_MDATA_BODY_7	r	GBD_7.7	GBD_7.6	GBD_7.5	GBD_7.4	GBD_7.3	GBD_7.2	GBD_7.1	GBD_7.0	---	---
105	69h	GAMUT_MDATA_BODY_8	r	GBD_8.7	GBD_8.6	GBD_8.5	GBD_8.4	GBD_8.3	GBD_8.2	GBD_8.1	GBD_8.0	---	---
106	6Ah	GAMUT_MDATA_BODY_9	r	GBD_9.7	GBD_9.6	GBD_9.5	GBD_9.4	GBD_9.3	GBD_9.2	GBD_9.1	GBD_9.0	---	---
107	6Bh	GAMUT_MDATA_BODY_10	r	GBD_10.7	GBD_10.6	GBD_10.5	GBD_10.4	GBD_10.3	GBD_10.2	GBD_10.1	GBD_10.0	---	---
108	6Ch	GAMUT_MDATA_BODY_11	r	GBD_11.7	GBD_11.6	GBD_11.5	GBD_11.4	GBD_11.3	GBD_11.2	GBD_11.1	GBD_11.0	---	---
109	6Dh	GAMUT_MDATA_BODY_12	r	GBD_12.7	GBD_12.6	GBD_12.5	GBD_12.4	GBD_12.3	GBD_12.2	GBD_12.1	GBD_12.0	---	---
110	6Eh	GAMUT_MDATA_BODY_13	r	GBD_13.7	GBD_13.6	GBD_13.5	GBD_13.4	GBD_13.3	GBD_13.2	GBD_13.1	GBD_13.0	---	---
112	70h	GAMUT_MDATA_BODY_14	r	GBD_14.7	GBD_14.6	GBD_14.5	GBD_14.4	GBD_14.3	GBD_14.2	GBD_14.1	GBD_14.0	---	---
113	71h	GAMUT_MDATA_BODY_15	r	GBD_15.7	GBD_15.6	GBD_15.5	GBD_15.4	GBD_15.3	GBD_15.2	GBD_15.1	GBD_15.0	---	---
114	72h	GAMUT_MDATA_BODY_16	r	GBD_16.7	GBD_16.6	GBD_16.5	GBD_16.4	GBD_16.3	GBD_16.2	GBD_16.1	GBD_16.0	---	---
115	73h	GAMUT_MDATA_BODY_17	r	GBD_17.7	GBD_17.6	GBD_17.5	GBD_17.4	GBD_17.3	GBD_17.2	GBD_17.1	GBD_17.0	---	---
116	74h	GAMUT_MDATA_BODY_18	r	GBD_18.7	GBD_18.6	GBD_18.5	GBD_18.4	GBD_18.3	GBD_18.2	GBD_18.1	GBD_18.0	---	---
117	75h	GAMUT_MDATA_BODY_19	r	GBD_19.7	GBD_19.6	GBD_19.5	GBD_19.4	GBD_19.3	GBD_19.2	GBD_19.1	GBD_19.0	---	---
118	76h	GAMUT_MDATA_BODY_20	r	GBD_20.7	GBD_20.6	GBD_20.5	GBD_20.4	GBD_20.3	GBD_20.2	GBD_20.1	GBD_20.0	---	---
120	78h	GAMUT_MDATA_BODY_21	r	GBD_21.7	GBD_21.6	GBD_21.5	GBD_21.4	GBD_21.3	GBD_21.2	GBD_21.1	GBD_21.0	---	---
121	79h	GAMUT_MDATA_BODY_22	r	GBD_22.7	GBD_22.6	GBD_22.5	GBD_22.4	GBD_22.3	GBD_22.2	GBD_22.1	GBD_22.0	---	---
122	7Ah	GAMUT_MDATA_BODY_23	r	GBD_23.7	GBD_23.6	GBD_23.5	GBD_23.4	GBD_23.3	GBD_23.2	GBD_23.1	GBD_23.0	---	---
123	7Bh	GAMUT_MDATA_BODY_24	r	GBD_24.7	GBD_24.6	GBD_24.5	GBD_24.4	GBD_24.3	GBD_24.2	GBD_24.1	GBD_24.0	---	---
124	7Ch	GAMUT_MDATA_BODY_25	r	GBD_25.7	GBD_25.6	GBD_25.5	GBD_25.4	GBD_25.3	GBD_25.2	GBD_25.1	GBD_25.0	---	---
125	7Dh	GAMUT_MDATA_BODY_26	r	GBD_26.7	GBD_26.6	GBD_26.5	GBD_26.4	GBD_26.3	GBD_26.2	GBD_26.1	GBD_26.0	---	---
126	7Eh	GAMUT_MDATA_BODY_27	r	GBD_27.7	GBD_27.6	GBD_27.5	GBD_27.4	GBD_27.3	GBD_27.2	GBD_27.1	GBD_27.0	---	---

Table 7: HDMI Map Register 0x80 to 0xFE

Address		Register Name	rw	7	6	5	4	3	2	1	0	Reset Value	(Hex)
128	80h	AVI_INF_VERS	r	AVI_INF_VERS.7	AVI_INF_VERS.6	AVI_INF_VERS.5	AVI_INF_VERS.4	AVI_INF_VERS.3	AVI_INF_VERS.2	AVI_INF_VERS.1	AVI_INF_VERS.0	---	---
129	81h	AVI_DATA BYTE_1	r	Y.1	Y.0	A	B.1	B.0	S:1	S:0	---	---	
130	82h	AVI_INF BYTE_2	r	C:1	C:0	M.1	M.0	R.3	R.2	R.1	R.0	---	---
131	83h	AVI_INF BYTE_3	r	ITC	EC:2	EC:1	EC:0	Q:1	Q:0	SC:1	SC:0	---	---
132	84h	AVI_INF BYTE_4	r		VIC.6	VIC.5	VIC.4	VIC.3	VIC.2	VIC.1	VIC.0	---	---
133	85h	AVI_INF BYTE_5	r					PR.3	PR.2	PR.1	PR.0	---	---
134	86h	AVI_INF_BYTE_6	r	LINE_END_LSB.7	LINE_END_LSB.6	LINE_END_LSB.5	LINE_END_LSB.4	LINE_END_LSB.3	LINE_END_LSB.2	LINE_END_LSB.1	LINE_END_LSB.0	---	---
136	88h	AVI_INF_BYTE_7	r	LINE_END_MSB.7	LINE_END_MSB.6	LINE_END_MSB.5	LINE_END_MSB.4	LINE_END_MSB.3	LINE_END_MSB.2	LINE_END_MSB.1	LINE_END_MSB.0	---	---
137	89h	AVI_INF_BYTE_8	r	LINE_START_LSB.7	LINE_START_LSB.6	LINE_START_LSB.5	LINE_START_LSB.4	LINE_START_LSB.3	LINE_START_LSB.2	LINE_START_LSB.1	LINE_START_LSB.0	---	---
138	8Ah	AVI_INF_BYTE_9	r	LINE_START_MSB.7	LINE_START_MSB.6	LINE_START_MSB.5	LINE_START_MSB.4	LINE_START_MSB.3	LINE_START_MSB.2	LINE_START_MSB.1	LINE_START_MSB.0	---	---
139	8Bh	AVI_INF_BYTE_10	r	PIXEL_END_LSB.7	PIXEL_END_LSB.6	PIXEL_END_LSB.5	PIXEL_END_LSB.4	PIXEL_END_LSB.3	PIXEL_END_LSB.2	PIXEL_END_LSB.1	PIXEL_END_LSB.0	---	---
140	8Ch	AVI_INF_BYTE_11	r	PIXEL_END_MSB.7	PIXEL_END_MSB.6	PIXEL_END_MSB.5	PIXEL_END_MSB.4	PIXEL_END_MSB.3	PIXEL_END_MSB.2	PIXEL_END_MSB.1	PIXEL_END_MSB.0	---	---
141	8Dh	AVI_INF_BYTE_12	r	PIXEL_START_LSB.7	PIXEL_START_LSB.6	PIXEL_START_LSB.5	PIXEL_START_LSB.4	PIXEL_START_LSB.3	PIXEL_START_LSB.2	PIXEL_START_LSB.1	PIXEL_START_LSB.0	---	---
142	8Eh	AVI_INF_BYTE_13	r	PIXEL_START_MSB.7	PIXEL_START_MSB.6	PIXEL_START_MSB.5	PIXEL_START_MSB.4	PIXEL_START_MSB.3	PIXEL_START_MSB.2	PIXEL_START_MSB.1	PIXEL_START_MSB.0	---	---
144	90h	AUDIO_INF_VERS	r	AUDIO_INF_VERS.7	AUDIO_INF_VERS.6	AUDIO_INF_VERS.5	AUDIO_INF_VERS.4	AUDIO_INF_VERS.3	AUDIO_INF_VERS.2	AUDIO_INF_VERS.1	AUDIO_INF_VERS.0	---	---
145	91h	AUDIO_INF_BYTE_1	r	CT.3	CT.2	CT.1	CT.0		CC.2	CC.1	CC.0	---	---
146	92h	AUDIO_INF_BYTE_2	r				SF.2	SF.1	SF.0	SS.1	SS.0	---	---
147	93h	AUDIO_INF_BYTE_3	r	AUDIO_INF_BYTE_3.7	AUDIO_INF_BYTE_3.6	AUDIO_INF_BYTE_3.5	AUDIO_INF_BYTE_3.4	AUDIO_INF_BYTE_3.3	AUDIO_INF_BYTE_3.2	AUDIO_INF_BYTE_3.1	AUDIO_INF_BYTE_3.0	---	---
148	94h	AUDIO_INF_BYTE_4	r	CA.7	CA.6	CA.5	CA.4	CA.3	CA.2	CA.1	CA.0	---	---
149	95h	AUDIO_INF_BYTE_5	r	DM_INH	LSV:3	LSV:2	LSV:1	LSV:0	not used	not used	not used	---	---
152	98h	SOURCE_PROD_INF_VERS	r	SOURCE_PROD_INF_VERS.7	SOURCE_PROD_INF_VERS.6	SOURCE_PROD_INF_VERS.5	SOURCE_PROD_INF_VERS.4	SOURCE_PROD_INF_VERS.3	SOURCE_PROD_INF_VERS.2	SOURCE_PROD_INF_VERS.1	SOURCE_PROD_INF_VERS.0	---	---
153	99h	SOURCE_PROD_INF_BYTE_1	r	VN1.7	VN1.6	VN1.5	VN1.4	VN1.3	VN1.2	VN1.1	VN1.0	---	---
154	9Ah	SOURCE_PROD_INF_BYTE_2	r	VN2.7	VN2.6	VN2.5	VN2.4	VN2.3	VN2.2	VN2.1	VN2.0	---	---
155	9Bh	SOURCE_PROD_INF_BYTE_3	r	VN3.7	VN3.6	VN3.5	VN3.4	VN3.3	VN3.2	VN3.1	VN3.0	---	---
156	9Ch	SOURCE_PROD_INF_BYTE_4	r	VN4.7	VN4.6	VN4.5	VN4.4	VN4.3	VN4.2	VN4.1	VN4.0	---	---
157	9Dh	SOURCE_PROD_INF_BYTE_5	r	VN5.7	VN5.6	VN5.5	VN5.4	VN5.3	VN5.2	VN5.1	VN5.0	---	---
158	9Eh	SOURCE_PROD_INF_BYTE_6	r	VN6.7	VN6.6	VN6.5	VN6.4	VN6.3	VN6.2	VN6.1	VN6.0	---	---
160	A0h	SOURCE_PROD_INF_BYTE_7	r	VN7.7	VN7.6	VN7.5	VN7.4	VN7.3	VN7.2	VN7.1	VN7.0	---	---
161	A1h	SOURCE_PROD_INF_BYTE_8	r	VN8.7	VN8.6	VN8.5	VN8.4	VN8.3	VN8.2	VN8.1	VN8.0	---	---
162	A2h	SOURCE_PROD_INF_BYTE_9	r	PD1.7	PD1.6	PD1.5	PD1.4	PD1.3	PD1.2	PD1.1	PD1.0	---	---
163	A3h	SOURCE_PROD_INF_BYTE_10	r	PD2.7	PD2.6	PD2.5	PD2.4	PD2.3	PD2.2	PD2.1	PD2.0	---	---
164	A4h	SOURCE_PROD_INF_BYTE_11	r	PD3.7	PD3.6	PD3.5	PD3.4	PD3.3	PD3.2	PD3.1	PD3.0	---	---
165	A5h	SOURCE_PROD_INF_BYTE_12	r	PD4.7	PD4.6	PD4.5	PD4.4	PD4.3	PD4.2	PD4.1	PD4.0	---	---
166	A6h	SOURCE_PROD_INF_BYTE_13	r	PD5.7	PD5.6	PD5.5	PD5.4	PD5.3	PD5.2	PD5.1	PD5.0	---	---
168	A8h	SOURCE_PROD_INF_BYTE_14	r	PD6.7	PD6.6	PD6.5	PD6.4	PD6.3	PD6.2	PD6.1	PD6.0	---	---
169	A9h	SOURCE_PROD_INF_BYTE_15	r	PD7.7	PD7.6	PD7.5	PD7.4	PD7.3	PD7.2	PD7.1	PD7.0	---	---
170	AAh	SOURCE_PROD_INF_BYTE_16	r	PD8.7	PD8.6	PD8.5	PD8.4	PD8.3	PD8.2	PD8.1	PD8.0	---	---
171	ABh	SOURCE_PROD_INF_BYTE_17	r	PD9.7	PD9.6	PD9.5	PD9.4	PD9.3	PD9.2	PD9.1	PD9.0	---	---
172	ACh	SOURCE_PROD_INF_BYTE_18	r	PD10.7	PD10.6	PD10.5	PD10.4	PD10.3	PD10.2	PD10.1	PD10.0	---	---
173	ADh	SOURCE_PROD_INF_BYTE_19	r	PD11.7	PD11.6	PD11.5	PD11.4	PD11.3	PD11.2	PD11.1	PD11.0	---	---
174	AEh	SOURCE_PROD_INF_BYTE_20	r	PD12.7	PD12.6	PD12.5	PD12.4	PD12.3	PD12.2	PD12.1	PD12.0	---	---
176	B0h	SOURCE_PROD_INF_BYTE_21	r	PD13.7	PD13.6	PD13.5	PD13.4	PD13.3	PD13.2	PD13.1	PD13.0	---	---
177	B1h	SOURCE_PROD_INF_BYTE_22	r	PD14.7	PD14.6	PD14.5	PD14.4	PD14.3	PD14.2	PD14.1	PD14.0	---	---
178	B2h	SOURCE_PROD_INF_BYTE_23	r	PD15.7	PD15.6	PD15.5	PD15.4	PD15.3	PD15.2	PD15.1	PD15.0	---	---
179	B3h	SOURCE_PROD_INF_BYTE_24	r	PD16.7	PD16.6	PD16.5	PD16.4	PD16.3	PD16.2	PD16.1	PD16.0	---	---
180	B4h	SOURCE_PROD_INF_BYTE_25	r	SOURCE_DEV_INF.7	SOURCE_DEV_INF.6	SOURCE_DEV_INF.5	SOURCE_DEV_INF.4	SOURCE_DEV_INF.3	SOURCE_DEV_INF.2	SOURCE_DEV_INF.1	SOURCE_DEV_INF.0	---	---
184	B8h	MPEG_SOURCE_INF_VERS	r	MPEG_SOURCE_INF_VERS.7	MPEG_SOURCE_INF_VERS.6	MPEG_SOURCE_INF_VERS.5	MPEG_SOURCE_INF_VERS.4	MPEG_SOURCE_INF_VERS.3	MPEG_SOURCE_INF_VERS.2	MPEG_SOURCE_INF_VERS.1	MPEG_SOURCE_INF_VERS.0	---	---
185	B9h	MPEG_SOURCE_INF_BYTE_1	r	MB0.7	MB0.6	MB0.5	MB0.4	MB0.3	MB0.2	MB0.1	MB0.0	---	---
186	BAh	MPEG_SOURCE_INF_BYTE_2	r	MB1.7	MB1.6	MB1.5	MB1.4	MB1.3	MB1.2	MB1.1	MB1.0	---	---
187	BBh	MPEG_SOURCE_INF_BYTE_3	r	MB2.7	MB2.6	MB2.5	MB2.4	MB2.3	MB2.2	MB2.1	MB2.0	---	---
188	BCh	MPEG_SOURCE_INF_BYTE_4	r	MB3.7	MB3.6	MB3.5	MB3.4	MB3.3	MB3.2	MB3.1	MB3.0	---	---
189	BDh	MPEG_SOURCE_INF_BYTE_5	r				FR			MF:1	MF:0	---	---
192	C0h	ACP_TYPE	r	ACP_TYPE.7	ACP_TYPE.6	ACP_TYPE.5	ACP_TYPE.4	ACP_TYPE.3	ACP_TYPE.2	ACP_TYPE.1	ACP_TYPE.0	---	---
193	C1h	ACP_PACKET_BYTE_0	r	ACP_PB0.7	ACP_PB0.6	ACP_PB0.5	ACP_PB0.4	ACP_PB0.3	ACP_PB0.2	ACP_PB0.1	ACP_PB0.0	---	---
194	C2h	ACP_PACKET_BYTE_1	r	ACP_PB1.7	ACP_PB1.6	ACP_PB1.5	ACP_PB1.4	ACP_PB1.3	ACP_PB1.2	ACP_PB1.1	ACP_PB1.0	---	---
195	C3h	ACP_PACKET_BYTE_2	r	ACP_PB2.7	ACP_PB2.6	ACP_PB2.5	ACP_PB2.4	ACP_PB2.3	ACP_PB2.2	ACP_PB2.1	ACP_PB2.0	---	---
196	C4h	ACP_PACKET_BYTE_3	r	ACP_PB3.7	ACP_PB3.6	ACP_PB3.5	ACP_PB3.4	ACP_PB3.3	ACP_PB3.2	ACP_PB3.1	ACP_PB3.0	---	---
197	C5h	ACP_PACKET_BYTE_4	r	ACP_PB4.7	ACP_PB4.6	ACP_PB4.5	ACP_PB4.4	ACP_PB4.3	ACP_PB4.2	ACP_PB4.1	ACP_PB4.0	---	---
198	C6h	ACP_PACKET_BYTE_5	r	ACP_PB5.7	ACP_PB5.6	ACP_PB5.5	ACP_PB5.4	ACP_PB5.3	ACP_PB5.2	ACP_PB5.1	ACP_PB5.0	---	---
200	C8h	ACP_PACKET_BYTE_6	r	ACP_PB6.7	ACP_PB6.6	ACP_PB6.5	ACP_PB6.4	ACP_PB6.3	ACP_PB6.2	ACP_PB6.1	ACP_PB6.0	---	---
201	C9h	ACP_PACKET_BYTE_7	r	ACP_PB7.7	ACP_PB7.6	ACP_PB7.5	ACP_PB7.4	ACP_PB7.3	ACP_PB7.2	ACP_PB7.1	ACP_PB7.0	---	---
202	CAh	ACP_PACKET_BYTE_8	r	ACP_PB8.7	ACP_PB8.6	ACP_PB8.5	ACP_PB8.4	ACP_PB8.3	ACP_PB8.2	ACP_PB8.1	ACP_PB8.0	---	---
203	CBh	ACP_PACKET_BYTE_9	r	ACP_PB9.7	ACP_PB9.6	ACP_PB9.5	ACP_PB9.4	ACP_PB9.3	ACP_PB9.2	ACP_PB9.1	ACP_PB9.0	---	---
204	CCh	ACP_PACKET_BYTE_10	r	ACP_PB10.7	ACP_PB10.6	ACP_PB10.5	ACP_PB10.4	ACP_PB10.3	ACP_PB10.2	ACP_PB10.1	ACP_PB10.0	---	---
205	CDh	ACP_PACKET_BYTE_11	r	ACP_PB11.7	ACP_PB11.6	ACP_PB11.5	ACP_PB11.4	ACP_PB11.3	ACP_PB11.2	ACP_PB11.1	ACP_PB11.0	---	---
206	CEh	ACP_PACKET_BYTE_12	r	ACP_PB12.7	ACP_PB12.6	ACP_PB12.5	ACP_PB12.4	ACP_PB12.3	ACP_PB12.2	ACP_PB12.1	ACP_PB12.0	---	---
208	D0h	ACP_PACKET_BYTE_13	r	ACP_PB13.7	ACP_PB13.6	ACP_PB13.5	ACP_PB13.4	ACP_PB13.3	ACP_PB13.2	ACP_PB13.1	ACP_PB13.0	---	---
209	D1h	ACP_PACKET_BYTE_14	r	ACP_PB14.7	ACP_PB14.6	ACP_PB14.5	ACP_PB14.4	ACP_PB14.3	ACP_PB14.2	ACP_PB14.1	ACP_PB14.0	---	---
210	D2h	ACP_PACKET_BYTE_15	r	ACP_PB15.7	ACP_PB15.6	ACP_PB15.5	ACP_PB15.4	ACP_PB15.3	ACP_PB15.2	ACP_PB15.1	ACP_PB15.0	---	---
211	D3h	ACP_PACKET_BYTE_16	r	ACP_PB16.7	ACP_PB16.6	ACP_PB16.5	ACP_PB16.4	ACP_PB16.3	ACP_PB16.2	ACP_PB16.1	ACP_PB16.0	---	---
212	D4h	ACP_PACKET_BYTE_17	r	ACP_PB17.7	ACP_PB17.6	ACP_PB17.5	ACP_PB17.4	ACP_PB17.3	ACP_PB17.2	ACP_PB17.1	ACP_PB17.0	---	---
213	D5h	ACP_PACKET_BYTE_18	r	ACP_PB18.7	ACP_PB18.6	ACP_PB18.5	ACP_PB18.4	ACP_PB18.3	ACP_PB18.2	ACP_PB18.1	ACP_PB18.0	---	---
214	D6h	ACP_PACKET_BYTE_19	r	ACP_PB19.7	ACP_PB19.6	ACP_PB19.5	ACP_PB19.4	ACP_PB19.3	ACP_PB19.2	ACP_PB19.1	ACP_PB19.0	---	---
216	D8h	ISRC1_INF	r	ISRC1_CONTINUED	ISRC1_VALID				ISRC1_STATUS.2	ISRC1_STATUS.1	ISRC1_STATUS.0	---	---
217	D9h	ISRC1_PACKET_BYTE_0	r	ISRC1_PB0.7	ISRC1_PB0.6	ISRC1_PB0.5	ISRC1_PB0.4	ISRC1_PB0.3	ISRC1_PB0.2	ISRC1_PB0.1	ISRC1_PB0.0	---	---
218	DAh	ISRC1_PACKET_BYTE_1	r	ISRC1_PB1.7	ISRC1_PB1.6	ISRC1_PB1.5	ISRC1_PB1.4	ISRC1_PB1.3	ISRC1_PB1.2	ISRC1_PB1.1	ISRC1_PB1.0	---	---
219	DBh	ISRC1_PACKET_BYTE_2	r	ISRC1_PB2.7	ISRC1_PB2.6	ISRC1_PB2.5	ISRC1_PB2.4	ISRC1_PB2.3	ISRC1_PB2.2	ISRC1_PB2.1	ISRC1_PB2.0	---	---
220	DCh	ISRC1_PACKET_BYTE_3	r	ISRC1_PB3.7	ISRC1_PB3.6	ISRC1_PB3.5	ISRC1_PB3.4	ISRC1_PB3.3	ISRC1_PB3.2	ISRC1_PB3.1	ISRC1_PB3.0	---	---
221	DDh	ISRC1_PACKET_BYTE_4	r	ISRC1_PB4.7	ISRC1_PB4.6	ISRC1_PB4.5	ISRC1_PB4.4	ISRC1_PB4.3	ISRC1_PB4.2	ISRC1_PB4.1	ISRC1_PB4.0	---	---
222	DEh	ISRC1_PACKET_BYTE_5	r	ISRC1_PB5.7	ISRC1_PB5.6	ISRC1_PB5.5	ISRC1_PB5.4	ISRC1_PB5.3	ISRC1_PB5.2	ISRC1_PB5.1	ISRC1_PB5.0	---	---
224	E0h	ISRC1_PACKET_BYTE_6	r	ISRC1_PB6.7	ISRC1_PB6.6	ISRC1_PB6.5	ISRC1_PB6.4	ISRC1_PB6.3	ISRC1_PB6.2	ISRC1_PB6.1	ISRC1_PB6.0	---	---
225	E1h	ISRC1_PACKET_BYTE_7	r	ISRC1_PB7.7	ISRC1_PB7.6	ISRC1_PB7.5	ISRC1_PB7.4	ISRC1_PB7.3	ISRC1_PB7.2	ISRC1_PB7.1	ISRC1_PB7.0	---	---
226	E2h	ISRC1_PACKET_BYTE_8	r	ISRC1_PB8.7	ISRC1_PB8.6	ISRC1_PB8.5	ISRC1_PB8.4	ISRC1_PB8.3	ISRC1_PB8.2	ISRC1_PB8.1	ISRC1_PB8.0	---	---
227	E3h	ISRC1_PACKET_BYTE_9	r	ISRC1_PB9.7	ISRC1_PB9.6	ISRC1_PB9.5	ISRC1_PB9.4	ISRC1_PB9.3	ISRC1_PB9.2	ISRC1_PB9.1	ISRC1_PB9.0	---	---
228	E4h	ISRC1_PACKET_BYTE_10	r	ISRC1_PB10.7	ISRC1_PB10.6	ISRC1_PB10.5	ISRC1_PB10.4	ISRC1_PB10.3	ISRC1_PB10.2	ISRC1_PB10.1	ISRC1_PB10.0	---	---
229	E5h	ISRC1_PACKET_BYTE_11	r	ISRC1_PB11.7	ISRC1_PB11.6	ISRC1_PB11.5	ISRC1_PB11.4	ISRC1_PB11.3	ISRC1_PB11.2	ISRC1_PB11.1	ISRC1_PB11.0	---	---
230	E6h	ISRC1_PACKET_BYTE_12	r	ISRC1_PB12.7	ISRC1_PB12.6	ISRC1_PB12.5	ISRC1_PB12.4	ISRC1_PB12.3	ISRC1_PB12.2	ISRC1_PB12.1	ISRC1_PB12.0	---	---
232	E8h	ISRC1_PACKET_BYTE_13	r	ISRC1_PB13.7	ISRC1_PB13.6	ISRC1_PB13.5	ISRC1_PB13.4	ISRC1_PB13.3	ISRC1_PB13.2	ISRC1_PB13.1	ISRC1_PB13.0	---	---
233	E9h	ISRC1_PACKET_BYTE_14	r	ISRC1_PB14.7	ISRC1_PB14.6	ISRC1_PB14.5	ISRC1_PB14.4	ISRC1_PB14.3	ISRC1_PB14.2	ISRC1_PB14.1	ISRC1_PB14.0	---	---
234	EAh	ISRC1_PACKET_BYTE_15	r	ISRC1_PB15.7	ISRC1_PB15.6	ISRC1_PB15.5	ISRC1_PB15.4	ISRC1_PB15.3	ISRC1_PB15.2	ISRC1_PB15.1	ISRC1_PB15.0	---	---
235	EBh	ISRC2_PACKET_BYTE_0	r	ISRC2_PB0.7	ISRC2_PB0.6	ISRC2_PB0.5	ISRC2_PB0.4	ISRC2_PB0.3	ISRC2_PB0.2	ISRC2_PB0.1	ISRC2_PB0.0	---	---
236	ECh	ISRC2_PACKET_BYTE_1	r	ISRC2_PB1.7	ISRC2_PB1.6	ISRC2_PB1.5	ISRC2_PB1.4	ISRC2_PB1.3	ISRC2_PB1.2	ISRC2_PB1.1	ISRC2_PB1.0	---	---
237	EDh	ISRC2_PACKET_BYTE_2	r	ISRC2_PB2.7	ISRC2_PB2.6	ISRC2_PB2.5	ISRC2_PB2.4	ISRC2_PB2.3	ISRC2_PB2.2	ISRC2_PB2.1	ISRC2_PB2.0	---	---
238	EEh	ISRC2_PACKET_BYTE_3	r	ISRC2_PB3.7	ISRC2_PB3.6	ISRC2_PB3.5	ISRC2_PB3.4	ISRC2_PB3.3	ISRC2_PB3.2	ISRC2_PB3.1	ISRC2_PB3.0	---	---
240	F0h	ISRC2_PACKET_BYTE_4	r	ISRC2_PB4.7	ISRC2_PB4.6	ISRC2_PB4.5	ISRC2_PB4.4	ISRC2_PB4.3	ISRC2_PB4.2	ISRC2_PB4.1	ISRC2_PB4.0	---	---
241	F1h	ISRC2_PACKET_BYTE_5	r	ISRC2_PB5.7	ISRC2_PB5.6	ISRC2_PB5.5	ISRC2_PB5.4	ISRC2_PB5.3	ISRC2_PB5.2	ISRC2_PB5.1	ISRC2_PB5.0	---	---
242	F2h	ISRC2_PACKET_BYTE_6	r	ISRC2_PB6.7	ISRC2_PB6.6	ISRC2_PB6.5	ISRC2_PB6.4	ISRC2_PB6.3	ISRC2_PB6.2	ISRC2_PB6.1	ISRC2_PB6.0	---	---
243	F3h	ISRC2_PACKET_BYTE_7	r	ISRC2_PB7.7	ISRC2_PB7.6	ISRC2_PB7.5	ISRC2_PB7.4	ISRC2_PB7.3	ISRC2_PB7.2	ISRC2_PB7.1	ISRC2_PB7.0	---	---
244	F4h	ISRC2_PACKET_BYTE_8	r	ISRC2_PB8.7	ISRC2_PB8.6	ISRC2_PB8.5	ISRC2_PB8.4	ISRC2_PB8.3	ISRC2_PB8.2	ISRC2_PB8.1	ISRC2_PB8.0	---	---
245	F5h	ISRC2_PACKET_BYTE_9	r	ISRC2_PB9.7	ISRC2_PB9.6	ISRC2_PB9.5	ISRC2_PB9.4	ISRC2_PB9.3	ISRC2_PB9.2	ISRC2_PB9.1	ISRC2_PB9.0	---	---
246	F6h	ISRC2_PACKET_BYTE_10	r	ISRC2_PB10.7	ISRC2_PB10.6	ISRC2_PB10.5	ISRC2_PB10.4	ISRC2_PB10.3	ISRC2_PB10.2	ISRC2_PB10.1	ISRC2_PB10.0	---	---
248	F8h	ISRC2_PACKET_BYTE_11	r	ISRC2_PB11.7	ISRC2_PB11.6	ISRC2_PB11.5	ISRC2_PB11.4	ISRC2_PB11.3	ISRC2_PB11.2	ISRC2_PB11.1	ISRC2_PB11.0	---	---
249	F9h	ISRC2_PACKET_BYTE_12	r	ISRC2_PB12.7	ISRC2_PB12.6	ISRC2_PB12.5	ISRC2_PB12.4	ISRC2_PB12.3	ISRC2_PB12.2	ISRC2_PB12.1	ISRC2_PB12.0	---	---
250	FAh	ISRC2_PACKET_BYTE_13	r	ISRC2_PB13.7	ISRC2_PB13.6	ISRC2_PB13.5	ISRC2_PB13.4	ISRC2_PB13.3	ISRC2_PB13.2	ISRC2_PB13.1	ISRC2_PB13.0	---	---
251	FBh	ISRC2_PACKET_BYTE_14	r	ISRC2_PB14.7	ISRC2_PB14.6	ISRC2_PB14.5	ISRC2_PB14.4	ISRC2_PB14.3	ISRC2_PB14.2	ISRC2_PB14.1	ISRC2_PB14.0	---	---
252	FCh	ISRC2_PACKET_BYTE_15	r	ISRC2_PB15.7	ISRC2_PB15.6	ISRC2_PB15.5	ISRC2_PB15.4	ISRC2_PB15.3	ISRC2_PB15.2	ISRC2_PB15.1	ISRC2_PB15.0	---	---
253	FDh	ISRC2_PACKET_BYTE_16	r	ISRC2_PB16.7	ISRC2_PB16.6	ISRC2_PB16.5	ISRC2_PB16.4	ISRC2_PB16.3	ISRC2_PB16.2	ISRC2_PB16.1	ISRC2_PB16.0	---	---
254	FEh	ISRC2_PACKET_BYTE_17	r	ISRC2_PB17.7	ISRC2_PB17.6	ISRC2_PB17.5	ISRC2_PB17.4	ISRC2_PB17.3	ISRC2_PB17.2	ISRC2_PB17.1	ISRC2_PB17.0	---	---

1.6 Repeater KSV Map

Table 8: Repeater KSV Map Register 0x00 to 0xA5

Address		Register Name	rw	7	6	5	4	3	2	1	0	Reset Value	(Hex)
0	00h	BKSV_0	r	BKSV.7	BKSV.6	BKSV.5	BKSV.4	BKSV.3	BKSV.2	BKSV.1	BKSV.0	---	---
1	01h	BKSV_1	r	BKSV.15	BKSV.14	BKSV.13	BKSV.12	BKSV.11	BKSV.10	BKSV.9	BKSV.8	---	---
2	02h	BKSV_2	r	BKSV.23	BKSV.22	BKSV.21	BKSV.20	BKSV.19	BKSV.18	BKSV.17	BKSV.16	---	---
3	03h	BKSV_3	r	BKSV.31	BKSV.30	BKSV.29	BKSV.28	BKSV.27	BKSV.26	BKSV.25	BKSV.24	---	---
4	04h	BKSV_4	r	BKSV.39	BKSV.38	BKSV.37	BKSV.36	BKSV.35	BKSV.34	BKSV.33	BKSV.32	---	---
8	08h	Ri_0	r	Ri.7	Ri.6	Ri.5	Ri.4	Ri.3	Ri.2	Ri.1	Ri.0	---	---
9	09h	Ri_1	r	Ri.15	Ri.14	Ri.13	Ri.12	Ri.11	Ri.10	Ri.9	Ri.8	---	---
10	0Ah	Pj	r	Pj.7	Pj.6	Pj.5	Pj.4	Pj.3	Pj.2	Pj.1	Pj.0	---	---
16	10h	AKSV_0	rw	AKSV.7	AKSV.6	AKSV.5	AKSV.4	AKSV.3	AKSV.2	AKSV.1	AKSV.0	00000000	00
17	11h	AKSV_1	rw	AKSV.15	AKSV.14	AKSV.13	AKSV.12	AKSV.11	AKSV.10	AKSV.9	AKSV.8	00000000	00
18	12h	AKSV_2	rw	AKSV.23	AKSV.22	AKSV.21	AKSV.20	AKSV.19	AKSV.18	AKSV.17	AKSV.16	00000000	00
19	13h	AKSV_3	rw	AKSV.31	AKSV.30	AKSV.29	AKSV.28	AKSV.27	AKSV.26	AKSV.25	AKSV.24	00000000	00
20	14h	AKSV_4	rw	AKSV.39	AKSV.38	AKSV.37	AKSV.36	AKSV.35	AKSV.34	AKSV.33	AKSV.32	00000000	00
21	15h	Ainfo	rw	Ainfo.7	Ainfo.6	Ainfo.5	Ainfo.4	Ainfo.3	Ainfo.2	Ainfo.1	Ainfo.0	00000000	00
22	18h	AN_0	rw	AN.7	AN.6	AN.5	AN.4	AN.3	AN.2	AN.1	AN.0	00000000	00
23	19h	AN_1	rw	AN.15	AN.14	AN.13	AN.12	AN.11	AN.10	AN.9	AN.8	00000000	00
24	1Ah	AN_2	rw	AN.23	AN.22	AN.21	AN.20	AN.19	AN.18	AN.17	AN.16	00000000	00
25	1Bh	AN_3	rw	AN.31	AN.30	AN.29	AN.28	AN.27	AN.26	AN.25	AN.24	00000000	00
26	1Ch	AN_4	rw	AN.39	AN.38	AN.37	AN.36	AN.35	AN.34	AN.33	AN.32	00000000	00
27	1Dh	AN_5	rw	AN.47	AN.46	AN.45	AN.44	AN.43	AN.42	AN.41	AN.40	00000000	00
28	1Eh	AN_6	rw	AN.55	AN.54	AN.53	AN.52	AN.51	AN.50	AN.49	AN.48	00000000	00
29	1Fh	AN_7	rw	AN.63	AN.62	AN.61	AN.60	AN.59	AN.58	AN.57	AN.56	00000000	00
30	20h	SHA_A_0	rw	SHA_A.7	SHA_A.6	SHA_A.5	SHA_A.4	SHA_A.3	SHA_A.2	SHA_A.1	SHA_A.0	00000000	00
31	21h	SHA_A_1	rw	SHA_A.15	SHA_A.14	SHA_A.13	SHA_A.12	SHA_A.11	SHA_A.10	SHA_A.9	SHA_A.8	00000000	00
32	22h	SHA_A_2	rw	SHA_A.23	SHA_A.22	SHA_A.21	SHA_A.20	SHA_A.19	SHA_A.18	SHA_A.17	SHA_A.16	00000000	00
33	23h	SHA_A_3	rw	SHA_A.31	SHA_A.30	SHA_A.29	SHA_A.28	SHA_A.27	SHA_A.26	SHA_A.25	SHA_A.24	00000000	00
34	24h	SHA_B_0	rw	SHA_B.7	SHA_B.6	SHA_B.5	SHA_B.4	SHA_B.3	SHA_B.2	SHA_B.1	SHA_B.0	00000000	00
35	25h	SHA_B_1	rw	SHA_B.15	SHA_B.14	SHA_B.13	SHA_B.12	SHA_B.11	SHA_B.10	SHA_B.9	SHA_B.8	00000000	00
36	26h	SHA_B_2	rw	SHA_B.23	SHA_B.22	SHA_B.21	SHA_B.20	SHA_B.19	SHA_B.18	SHA_B.17	SHA_B.16	00000000	00
37	27h	SHA_B_3	rw	SHA_B.31	SHA_B.30	SHA_B.29	SHA_B.28	SHA_B.27	SHA_B.26	SHA_B.25	SHA_B.24	00000000	00
38	28h	SHA_C_0	rw	SHA_C.7	SHA_C.6	SHA_C.5	SHA_C.4	SHA_C.3	SHA_C.2	SHA_C.1	SHA_C.0	00000000	00
39	29h	SHA_C_1	rw	SHA_C.15	SHA_C.14	SHA_C.13	SHA_C.12	SHA_C.11	SHA_C.10	SHA_C.9	SHA_C.8	00000000	00
40	2Ah	SHA_C_2	rw	SHA_C.23	SHA_C.22	SHA_C.21	SHA_C.20	SHA_C.19	SHA_C.18	SHA_C.17	SHA_C.16	00000000	00
41	2Bh	SHA_C_3	rw	SHA_C.31	SHA_C.30	SHA_C.29	SHA_C.28	SHA_C.27	SHA_C.26	SHA_C.25	SHA_C.24	00000000	00
42	2Ch	SHA_D_0	rw	SHA_D.7	SHA_D.6	SHA_D.5	SHA_D.4	SHA_D.3	SHA_D.2	SHA_D.1	SHA_D.0	00000000	00
43	2Dh	SHA_D_1	rw	SHA_D.15	SHA_D.14	SHA_D.13	SHA_D.12	SHA_D.11	SHA_D.10	SHA_D.9	SHA_D.8	00000000	00
44	2Eh	SHA_D_2	rw	SHA_D.23	SHA_D.22	SHA_D.21	SHA_D.20	SHA_D.19	SHA_D.18	SHA_D.17	SHA_D.16	00000000	00
45	2Fh	SHA_D_3	rw	SHA_D.31	SHA_D.30	SHA_D.29	SHA_D.28	SHA_D.27	SHA_D.26	SHA_D.25	SHA_D.24	00000000	00
46	30h	SHA_E_0	rw	SHA_E.7	SHA_E.6	SHA_E.5	SHA_E.4	SHA_E.3	SHA_E.2	SHA_E.1	SHA_E.0	00000000	00
47	31h	SHA_E_1	rw	SHA_E.15	SHA_E.14	SHA_E.13	SHA_E.12	SHA_E.11	SHA_E.10	SHA_E.9	SHA_E.8	00000000	00
48	32h	SHA_E_2	rw	SHA_E.23	SHA_E.22	SHA_E.21	SHA_E.20	SHA_E.19	SHA_E.18	SHA_E.17	SHA_E.16	00000000	00
49	33h	SHA_E_3	rw	SHA_E.31	SHA_E.30	SHA_E.29	SHA_E.28	SHA_E.27	SHA_E.26	SHA_E.25	SHA_E.24	00000000	00
64	40h	Bcaps	rw	Bcaps.7	Bcaps.6	Bcaps.5	Bcaps.4	Bcaps.3	Bcaps.2	Bcaps.1	Bcaps.0	00000000	00
65	41h	BStatus_0	rw	BStatus.7	BStatus.6	BStatus.5	BStatus.4	BStatus.3	BStatus.2	BStatus.1	BStatus.0	00000000	00
66	42h	BStatus_1	rw	BStatus.15	BStatus.14	BStatus.13	BStatus.12	BStatus.11	BStatus.10	BStatus.9	BStatus.8	00000000	00
112	70h	SPA_PortB_A_B	rw	SPA_PortB_A.3	SPA_PortB_A.2	SPA_PortB_A.1	SPA_PortB_A.0	SPA_PortB_B.3	SPA_PortB_B.2	SPA_PortB_B.1	SPA_PortB_B.0	00000000	00
113	71h	SPA_PortB_C_D	rw	SPA_PortB_C.3	SPA_PortB_C.2	SPA_PortB_C.1	SPA_PortB_C.0	SPA_PortB_D.3	SPA_PortB_D.2	SPA_PortB_D.1	SPA_PortB_D.0	00000000	00
114	72h	SPA_Location	rw	SPA_Location.7	SPA_Location.6	SPA_Location.5	SPA_Location.4	SPA_Location.3	SPA_Location.2	SPA_Location.1	SPA_Location.0	00000000	00
115	73h	CTRL_BITS	rw						EDID_A_Enable	EDID_B_Enable	KSV_List_Ready	00000000	00
118	76h	PortB_Chksum	rw	PortB_Chksum.7	PortB_Chksum.6	PortB_Chksum.5	PortB_Chksum.4	PortB_Chksum.3	PortB_Chksum.2	PortB_Chksum.1	PortB_Chksum.0	00000000	00
128	80h	KSV0_B0	rw	KSV0.7	KSV0.6	KSV0.5	KSV0.4	KSV0.3	KSV0.2	KSV0.1	KSV0.0	00000000	00
129	81h	KSV0_B1	rw	KSV0.15	KSV0.14	KSV0.13	KSV0.12	KSV0.11	KSV0.10	KSV0.9	KSV0.8	00000000	00
130	82h	KSV0_B2	rw	KSV0.23	KSV0.22	KSV0.21	KSV0.20	KSV0.19	KSV0.18	KSV0.17	KSV0.16	00000000	00
131	83h	KSV0_B3	rw	KSV0.31	KSV0.30	KSV0.29	KSV0.28	KSV0.27	KSV0.26	KSV0.25	KSV0.24	00000000	00
132	84h	KSV0_B4	rw	KSV0.39	KSV0.38	KSV0.37	KSV0.36	KSV0.35	KSV0.34	KSV0.33	KSV0.32	00000000	00
133	85h	KSV1_B0	rw	KSV1.7	KSV1.6	KSV1.5	KSV1.4	KSV1.3	KSV1.2	KSV1.1	KSV1.0	00000000	00
134	86h	KSV1_B1	rw	KSV1.15	KSV1.14	KSV1.13	KSV1.12	KSV1.11	KSV1.10	KSV1.9	KSV1.8	00000000	00
135	87h	KSV1_B2	rw	KSV1.23	KSV1.22	KSV1.21	KSV1.20	KSV1.19	KSV1.18	KSV1.17	KSV1.16	00000000	00
136	88h	KSV1_B3	rw	KSV1.31	KSV1.30	KSV1.29	KSV1.28	KSV1.27	KSV1.26	KSV1.25	KSV1.24	00000000	00
137	89h	KSV1_B4	rw	KSV1.39	KSV1.38	KSV1.37	KSV1.36	KSV1.35	KSV1.34	KSV1.33	KSV1.32	00000000	00
138	8Ah	KSV2_B0	rw	KSV2.7	KSV2.6	KSV2.5	KSV2.4	KSV2.3	KSV2.2	KSV2.1	KSV2.0	00000000	00
139	8Bh	KSV2_B1	rw	KSV2.15	KSV2.14	KSV2.13	KSV2.12	KSV2.11	KSV2.10	KSV2.9	KSV2.8	00000000	00
140	8Ch	KSV2_B2	rw	KSV2.23	KSV2.22	KSV2.21	KSV2.20	KSV2.19	KSV2.18	KSV2.17	KSV2.16	00000000	00
141	8Dh	KSV2_B3	rw	KSV2.31	KSV2.30	KSV2.29	KSV2.28	KSV2.27	KSV2.26	KSV2.25	KSV2.24	00000000	00
142	8Eh	KSV2_B4	rw	KSV2.39	KSV2.38	KSV2.37	KSV2.36	KSV2.35	KSV2.34	KSV2.33	KSV2.32	00000000	00
143	8Fh	KSV3_B0	rw	KSV3.7	KSV3.6	KSV3.5	KSV3.4	KSV3.3	KSV3.2	KSV3.1	KSV3.0	00000000	00
144	90h	KSV3_B1	rw	KSV3.15	KSV3.14	KSV3.13	KSV3.12	KSV3.11	KSV3.10	KSV3.9	KSV3.8	00000000	00
145	91h	KSV3_B2	rw	KSV3.23	KSV3.22	KSV3.21	KSV3.20	KSV3.19	KSV3.18	KSV3.17	KSV3.16	00000000	00
146	92h	KSV3_B3	rw	KSV3.31	KSV3.30	KSV3.29	KSV3.28	KSV3.27	KSV3.26	KSV3.25	KSV3.24	00000000	00
147	93h	KSV3_B4	rw	KSV3.39	KSV3.38	KSV3.37	KSV3.36	KSV3.35	KSV3.34	KSV3.33	KSV3.32	00000000	00
148	94h	KSV4_B0	rw	KSV4.7	KSV4.6	KSV4.5	KSV4.4	KSV4.3	KSV4.2	KSV4.1	KSV4.0	00000000	00
149	95h	KSV4_B1	rw	KSV4.15	KSV4.14	KSV4.13	KSV4.12	KSV4.11	KSV4.10	KSV4.9	KSV4.8	00000000	00
150	96h	KSV4_B2	rw	KSV4.23	KSV4.22	KSV4.21	KSV4.20	KSV4.19	KSV4.18	KSV4.17	KSV4.16	00000000	00
151	97h	KSV4_B3	rw	KSV4.31	KSV4.30	KSV4.29	KSV4.28	KSV4.27	KSV4.26	KSV4.25	KSV4.24	00000000	00
152	98h	KSV4_B4	rw	KSV4.39	KSV4.38	KSV4.37	KSV4.36	KSV4.35	KSV4.34	KSV4.33	KSV4.32	00000000	00
153	99h	KSV5_B0	rw	KSV5.7	KSV5.6	KSV5.5	KSV5.4	KSV5.3	KSV5.2	KSV5.1	KSV5.0	00000000	00
154	9Ah	KSV5_B1	rw	KSV5.15	KSV5.14	KSV5.13	KSV5.12	KSV5.11	KSV5.10	KSV5.9	KSV5.8	00000000	00
155	9Bh	KSV5_B2	rw	KSV5.23	KSV5.22	KSV5.21	KSV5.20	KSV5.19	KSV5.18	KSV5.17	KSV5.16	00000000	00
156	9Ch	KSV5_B3	rw	KSV5.31	KSV5.30	KSV5.29	KSV5.28	KSV5.27	KSV5.26	KSV5.25	KSV5.24	00000000	00
157	9Dh	KSV5_B4	rw	KSV5.39	KSV5.38	KSV5.37	KSV5.36	KSV5.35	KSV5.34	KSV5.33	KSV5.32	00000000	00
158	9Eh	KSV6_B0	rw	KSV6.7	KSV6.6	KSV6.5	KSV6.4	KSV6.3	KSV6.2	KSV6.1	KSV6.0	00000000	00
159	9Fh	KSV6_B1	rw	KSV6.15	KSV6.14	KSV6.13	KSV6.12	KSV6.11	KSV6.10	KSV6.9	KSV6.8	00000000	00
160	A0h	KSV6_B2	rw	KSV6.23	KSV6.22	KSV6.21	KSV6.20	KSV6.19	KSV6.18	KSV6.17	KSV6.16	00000000	00
161	A1h	KSV6_B3	rw	KSV6.31	KSV6.30	KSV6.29	KSV6.28	KSV6.27	KSV6.26	KSV6.25	KSV6.24	00000000	00
162	A2h	KSV6_B4	rw	KSV6.39	KSV6.38	KSV6.37	KSV6.36	KSV6.35	KSV6.34	KSV6.33	KSV6.32	00000000	00
163	A3h	KSV7_B0	rw	KSV7.7	KSV7.6	KSV7.5	KSV7.4	KSV7.3	KSV7.2	KSV7.1	KSV7.0	00000000	00
164	A4h	KSV7_B1	rw	KSV7.15	KSV7.14	KSV7.13	KSV7.12	KSV7.11	KSV7.10	KSV7.9	KSV7.8	00000000	00
165	A5h	KSV7_B2	rw	KSV7.23	KSV7.22	KSV7.21	KSV7.20	KSV7.19	KSV7.18	KSV7.17	KSV7.16	00000000	00

Table 9: Repeater KSV Map Register 0xA6 to 0xF7

Address		Register Name	rw	7	6	5	4	3	2	1	0	Reset Value	(Hex)
166	A6h	KSV7_B3	rw	KSV7.31	KSV7.30	KSV7.29	KSV7.28	KSV7.27	KSV7.26	KSV7.25	KSV7.24	00000000	00
167	A7h	KSV7_B4	rw	KSV7.39	KSV7.38	KSV7.37	KSV7.36	KSV7.35	KSV7.34	KSV7.33	KSV7.32	00000000	00
168	A8h	KSV8_B0	rw	KSV8.7	KSV8.6	KSV8.5	KSV8.4	KSV8.3	KSV8.2	KSV8.1	KSV8.0	00000000	00
169	A9h	KSV8_B1	rw	KSV8.15	KSV8.14	KSV8.13	KSV8.12	KSV8.11	KSV8.10	KSV8.9	KSV8.8	00000000	00
170	AAh	KSV8_B2	rw	KSV8.23	KSV8.22	KSV8.20	KSV8.19	KSV8.19	KSV8.18	KSV8.17	KSV8.16	00000000	00
171	ABh	KSV8_B3	rw	KSV8.31	KSV8.30	KSV8.29	KSV8.28	KSV8.27	KSV8.26	KSV8.25	KSV8.24	00000000	00
172	ACh	KSV8_B4	rw	KSV8.39	KSV8.38	KSV8.37	KSV8.36	KSV8.35	KSV8.34	KSV8.33	KSV8.32	00000000	00
173	ADh	KSV9_B0	rw	KSV9.7	KSV9.6	KSV9.5	KSV9.4	KSV9.3	KSV9.2	KSV9.1	KSV9.0	00000000	00
174	AEh	KSV9_B1	rw	KSV9.15	KSV9.14	KSV9.13	KSV9.12	KSV9.11	KSV9.10	KSV9.9	KSV9.8	00000000	00
175	AFh	KSV9_B2	rw	KSV9.23	KSV9.22	KSV9.21	KSV9.20	KSV9.19	KSV9.18	KSV9.17	KSV9.16	00000000	00
176	B0h	KSV9_B3	rw	KSV9.31	KSV9.30	KSV9.29	KSV9.28	KSV9.27	KSV9.26	KSV9.25	KSV9.24	00000000	00
177	B1h	KSV9_B4	rw	KSV9.39	KSV9.38	KSV9.37	KSV9.36	KSV9.35	KSV9.34	KSV9.33	KSV9.32	00000000	00
178	B2h	KSV10_B0	rw	KSV10.7	KSV10.6	KSV10.5	KSV10.4	KSV10.3	KSV10.2	KSV10.1	KSV10.0	00000000	00
179	B3h	KSV10_B1	rw	KSV10.15	KSV10.14	KSV10.13	KSV10.12	KSV10.11	KSV10.10	KSV10.9	KSV10.8	00000000	00
180	B4h	KSV10_B2	rw	KSV10.23	KSV10.22	KSV10.21	KSV10.20	KSV10.19	KSV10.18	KSV10.17	KSV10.16	00000000	00
181	B5h	KSV10_B3	rw	KSV10.31	KSV10.30	KSV10.29	KSV10.28	KSV10.27	KSV10.26	KSV10.25	KSV10.24	00000000	00
182	B6h	KSV10_B4	rw	KSV10.39	KSV10.38	KSV10.37	KSV10.36	KSV10.35	KSV10.34	KSV10.33	KSV10.32	00000000	00
183	B7h	KSV11_B0	rw	KSV11.7	KSV11.6	KSV11.5	KSV11.4	KSV11.3	KSV11.2	KSV11.1	KSV11.0	00000000	00
184	B8h	KSV11_B1	rw	KSV11.15	KSV11.14	KSV11.13	KSV11.12	KSV11.11	KSV11.10	KSV11.9	KSV11.8	00000000	00
185	B9h	KSV11_B2	rw	BKSV11.23	BKSV11.22	BKSV11.21	BKSV11.20	BKSV11.19	BKSV11.18	BKSV11.17	BKSV11.16	00000000	00
186	BAh	KSV11_B3	rw	KSV11.31	KSV11.30	KSV11.29	KSV11.28	KSV11.27	KSV11.26	KSV11.25	KSV11.24	00000000	00
187	BBh	KSV11_B4	rw	KSV11.39	KSV11.38	KSV11.37	KSV11.36	KSV11.35	KSV11.34	KSV11.33	KSV11.32	00000000	00
188	BCh	KSV12_B0	rw	KSV12.7	KSV12.6	KSV12.5	KSV12.4	KSV12.3	KSV12.2	KSV12.1	KSV12.0	00000000	00
189	BDh	KSV12_B1	rw	KSV12.15	KSV12.14	KSV12.13	KSV12.12	KSV12.11	KSV12.10	KSV12.9	KSV12.8	00000000	00
190	BEh	KSV12_B2	rw	KSV12.23	KSV12.22	KSV12.21	KSV12.20	KSV12.19	KSV12.18	KSV12.17	KSV12.16	00000000	00
191	BFh	KSV12_B3	rw	KSV12.31	KSV12.30	KSV12.29	KSV12.28	KSV12.27	KSV12.26	KSV12.25	KSV12.24	00000000	00
192	C0h	KSV12_B4	rw	KSV12.39	KSV12.38	KSV12.37	KSV12.36	KSV12.35	KSV12.34	KSV12.33	KSV12.32	00000000	00
193	C1h	KSV13_B0	rw	KSV13.7	KSV13.6	KSV13.5	KSV13.4	KSV13.3	KSV13.2	KSV13.1	KSV13.0	00000000	00
194	C2h	KSV13_B1	rw	KSV13.15	KSV13.14	KSV13.13	KSV13.12	KSV13.11	KSV13.10	KSV13.9	KSV13.8	00000000	00
195	C3h	KSV13_B2	rw	KSV13.23	KSV13.22	KSV13.21	KSV13.20	KSV13.19	KSV13.18	KSV13.17	KSV13.16	00000000	00
196	C4h	KSV13_B3	rw	KSV13.31	KSV13.30	KSV13.29	KSV13.28	KSV13.27	KSV13.26	KSV13.25	KSV13.24	00000000	00
197	C5h	KSV13_B4	rw	KSV13.39	KSV13.38	KSV13.37	KSV13.36	KSV13.35	KSV13.34	KSV13.33	KSV13.32	00000000	00
198	C6h	KSV14_B0	rw	KSV14.7	KSV14.6	KSV14.5	KSV14.4	KSV14.3	KSV14.2	KSV14.1	KSV14.0	00000000	00
199	C7h	KSV14_B1	rw	KSV14.15	KSV14.14	KSV14.13	KSV14.12	KSV14.11	KSV14.10	KSV14.9	KSV14.8	00000000	00
200	C8h	KSV14_B2	rw	KSV14.23	KSV14.22	KSV14.21	KSV14.20	KSV14.19	KSV14.18	KSV14.17	KSV14.16	00000000	00
201	C9h	KSV14_B3	rw	KSV14.31	KSV14.30	KSV14.29	KSV14.28	KSV14.27	KSV14.26	KSV14.25	KSV14.24	00000000	00
202	CAh	KSV14_B4	rw	KSV14.39	KSV14.38	KSV14.37	KSV14.36	KSV14.35	KSV14.34	KSV14.33	KSV14.32	00000000	00
203	CBh	KSV15_B0	rw	KSV15.7	KSV15.6	KSV15.5	KSV15.4	KSV15.3	KSV15.2	KSV15.1	KSV15.0	00000000	00
204	CCh	KSV15_B1	rw	KSV15.15	KSV15.14	KSV15.13	KSV15.12	KSV15.11	KSV15.10	KSV15.9	KSV15.8	00000000	00
205	CDh	KSV15_B2	rw	KSV15.23	KSV15.22	KSV15.21	KSV15.20	KSV15.19	KSV15.18	KSV15.17	KSV15.16	00000000	00
206	CEh	KSV15_B3	rw	KSV15.31	KSV15.30	KSV15.29	KSV15.28	KSV15.27	KSV15.26	KSV15.25	KSV15.24	00000000	00
207	CFh	KSV15_B4	rw	KSV15.39	KSV15.38	KSV15.37	KSV15.36	KSV15.35	KSV15.34	KSV15.33	KSV15.32	00000000	00
208	D0h	KSV16_B0	rw	KSV16.7	KSV16.6	KSV16.5	KSV16.4	KSV16.3	KSV16.2	KSV16.1	KSV16.0	00000000	00
209	D1h	KSV16_B1	rw	KSV16.15	KSV16.14	KSV16.13	KSV16.12	KSV16.11	KSV16.10	KSV16.9	KSV16.8	00000000	00
210	D2h	KSV16_B2	rw	KSV16.23	KSV16.22	KSV16.21	KSV16.20	KSV16.19	KSV16.18	KSV16.17	KSV16.16	00000000	00
211	D3h	KSV16_B3	rw	KSV16.31	KSV16.30	KSV16.29	KSV16.28	KSV16.27	KSV16.26	KSV16.25	KSV16.24	00000000	00
212	D4h	KSV16_B4	rw	KSV16.39	KSV16.38	KSV16.37	KSV16.36	KSV16.35	KSV16.34	KSV16.33	KSV16.32	00000000	00
213	D5h	KSV17_B0	rw	KSV17.7	KSV17.6	KSV17.5	KSV17.4	KSV17.3	KSV17.2	KSV17.1	KSV17.0	00000000	00
214	D6h	KSV17_B1	rw	KSV17.15	KSV17.14	KSV17.13	KSV17.12	KSV17.11	KSV17.10	KSV17.9	KSV17.8	00000000	00
215	D7h	KSV17_B2	rw	KSV17.23	KSV17.22	KSV17.21	KSV17.20	KSV17.19	KSV17.18	KSV17.17	KSV17.16	00000000	00
216	D8h	KSV17_B3	rw	KSV17.31	KSV17.30	KSV17.29	KSV17.28	KSV17.27	KSV17.26	KSV17.25	KSV17.24	00000000	00
217	D9h	KSV17_B4	rw	KSV17.39	KSV17.38	KSV17.37	KSV17.36	KSV17.35	KSV17.34	KSV17.33	KSV17.32	00000000	00
218	DAh	KSV18_B0	rw	KSV18.7	KSV18.6	KSV18.5	KSV18.4	KSV18.3	KSV18.2	KSV18.1	KSV18.0	00000000	00
219	DBh	KSV18_B1	rw	KSV18.15	KSV18.14	KSV18.13	KSV18.12	KSV18.11	KSV18.10	KSV18.9	KSV18.8	00000000	00
220	DCh	KSV18_B2	rw	KSV18.23	KSV18.22	KSV18.21	KSV18.20	KSV18.19	KSV18.18	KSV18.17	KSV18.16	00000000	00
221	DDh	KSV18_B3	rw	KSV18.31	KSV18.30	KSV18.29	KSV18.28	KSV18.27	KSV18.26	KSV18.25	KSV18.24	00000000	00
222	DEh	KSV18_B4	rw	KSV18.39	KSV18.38	KSV18.37	KSV18.36	KSV18.35	KSV18.34	KSV18.33	KSV18.32	00000000	00
223	DFh	KSV19_B0	rw	KSV19.7	KSV19.6	KSV19.5	KSV19.4	KSV19.3	KSV19.2	KSV19.1	KSV19.0	00000000	00
224	E0h	KSV19_B1	rw	KSV19.15	KSV19.14	KSV19.13	KSV19.12	KSV19.11	KSV19.10	KSV19.9	KSV19.8	00000000	00
225	E1h	KSV19_B2	rw	KSV19.23	KSV19.22	KSV19.21	KSV19.20	KSV19.19	KSV19.18	KSV19.17	KSV19.16	00000000	00
226	E2h	KSV19_B3	rw	KSV19.31	KSV19.30	KSV19.29	KSV19.28	KSV19.27	KSV19.26	KSV19.25	KSV19.24	00000000	00
227	E3h	KSV19_B4	rw	KSV19.39	KSV19.38	KSV19.37	KSV19.36	KSV19.35	KSV19.34	KSV19.33	KSV19.32	00000000	00
228	E4h	KSV20_B0	rw	KSV20.7	KSV20.6	KSV20.5	KSV20.4	KSV20.3	KSV20.2	KSV20.1	KSV20.0	00000000	00
229	E5h	KSV20_B1	rw	KSV20.15	KSV20.14	KSV20.13	KSV20.12	KSV20.11	KSV20.10	KSV20.9	KSV20.8	00000000	00
230	E6h	KSV20_B2	rw	KSV20.23	KSV20.22	KSV20.21	KSV20.20	KSV20.19	KSV20.18	KSV20.17	KSV20.16	00000000	00
231	E7h	KSV20_B3	rw	KSV20.31	KSV20.30	KSV20.29	KSV20.28	KSV20.27	KSV20.26	KSV20.25	KSV20.24	00000000	00
232	E8h	KSV20_B4	rw	KSV20.39	KSV20.38	KSV20.37	KSV20.36	KSV20.35	KSV20.34	KSV20.33	KSV20.32	00000000	00
233	E9h	KSV21_B0	rw	KSV21.7	KSV21.6	KSV21.5	KSV21.4	KSV21.3	KSV21.2	KSV21.1	KSV21.0	00000000	00
234	EAh	KSV21_B1	rw	KSV21.15	KSV21.14	KSV21.13	KSV21.12	KSV21.11	KSV21.10	KSV21.9	KSV21.8	00000000	00
235	EBh	KSV21_B2	rw	KSV21.23	KSV21.22	KSV21.21	KSV21.20	KSV21.19	KSV21.18	KSV21.17	KSV21.16	00000000	00
236	ECh	KSV21_B3	rw	KSV21.31	KSV21.30	KSV21.29	KSV21.28	KSV21.27	KSV21.26	KSV21.25	KSV21.24	00000000	00
237	EDh	KSV21_B4	rw	KSV21.39	KSV21.38	KSV21.37	KSV21.36	KSV21.35	KSV21.34	KSV21.33	KSV21.32	00000000	00
238	EEh	KSV22_B0	rw	KSV22.7	KSV22.6	KSV22.5	KSV22.4	KSV22.3	KSV22.2	KSV22.1	KSV22.0	00000000	00
239	EFh	KSV22_B1	rw	KSV22.15	KSV22.14	KSV22.13	KSV22.12	KSV22.11	KSV22.10	KSV22.9	KSV22.8	00000000	00
240	F0h	KSV22_B2	rw	KSV22.23	KSV22.22	KSV22.21	KSV22.20	KSV22.19	KSV22.18	KSV22.17	KSV22.16	00000000	00
241	F1h	KSV22_B3	rw	KSV22.31	KSV22.30	KSV22.29	KSV22.28	KSV22.27	KSV22.26	KSV22.25	KSV22.24	00000000	00
242	F2h	KSV22_B4	rw	KSV22.39	KSV22.38	KSV22.37	KSV22.36	KSV22.35	KSV22.34	KSV22.33	KSV22.32	00000000	00
243	F3h	KSV23_B0	rw	KSV23.7	KSV23.6	KSV23.5	KSV23.4	KSV23.3	KSV23.2	KSV23.1	KSV23.0	00000000	00
244	F4h	KSV23_B1	rw	KSV23.15	KSV23.14	KSV23.13	KSV23.12	KSV23.11	KSV23.10	KSV23.9	KSV23.8	00000000	00
245	F5h	KSV23_B2	rw	KSV23.23	KSV23.22	KSV23.21	KSV23.20	KSV23.19	KSV23.18	KSV23.17	KSV23.16	00000000	00
246	F6h	KSV23_B3	rw	KSV23.31	KSV23.30	KSV23.29	KSV23.28	KSV23.27	KSV23.26	KSV23.25	KSV23.24	00000000	00
247	F7h	KSV23_B4	rw	KSV23.39	KSV23.38	KSV23.37	KSV23.36	KSV23.35	KSV23.34	KSV23.33	KSV23.32	00000000	00

2 I²C Details Register Map Details

2.1 User Map

Grayed out sections in the following tables mark the reset value of the Details Register.

Table 10: User Map Details Details Register 0x00

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x00 R/W	Input Control	**INSEL [3:0]** The INSEL bits allow the user to select an input channel as well as the input format					0	0	0	0	CVBS in on AIN1	Composite
							0	0	0	1	CVBS in on AIN2	
							0	0	1	0	CVBS in on AIN3	
							0	0	1	1	CVBS in on AIN4	
							0	1	0	0	CVBS in on AIN5	
							0	1	0	1	CVBS in on AIN6	
							0	1	1	0	Y on AIN1, C on AIN4	S-Video
							0	1	1	1	Y on AIN2, C on AIN5	
							1	0	0	0	Y on AIN3, C on AIN6	
							1	0	0	1	Y on AIN1, Pr on AIN4, Pb on AIN5	YPrPb
							1	0	1	0	Y on AIN2, Pr on AIN3, Pb on AIN6	
							1	0	1	1	CVBS in on AIN7	Composite
							1	1	0	0	CVBS in on AIN8	
							1	1	0	1	CVBS in on AIN9	
							1	1	1	0	CVBS in on AIN10	
							1	1	1	1	CVBS in on AIN11	
		VID_SEL [3:0] The VID_SEL bits allow the user to select the input video standard	0	0	0	0					Auto detect PAL (BGHID), NTSC (without pedestal)	
			0	0	0	1					Auto detect PAL (BGHID), NTSC (M) (with pedestal)	
			0	0	1	0					Auto detect PAL (N), NTSC (M) (without pedestal)	
			0	0	1	1					Auto detect PAL (N), NTSC (M) (with pedestal)	
			0	1	0	0					NTSC (J)	
			0	1	0	1					NTSC (M)	
			0	1	1	0					PAL 60	
			0	1	1	1					NTSC 4.43	
			1	0	0	0					PAL BGHID	
			1	0	0	1					PAL N (BGHID without pedestal)	
			1	0	1	0					PAL M (without pedestal)	
			1	0	1	1					PAL M	
			1	1	0	0					PAL combination N	
			1	1	0	1					PAL combination N (with Pedestal)	
			1	1	1	0					SECAM	
			1	1	1	1					SECAM (with pedestal)	

Table 11: User Map Details Details Register 0x01 to 0x03

Subaddress	Register	Bit Desciption	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x01 R/W	Video selection	Reserved						0	0	0	Set to Default	
		ENVSPROC					0				Disable VSync Processor	
							1				Enable VSync Processor	
		Reserved				0					Set to Default	
		BETACAM			0						Standard video input	
					1						Betacam input enable	
		ENHSPLL		0							Disable HSync PLL	
				1							Enable HSync PLL	
		Reserved	1								Reserved set to 1	
0x02 R/W	Reserved	Reserved	0	0	0	0	0	1	0	0	Set to Default	
0x03 R/W	Output Control	**SD_DUP_AV** duplicate the AV codes from the Luma into the chroma path								0	AV codes to suit 8-bit interleaved data output	
										1	AV codes duplicated (for 16-bit interfaces)	
		Reserved							0		Set as default	
		OF_SEL [3:0] Allows the user to choose from a set of output formats.			0	0	0	0			10-bit @ LLC1 4:2:2 ITU-R BT.656	
					0	0	0	1			20-bit @ LLC2 4:2:2	
					0	0	1	0			16-bit @ LLC2 4:2:2	
					0	0	1	1			8-bit@LLC1 4:2:2 ITU-R BT.656	
					0	1	0	0			30-bit @ LLC2 4:4:4	
					0	1	0	1			24-bit @ LLC2 4:4:4	
					0	1	1	0			Not Used	
					0	1	1	1			Not Used	
					1	0	0	0			Not Used	
					1	0	0	1			Not Used	
					1	0	1	0			Not Used	
					1	0	1	1			Not Used	
					1	1	0	0			Not Used	
					1	1	0	1			Not Used	
					1	1	1	0			Not Used	
					1	1	1	1			Not Used	
		TOD Tri-State Output Drivers. This bit allows the		0							Output pins enabled	See also TIM_OE;
				1							Drivers tri-stated.	
		VBI_EN Allows VBI data (lines 1 to 21) to be passed through with only a mininum amount of filtering performed.	0								All lines filtered and scaled	
			1								Only active video region filtered	

Table 12: User Map Details Details Register 0x04

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x04 R/W	Extended Output Control	**RANGE** Allows the user to select the range of output values. Can be BT656 compliant or fill the whole accessible number range.								0	16<Y<235,16<C<240	ITU-R BT.656
										1	1<Y<254,1<C<254	Extended Range
		EN_SFL_PIN							0		SFL output is disabled	SFL output enables Encoder & Decoder to be connected directly
									1		SFL information output on the SFL pin	
		BL_C_VBI Blank Chroma During VBI. If set will enable data in the VBI region to be passed through the decoder undistorted						0			Decode and Output colour	During VBI
								1			Blank Cr and Cb	
		TIM_OE Timing Signals Output Enable					0				HS,VS,F tri-stated	Controlled by TOD
							1				HS,VS,F forced active	
		INT2_EN Shared pin with the SFL/SYNC_OUT function. Bit enables this pin to be used as an interrupt pin. It is similar to the SFL_EN bit (ADDR 04h bit 1)				0					INT2_EN disabled	Shared pin with the SFL/SYNC_OUT function
						1					INT2_EN enabled	
		Reserved			x						Set to 0	
		Reserved		1							Set to 1	
		BT656-4 Allows the user to select an output mode that is compatible with ITU-R BT656-3/4	0								BT656-3 compatible	
			1								BT656-4 compatible	

Table 13: User Map Details Register 0x05

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Processor	Comment
0x05 R/W	Primary Mode	**PRIM_MODE[3:0]** Selects the primary mode of operation of the decoder. Used with **VID_STD[4:0]**					0	0	0	0	Standard Definition	SDP	CVBS,YC,YPrPb
							0	0	0	1	Component Video (YPbPr/RGB)	CP	SD, HD and PR
							0	0	1	0	RGB Graphics mode	CP	VGA to SXGA
							0	0	1	1	Reserved		
							0	1	0	0	HDMI	HDMI	SD
							0	1	0	1	HDMI	HDMI	ED/HD
							0	1	1	0	HDMI	HDMI	VGA to SXGA
							0	1	1	1	Reserved		
							1	0	0	0	Reserved		
							1	0	0	1	Reserved		
							1	0	1	0	Reserved		
							1	0	1	1	Reserved		
							1	1	0	0	Reserved		
							1	1	0	1	Reserved		
							1	1	1	0	Reserved		
							1	1	1	1	Reserved		
		[7:4] Reserved	0	0	0	0					Set to default		

Table 14: User Map Details Register 0x06

Sub address	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Processor	Comment
0x06 R/W	Video Standard	**VID_STD[4:0]** Sets the input and output Video standards dependant on **PRIM_MODE[3:0]**				0	0	0	0	0	Reserved		PRIM_MODE= 0000 (SD-M)
						0	0	0	0	1	Reserved		
						0	0	0	1	0	SD 4x1 (54 MHz sampling)	SDP	
						0	0	0	1	1	Reserved		
						0	0	1	0	0	Reserved		
						0	0	1	0	1	Reserved		
						0	0	1	1	0	Reserved		
						0	0	1	1	1	Reserved		
						0	1	0	1	0	SD 4X1 525i (720x480)	CP	YUV through CP
						0	1	0	1	1	SD 4X1 625i (720x576)	CP	
						0	1	1	0	0	SD 1X1 525i (720x480)	CP	
						0	1	1	0	1	SD 1X1 625i (720x576)	CP	
						0	1	1	1	0	SD 2X1 525i (720x480)	CP	
						0	1	1	1	1	SD 2X1 625i (720x576)	CP	
						1	x	x	x	x	Reserved		
						0	0	0	0	0	525i 2X2 (1440x480)	CP	PRIM_MODE= 0001 (COMP SD/HD/PR)
						0	0	0	0	1	625i 2X2 (1440x576)	CP	
						0	0	0	1	0	525i 4X2 (1440x480)	CP	
						0	0	0	1	1	625i 4X2 (1440x576)	CP	
						0	0	1	0	0	525P 1X1 (720x480)	CP	
						0	0	1	0	1	625P 1X1 (720x576)	CP	
						0	0	1	1	0	525P 2X1 (720x480)	CP	
						0	0	1	1	1	625P 2X1 (720x576)	CP	
						0	1	0	0	0	525P 2X2 (1440x480)	CP	
						0	1	0	0	1	625P 2X2 (1440x576)	CP	
						0	1	0	1	0	HD 720P 1X1 (1280x720)	CP	
						0	1	0	1	1	HD 1080P 1X1 (1920x1080)	CP	
						0	1	1	0	0	HD 1125 1X1 (1920x1080)	CP	
						0	1	1	0	1	HD 1125 1X1 (1920x1035)	CP	
						0	1	1	1	0	HD 1250 1X1 (1920x1080)	CP	
						0	1	1	1	1	HD 1250 1X1 (1920x1152)	CP	
						1	0	0	0	0	External Clock and Clamp Mode 1		
						1	0	0	0	1	External Clock and Clamp Mode 2		
						1	0	0	1	0	Reserved		
						1	0	0	1	1	Reserved		
						1	0	1	0	0	Reserved		
						1	0	1	0	1	Reserved		
						1	0	1	1	0	525P 4X1 (720x480)	CP	
						1	0	1	1	1	625P 4X1 (720x576)	CP	
						1	1	0	0	0	Reserved		
						1	1	0	0	1	Reserved		
						1	1	0	1	0	Reserved		
						1	1	0	1	1	HD 1250P 1X1 (1920x1080)	CP	
						1	1	1	0	0	Reserved		
						1	1	1	0	1	Reserved		
						1	1	1	1	0	Reserved		
						1	1	1	1	1	Reserved		
						0	0	0	0	0	SVGA (800x600@56)	CP	PRIM_MODE= 0010 (Analog Graphics)
						0	0	0	0	1	SVGA (800x600@60)	CP	
						0	0	0	1	0	SVGA (800x600@72)	CP	
						0	0	0	1	1	SVGA (800x600@75)	CP	
						0	0	1	0	0	SVGA (800x600@85)	CP	
						0	0	1	0	1	SXGA (1280x1024@60)	CP	
						0	0	1	1	0	SXGA (1280x1024@75)	CP	
						0	0	1	1	1	Auto graphic mode (Refer to the Hardware manual)		
						0	1	0	0	0	VGA (640x480@60)	CP	
						0	1	0	0	1	VGA (640x480@72)	CP	
						0	1	0	1	0	VGA (640x480@75)	CP	
						0	1	0	1	1	VGA (640x480@85)	CP	
						0	1	1	0	0	XVGA (1024x768@60)	CP	
						0	1	1	0	1	XVGA (1024x768@70)	CP	
						0	1	1	1	0	XVGA (1024x768@75)	CP	
						0	1	1	1	1	XVGA (1024x768@85)	CP	
						1	x	x	x	x	Reserved		

Table 15: User Map Details Register 0x06 (Continued 1)

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Processor	Comment
0x06 R/W	Video Standard	**VID_STD[4:0]** Sets the input and output Video standards dependant on **PRIM_MODE[3:0]**				x	x	x	x	x	Reserved		PRIM_MODE= 0011
						0	0	0	0	0	Reserved	HDMI	PRIM_MODE= 0100 (HDMI-SD)
						~	~	~	~	~	Reserved		
						0	1	0	1	1	Reserved		
						0	1	1	0	0	SD 1X1 525i (720x480)		
						0	1	1	0	1	SD 1X1 625i (720x576)		
						0	1	1	1	0	Reserved		
						0	1	1	1	1	Reserved		
						1	x	x	x	x	Reserved		
						0	0	0	0	0	Reserved	HDMI	PRIM_MODE= 0101 (HDMI-COMP)
						~	~	~	~	~	Reserved		
						0	0	0	1	1	Reserved		
						0	0	1	0	0	ED 1X1 525P (720x480)		
						0	0	1	0	1	ED 1X1 625P (720x576)		
						0	0	1	1	0	Reserved		
						~	~	~	~	~	Reserved		
						0	1	0	0	1	Reserved		
						0	1	0	1	0	HD 1X1 720P (1280x720)		
						0	1	0	1	1	HD 1X1 1080P (1920x1080)		
						0	1	1	0	0	HD 1X1 1125i (1920x1080)		
						0	1	1	0	1	HD 1X1 1125i (1920x1035)		
						0	1	1	1	0	HD 1X1 1250i (1920x1080)		
						0	1	1	1	1	HD 1X1 1250i (1920x1152)		
						1	0	0	0	0	Reserved		
						~	~	~	~	~	Reserved		
						1	1	0	1	0	Reserved		
						1	1	0	1	1	HD 1X1 1250P (1920x1080)		
						1	1	1	0	0	Reserved		
						~	~	~	~	~	Reserved		
						1	1	1	1	1	Reserved		
						0	0	0	0	0	SVGA (800x600@56)	HDMI	PRIM_MODE= 0110 (HDMI-GR)
						0	0	0	0	1	SVGA (800x600@60)		
						0	0	0	1	0	SVGA (800x600@72)		
						0	0	0	1	1	SVGA (800x600@75)		
						0	0	1	0	0	SVGA (800x600@85)		
						0	0	1	0	1	SXGA (1280x1024@60)		
						0	0	1	1	0	SXGA (1280x1024@75)		
						0	0	1	1	1	Reserved		
						0	1	0	0	0	VGA (640x480@60)		
						0	1	0	0	1	VGA (640x480@72)		
						0	1	0	1	0	VGA (640x480@75)		
						0	1	0	1	1	VGA (640x480@85)		
						0	1	1	0	0	XGA (1024x768@60)		
						0	1	1	0	1	XGA (1024x768@70)		
						0	1	1	1	0	XGA (1024x768@75)		
						0	1	1	1	1	XGA (1024x768@85)		
						1	x	x	x	x	Reserved		

Table 16: User Map Details Register 0x06 (Continued 2)

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Processor	Comment
0x06 R/W	Video Standard	**VID_STD[4:0]** Sets the input and output Video standards dependant on **PRIM MODE[3:0]**				x	x	x	x	x	Reserved		PRIM_MODE= 0111
						x	x	x	x	x	Reserved		PRIM_MODE= 1000
						x	x	x	x	x	Reserved		PRIM_MODE= 1001
						x	x	x	x	x	Reserved		PRIM_MODE= 1010
						x	x	x	x	x	Reserved		PRIM_MODE= 1011
						x	x	x	x	x	Reserved		PRIM_MODE= 1100
						x	x	x	x	x	Reserved		PRIM_MODE= 1101
						x	x	x	x	x	Reserved		PRIM_MODE= 1110
						x	x	x	x	x	Reserved		PRIM_MODE= 1111

Table 17: User Map Details Register 0x06 (Continued 3)

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x06 R/W	Primary Mode	**CP_V_FREQ[2:0]** These bits are used when the decoder is required to support HD standards SMPTE 274, systems 6, 7, 8, 9, 10 and 11 ; SPMPTE 296, systems 3, 4, 5 and 6. These starndards have 50Hz, 30Hz, 25Hz and 24Hz refreshing rates.	0	0	0						Vertical frequency is 60Hz	720p 1x1 mode PRIM_MODE = 0001 VID_STD = 01010
			0	0	1						Vertical frequency is 50Hz	
			0	1	0						Vertical frequency is 30Hz	
			0	1	1						Vertical frequency is 25Hz	
			1	0	0						Vertical frequency is 24Hz	
			1	0	1						Reserved	
			1	1	0						Reserved	
			1	1	1						Reserved	
			0	0	0						Vertical frequency is 60Hz	1035i 1x1 mode PRIM_MODE = 0001 VID_STD = 01101
			0	0	1						Vertical frequency is 50Hz	
			0	1	0						Vertical frequency is 30Hz	
			0	1	1						Vertical frequency is 25Hz	
			1	0	0						Vertical frequency is 24Hz	
			1	0	1						Reserved	
			1	1	0						Reserved	
			1	1	1						Reserved	
			0	0	0						Vertical frequency is 60Hz	1080i 1x1 mode PRIM_MODE = 0001 VID_STD = 01100
			0	0	1						Vertical frequency is 50Hz	
			0	1	0						Vertical frequency is 30Hz	
			0	1	1						Vertical frequency is 25Hz	
			1	0	0						Vertical frequency is 24Hz	
			1	0	1						Reserved	
			1	1	0						Reserved	
			1	1	1						Reserved	
			0	0	0						Vertical frequency is 60Hz	1080p 1x1 mode PRIM_MODE = 0001 VID_STD = 01011
			0	0	1						Vertical frequency is 50Hz	
			0	1	0						Reserved	
			0	1	1						Reserved	
			1	0	0						Reserved	
			1	0	1						Reserved	
			1	1	0						Reserved	
			1	1	1						Reserved	

Table 18: User Map Details Register 0x07 to 0x0D

Subadress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x07 R/W	Auto Detect Enable	**AD_PAL_EN** PAL B/G/I/H autodetect enable								0	Disable	
										1	Enable	
		AD_NTSC_EN NTSC autodetect enable							0		Disable	
									1		Enable	
		AD_PALM_EN PAL M autodetect enable						0			Disable	
								1			Enable	
		AD_PALN_EN PAL N autodetect enable					0				Disable	
							1				Enable	
		AD_P60_EN PAL 60 autodetect enable				0					Disable	
						1					Enable	
		AD_N443_EN NTSC443 autodetect enable			0						Disable	
					1						Enable	
		AD_SECAM_EN SECAM autodetect enable		0							Disable	
				1							Enable	
		AD_SEC525_EN SECAM 525 autodetect enable	0								Disable	
			1								Enable	
0x08 R/W	Contrast register	**CON[7:0]** Contrast Adjust. This is the user control for contrast adjustment	1	0	0	0	0	0	0	0	Luma gain = 1	00h Gain = 0 80h Gain = 1 FFh Gain = 2
0x09 R/W	Reserved	Reserved	1	0	0	0	0	0	0	0	Set to default	
0x0A R/W	Brightness register	**BRI[7:0]** This register controls the brightness of the video signal.	0	0	0	0	0	0	0	0		00h = 0IRE 7Fh = 100IRE 80h = -100IRE
0x0B R/W	Hue Register	**HUE[7:0]** This register contains the value for the colour hue adjustment.	0	0	0	0	0	0	0	0		Hue Range = -90 degree to +90 degree
0x0C R/W	Default Value Y	**DEF_ VAL_ EN** Default Value Enable								0	Free Run mode dependent on DEF_ VAL_ AUTO_EN	
										1	Force SDP Free Run mode on and output Blue Screen	
		DEF_ VAL_ AUTO_EN Default Value Auto Enable. In the case of lost lock enables/disables default Y & C values.							0		Disable SDP Free Run mode	When lock is lost Free Run mode can be enabled to output stable timing, clock and a set color
									1		Enable Automatic Free Run Mode (Blue Screen)	
		DEF_Y[5:0] Default Value Y. This register holds the Y default value	0	0	1	1	0	1			Default Y value output in free-run mode Y[7:0]={DEF_Y[5:0], 0,0}	
0x0D R/W	Default Value C	**DEF_C[7:0]** Default Value C. Cr and Cb default values are defined in this register. User can control SDP Free output color from a reset default of blue to any other color	0	1	1	1	1	1	0	0	Cr[7:0]={DEF_C[7:4], 0,0,0,0} Cb[7:0]={DEF_C[3:0] ,0,0,0,0}	Default values give blue screen output

Table 19: User Map Details Register 0x0E to 0x10

Sub address	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x0E R/W	uss2 slave address	**USS2_ADDR[7:0]** I2C address of User Map 2	0	1	1	0	0	0	0	0		
0x0F R/W	Power Management	**[1:0]** Reserved								0	Set to Zero	
		FB_PWRDN							0		FB input operational	
									1		FB input in power save mode	
		PWRDN[0] Power Down places the decoder in a full power down mode.						0			System functional	Decoder is powered down when both PWRDN[0] and PWRDN[1] = 1
								1			Powered down if PWRDN[1] = 1	
		CP_PWRDN					0				CP Operational	
							1				CP in Power save	
		PWRSAV Power save mode powers down the clock generator.				0					System functional	
						1					Enable PWRSAV	
		PWRDN[1] Power Down places the decoder in a full power down mode.			0						System functional	Decoder is powered down when both PWRDN[0] and PWRDN[1] = 1
					1						Powered down if PWRDN[0] = 1	
		Reserved		0							Set to Zero	
		RESET Chip Reset will load all I2C bits with default values.	0								Normal orperation	Executing reset takes approx. 2ms. This bit is self clearing
			1								Start reset sequence	
0x10 Read	Status 1 Read only	**IN_LOCK** (STATUS_1[0])								x	In Lock (right now) =1	
		LOST_LOCK (STATUS_1[1])							x		Lost Lock (Since last read) =1	
		FSC_LOCK (STATUS_1[2])						x			Fsc Lock (right now) =1	
		FOLLOW_PW (STATUS_1[3])					x				Peak White AGC mode active =1	
		AD_RESULT[2:0], (STATUS_1[6:4] **)** AutoDetection Result reports the findings from the autodetection block.		0	0	0					NTSM-MJ	Detected Standard
				0	0	1					NTSC-443	
				0	1	0					PAL-M	
				0	1	1					PAL-60	
				1	0	0					PAL-BGHID	
				1	0	1					SECAM	
				1	1	0					PAL Combination N	
				1	1	1					SECAM 525	
		COL_KILL (STATUS_1[7] **)** Colour Kill	x								Colour Kill is active =1	

Table 20: User Map Details Register 0x11

Sub address	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x11 Read	Info Register Read Only	**IDENT[7:0]** Provides identification on the revision of the part.	x	x	x	x	x	x	x	x	ident = 0x01(ES1) ident = 0x02(ES2) ident = 0x04(ES3)	

Table 21: User Map Details Register 0x12 to 0x15

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x12 Read	Status Register 2 Read only	**MCVS DET** (STATUS_2[0])								x	MV Colour striping detected	1= detected
		MCVS T3 (STATUS_2[1])							x		MV Colour striping type	0=type2, 1=type3
		MV PS DET (STATUS_2[2])						x			MV Pseudo Sync detected	1= detected
		MV AGC (STATUS_2[3])					x				MV AGC pulses detected	1= detected
		LL NSTD (STATUS_2[4])				x					Non Standard line length	1= detected
		FSC NSTD (STATUS_2[5])			x						Fsc Frequency non standard	1= detected
		CP_FREE_RUN (STATUS_2[6]) Component processor is free running.		x							0=Valid Video signal found. 1=CP free running	
		TLLC PLL LOCK (STATUS_2[7]) True Line Lock clock PLL in lock	x								1=PLL Locked	Locked to input H_Syncs
0x13 Read	Status Register 3 Read only	**INST_HLOCK** (STATUS_3[0])								x	1=Horizontal lock achieved	Unfiltered
		GEMD (STATUS_3[1])							x		1= Gemstar data detected	
		SD_OP_50Hz (STATUS_3[2])						0			SD 60Hz detected	SD Field Rate Detect
								1			SD 50Hz detected	
		CVBS (STATUS_3[3])					x				Result of CVBS / Y/C autodetection	0 = Y/C 1 = CVBS signal
		FREE_RUN_ACT (STATUS_3[4])				x					1=Free Run mode Active	`Blue Screen` o/p
		STD FLD LEN			x						1=Field length standard	
		INTERLACE (STATUS_3[6])		x							1=Interlaced Video detected	
		PAL SW LOCK (STATUS_3[7])	x								1=Swinging Burst Detected	Reliable sequence
0x13 Write	Analogue Control Internal	Reserved								0	Set to Default	
		AA_FILT_HIGH_BW_EN Enable Anti-Aliasing Filter for High Frequency Modes							0		Disable	
									1		Enable	
		Reserved	0	0	0	0	0	0			Set to Default	
0x14	Analogue Clamp	Reserved					0	0	1	0	Set to default	
		CCLEN Current Clamp Enable				0					Current sources switched off	
						1					Current sources enabled	
		Reserved	0	0	0						Set to Default	
0x15	Digital Clamp	Reserved				0	x	x	x	x	Set to Zero	
		DCT[1:0] Digital Clamp Timing		0	0						Slow (TC: 1sec)	
				0	1						Medium (TC: 0.5sec)	
				1	0						Fast (TC:0.1sec)	
				1	1						TC dependant on Video	
		Reserved	0								Set to Zero	

Table 22: User Map Details Register 0x17

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x17 R/W	Shaping Filter Control	**YSFM[4:0]** Selects Y Shaping Filter Mode when in CVBS only mode. It allows the user to select a wide range of low pass and notch filters.				0	0	0	0	0	Auto Wide notch for poor quality sources or wide band filter with Comb for good quality input	Decoder selects optimum Y shaping filter depending on CVBS quality.
		If either Auto mode is selected the decoder selects the optimum Y filter depending on the CVBS video source quality (good v's bad).				0	0	0	0	1	Auto narrow notch for poor quality sources or wide band filter with Comb for good quality input	
						0	0	0	1	0	SVHS 1	If one of these modes is selected the deocder does not change filter modes depending on video quality, a fixed filter response (the one selected) is used for good and bad quality video.
						0	0	0	1	1	SVHS 2	
						0	0	1	0	0	SVHS 3	
						0	0	1	0	1	SVHS 4	
						0	0	1	1	0	SVHS 5	
						0	0	1	1	1	SVHS 6	
						0	1	0	0	0	SVHS 7	
						0	1	0	0	1	SVHS 8	
						0	1	0	1	0	SVHS 9	
						0	1	0	1	1	SVHS 10	
						0	1	1	0	0	SVHS 11	
						0	1	1	0	1	SVHS 12	
						0	1	1	1	0	SVHS 13	
						0	1	1	1	1	SVHS 14	
						1	0	0	0	0	SVHS 15	
						1	0	0	0	1	SVHS 16	
						1	0	0	1	0	SVHS 17	
						1	0	0	1	1	SVHS 18 (CCIR601)	
						1	0	1	0	0	PAL NN1	
						1	0	1	0	1	PAL NN2	
						1	0	1	1	0	PAL NN3	
						1	0	1	1	1	PAL WN 1	
						1	1	0	0	0	PAL WN 2	
						1	1	0	0	1	NTSC NN1	
						1	1	0	1	0	NTSC NN2	
						1	1	0	1	1	NTSC NN3	
						1	1	1	0	0	NTSC WN1	
						1	1	1	0	1	NTSC WN2	
						1	1	1	1	0	NTSC WN3	
						1	1	1	1	1	Reserved	
		CSFM[2:0] C Shaping Filter Mode allows the selection from a range of low pass chrominance filters. If either Auto mode is selected the decoder selects the optimum C filter depending on the CVBS video source quality (good v's bad). Non auto settings	0	0	0						Auto selection 1.5Mhz	Automatically selects a C filter
			0	0	1						Auto selection 2.17Mhz	
			0	1	0						SH1	Selects a C filter for all video standards and for good and bad video.
			0	1	1						SH2	
			1	0	0						SH3	
			1	0	1						SH4	
			1	1	0						SH5	
			1	1	1						Wide Band Mode	

Table 23: User Map Details Register 0x18 to 0x19

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register setting	Comment
0x18 R/W	Shaping Filter Control 2	**WYSFM[4:0]** Wideband Y Shaping Filter Mode allows the user to select which Y Shaping filter is used for the Y component of Y/C, YPbPr, B/W input signals and is also used when good quality input CVBS signal is detected. For all other inputs, the Y shaping filter chosen is controlled by YSFM[4:0].				0	0	0	0	0	Reserved Do Not Use	
						0	0	0	0	1	Reserved Do Not Use	
						0	0	0	1	0	SVHS 1	
						0	0	0	1	1	SVHS 2	
						0	0	1	0	0	SVHS 3	
						0	0	1	0	1	SVHS 4	
						0	0	1	1	0	SVHS 5	
						0	0	1	1	1	SVHS 6	
						0	1	0	0	0	SVHS 7	
						0	1	0	0	1	SVHS 8	
						0	1	0	1	0	SVHS 9	
						0	1	0	1	1	SVHS 10	
						0	1	1	0	0	SVHS 11	
						0	1	1	0	1	SVHS 12	
						0	1	1	1	0	SVHS 13	
						0	1	1	1	1	SVHS 14	
						1	0	0	0	0	SVHS 15	
						1	0	0	0	1	SVHS 16	
						1	0	0	1	0	SVHS 17	
						1	0	0	1	1	SVHS 18 (CCIR 601)	
						1	0	1	0	0	Reserved Do Not Use	
						~	~	~	~	~	Reserved Do Not Use	
						1	1	1	1	1	Reserved Do Not Use	
		Reserved		0	0						Set to Default	
		WYSFMOVR enables the use of automatic WYSFN filter selection.	0								Auto selection of best filter	
			1								Manual select filter using WYSFM[4:0]	
0x19 R/W	Comb Filter Control	**PSFSEL[1:0]** Control the signal bandwidth which is fed to the comb filters (PAL)							0	0	Narrow	
									0	1	Medium	
									1	0	Wide	
									1	1	Widest	
		NSFSEL[1:0] Control the signal bandwidth which is fed to the comb filters (NTSC)					0	0			Narrow	
							0	1			Medium	
							1	0			Medium	
							1	1			Wide	
		Reserved	1	1	1	1					Reserved set to 1	

Table 24: User Map Details Register 0x1D

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x1D R/W	Vertical Scale Value 1	Reserved			0	0	0	x	x	x	Set to 0	
		28MHz Crystal Mode		0							Use 27MHz Crystal	
				1							Use 28.63636MHz Crystal (Recommended configuration)	
		LLC Tristate	0								LLC Pin Active	
			1								LLC Pin Tristated	

Table 25: User Map Details Register 0x27 to 0x2C

Subaddres	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register setting	Comment
0x27 R/W	Pixel Delay Control	**LTA[1:0]** Luma timing adjust allows the user to specify a timing difference between chroma and luma samples.							0	0	No Delay	CVBS mode LTA[1:0] = 00b, S-Video mode LTA[1:0]= 01b, YPrPb mode
									0	1	Luma 1 clk(37nS) delayed	
									1	0	Luma 2 clk(74nS) early	
									0	1	Luma 1 clk(37nS) early	
		Reserved						0			Set to Zero	
		CTA[2:0] Chroma Timing Adjust allows a specified timing defference between the Luma and Chroma samples			0	0	0				Not valid setting	CVBS mode CTA[2:0] = 011b, S-Video mode CTA[2:0]= 101b, YPrPb mode CTA[2:0] = 110b
					0	0	1				Chroma+2 pixel (early)	
					0	1	0				Chroma+1 pixel (early)	
					0	1	1				No Delay	
					1	0	0				Chroma-1 pixel (late)	
					1	0	1				Chroma-2 pixel (late)	
					1	1	0				Chroma-3 pixel (late)	
					1	1	1				Not valid setting	
		AUTO_PDC_EN Automatically programs the LTA / CTA values so that luma and chroma aligned at output for all modes of operation.		0							Use values in LTA[1:0] and CTA[2:0] for delaying luma/chroma samples.	
				1							LTA and CTA values determined automatically	
		SWPC This bit allows the Cr and Cb samples to be swapped.	0								No swapping	See; SWAP_CR_CB_W
			1								Swap the Cr and Cb	
0x28 to 0x2A	Reserved	Reserved										
0x2B R/W	Misc Gain Control	**PW_UPD** Peak white update determines the rate of gain.								0	Update once per video line	Peak white must be enabled see LAGC[2:0]
										1	Update once per field	
		Reserved			1	0	0	0	0		Set to default	
		CKE Colour kill enable allows the colour kill function to be switched on and off.		0							Colour kill disabled	For SECAM colour kill threshold is set at 8%
				1							Colour kill enabled	see CKILLTHR[2:0]
		Reserved	1								Set to 1	
0x2C R/W	AGC Mode Control	**CAGC[1:0]** Chroma Automatic Gain Control selects the basic mode of operation for the AGC in the chroma path.							0	0	Manual Fixed gain	Use CMG[11:0]
									0	1	Use luma gain for chroma	
									1	0	Automatic gain	Based on colour burst
									1	1	Freeze chroma gain	
		Reserved					1	1			Set to default	
		LAGC[2:0] Luma Automatic Gain Control selects the mode of operation for the gain control in the luma path		0	0	0					Manual Fixed gain	Use LMG[11:0]
				0	0	1					AGC no override through white peak. Man IRE control	Blank level to sync tip
				0	1	0					AGC auto override through white peak. Man IRE control	Blank level to sync tip
				0	1	1					AGC no override through white peak. Auto IRE control	Blank level to sync tip
				1	0	0					AGC auto override through white peak. Auto IRE control	Blank level to sync tip
				1	0	1					AGC active video with white peak	
				1	1	0					AGC active video with average video.	
				1	1	1					Freeze gain	
		Reserved	1								Set to 1	

Table 26: User Map Details Register 0x2D to 0x33

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register setting	Comment
0x2D Write	Chroma Gain Control 1 Write Only	**CMG[11:8]** Chroma Manual Gain can be used to program a desired manual chroma gain. Reading back from this register in AGC mode gives the current gain setting					0	1	0	0	CAGC[1:0] settings will decide what mode CMG[11:0] operates in	
		Reserved			1	1					Set to Default	
		CAGT[1:0] Chroma Automatic Gain Timing allows adjustment of the Chroma AGC tracking speed	0	0							Slow (TC: 2 sec)	Will only have effect if CAGC[1:0] is set to auto gain (`10`)
			0	1							Medium (TC: 1 sec)	
			1	0							Fast (TC: 0.2 sec)	
			1	1							Adaptive	
0x2E Write	Chroma Gain Control 2 Write Only	**CMG[7:0]** Chroma Manual Gain lower 8-bits, see CMG[11:8] for discription	0	0	0	0	0	0	0	0	CMG[11:0] = 750dec the gain is 1 in NTSC CMG[11:0] = 741dec the gain is 1 in PAL	Min value is 0dec(G=-60db) Max value is 3750(Gain = 5)
0x2F Write	Luma Gain Control 1 Write Only	**LMG[11:8]** Luma Manual Gain can be used program a desired manual chroma gain or read back the actual used gain value					x	x	x	x	LAGC[1:0] settings will decide what mode LMG[11:0] operates in	
		Reserved			1	1					Set to One	
		LAGT[1:0] Luma Automatic Gain Timing allows adjustment of the Luma AGC tracking speed	0	0							Slow (TC: 2 sec)	Will only have effect if LAGC[1:0] is set to auto gain (001,010,011or 100)
			0	1							Medium (TC: 1 sec)	
			1	0							Fast (TC: 0.2 sec)	
			1	1							Dependent on VID_QUAL	
0x30 Write	Luma Gain Control 2 Write Only	**LMG[7:0]** Luma Manual Gain can be used to program a desired manual chroma gain or read back the actual used gain value	x	x	x	x	x	x	x	x	LMG[11:0] =1234dec the gain is 1 in NTSC LMG[11:0] = 1266dec the gain is 1 in PAL	Min value NTSC 1024 (G= 0.85) PAL (G=0.81) Max value NTSC = 2468(G = 2) & PAL = 2532 (G = 2)
0x31 R/W	VS & FIELD control 1	Reserved						0	1	0	Set to default	
		HVSTIM selects where within a line of video the VS signal is asserted.					0				Start of line relative to HSE	HSE=Hsync end
							1				Start of line relative to HSB	HSB=Hsync begin
		NEWAVMODE Sets the EAV/SAV mode				0					EAV/SAV codes generated to suit ADV	
						1					Manual VS/Field position controlled by registers 32h,33h,E5h-EAh	
		Reserved	0	0	0						Set to default	
0x32 R/W	Vsync Field control 2	Reserved			0	0	0	0	0	1	Set to default	
		VSBHE		0							VS goes high in middle of line (even field)	NEWAVMODE bit must be set high
				1							VS changes state at start of line (even field)	
		VSBHO	0								VS goes high in middle of line (odd field)	
			1								VS changes state at start of line (odd field)	
0x33 R/W	Vsync Field control 3	Reserved			0	0	0	1	0	0	Set to default	
		VSEHE		0							VS goes low in middle of line (even field)	
				1							VS changes state at start of line (even field)	
		VSEHO	0								VS goes low in middle of line (odd field)	
			1								VS changes state at start of line (odd field)	

Table 27: User Map Details Register 0x34 to 0x38

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x34 R/W	HS Position Control 1	**HSE[10:8]** HS End allows the positioning of the HS output within the video line									HS output ends HSE[10:0] pixels after falling edge of HSync	Using HSB & HSE the user can program the position and length of the output Hsync
								0	0	0		
		Reserved					0				Reserved set to 0	
		HSB[10:8] HS begin allows the positioning of HS output within the video line		0	0	0					HS output starts HSB[10:0] pixels after the falling edge of HSync	
		Reserved	0								Reserved set to 0	
0x35 R/W	HS Position Control 2	**HSB[7:0]** See above, using HSB[9:0] and HSE[9:0] the user can program the position and length of HS output signal	0	0	0	0	0	0	1	0		
0x36 R/W	HS Position Control 3	**HSE[7:0]** See above.	0	0	0	0	0	0	0	0		
0x37 R/W	Polarity	**PCLK** Sets the polarity of LLC1								0	Invert Polarity	
										1	Normal polarity as per timing diagrams	
		Reserved						0	0		Reserved set to 0	
		PF sets the FIELD polarity					0				Active High	
							1				Active Low	
		Reserved				0					Reserved set to 0	
		PVS sets the VS Polarity			0						Active High	
					1						Active Low	
		Reserved		0							Reserved set to 0	
		PHS sets HS Polarity	0								Active High	
			1								Active Low	
0x38 R/W	NTSC comb control	**YCMN[2:0]** Luma Comb Mode NTSC						0	0	0	Adaptive 3 Line 3 tap luma comb	
								1	0	0	Use Low pass notch	
								1	0	1	Fixed Luma Comb (2 Line)	Top lines of memory
								1	1	0	Fixed Luma Comb (3 Line)	All lines of memory
								1	1	1	Fixed Luma Comb (2 Line)	Bottom lines of mem
		CCMN[2:0] Chroma Comb Mode NTSC			0	0	0				3 line adaptive for CTAPSN =01 4 line adaptive for CTAPSN =10 5 line adaptive for CTAPSN =11	
					1	0	0				Disable Chroma Comb	
					1	0	1				fixed 2 line for CTAPSN =01 fixed 3 line for CTAPSN =10 fixed 4 line for CTAPSN =11	Top lines of memory
					1	1	0				fixed 3 line for CTAPSN =01 fixed 4 line for CTAPSN =10 fixed 5 line for CTAPSN =11	All lines of memory
					1	1	1				fixed 2 line for CTAPSN =01 fixed 3 line for CTAPSN =10 fixed 4 line for CTAPSN =11	Bottom lines of memory
		CTAPSN[1:0] Chroma Comb Taps NTSC	0	0							Not Used	
			0	1							adapts 3 lines ---2 lines	
			1	0							adapts 5 lines ---3 lines	
			1	1							adapts 5 lines ---4 lines	

Table 28: User Map Details Register 0x39

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x39 R/W	PAL comb control	**YCMP[2:0]** Luma Comb Mode PAL						0	0	0	Adaptive 5 Line 3 tap luma comb	
								1	0	0	Use Low pass notch	
								1	0	1	Fixed Luma Comb (3 Line)	Top lines of memory
								1	1	0	Fixed Luma Comb (5 Line)	All lines of memory
								1	1	1	Fixed Luma Comb (3 Line)	Bottom lines of mem
		CCMP[2:0] Chroma Comb Mode PAL			0	0	0				3 line adaptive for CTAPSN =01 4 line adaptive for CTAPSN =10 5 line adaptive for CTAPSN =11	
					1	0	0				Disable Chroma Comb	
					1	0	1				fixed 2 line for CTAPSN =01 fixed 3 line for CTAPSN =10 fixed 4 line for CTAPSN =11	Top lines of memory
					1	1	0				fixed 3 line for CTAPSN =01 fixed 4 line for CTAPSN =10 fixed 5 line for CTAPSN =11	All lines of memory
					1	1	1				fixed 2 line for CTAPSN =01 fixed 3 line for CTAPSN =10 fixed 4 line for CTAPSN =11	Bottom lines of mem
		CTAPSP[1:0] Chroma Comb Taps PAL	0	0							Not Used	
			0	1							adapts 5 lines ---2 lines (2 taps)	
			1	0							adapts 5 lines ---3 lines (3 taps)	
			1	1							adapts 5 lines ---4 lines (4 taps)	

Table 29: User Map Details Register 0x3A

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x3A R/W	ADC Control	**PWRDN_ADC_3** Enable powerdown of ADC3.								0	ADC3 normal operation	
										1	Powerdown ADC3	
		PWRDN_ADC_2 Enable powerdown of ADC2.							0		ADC2 normal operation	
									1		Powerdown ADC2	
		PWRDN_ADC_1 Enable powerdown of ADC1						0			ADC1 normal operation	
								1			Powerdown ADC1	
		PWRDN_ADC_0 Enable powerdown of ADC0					0				ADC0 normal operation	
							1				Powerdown ADC0	
		Reserved	0	0	0	0						

Table 30: User Map Details Register 0x3C to 0x49

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x3C R/W	TLLC CONTROL ANALOG	**PLL_QPUMP[2:0]** Manual PLL charge pump current settings						0	0	0	50uA	**See also Auto PLL Param Ctrl** register.
								0	0	1	100uA	
								0	1	0	150uA	
								0	1	1	250uA	
								1	0	0	350uA	
								1	0	1	500uA	
								1	1	0	750uA	
								1	1	1	1500uA	
		SOG_SYNC_LEVEL[4:0] embedded sync trigger level. Allows the setting of the analogue trigger threshold for the sync detection Vth=300mVxSOG_S_L[4:0] /32	0	1	0	1	1				Slice level set at 103mV above the lowest analog voltage level within the input video line	
0x3D R/W	Manual Window Control	Reserved					0	0	1	0	Set to Default	
		CKILLTHR[2:0] Sets the threshold at which color kill is enabled for PAL and NTSC. SECAM is fixed at 8%		0	0	0					kill at .5%	CKE = 1 enables the color kill function and must be enabled for CKILLTHR[2:0] to take effect
				0	0	1					kill at 1.5%	
				0	1	0					kill at 2.5%	
				0	1	1					kill at 4%	
				1	0	0					kill at 8.5%	
				1	0	1					kill at 16%	
				1	1	0					kill at 32%	
				1	1	1					Reserved	
		Reserved	1								Reserved set to 1	
0x3E to 0x40	Reserved	Reserved										
0x41 R/W	Resample Control	Reserved			0	0	0	0	0	1	Set to default	
		SFL_INV Controls the behaviour of the PAL switch bit		0							SFL compatible with ADV7190/91/94 encoders	
				1							SFL compatible with ADV717x encoders	
		Reserved	0								Set to Zero.	
0x42 to 0x47	Reserved	Reserved										
0x48 R/W	Gemstar Control 1	GDECEL[15:0] 16 individual enable bits that select the lines of video (even field lines 10-25) that the decoder checks for Gemstar compatible data										LSB= Line 10 MSB= Line 25 Default = Do not check for gemstar compatible data on any lines [10-25] in even fields
		GDECEL[15:8] see above	0	0	0	0	0	0	0	0		
0x49 R/W	Gemstar Control 2	**GDECEL[7:0]** see above	0	0	0	0	0	0	0	0		

Table 31: User Map Details Register 0x4A to 0x50

Subaddres	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x4A R/W	Gemstar Control 3	**GDECOL[15:0]** 16 individual enable bits that select the lines of video (odd field lines 10-25) that the decoder checks for Gemstar compatible data										LSB= Line 10 MSB= Line 25 Default = Do not check for gemstar compatible data on any lines [10-25] in odd fields
		GDECOL[15:8] see above	0	0	0	0	0	0	0	0		
0x4B R/W	Gemstar Control 4	**GDECOL[7:0]** see above	0	0	0	0	0	0	0	0		
0x4C R/W	Gemstar Control 5	**GDECAD** Controls the manor in which decoded Gemstar data is inserted into the horizontal								0	Split data into half byte	To avoid 00/ FF code
										1	Output in straight 8-bit format	
		Reserved	x	x	x	x	0	0	0		Reserved set to Zero	
0x4D R/W	CTI DNR control 1	**CTI_EN** CTI enable								0	Disable CTI	
										1	Enable CTI	
		CTI_AB_EN enables the mixing of the transient improved chroma							0		Disable CTI alpha blender	
									1		Enable CTI alpha blender	
		CTI_AB[1:0] controls the behaviour of the alpha-blend circuitry					0	0			Sharpest mixing	
							0	1			Sharp mixing	
							1	0			Smooth	
							1	1			Smoothest	
		Reserved				0					Set to Default	
		DNR_EN Enable or bypass the DNR block			0						Bypass the DNR block	
					1						Enable the DNR block	
		Reserved		1							Reserved set to 1	
		Reserved	1								Reserved set to 1	
0x4E R/W	CTI DNR control 2	**CTI_CTH[7:0]** Specifies how big the amplitude step must be to be steepened by the CTI block	0	0	0	0	1	0	0	0		
0x4F R/W	Reserved	Reserved										
0x50 R/W	CTI DNR control 4	**DNR_TH[7:0]** specifies the max. edge that will be interpreted as noise and therefore blanked	0	0	0	0	1	0	0	0		

Table 32: User Map Details Register 0x51

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x51 R/W	Lock Count	**CIL[2:0]** Count into Lock determines the number of lines that the system has to remain in lock before the system shows a locked status						0	0	0	1 Line of Video	Only operational for SDP modes
								0	0	1	2 Line of Video	
								0	1	0	5 Line of Video	
								0	1	1	10 Line of Video	
								1	0	0	100 Line of Video	
								1	0	1	500 Line of Video	
								1	1	0	1000 Line of Video	
								1	1	1	100000 Line of Video	
		COL[2:0] Count out of Lock determines the number of lines that the system has to remain out of lock before the system shows a lost locked status			0	0	0				1 Line of Video	
					0	0	1				2 Lines of Video	
					0	1	0				5 Lines of Video	
					0	1	1				10 Lines of Video	
					1	0	0				100 Lines of Video	
					1	0	1				500 Lines of Video	
					1	1	0				1000 Lines of Video	
					1	1	1				100000 Lines of Video	
		SRLS Select Raw Lock Signal selects the determination of the		0							Over field with verticle info	
				1							Line to Line evaluation	
		FSCLE Fsc Lock Enable	0								Lock Status set only by horizontal lock	FSCLE must be set to 0 in YPrPb mode if a reliable LOST_LOCK bit is
			1								Lock Status set by horizontal lock and subcarrier lock	

Table 33: User Map Details Register 0x52 to 0x58

Subaddres	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x52 R/W	CSC_1	A4[12:0] Contains the 13-bit offset for the A channel										CSC only available in CP modes See CSC section of the Hardware Manual for more details and programming examples
		A4[12:8] see A4[12:0] above				0	0	0	0	0		
		Reserved			0						Reserved set to Zero	
		CSC_SCALE bit allows to cater for coefficients which extend the supported range	0	0							No Scaling	
			0	1							2x scaling	
			1	0							Reserved	
			1	1							Reserved	
0x53 R/W	CSC_2	**A4[7:0]** see A4[12:0] above	0	0	0	0	0	0	0	0		
0x54 R/W	CSC_3	A3[12:0] Contains the 13-bit A3 coefficient for channel A										
		A3[12:6] see A3[12:0] above		0	0	0	0	0	0	0		
		Reserved	0								Reserved set to Zero	
0x55 R/W	CSC_4	A2[12:0] Contains the 13-bit A2 coefficient for channel A										
		A2[12:11] see A2[12:0] above							0	0		
		A3[5:0] see A3[12:0] above	0	0	0	0	0	0				
0x56 R/W	CSC_5	**A2[10:3]** see A2[12:0] above										
		A2[10:3] see A2[12:0] above	0	0	0	0	0	0	0	0		
0x57 R/W	CSC_6	A1[12:0] Contains the 13-bit A1 coefficient for channel A										
		A1[12:8] see A1[12:0] above				0	1	0	0	0		
		A2[2:0] see A2[12:0] above	0	0	0							
0x58 R/W	CSC_7	**A1[7:0]** see A1[12:0] above	0	0	0	0	0	0	0	0		

Table 34: User Map Details Register 0x59 to 0x66

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x59 R/W	CSC_8	B4[12:0] Contains the 13-bit offset for the B channel										CSC only available in CP modes See CSC section in this document for more details and programming examples
		B4[12:8] see B4[12:0] above				0	0	0	0	0		
		Reserved	0	0	0						Reserved set to Zero	
0x5A R/W	CSC_9	**B4[7:0]** see B4[12:0] above	0	0	0	0	0	0	0	0		
0x5B R/W	CSC_10	B3[12:0] Contains the 13-bit B3 coefficient for channel B										
		B3[12:6] see B3[12:0] above		0	0	0	0	0	0	0		
		Reserved	0								Reserved set to Zero	
0x5C R/W	CSC_11	B2[12:0] Contains the 13-bit B2 coefficient for channel B										
		B2[12:11] see B2[12:0] above							0	1		
		B3[5:0] see B3[12:0] above	0	0	0	0	0	0				
0x5D R/W	CSC_12	**B2[10:3]** see B2[12:0] above	0	0	0	0	0	0	0	0		
0x5E R/W	CSC_13	B1[12:0] Contains the 13-bit B1 coefficient for channel B										
		B1[12:8] see B1[12:0] above				0	0	0	0	0		
		B2[2:0] see B2[12:0] above	0	0	0							
0x5F R/W	CSC_14	**B1[7:0]** see B1[12:0] above	0	0	0	0	0	0	0	0		
0x60 R/W	CSC_15	C4[12:0] Contains the 13-bit offset for the C channel										
		C4[12:8] see C4[12:0] above				0	0	0	0	0		
		Reserved	0	0	0						Reserved set to Zero	
0x61 R/W	CSC_16	**C4[7:0]** see C4[12:0] above	0	0	0	0	0	0	0	0		
0x62 R/W	CSC_11	C3[12:0] Contains the 13-bit C3 coefficient for channel C										
		C3[12:6] see C3[12:0] above		0	1	0	0	0	0	0		
		Reserved	0								Reserved set to Zero	
0x63 R/W	CSC_17	C2[12:0] Contains the 13-bit C2 coefficient for channel C										
		C2[12:11] see C2[12:0] above							0	1		
		C3[5:0] see C3[12:0] above	0	0	0	0	0	0				
0x64 R/W	CSC_18	**C2[10:3]** see C2[12:0] above	0	0	0	0	0	0	0	0		
0x65 R/W	CSC_19	C1[12:0] Contains the 13-bit C1 coefficient for channel C										
		C1[12:8] see C1[12:0] above				0	0	0	0	0		
		C2[2:0] see C2[12:0] above	0	0	0							
0x66 R/W	CSC_20	**C1[7:0]** see C1[12:0] above	0	0	0	0	0	0	0	0		

Table 35: User Map Details Register 0x67 to 0x68

Sub addres	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x67 R/W	CSC_22	**INP_CSPACE[2:0]** This allows for automatic CSC selection.						0	0	0	Force RGB (Range 16-235) input	Used in conjunction with CSC_ALT_GAMA and RGB_OUT located in Reg 0x68
								0	0	1	Force RGB (Range 0-255) input	
								0	1	0	Force YCrCb input (601 color space)	
								0	1	1	Force YCrCb input (709 color space)	
								1	0	0	Force XVYCC 601	
								1	0	1	Force XVYCC 709	
								1	1	1	In Analog mode input colorspace depends on Primary Mode & Video Standard. In HDMI mode input color space depends on colorspace reported by HDMI block	
		DS_ONLY Enables downsampling (data dropping) only in DPP					0				Filter and downsanple	
							1				downsample only (no filtering)	
		SOFT_FILT DPP ChB/ChC decimation filter transition band selection				0					Steep roll-off in transition band	
						1					Shallow roll-off in transition band	
		EmbSyncOnAll Controls the agc target value based on the effects of equations on the syncs on Channel A.			0						Defaults to LO (SoY or SoG only).	Used in auto CSC mode only
					1						Expects sync embedded on all 3 inputs	
		Reserved	0	0							Set to default	
0x68 R/W	CSC_23	**CSC_ALT_GAMA** This bit is used in cunjunction with INP_CSPACE[2:0] and RGB_OUT bits to select the applaied CSC. Output YPrPb can be in the YPrPb601 or YPrPb709 formats, irrespective of the input format. If this bit is set, it gives an output that is in a different format from the input.								0	YPrPb601 output.	YPrPb601 input and RGB_OUT =0
											YPrPb709 output	YPrPb709 input and RGB_OUT =0
										1	YPrPb709 output.	YPrPb601 input and RGB_OUT =0
											YPrPb601 output	YPrPb709 input and RGB_OUT =0
		RGB_OUT This bit is used in conjunction with **INP_COLOR_SPACE[1:0]** and **CSC_ALT_GAMMA** bits to select the appaled CSC. Is sets up the output color space, the correct digital blank level and offsets for RGB or YPrPb output.							0		YPrPb Output	
									1		RGB Output	
		ALT_DATA_SAT Control to disable the data-saturator that limits the output range in dependantly of CP_OP_656_RANGE						0			Data-saturator setting (enabled/disabled) set according to OP_656_RANGE setting	
								1			Reverses OP_656_RANGE decision to enable or disable the data-saturator.	
		Reserved					x					
		CSC_COEFF_SEL[3:0] CSC automatic mode enable	0	0	0	0					CSC configuration in manual mode	
			0	0	0	1					Reserved	
			~	~	~	~					Reserved	
			1	1	1	0					Reserved	
			1	1	1	1					CSC configuration in automatic mode	

Table 36: User Map Details Register 0x69

Sub addres	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x69 R/W	Configure 1	**SDM_SEL[1:0]** Standard definition mode selection							0	0	as per INSEL[3:0]	
									0	1	CVBS on AIN11	
									1	0	Y/C on AIN10 and AIN12	
									1	1	CVBS Ain11,Y=Ain11, C=Ain12	CVBS,Y/C autodetect
		SWAP_CSC_COEFF Controls the DPP_CSC colorspace conversion configuration				0					By-pass DPP_CSC, CP_CSC	This bit is only valid if CP_CSC_EN is set to 1.
						1					DPP_CSC implaments a colorspace conversion.	
		CP_CSC_EN CP_CSC Enable Control				0					Disable CP_CSC	
						1					Enable CP_CSC	
		INV_DINCLK invert the Digital input clock			0						Invert	
					1						Normal	
		SYN_LOTRIG External Sync Input Trigger Level		0							3.3V trigger for HS/VS	Threshold aprox.1.5V
				1							1V trigger for HS/VS	Threshold aprox.0.6V
		TRI_LEVEL	0								Sync detection for bi-level sync	
			1								Sync detection for tri level sync	

Table 37: User Map Details Register 0x6A to 0x6C

Sub addres	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x6A R/W	TLLC Phase Adjust	**DLL_PH[4:0]** sets the ADC sampling point into 32 evenly spaced sampling points				0	0	0	0	0	Select Phase 0	Only use in CP RGB graphics modes. Backend IC should be used to determines optimum
						~	~	~	~	~		
						1	1	1	1	1	Select Phase 31	
		BYP_DLL allows the user to bypass the DLL block			0						ADC clock through DLL block	
					1						Bypass DLL block	
		PLL_DLL_UPD_VS_EN		0							PLL Divide Ratio and DLL Phase update immediately	
				1							PLL Divide Ratio and DLL Phase update with following Vsync	
		Reserved	0								Reserved set to Zero	
0x6B R/W	CP output selection	**CPOP_SEL[3:0]** This bit combines with DDR_2X_CLK, DDR_EN, CP_PREC[1:0] to determine the output format when in CP mode. (Refer to the Hardware Manual for detailed explanation)					0	0	1	0	Refer to the Hardware Manual for setting CPOP_SEL[3:0]	
		OP_656_RANGE This bit decides the output range of the digital data.				0					Output range is 0 to 255.	In HDMI mode: RGB (0-255) => Gain = 1 YUV(16-235) => Gain = 255/(235-16) = 1.164
												In Analog Mode: Gain = (255-0+1) x 16/1792
						1					Output range is 16 to 255.	In HDMI mode: RGB (0-255) => Gain = (235-16)/255 = 0.859 YUV(16-235) => Gain = 1
												In Analog Mode: Gain = (235-16+1) x 16/1792
		DE_OUT_SEL This bit selects either FIELD or DE output.			0						Field output selected	
					1						DE output selected	
		VS_OUT_SEL allows the switching of an active window		0							Field signal o/p on FIELD pin	
				1							VS output on the FIELD pin	
		HS_OUT_SEL allows the switching of a CSync output on	0								CSync o/p on the HS pin	
			1								HSync o/p on the HS pin	
0x6C R/W	CP Clamp1	CLMP_A[11:0] Manual Clamp for channel A, 12-bit value to be subtracted from the incoming video signal.									To change CLMP_A[11:0] value, registers 0x6C and 0x6D must be written to in this order with no I2C access in between.	
		CLMP_A[11:8] see CLMP_A[11:0] above					0	0	0	0		
		Reserved				1					Set to 1	
		CLMP_FREEZE stops the digital fine clamp loops, A, B & C from updating			0						Clamp loop operational	update every line
					1						Clamps stopped	No update
		CLMP_BC_MAN manual or automatic control of channels B and C. No individual control		0							Auto-determined by clamp loop	CLMP_BC_MAN bit must to set for CLMP_B[11:0] & CLMP_C[11:0] to be
				1							Manual-determined by CLMP_B[11:0] and CLMP_C[11:0]	
		CLMP_A_MAN manual or automatic control of channel A	0								Auto-determined by clamp loop	CLMP_A_MAN bit must to set for CLMP_A[11:0] to be active.
			1								Manual-determined by CLMP_A[11:0]	

Table 38: User Map Details Register 0x6D to 0x72

Subadress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x6D R/W	CP Clamp2	**CLMP_A[7:0]** see CLMP_A[11:0] above	0	0	0	0	0	0	0	0		
0x6E R/W	CP Clamp3	CLMP_B[11:0] Manual Clamp for channel B, 12-bit value to be subtracted from the incoming video signal.									To change CLMP_B[11:0] value, registers 0x6E and 0x6F must be written to in this order with no I2C access in between.	
		CLMP_B[11:4] see CLMP_B[11:0] above	0	0	0	0	0	0	0	0		
0x6F R/W	CP Clamp4	CLMP_C[11:0] Manual Clamp for channel C, 12-bit value to be subtracted from the incoming video signal.									To change CLMP_C[11:0] value, registers 0x6F and 0x70 must be written to in this order with no I2C access in between.	
		CLMP_C[11:8] see CLMP_C[11:0] above					0	0	0	0		
		CLMP_B[3:0] see CLMP_B[11:0] above	0	0	0	0						
0x70 R/W	CP Clamp5	**CLMP_C[7:0]** see CLMP_C[11:0] above	0	0	0	0	0	0	0	0		
0x71 R/W	CP AGC 1	**AGC_TIM[2:0]** AGC time constant						0	0	0	100 Lines	
								0	0	1	1 frame	
								0	1	0	.5 seconds	
								0	1	1	1 seconds	
								1	0	0	2 seconds	
								1	0	1	3 seconds	
								1	1	0	5 seconds	
								1	1	1	7 seconds	
		HS_NORM nominal Hsync depth selection					0				Scale as per 300mV Hsync	
							1				Scale as per 286mV Hsync	
		AGC FREEZE agc freeze enable				0					AGC loop operational	
						1					Freeze AGC loop	
		AGC_TAR_MAN manual target level enable			0						AGC scales to 300/286mV HSync	
					1						AGC scales to value AGC_TAR[9:0]	
		AGC_TAR[9:0] Manual target level set the target value for Sync depth after gain has been applied										
		AGC_TAR[9:8] see AGC_TAR[9:0]	0	0								
0x72 R/W	CP AGC 2	**AGC_TAR[7:0]** see AGC_TAR[9:0]	0	0	0	0	0	0	0	0		

Table 39: User Map Details Register 0x73 to 0x76

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x73 R/W	CP AGC 3	A_GAIN[9:0] manual gain value for channel A									To change A_GAIN[9:0] value, register 0x73 and 0x74 must be written to in this order with no I2C acces in between.	
		A_GAIN[9:4] see A_GAIN[9:0] next page			0	1	0	0	0	0		
		AGC_MODE_MAN switch control of gain operation mode from SSPD block to GAIN_MAN		0							Enable AGC based on SSPD decision	
				1							Gain operation controlled by GAIN_MAN	
		GAIN_MAN enable the gain factor to be set by the AGC or manually	0								Automatic Gain mode enabled	
			1								Manual gain mode set by A_GAIN[9:0], B_GAIN[9:0] and C_GAIN[9:0]	
0x74 R/W	CP AGC 4	B_GAIN[9:0] manual gain value for channel B									To change B_GAIN[9:0] value, register 0x74 and 0x75 must be written to in this order with no I2C acces in between.	
		B_GAIN[9:6] see B_GAIN[9:0] above					0	1	0	0		
		A_GAIN[3:0] see A_GAIN[9:0] on previous page	0	0	0	0						
0x75 R/W	CP AGC 5	C_GAIN[9:0] manual gain value for channel C									To change C_GAIN[9:0] value, register 0x75 and 0x76 must be written to in this order with no I2C acces in between.	
		C_GAIN[9:8] see C_GAIN[9:0] above							0	1		
		B_GAIN[5:0] see B_GAIN[9:0] above	0	0	0	0	0	0				
0x76 R/W	CP AGC 6	**C_GAIN[7:0]** see C_GAIN[9:0] above	0	0	0	0	0	0	0	0		

Table 40: User Map Details Register 0x77 to 0x7A

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x77 R/W	CP OFFSET1	A_OFFSET[9:0] Channel A offset **A_OFFSET[9:4]**									To change A_OFFSET[9:0] value, register 0x77 and 0x78 must be written to in this order with no I2C access in between	Set offsets accordingly for YPrPb or RGB mode. When A/B/C_OFFSET= 3FFh then that offset is determined automatically.
		A_OFFSET[9:4]			1	1	1	1	1	1		
		CP_PREC[1:0]	0	0							Rounds and Truncates data in Channels A, B & C to 10-bit precision	
			0	1							Rounds and Truncates data in Channels A, B & C to 12-bit precision	
			1	0							Rounds and Truncates data in Channels A, B & C to 8-bit precision	
			1	1							Determine the precision based on the CPOP_SEL[3:0] register.	
0x78 R/W	CP OFFSET2	B_OFFSET[9:0] Channel B offset									To change A_OFFSET[9:0] value, register 0x78 and 0x79 must be written to in this order with no I2C access in between	
		B_OFFSET[9:6]					1	1	1	1		
		A_OFFSET[3:0]	1	1	1	1						
0x79 R/W	CP OFFSET3	C_OFFSET[9:0] Channel C offset									To change A_OFFSET[9:0] value, register 0x79 and 0x7A must be written to in this order with no I2C access in between	
		C_OFFSET[9:8]							1	1		
		B_OFFSET[5:0]	1	1	1	1	1	1				
0x7A R/W	CP OFFSET4	**C_OFFSET[7:0]**	1	1	1	1	1	1	1	1		

Table 41: User Map Details Register 0x7B to 0x7C

Sub address	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x7B R/W	CP AV CONTROL	**DE_WITH_AVCODE** This bit control AV code insertion in relation to the DE output signal.								0	AV codes locked to default values. DE position can be moved independantly.	
										1	Iserted AV codes will move in relation to DE position change.	
		AV_CODE_EN allows the insertion of AV codes into the							0		Do not insert AV codes	
									1		Insert AV codes in the data stream	
		Reserved						1			Set to default	
		AV_BLANK_ENABLE sets the data output during blanking					0				Output clamped and gained data during the horizontal and vertical blanking periods	
							1				Replaces data in horizontal and vertical blanking period with default values	
		Reserved			0	0					Set to default	
		AV_INV_V Invert V bit in AV code		0							Insert V bit with default polarity	
				1							Invert V bit before Inserting	
		AV_INV_F Invert F bit in AV code	0								Insert F bit with default polarity	
			1								Invert F bit before Inserting	
0x7C R/W	CP HVF CONTROL 1	END_HS[9:0] End HS signal 10-bit 2`s complement number controlling the end of Hsync										e.g. 3F0=HS ends 16 llc early, 100h= HS ends 256 LLC1 late
		END_HS[9:8] see END_HS[9:0] above							0	0		
		START_HS[9:0] Start HS signal 10-bit 2`s complement number controlling the start of HS										e.g. 3FF=HSstarts 1 LLC1 early, 005h= HS starts 5 LLC1 late
		START_HS[9:8] see START_HS[9:0] above					0	0				
		PIN_INV_DE Invert polarity of DE outputsignal				0					DE active high	
						1					DE active low	
		PIN_INV_F Invert polarity of FIELD signal			0						Interlaced-low for odd, low for even. Progressive-permanently low	FIELD active high if selected
					1						Interlaced-high for odd, high for even. Progressive-permanently high	FIELD active low if selected
		PIN_INV_VS Invert polarity of HS signal		0							Positive polarity Vsync	
				1							Negative polarity Vsync	
		PIN_INV_HS Invert polarity of HS signal (or CSync if selected)	0								Positive polarity	
			1								Negative polarity	

Table 42: User Map Details Register 0x7D to 0x80

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x7D R/W	CP HVF CONTROL 2	**END_HS[7:0]** see END_HS[9:0] above	0	0	0	0	0	0	0	0		
0x7E R/W	CP HVF CONTROL 3	**START_HS[7:0]** see START_HS[9:0] above	0	0	0	0	0	0	0	0		
0x7F R/W	CP HVF CONTROL 4	**END_VS[3:0]** End VS signal 4-bit 2`s complement number controlling the end of VSync					0	0	0	0		e.g. 0x0E=VS ends 2 lines early, 0x01= VS ends 1 line late
		START_VS[3:0] Start VS signal 4-bit 2`s complement number controlling the start of VSync	0	0	0	0						e.g. 0x0F=VS starts 1 line early, 0x01= VS end 3 lines late
0x80 R/W	CP HVF CONTROL 5	**START_FO[3:0]** Start FIELD odd signal 4-bit 2`s complement number controlling the start of odd field output					0	0	0	0		e.g. 0x0F=FIELD starts 1 line early, 0x02= FIELD ends 2 lines late
		START_FE[3:0] Start FIELD even signal 4-bit 2`s complement number controlling the start of even field output	0	0	0	0						e.g. 0x0D=FIELD starts 3 lines early, 0x05= FIELD starts 5 lines later

Table 43: User Map Details Register 0x81 to 0x83

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x81 R/W	CP_REG_81	MEAS_WL[7:0] Measurement window start used for noise									Start value (in LLC clock cycles) of the measurement	
		MEAS_WL[11:8] see description above					1	0	1	0		
		GR_AV_BL_EN Embedded time code or/and data blanking insertion enable				0					Disable embedded time code or/and data blanking insertion enable	
						1					Enable embedded time code or/and data blanking insertion enable	
		Reserved			0						Set to default	
		MEAS_WL[1:0] Measurement window length used for noise measurement (refer to NOISE[7:0]) and calibration (refer to CALIB[10:0]	0	0							Window length is 128 LLC clock cycles	
			0	1							Window length is 64 LLC clock cycles	
			1	0							Window length is 32 LLC clock cycles	
			1	1							Window length is 16 LLC clock cycles	
0x82 R/W	CP_REG_82	**MEAS_WL[7:0]** see register 0x81	0	0	0	0	0	1	0	0		
0x83 R/W	CP_REG_83	ISD_THR[7:0] Threshold for SID measurement. A value o zero causes the threshold to be calculated automatically. The threshold is set to (calculated level of HSync tip) + 0x5 * (Calculated HSync depth)										
		ISD_THR[7:0] See description above	0	0	0	0	0	0	0	0		

Table 44: User Map Details Register 0x84 to 0x85

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x84	CP_NOISE_MEAS_4	**IFSD_AVG** ISD Averaging								0	ISD[8:0] is averaged over 128	Refer to IFSD[8:0] at
										1	ISD[8:0] is averaged over 256 lines of video to generate IFSD[8:0]	
		Reserved					1	1	0		Set to default	
		CP_GAIN_FILT[3:0] Filter selection option for manual gain	0	0	0	0					No filtering, i.e. coefficient A = 1	K = 1024
			0	0	0	1					Coefficient A = 1/128 lines	
			0	0	1	0					Coefficient A = 1/256 lines	
			0	0	1	1					Coefficient A = 1/512 lines	
			0	1	0	0					Coefficient A = 1/1024 lines	
			0	1	0	1					Coefficient A = 1/2048 lines	
			0	1	1	0					Coefficient A = 1/4096 lines	
			0	1	1	1					Coefficient A = 1/8192 lines	
			1	0	0	0					Coefficient A = 1/16K lines	
			1	0	0	1					Coefficient A = 1/32K lines	
			1	0	1	0					Coefficient A = 1/68K lines	
			1	0	1	1					Coefficient A = 1/128K lines	
			1	1	0	0					Reserved	
			~	~	~	~					Reserved	
			1	1	1	1					Reserved	
0x85 R/W	CP DETECTION CONTROL 1	**DS_OUT** digital sync output enable								0	output asynchronous VS / asynchronous HS	
										1	output synchronous VS / asynchronous CS	
		SSPD_CONT sync source and polarity detector continuous mode							0		one shot triggered by TRIG_SSPD	
									1		Detector in continous mode	
		TRIG_SSPD trigger sync source and polarity detector						0			0 to 1 transition will cause SSPD block to examine sync signals	Not self clearing needs to be reset by the user
		SYN_SRC[1:0] SSPD sync source selection				0	0				Autodetect mode for sync source	
						0	1				Manual, separate HS & VS	
						1	0				Manual, CS on HS/CS pin	
						1	1				Manual, sync on SOG/SOG	
		POL_HSCS manual overwrite for polarity of HS SSPD			0						HS/CS pin negative polarity (HS or CS)	For this bit to be active POL_MAN_EN=1
					1						HS/CS pin positive polarity (HS or CS)	
		POL_VS manual overwrite for polarity of VS SSPD		0							VS pin negative polarity	
				1							VS pin positive polarity	
		POL_MAN_EN manual overwrite for polarity detection	0								Use result from SSPD autodetection	
			1								Use POL_VS and POL_HS	

Table 45: User Map Details Register 0x86 to 0x8A

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x86 R/W	CP MISC CONTROL 1	Reserved								1	Reserved set to Zero	
		STDI_CONT standard identification continous							0		one shot triggered by TRIG_STDI	
									1		Detector in continous mode	
		TRIG_STDI trigger standard identification						0			0 to 1 transition triggers SDI measurement. Bit is not self clearing	
								1				
		Reserved					1				Set to 1	
		CPOP_INV_Crb Swap the interleaving of Cr and Cb in the output data stream				0					Output Cr & Cb interleaved	As per standard
						1					invert the order of Cr & Cb o/p	CPOP_SEL[3:0] set to 4:2:2 ouput format. No effect in 24-bit CP output format modes.
		Reserved	0	0	x						Reserved set to Zero	
0x87 R/W	CP TLLC CONTROL 1	**PLL_DIV_RATIO[11:0]** 12-bit multiplying factor that can be used in the sampling PLL									To change PLL_DIV_RATIO[11:0 value, register 0x87 and 0x88 must be written to in this order with no I2C access in between.	
		PLL_DIV_RATIO[11:8] see PLL_DIV_RATIO[11:0] above					0	0	1	1		
		Reserved		1	1	0					set to default	
		PLL_DIV_MAN_EN pll divide ratio manual enable	0								Auto-from PRIM_MODE[1:0] & VID_STD[3:0]	
			1								Use PLL_DIV_RATIO[11:0] as the multiplying factor	
0x88 R/W	CP TLLC CONTROL 2	**PLL_DIV_RATIO[7:0]** see PLL_DIV_RATIO[11:0] above	0	1	0	1	1	0	1	0		
0x89 R/W	CP TLLC CONTROL 3	Reserved	0	0	0	0	1	0	0	0	Set to Default	
0x8A R/W	CP TLLC CONTROL 4	Reserved				1	0	0	0	0	set to default	
		VCO_RANGE[1:0] manual PLL operating range		0	0						VCO center freq. 21Mhz . Max range 2.5Mhz to 27Mhz	For these settings to be active VCO_RANGE_MAN bit must be set to 1
				0	1						VCO center freq. 42Mhz . Max range 5Mhz to 55Mhz	
				1	0						VCO center freq. 85Mhz . Max range 10Mhz to 110Mhz	
				1	1						VCO center freq. 170Mhz . Max range 20Mhz to 220Mhz	
		VCO_RANGE_MAN Enable manual PLL operating range	0								Automatic VCO Range selection according to PRIM_MODE[1:0] and VID_STD[3:0]	
			1								PLL range from VCO_RANGE[1:0]	

Table 46: User Map Details Register 0x8B to 0x8E

Subadress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x8B R/W	CP DE Ctrl 1_58	**DE_H_END[9:0]** This register is used to vary the width of the picture by varying the end of the active region of the DE signal. This register is signed.										
		DE_H_END[9:8] Refer to description above.							0	0		
		DE_H_START[9:0] This register is used to vary the width of the picture by varying the start of the active region of the DE signal. This register is signed.										
		DE_H_START[9:8] Refer to description above.					0	0				
		IGNR_CLMP_VS_MAR[3:0] This register is used to set the number of lines -before and after leading edged of Vsync- for which clamping is disabled.	0	1	0	0						
0x8C R/W	CP DE Ctrl 2_59	**DE_H_END[7:0]** See DE_H_END[9:8] in register 0x8B	0	0	0	0	0	0	0	0		
0x8D R/W	CP DE Ctrl 3_60	**DE_H_START[7:0]** See DE_H_START[9:0] in register 0x8B	0	0	0	0	0	0	0	0		
0x8E R/W	CP DE Ctrl 4_61	**DE_V_END[3:0]** This register is used to vary the height of the picture by varying the end of the vbi region. This register is signed.										
		DE_V_END[3:0] See description above.					0	0	0	0		
		DE_V_START[3:0] This register is used to vary the height of the picture by varying the start of the vbi region. This register is signed.										
		DE_V_START[3:0] See description above.	0	0	0	0						

Table 47: User Map Details Register 0x8F to 0x90

Sub address	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x8F Write	Free Run Line Length 1 Write Only register	**FR_LL[10:0]** Free Run Line length Expected number of 28.63636MHz clock cycles in one line of video										Sets expected number of 28.63636MHz clock cycles for one line of video been processed in CP mode
		FR_LL[10:8] See FR_LL[10:0] above						0	0	0		
		Reserved					0				Set to default	
		LLC_PAD_SEL [2:0]		0	0	0					Automatic	
				1	1	1					Output Clock at twice data rate for data processed through the CP core only	
		Reserved	0								Set to default	
0x90 Read	Free Run Line Length 2 Write Only Details	**FR_LL[7:0]** See FR_LL[10:0] in register 0x8F	0	0	0	0	0	0	0	0		

Table 48: User Map Details Register 0x91 to 0x9D

Sub address	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x91 Write	DPP_CP_65 Write only register	Reseved	0								Set to default	
		INTERLACED Set the expected interlaced/progressive mode of the incoming video processed in CP mode. Note that this register is only used to configure the free run feature.		0							Progressive mode	
				1							Intelace mode	
		Reserved			0	1	x	x	x	x	Set to 010000	
0x91 Read	**WSS1[7:0]** wide screen signalling data. Read Only Register	WSS1[7:0]	x	x	x	x	x	x	x	x		
0x92 Read	**WSS2[7:0]** wide screen signalling data. Read Only Register	WSS2[7:0]	x	x	x	x	x	x	x	x	WSS2[7:6] are undetermined	
0x93 Read	**EDTV1[7:0]** EDTV data register. Read Only Register	EDTV1[7:0]	x	x	x	x	x	x	x	x		
0x94 Read	**EDTV2[7:0]** EDTV data register. Read Only Register	EDTV2[7:0]	x	x	x	x	x	x	x	x		
0x95 read	**EDTV3[7:0]** EDTV data register. Read Only Register	EDTV3[7:0]	x	x	x	x	x	x	x	x	EDTV3[7:6] are undetermined	EDTV3[5] reserved for future use
0x96 Read	**CGMS1[7:0]** CGMS data register. Read Only Register	CGMS1[7:0]	x	x	x	x	x	x	x	x		
0x97 Read	**CGMS2[7:0]** CGMS data register. Read Only Register	CGMS2[7:0]	x	x	x	x	x	x	x	x	CGMS3[7:4] are undetermined	
0x98 Read	**CGMS3[7:0]** CGMS data register. Read Only Register	CGMS3[7:0]	x	x	x	x	x	x	x	x		
0x99 Read	**CCAP1[7:0]** Closed caption data register. Read Only Register	CCAP1[7:0]	x	x	x	x	x	x	x	x		
0x9A Read	**CCAP2[7:0]** Closed caption data register. Read Only Register	CCAP2[7:0]	x	x	x	x	x	x	x	x		
0x9B Read	**Letterbox 1** Read Only Register	LB_LCT[7:0]	x	x	x	x	x	x	x	x	Reports number of black lines detected at top of active video	This feature examines the active video at the start and at the end of each field. It enables format detection even if the video is not accompanied by a
0x9C Read	**Letterbox 2** Read Only Register	LB_LCM[7:0]	x	x	x	x	x	x	x	x	Reports number of black lines detected in bottom half of active video if subtitles detected	
0x9D Read	**Letterbox 3** Read Only Register	LB_LCB[7:0]	x	x	x	x	x	x	x	x	Reports number of black lines detected at bottom of active video	

Table 49: User Map Details Register 0xA0 to 0xA3

Subaddres	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0xA0 Read	RB CP AGC1 Read Only Register	**CP_AGC_GAIN[9:0]** feedback value of the actual gain used on channel A										
		CP_AGC_GAIN[9:8]							x	x		
		Reserved	0	0	0	0	0	0				
0xA1 Read	RB CP AGC2 Read Only Register	**CP_AGC_GAIN[7:0]**	x	x	x	x	x	x	x	x		
0xA2 Read	RB CP Measure 1 Read Only Register	**NOISE[7:0]** Represent difference between maximum value and minimum value measured in window meaurement configured by MEAS_WS and MEAS_WL.										MEAS_WS is located in registers 0x81 and 0x82. MEAS_WL is located in register 0x81
		NOISE[7:0] See description above	x	x	x	x	x	x	x	x		
0xA3 Write	DDP_CP_81 Write Only Register	**CP_START_SAV[11:0]** Total number if pixels between start of non-active video and active video within a horizontal line of video										
		CP_START_SAV[3:0] LSBs of CP_START_SAV[11:0] control to set …..	0	0	0	0	0	0	0	0		
0xA3 Read	RB CP Measure 2 Read Only Register	**ISD[8:0]** Measurement of the area of the Horizontal synchronization that falls below the slicing threshold set by ISD_THR[7:0] in register 0x83									ISD[8] is located in Reg 0xE3. ISD[7:0] is located in Reg 0xE4.	
		ISD[8] See description above							0			
		IFSD[8:0] Average of the ISD[8:0]. See ISD_AVG bit for information on the average unction.									IFSD[8] is located in Reg 0xE3. ISFD[7:0] is located in Reg 0xE5.	
		IFSD[8] See description above								0		
		CALIB[10:0] calibration measurement feedback (average level over the extent of the window configured by MEAS_WS and MEAS_WL)									CALIB[10:8] is located in Reg 0xE3. CALIB[7:0] is located in Reg 0xE6.	MEAS_WS is located in registers 0x81 and 0x82. MEAS_WL is located in register 0x81
		CALIB[10:8] See description above				0	0	0				

Table 50: User Map Details Register 0xA3 to 0xA7

Subaddres	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0xA3 Write	DPP_CP_82 Write Only Register	**CP_START_SAV[3:0]** See description in Register 0xA3	0	0	0	0						
		CP_START_EAV[11:0] Total number if pixels between end of active video and start of active video									This register is optionally set in Auto Graphics mode (Refer to the Hardware Manual)	
		CP_START_EAV[11:8] See description above]					0	0	0	0		
0xA4 Read	RB measure 3 Read Only Register	**ISD[7:0]** See description in Register 0xA3	x	x	x	x	x	x	x	x		
0xA4 Write	DPP_CP_83	**CP_START_EAV[7:0]** See description in Register 0xA3	0	0	0	0	0	0	0	0		
0xA5 Read	RB measure 4 Read Only Register	**IFSD[7:0]** See description in Register 0xA3	x	x	x	x	x	x	x	x		
0xA5 Write	DPP_CP_84 Write Only Register	**CP_START_VBI[11:0]** Total number of lines at the start of a frame of non interlace standard. Or the total number of line at the start of an odd field of interlaced standard.									This register is optionally set in Auto Graphics mode (Refer to the Hardware Manual)	
		CP_START_VBI[11:4] See description above	0	0	0	0	0	0	0	0		
0xA6 Read	CP_REG_E6 Read Only Register	**CALIB[7:0]** See description in Register 0xA3	0	0	0	0	0	0	0	0		
0xA6 Write	DPP_CP_85 Write Only Register	**CP_START_VBI[3:0]** See decription in Register 0xA5	0	0	0	0						
		CP_END_VBI[11:0] Total number of lines at the start of a frame of non interlace standard. Or the total number of line at the start of an odd field of interlaced standard.									This register is optionally set in Auto Graphics mode (Refer to the Hardware Manual)	
		CP_END_VBI[11:8] See description above					0	0	0	0		
0xA7 Read	RB CP Hsync Dept 1 Read Only Register	HSD_CHA[9:0] Hsync depth channel A read back										
		HSD_CHA[9:8] See description above							x	x		
		HSD_CHB[9:0] Hsync depth channel B read back										
		HSD_CHB[9:8] See description above					x	x				
		HSD_CHC[9:0] Hsync depth channel C read back										
		HSD_CHC[9:8] See description above			x	x						
		Reserved	x	x								
0xA7 Write	DPP_CP_86 Write Only Register	**CP_END_VBI[7:0]** See description in Register 0xA6	0	0	0	0	0	0	0	0		

Table 51: User Map Details Register 0xA8 to 0xAC

Subaddres	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0xA8 Read	RB CP Hsync Dept 2 Read Only Register	**HSD_CHA[7:0]** See description in Register 0xA7	x	x	x	x	x	x	x	x		
0xA8 Write	DPP_CP_87 Write Only Register	**CP_START_VBI_EVEN[11:4]** The total number of line at the start of an even field of interlaced standard.									This register is optionally set in Auto Graphics mode (Refer to the Hardware Manual)	
		CP_START_VBI_EVEN[11:4] See description above	0	0	0	0	0	0	0	0		
0xA9 Read	RB CP Hsync Dept 3 Read Only Register	**HSD_CHB[7:0]** See description in Register 0xA6	x	x	x	x	x	x	x	x		
0xA9 Write	DPP_CP_85 Write Only Register	**CP_START_VBI_EVEN[3:0]** See description in Register 0xA8	0	0	0	0						
		CP_END_VBI_EVEN[11:8] The total number of line at the start of an even field of interlaced standard.									This register is optionally set in Auto Graphics mode (Refer to the Hardware Manual)	
		CP_END_VBI_EVEN[11:8] See description above.					0	0	0	0		
0xAA Read	RB CP Hsync Dept 4 Read Only Register	**HSD_CHC[7:0]** See description in Register 0xA6	x	x	x	x	x	x	x	x		
0xAA Write	DPP_CP_87 Write Only Register	**CP_END_VBI_EVEN[7:0]** See description in Register 0xA9	0	0	0	0	0	0	0	0		
0xAB Read	RB CP Hsync Dept 5 Read Only Register	**HSD_FB[11:0]** Hsync dept channel A read back (after gain multiplier)										
		HSD_FB[11:8] See description above.					x	x	x	x	2's complement number	
		Reserved	0	0	0	0						
0xAB Write	DPP_CP_90 Write Only Register	**CP_LCOUNT_MAX[11:4]** Control for the total number of line per frame expected by the CP. This register to be used for manual configuration of Free Run.										
		CP_LCOUNT_MAX[11:4] See description above	0	0	0	0	0	0	0	0		
0xAC Write	DPP_CP_90 Write only Register	**CP_LCOUNT_MAX[3:0]** See description in Register 0xAB	0	0	0	0						
		Reserved					x	x	x	x	Set to 0	
0xAC Read	RB CP Hsync Dept 6 Read Only Register	**HSD_FB[7:0]** See description in register 0xAB.	x	x	x	x	x	x	x	x		

Table 52: User Map Details Register 0xAD to 0xB5

Subaddress	Register	Bit Desciption	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0xAD Read	RB CP Peak Video 1 Read Only Register	PKV_CHA[9:0] peak video value on channel A read back										
		PKV_CHB[9:0] peak video value on channel B read back										
		PKV_CHC[9:0] peak video value on channel C read back										
		PKV_CHC[9:8]							x	x		
		PKV_CHB[9:8]					x	x				
		PKV_CHA[9:8]			x	x						
		Reserved	0	0								
0xAE Read	RB CP Peak Video 2 Read Only Register	**PKV_CHA[7:0]**	x	x	x	x	x	x	x	x		
0xAF Read	RB CP Peak Video 3 Read Only Register	**PKV_CHB[7:0]**	x	x	x	x	x	x	x	x		
0xB0 Read	RB CP Peak Video 4 Read Only Register	**PKV_CHC[7:0]**	x	x	x	x	x	x	x	x		
0xB1 Read	RB Standard Ident 1 Read Only Register	BL[13:0] block length readback, number of 28Mhz cycles in a block of 8 lines of input video										
		BL[13:8]			x	x	x	x	x	x		
		STDI_INTLCD		0							Non-Interlaced standard detected	
				1							Interlaced I/P standard detected	
		STDI_DVALID standard identification data valid read back. Indicates that the	0								BL, LCVS and LCF not valid	
			1								Valid BL, LCVS and LCF parameters	
0xB2 Write	RB Standard Ident 2 Write Only Register	Reserved							0	0	Reserved set to Zero	See CGMSD Address 90h, and CGMS1/2/3 Address 96h, 97h, 98h
		CRC_ENABLE Enable CRC checksum decoded from CGMS packet to validate CGMSD						0			Turn off CRC check.	
								1			CGMSD goes high with valid checksum	
		Reserved	0	0	0	1	1				Set as default	
0xB2 Read	RB Standard Ident 2 Read Only Register	**BL[7:0]**	x	x	x	x	x	x	x	x		
0xB3 Write	DPP_CP_98 Write Only Register	**CP_F_RUN_TH[2:0]** CP Free Run Threshold.						1	0	0	Default threshold	
		CP_FL_FR_THRESHOLD[1:0				1	0				Default threshold	
		Reserved	0	1	0						Set to default	
0xB3 Read	RB Standard Ident 3 Read Only Register	LCF[10:0] Number of lines in field.										
		LCVS[4:0] Number of lines in a Vsync period.										
		LCF[10:8]						x	x	x		
		LCVS[4:0]	x	x	x	x	x					
0xB4 Read	RB Standard Ident 4 Read Only Register	**LCF[7:0]**	x	x	x	x	x	x	x	x		
0xB5 Read	RB Standard Ident 5 Read Only Register	**CUR_SYNC[1:0]** current sync source selection SSPD read back							0	0	Invalid	
									0	1	Separate HS and VS sync on pins	
									1	0	Externl CS sync on HS_IN pin	
									1	1	Embedded SOG/SOY	
		Reserved						x				
		CUR_POL_HS currently detected polarity of HS_IN SSPD (CP)					1				HS_IN pin -negative polarity signal	
							0				HS_IN pin -positive polarity signal	
		HS_ACT activity of HS_IN SSPD (CP)				1					No activity detected	
						0					HS_IN pin carries an active signal	
		CUR_POL_VS currently detected polarity of VS SSPD			1						VS_IN pin -negative polarity	
					0						VS_IN pin -positive polarity signal	
		VS_ACT activity of VS _IN SSPD (CP)		1							No activity detected	
				0							HS_IN pin carries an active signal	
		SSPD_DVALID Valid Read back values	1								SSPD results not valid for read back	
			0								SSPD results valid	

Table 53: User Map Details Register 0xBA to 0xBD

Subaddres	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0xBA R/W	DPP_CP_105	**HDMI_FRUN_EN** HDMI Free Run Enable								0	Disable free run in HDMI mode	
										1	Enable free run in HDMI mode	
		HDMI_FRUN_MODE HDMI Free Run Mode							0		HDMI free run Mode 0 (Free Run when TMDS clock is not detected on active HDMI port)	
									1		HDMI free run Mode 1 (Free run when TMDS clock is not detected on active HDMI port or if an expected video mode is not detected by the STDI section)	
				0	1	0	0	x				
		ADC_HDMI_SIMULTANEOUS_MODE Controls the HDMI & Analog similutaneous mode.	0								Disable Simultaneous Mode	
			1								Enable Simultaneous Mode	
0xBC Read	DDP_CP_107 Read-only	**CSC_COEFF_SEL_RB[3:0]** Read back for CSC automatic mode	0	0	0	0					Reserved	
			0	0	0	1					YPbPr 601 [16-235] to RGB[16-235]	
			0	0	1	0					YPbPr 601 [16-235] to RGB[0-255]	
			0	0	1	1					YPbPr 709 [16-235] to RGB[16-235]	
			0	1	0	0					YPbPr 709 [16-235] to RGB[0-255]	
			0	1	0	1					RGB [16-235] to YPbPr601[16-235]	
			0	1	1	0					RGB [0-255] to YPbPr601 [16-235]	
			0	1	1	1					RGB [16-235] to YPbPr709 [16-235]	
			1	0	0	0					RGB [0-255] to YPbPr709 [16-235]	
			1	0	0	1					YPbPr 709 to YPbPr601 [16-235]	
			1	0	1	0					YPbPr 601 to YPbPr[16-235]	
			1	0	1	1					Reserved	
			~	~	~	~					Reserved	
			1	1	1	1					Reserved	
0xBD R/W	CP_Register_BD	Reserved					1	0	1	1	Set to default	
		DPP_BYPASS_EN				0					Do not bypass the DPP block	
						1					Bypass the DPP block	
		Reserved	0	0	0						Set to default	

Table 54: User Map Details Register 0xBF to 0xC2

Subaddres	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0xBF R/W	CP DEF COL 1	**CP_FORCE_FREERUN** Force Free Run								0	Do not force free run	
										1	Force free run	
		CP_DEF_COL_AUTO automatic output of default colours							0		Disable auto insertion of default color when free-run conditions are met.	
									1		Output default colours when free-run conditions are met	
		CP_DEF_COL_MAN_VAL enable manual selection of default colours						0			Use default colour blue	
								1			Output user programmable value	CP_DEF_COL_CHA/B/C[7:0] define the user programmable color.
		Reserved					x				Set to 0	
		Reserved				1					Set to 1	
		CP_HCOUNT_ALIGN_ADJ	0	0	0						Do not adjust Hcount	
			0	0	1						Add 1 clock	
			0	1	0						Add 2 clocks	
			0	1	1						Add 3 clocks	
			1	0	0						Reserved	
			1	0	1						Subtract 1 clock	
			1	1	0						Subtract 2 clocks	
			1	1	1						Subtract 3 clocks	
0xC0 R/W	CP DEF COL 2	**DEF_COL_CHA[7:0]** manual default colour channel A for free-run output.	x	x	x	x	x	x	x	x		
0xC1 R/W	CP DEF COL 3	**DEF_COL_CHB[7:0]** manual default colour channel B for free-run output.	x	x	x	x	x	x	x	x		
0xC2 R/W	CP DEF COL 4	**DEF_COL_CHC[7:0]** manual default colour channel C for free-run output.	x	x	x	x	x	x	x	x		

Table 55: User Map Details Register 0xC3 to 0xC4

Subaddres	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0xC3 R/W	ADC SWITCH 1	**ADC0_SW[3:0]** manual muxing control for ADC0					0	0	0	0	No connection	SETADC_sw_man_en = 1
							0	0	0	1	Ain1	
							0	0	1	0	Ain2	
							0	0	1	1	Ain3	
							0	1	0	0	Ain4	
							0	1	0	1	Ain5	
							0	1	1	0	Ain6	
							0	1	1	1	No connection	
							1	0	0	0	No connection	
							1	0	0	1	Ain7	
							1	0	1	0	Ain8	
							1	0	1	1	Ain9	
							1	1	0	0	Ain10	
							1	1	0	1	Ain11	
							1	1	1	0	Ain12	
							1	1	1	1	No connection	
		ADC1_SW[3:0] manual muxing	0	0	0	0					No connection	
			0	0	0	1					No connection	
			0	0	1	0					No connection	
			0	0	1	1					Ain3	
			0	1	0	0					Ain4	
			0	1	0	1					Ain5	
			0	1	1	0					Ain6	
			0	1	1	1					No connection	
			1	0	0	0					No connection	
			1	0	0	1					No connection	
			1	0	1	0					No connection	
			1	0	1	1					Ain9	
			1	1	0	0					Ain10	
			1	1	0	1					Ain11	
			1	1	1	0					Ain12	
			1	1	1	1					No connection	
0xC4 R/W	ADC SWITCH 2	**ADC2_SW[3:0]** manual muxing control for ADC2					0	0	0	0	No connection	SETADC_sw_man_en = 1
							0	0	0	1	No connection	
							0	0	1	0	Ain2	
							0	0	1	1	No connection	
							0	1	0	0	Ain 4	
							0	1	0	1	Ain5	
							0	1	1	0	Ain6	
							0	1	1	1	No connection	
							1	0	0	0	No connection	
							1	0	0	1	No connection	
							1	0	1	0	Ain8	
							1	0	1	1	No connection	
							1	1	0	0	No connection	
							1	1	0	1	Ain11	
							1	1	1	0	Ain12	
							1	1	1	1	No connection	
		Reserved			0	0					Set to default.	
		SOG_SEL selects the routing of the analogue sync stripper		0							Sync stripper connected to SOY	
				1							Sync stripper connected to SOG	
		ADC_SW_MAN _EN enable manual setting of the input signal muxing	0								Disable	
			1								Enable	

Table 56: User Map Details Register 0xC5 to 0xCB

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0xC5 R/W	CP Clamp Pos HS Ctrl1	Reserved					0	0	0	1	Set to default	
		EXT_VCLAMP_REGEN This bit controls the external clamp mode, selecting between regeneration and non regeneration mode.				0					Non regeneration mode, clamp controlled directly with external clamp pulse.	
						1					Regeneration mode clamp controlled with the external clamp pulse regenerated internally.	
		Reserved			0						Set to default.	
		CP Clamp Average Factor	0	0							No Averaging	
			0	1							Averaging with A =1/8	
			1	0							Averaging with A =1/16	default
			1	1							Averaging with A =1/32	
0xC6 to 0xC8	Reserved	Reserved										
0xC9 R/W	DDR Mode	**DPP_CP_BYPASS**								0	Data is processed by the DPP and CP blocks	
										1	Data bypasses the DPP and CP blocks.	
		EXT_CLK_EN							0		Do not use an external clock to ADCs for sampling.	
									1		Use an external clock to ADCs for sampling.	Used in External Clock and Clamp Mode
		DDR I2C RC FIRST						0			Red component out Last	12 bit DDR mode
								1			Red component out first	
		DDR EN					0				DDR Mode Disabled	
							1				DDR Mode Enabled	
		DDR_2X_CLK enables a 2x clk from the HDMI section				0					Clk disabled	Should only be used for HDMI i/ps
						1					Clk enabled	
		Reserved	0	0	0						Reserved set to Zero	
0xCA R/W	Field Length Count 1 Read Only Register	FCL[12:0] The number of 28MHz clock cycles between sucessive VSYNCS										
		FCL[12:8] See FCL[12:0] above				x	x	x	x	x		
		Reserved	x	x	x							
0xCB Read	Field Length Count 2 Read Only Register	**FCL[7:0]** See FCL[12:0] above	x	x	x	x	x	x	x	x		

Table 57: User Map Details Register 0xDC to 0xE4

Subaddres	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0xDC R/W	Letterbox Contorl 1	**LB_TH [4:0]** Set the threshold value which will detect a black line				0	1	1	0	0	Default threshold for detection of black lines.	
		Reserved	1	0	1						Reserved set to Zero	
0xDD R/W	Letterbox Control 2	**LB_EL[3:0]** programme the end line of the activity window for LB detection (end of field).					1	1	0	0	LB detection ends with last line of active video on a field. 1100: 262/525	
		LB_SL[3:0] programme the start line of the activity window for LB detection (start of field).	0	1	0	0					Letterbox detection aligned with start of active video. 0100: 23/286 NTSC	
0xDE Read	ST Noise Readback 1 Read Only Register	**ST_NOISE[10:0]** Noise measurement.										
		ST_NOISE[10:8] See ST_NOISE[10:0] above						x	x	x		
		ST_NOISE_VLD					0				ST_Noise[10:0] measurement is not valid	
							1				ST_Noise[10:0] measurement is valid	
		Reserved	x	x	x	x						
0xDF Read	ST Noise Readback 2 Read Only Register	**ST_NOISE[7:0]** See ST_NOISE[10:0] above	x	x	x	x	x	x	x	x		
0xE1 R/W	SD Offset Cb	**SD_OFF_CB [7:0]** adjust hue by selecting offset for Cb channel	1	0	0	0	0	0	0	0		
0xE2 R/W	SD Offset Cr	**SD_OFF_CR [7:0]** adjust hue by selecting offset for Cr channel	1	0	0	0	0	0	0	0		
0xE3 R/W	SD Saturation Cb	**SD_SAT_CB [7:0]** adjust saturation of picture by affecting gain on Cb channel	1	0	0	0	0	0	0	0	Chroma gain =0dB	
0xE4 R/W	SD Saturation Cr	**SD_SAT_CR [7:0]** adjust saturation of picture by affecting gain on Cr channel	1	0	0	0	0	0	0	0	Chroma gain =0dB	

Table 58: User Map Details Register 0xE5 to 0xEA

Subadress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Settin	Comment
0xE5 R/W	NTSC V bit begin	**NVBEG[4:0]** how many lines after lcount rollover to set V high				0	0	1	0	1	NTSC Default (BT.656)	
		NVBEGSIGN			0						Set to low when manual programming	
					1						Not suitable for user programming	
		NVBEGDELE Delay V bit going		0							No delay	
		high by one line relative to		1							Additional delay by 1 line	
		NVBEGDELO Delay V bit	0								No delay	
		going high by one line relative to	1								Additional delay by 1 line	
0xE6 R/W	NTSC V bit end	**NVEND[4:0]** how many lines after lcount rollover to set V low				0	0	1	0	0	NTSC Default (BT.656)	
		NVENDSIGN			0						Set to low when manual programming	
					1						Not suitable for user programming	
		NVENDDELE Delay V bit going		0							No delay	
		low by one line relative to		1							Additional delay by 1 line	
		NVENDDELO Delay V bit	0								No delay	
		going low by one line relative to	1								Additional delay by 1 line	
0xE7 R/W	NTSC F bit toggle	**NFTOG[4:0]** how many lines after lcount rollover to toggle F signal				0	0	0	1	1	NTSC Default (BT.656)	
		NFTOGSIGN			0						Set to low when manual programming	
					1						Not suitable for user programming	
		NFTOGDELE Delay F transition		0							No delay	
		by one line relative to NFTOG		1							Additional delay by 1 line	
		NFTOGDELO Delay F	0								No delay	
		transition by one line relative to	1								Additional delay by 1 line	
0xE8 R/W	PAL V bit begin	**PVBEG[4:0]** how many lines after lcount rollover to set V high										
						0	0	1	0	1	PAL Default (BT.656)	
		PVBEGSIGN			0						Set to low when manual programming	
					1						Not suitable for user programming	
		PVBEGDELE Delay V bit going		0							No delay	
		high by one line relative to		1							Additional delay by 1 line	
		PVBEGDELO Delay V bit going	0								No delay	
		high by one line relative to	1								Additional delay by 1 line	
0xE9 R/W	PAL V bit end	**PVEND[4:0]** how many lines after lcount rollover to set V low				1	0	1	0	0	PAL Default (BT.656)	
		PVENDSIGN			0						Set to low when manual programming	
					1						Not suitable for user programming	
		PVENDDELE Delay V bit going		0							No delay	
		low by one line relative to		1							Additional delay by 1 line	
		PVENDDELO Delay V bit going	0								No delay	
		low by one line relative to	1								Additional delay by 1 line	
0xEA R/W	PAL F bit toggle	**PFTOG[4:0]** how many lines after lcount rollover to toggle F signal				0	0	0	1	1	PAL Default (BT.656)	
		PFTOGSIGN			0						Set to low when manual programming	
					1						Not suitable for user programming	
		PFTOGDELE Delay F transition		0							No delay	
		by one line relative to PFTOG		1							Additional delay by 1 line	
		PFTOGDELO Delay F transition	0								No delay	
		by one line relative to PFTOG	1								Additional delay by 1 line	

Table 59: User Map Details Register 0xEB to 0xEC

Subadress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0xEB R/W	V Blank Control 1	**PVBIELCM[1:0]** PAL VBI Even Field Line Control							0	0	VBI ends 1 line earlier (Line 335)	Controls position of first active (comb filtered) line after VBI on Even field in **PAL**
									0	1	ITU-R BT.470 Compliant(Line 336)	
									1	0	VBI ends 1 line later (Line 337)	
									1	1	VBI ends 2 lines later (Line 338)	
		PVBIOLCM[1:0] PAL VBI Odd Field Line Control					0	0			VBI ends 1 line earlier (Line 22)	Controls position of first active (comb filtered) line after VBI on Odd field in
							0	1			ITU-R BT.470 Compliant (Line23)	
							1	0			VBI ends 1 line later (Line 24)	
							1	1			VBI ends 2 lines later (Line 25)	
		NVBIELCM[1:0] NTSC VBI Even Field Line Control			0	0					VBI ends 1 line earlier (Line 282)	Controls position of first active (comb filtered) line after VBI on Even field
					0	1					ITU-R BT.470 Compliant (Line 283)	
					1	0					VBI ends 1 line later (Line 284)	
					1	1					VBI ends 2 lines later (Line 285)	
		NVBIOLCM[1:0] NTSC VBI Odd Field Line Control	0	0							VBI ends 1 line earlier (Line 20)	Controls position of first active (comb filtered) line after VBI on Odd field in
			0	1							ITU-R BT.470 Compliant (Line21)	
			1	0							VBI ends 1 line later (Line 22)	
			1	1							VBI ends 2 lines later (Line 23)	
0xEC R/W	V Blank Control 2	**PVBIECCM[1:0]** PAL VBI Even field Colour control							0	0	Colour output beginning line 335	Controls the position of first line which outputs colour after VBI on Even Field in **PAL**
									0	1	Colour output beginning line 336 ITU-R BT470 Compliant	
									1	0	Colour output beginning line 337	
									1	1	Colour output beginning line 338	
		PVBIOCCM[1:0] PAL VBI Odd field Colour control					0	0			Colour output beginning line 22	Controls the position of first line which outputs colour after VBI on Odd Field in **PAL**
							0	1			Colour output beginning line 23 ITU-R BT470 Compliant	
							1	0			Colour output beginning line 24	
							1	1			Colour output beginning line 25	
		NVBIECCM[1:0] NTSC VBI Even Field Colour Control			0	0					Colour output beginnng line 282	Controls the position of first line which outputs colour after VBI on Even Field in **NTSC**
					0	1					Colour output beginning line 283 ITU-R BT470 compliant	
					1	0					Colour output beginning line 284	
					1	1					Colour output beginning line 285	
		NVBIOCCM[1:0] NTSC VBI Odd Field Colour Control	0	0							Colour output beginnng line 20	Controls the position of first line which outputs colour after VBI on Odd Field in **NTSC**
			0	1							Colour output beginning line 21 ITU-R BT470 compliant	
			1	0							Colour output beginning line 22	
			1	1							Colour output beginning line 23	

Table 60: User Map Details Register 0xED to 0xEF

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0xED Write	FB_CONTROL 1 Write Only register	**FB_MODE[1:0]** PAL VBI Even field Colour control							0	0	Static Switch mode - Full RGB or Full CVBS data	
									0	1	Fixed Alpha Blending - See MAN_ALPHA_VAL[6:0]	
									1	0	Dynamic Switching (Fast Mux)	
									1	1	Dynamic Switching with edge enhancement	
		CVBS_RGB_SEL						0			CVBS Source	Selects either CVBS or RGB to be O/P
								1			RGB Source	
		FB_INV					0				FB pin active High	
							1				FB pin active Low	
		Reserved	0	0	0	1						
0xED Read	FB_STATUS Read Only register	Reserved					x	x	x	x		
		FB_STATUS[3:0] Provides information on the status of the FB pin										
		FB_STATUS[0]				x					FB_RISE, 1 = there has beeen a rising edge on FB pin since last I2C read	Self Clearing Bit
		FB_STATUS[1]			x						FB_FALL, 1 = there has been a falling edge on FB pin since last I2C read	Self Clearing Bit
		FB_STATUS[2]		x							FB_STAT, Instantaneous value of FB signal at time if I2C read	
		FB_STATUS[3]	x								FB_HIGH, Indicates that the FB signal gas gone high since the las read of this register	Self Clearing Bit
0xEE R/W	FB_CONTROL 2	**MAN_ALPHA_VAL[6:0]** Determines in what proportion the video from the CVBS source and the RGB source are blended		0	0	0	0	0	0	0	0d = 100% CVBS signal 32d = 50% CVBS, 50% RGB 64d = 100% RGB	FB_MODE[1:0] = 01b (Fixed alpha blending selected)
		FB_CSC_MAN	0								Automatic configuration of the CSC for SCART support	CSC is used to convert RGB porion of SCART signal to
			1								Enable manual programming of CSC	
0xEF R/W	FB_CONTROL 3	**FB_EDGE_SHAPE[2:0]**						0	0	0	No Edge Shaping	Improves picture transition for high speed fast blank switching
								0	0	1	Level 1 Edge Shaping	
								0	1	0	Level 2 Edge Shaping	
								0	1	1	Level 3 Edge Shaping	
								1	0	0	Level 4 Edge Shaping	
		CNTR_ENABLE					0				Contrast Reduction mode disabled, FB signal is interpreted as a binary signal	
							1				Contrast Reduction mode enabled, FB signal is interpreted as a tri-level signal	
		FB_SP_ADJUST[3:0]	0	1	0	0					Adjusts FB timing in reference to the sampling clock	Each LSB corresponds to 1/8 of an ADC clock cycle

Table 61: User Map Details Register 0xF0 to 0xF1

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0xF0 R/W	FB_CONTROL 4	**FB_DELAY[3:0]**					0	0	1	1	Delay on FB signal in 28MHz clock cycles	
		Reserved	0	1	0	0					Set to default	
0xF1 R/W	FB_CONTROL 5	**RGB_IP_SEL**								0	SD RGB input for FB on AIN 7, AIN8 & AIN9	
										1	SD RGB input for FB on AIN4, AIN5 & AIN6	
		CNTR_MODE[1:0]									Contrast reduction threshold	
		Allows adjustment of contrast						0	0		25%	
		level in the contrast reduction box						0	1		50%	
								1	0		75%	
								1	1		100%	
		FB_LEVEL[2:0]									Fast Blank threshold (V)	
		Controls Reference Level for Fast			0	0	0				0.4	
		Blank Comparator			0	0	1				0.7	
					0	1	0				0.9	
					0	1	1				1.1	
					1	0	0				1.3	
					1	0	1				1.7	
					1	1	0				2.2	
					1	1	1				2.7	
											Contrast reduction threshold	
		CNTR_LEVEL[1:0]	0	0							0.4	
		Controls Reference Level for	0	1							0.7	
		Contrast Reduction Comparator	1	0							0.9	
			1	1							1.1	

Table 62: User Map Details Register 0xF3 to 0xF4

Sub address	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0xF3 R/W	AFE_CONTROL 1	**AA_FILT_EN[0]**								0	Disables the internal anti-aliasing filter on channel 0	
										1	Enables the internal anti-aliasing filter on channel 0	
		AA_FILT_EN[1]							0		Disables the internal anti-aliasing filter on channel 1	
									1		Enables the internal anti-aliasing filter on channel 1	
		AA_FILT_EN[2]						0			Disables the internal anti-aliasing filter on channel 2	
								1			Enables the internal anti-aliasing filter on channel 2	
		Reserved					0					
		ADC3_SW[3:0] manual muxing control for ADC3	0	0	0	0					No connection	
			0	0	0	1					No connection	
			0	0	1	0					No connection	
			0	0	1	1					No connection	
			0	1	0	0					Ain4	
			0	1	0	1					No connection	
			0	1	1	0					No connection	
			0	1	1	1					No connection	
			1	0	0	0					No connection	
			1	0	0	1					Ain7	
			1	0	1	0					No connection	
			1	0	1	1					No connection	
			1	1	0	0					No connection	
			1	1	0	1					No connection	
			1	1	1	0					No connection	
			1	1	1	1					No connection	
0xF4 R/W	Drive Strength	**DR_STR_S[1:0]** Select the drive strength of the sync signals HS,VS and F, can be increased or decreased for EMC or cross-talk reasons.							0	0	Reserved	
									0	1	Medium low (2x) for LLC1 up to 60MHz	
									1	0	Medium high (3x) for LLC1 from 55MHz to 105MHz	
									1	1	High drive strength (4x) for LLC1 greater than 100MHz	
		DR_STR_C[1:0] Select the strength of the clock signal output driver, can be increased or decreased for EMC or cross-talk					0	0			low drive strength (1x)	
							0	1			medium low (2x)	
							1	0			medium high (3x)	
							1	1			high drive strength (4x)	
		DR_STR[1:0] Drive Strength of data output drivers. Can be increased or decreased for EMC or cross-talk reasons.			0	0					Low Drive 1X	Recommended
					0	1					Medium Low 2X	
					1	0					Medium High 3X	
					1	1					High Drive 4X	
		AA_FILT_PROG_BW[1:0] BW of the antialias filter is programmables through these bits									**-1.2dB F_c (MHz)**	**-3dB F_c**
			0	0							6	10
			0	1							8	13.3
			1	0							10	16.6
			1	1							13	21.6

Table 63: User Map Details Register 0xF9 to 0xFE

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0xF9 R/W	VS Mode Control	**EXTEND_VS_MAX_FREQ**								0	Limit Maximum Vsync frequency to 66.25Hz (475 lines/frame)	
										1	Limit Maximum Vsync frequency to 70.09Hz (449 lines/frame)	
		EXTEND_VS_MIN_FREQ							0		Limit Minimum Vsync frequency to 42.75Hz (731 lines/frame)	
									1		Limit Minimum Vsync frequency to 39.51Hz (791 lines/frame)	
		VS_COAST_MODE[1:0]					0	0			Auto Coast Mode	This value sets up the output coast frequency for the SDP
							0	1			50Hz Coast Mode	
							1	0			60Hz Coast Mode	
							1	1			Reserved	
		Reserved	0	0	0	0					Set to default	
0xFA R/W	Reserved	Reserved	1	0	1	0	0	0	0	0	Set to default	
0xFB R/W	Peaking Control	**PEAKING_GAIN[7:0]** Increases / decreses the gain for high frequency portions of the video signal	0	1	0	0	0	0	0	0		
0xFC R/W	Coring Threshold 2	**DNR_TH2[7:0]**	0	0	0	0	0	1	0	0	specifies the max. edge that will be interpreted as noise and therefore blanked	
0xFD R/W	general_chip_ctl	**PIN_CHECKER_EN** When this is enabled, by setting this bit high, the 8-bit word in PIN_CHECKER_OP gets mapped to the PIXEL pins								0	Disabled by default	
										1	the 8-bit word in PIN_CHECKER_OP gets mapped to these pins as follows: PIN_CHECKER_OP[7:0] -> P[7:0] PIN_CHECKER_OP[7:0] -> P[15:8] PIN_CHECKER_OP[7:0] -> PIN_CHECKER_OP[5:0] ->	
		[7:1] Reserved	0	0	0	0	0	0	0		Set to default	
0xFE R/W	Pin_Checker_Op	**PIN_CHECKER_OP[7:0]** A pseudo boundary scan scheme is implemented on the pixel pins P[29:0]. When this is enabled, by setting PIN_CHECKER_EN bit high, the 8-bit word in PIN_CHECKER_OP gets mapped to the Pixel Pins	1	0	1	0	1	0	1	0	When enabled, the 8-bit word in PIN_CHECKER_OP gets mapped as follows :- PIN_CHECKER_OP[7:0] ->P[7:0] PIN_CHECKER_OP[7:0] ->P[15:8] PIN_CHECKER_OP[7:0] -> P[23:16]	

2.2 User Map 1

Table 64: User Map 1 Details Register 0x40 to 0x41

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Comment	Note
0x40 R/W	Interrupt configuration 0	**INTRQ_OP_SEL[1:0]** Interrupt INT1 output select							0	0	Open Drain	
									0	1	Drive Low when active	
									1	0	Drive high when active	
									1	1	Reserved	
		MPU_STIM_INTRQ Manual Interrupt Set mode						0			Manual Interrupt Mode disabled	
								1			Manual Interrupt Mode enabled	
		INTERNAL_MUTE_INT Audio mute signal enable for					0				Do not output audio mute signal on INT1	
							1				Output audio mute signal on INT1	
		MV_INTRQ_SEL[1:0] Macrovision Interrupt Select			0	0					Reserved	
					0	1					Pseudo Sync Only	
					1	0					Color Stripe Only	
					1	1					Pseudo Sync or Colour Stripe	
		INTRQ_DUR_SEL[1:0] Interrupt duration Select	0	0							3 Xtal Periods	
			0	1							15 Xtal Periods	
			1	0							63 Xtal Periods	
			1	1							Active until cleared	
0x41 R/W	Interrupt configuration 1	**INTRQ2_OP_SEL[1:0]** Interrupt INT2 output select							0	0	Open Drain	
									0	1	Drive Low when active	
									1	0	Drive high when active	
									1	1	Reserved	
		Reserved						0				
		INTERNAL_MUTE_INT Audio mute signal enable for					0				Do not output audio mute signal on INT2	
							1				Output audio mute signal on INT2	
		[5:4] Reserved			0	0					Set to default	
		INTRQ2_DUR_SEL[1:0] Interrupt INT2 duration Select	0	0							3 Xtal Periods	
			0	1							15 Xtal Periods	
			1	0							63 Xtal Periods	
			1	1							Active until cleared	

Table 65: User Map 1 Details Register 0x42

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Comment	Note
0x42 Read	Interrupt Status 1	**SD_LOCK_Q**								0	No change	These Bits can be cleared and masked/unmasked in Registers 42h, 43h and 44h
										1	SD Input has caused the Decoder to go from an unlocked state to a locked state	
		SD UNLOCK_Q							0		No change	
									1		SD Input has caused the Decoder to go from a locked state to an unlocked state	
		CP_LOCK_Q						0			No change	
								1			CP Input has caused the Decoder to go from an unlocked state to a locked state	
		CP_UNLOCK_Q					0				No change	
							1				CP Input has caused the Decoder to go from a locked state to an unlocked state	
		STDI_DVALID_Q				0					No change	
						1					The STDI Valid has changed state.	
		SD_FR_CHNG_Q			0						No change	
					1						Denotes a change in the Free run status.	
		MV_PS_CS_Q		0							No change	
				1							Pseudo sync / Color striping detected. See Reg 40h MV_INT_SEL[1:0] for selection	
		SSPD_RESULT_Q	0								No change	
			1								Denotes following changes: - Activity on HS/CS pin - Activity on VS pin - HS polarity - VS polarity	
0x42 Write	Interrupt Clear 1	**SD_LOCK_CLR**								0	Do not Clear	
										1	Clears SD_LOCK_Q Bit	
		SD UNLOCK_CLR							0		Do not Clear	
									1		Clears SD_UNLOCK_Q Bit	
		CP_LOCK_CLR						0			Do not Clear	
								1			Clears CP_LOCK_Q Bit	
		CP_UNLOCK_CLR					0				Do not Clear	
							1				Clears CP_UNLOCK_Q Bit	
		STDI_DVALID_CLR				0					Do not Clear	
						1					Clears STDI_DVALID_Q Bit	
		SD_FR_CHNG_CLR			0						Do not Clear	
					1						Clears SD_FR_CHNG_Q Bit	
		MV_PS_CS_CLR		0							Do not Clear	
				1							Clears MV_PS_CS_Q Bit	
		SSPD_RESULT_CLR	1								Do not Clear	
			0								Clears SSPD_RESULT_Q	

Table 66: User Map 1 Details Register 0x43 to 0x45

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Comment	Note
0x43 R/W	Interrupt 2 Mask 1	**SD_LOCK_MSKB2**								0	Masks SD_LOCK_Q Bit	
										1	Unmasks SD_LOCK_Q Bit	
		SD UNLOCK_MSKB2							0		Masks SD_UNLOCK_Q Bit	
									1		Unmasks SD_UNLOCK_Q Bit	
		CP_LOCK_MSKB2						0			Masks CP_LOCK_Q Bit	
								1			Unmasks CP_LOCK_Q Bit	
		CP_UNLOCK_MSKB2					0				Masks CP_UNLOCK_Q Bit	
							1				Unmasks CP_UNLOCK_Q Bit	
		STDI_DVALID_MSKB2				0					Masks STDI_DVALID_Q Bit	
						1					Unmasks STDI_DVALID_Q Bit	
		SD_FR_CHNG_MSKB2			0						Masks SD_FR_CHNG_Q Bit	
					1						Unmasks SD_FR_CHNG_Q Bit	
		MV_PS_CS_MSKB2		0							Masks MV_PS_CS_Q Bit	
				1							Unmasks MV_PS_CS_Q Bit	
		SSPD_RESULT_MSKB2	0								Masks SSPD_RESULT_Q	
			1								Unmask SSPD_RESULT_Q	
0x44 R/W	Interrupt 1 Mask 1	**SD_LOCK_MSKB**								0	Masks SD_LOCK_Q Bit	
										1	Unmasks SD_LOCK_Q Bit	
		SD UNLOCK_MSKB							0		Masks SD_UNLOCK_Q Bit	
									1		Unmasks SD_UNLOCK_Q Bit	
		CP_LOCK_MSKB						0			Masks CP_LOCK_Q Bit	
								1			Unmasks CP_LOCK_Q Bit	
		CP_UNLOCK_MSKB					0				Masks CP_UNLOCK_Q Bit	
							1				Unmasks CP_UNLOCK_Q Bit	
		STDI_DVALID_MSKB				0					Masks STDI_DVALID_Q Bit	
						1					Unmasks STDI_DVALID_Q Bit	
		SD_FR_CHNG_MSKB			0						Masks SD_FR_CHNG_Q Bit	
					1						Unmasks SD_FR_CHNG_Q Bit	
		MV_PS_CS_MSKB		0							Masks MV_PS_CS_Q Bit	
				1							Unmasks MV_PS_CS_Q Bit	
		SSPD_RESULT_MSKB	0								Masks SSPD_RESULT_Q	
			1								Unmask SSPD_RESULT_Q	
0x45 Read	Raw Status 2	**CCAPD**								0	No CCAPD data detected	These bits are status bits only. They **cannot** be cleared or masked.
										1	CCAPD data detected	
		Reserved					x	x	x			
		EVEN_FIELD				0					Current SD field is not EVEN	
						1					Current SD field is EVEN	
		Reserved		x	x							
		MPU_STIM_INTRQ	0								MPU_STIM_INTRQ = 0	
			1								MPU_STIM_INTRQ = 1	

Table 67: User Map 1 Details Register 0x46

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Comment	Note
0x46 Read	Interrupt status 2	**CCAPD_Q**								0	Closed Captioning not detected in the input video signal	These bits can be cleared or masked by Registers 47h and 48h respectively Note that interrupt in register 0x46 for the CCAP, Gemstar, CGMS and WSS data is using the mode 1 VBI data slicer. (i.e. not VDP)
										1	Close Captioning data detected in the video input signal	
		GEMD_Q							0		Gemstar Data not detected in the input video signal	
									1		Gemstar data detected in the input Video signal	
		CGMS_CHNGD_Q						0			No change detected in CGMS data in the input video signal	
								1			A change in CGMS data detected in the input video Signal	
		WSS_CHNGD_Q					0				No change in WSS data detected in the input video Signal	
							1				A change in WSS data detected in the input video Signal	
		SD_FIELD_CHNGD_Q				0					SD signal has not changed Field from ODD to EVEN or vice vearsa	
						1					SD signal has changed Field from ODD to EVEN or vice vearsa	
		Not used		x	x						Not used	
		MPU_STIM_INT_Q	0								Manual interrupt not Set	
			1								Manual interrupt Set	
0x46 Write	Interrupt Clear 2	**CCAPD_CLR**								0	Do not clear	Note that interrupt in register 0x46 for the CCAP, Gemstar, CGMS and WSS data is using the mode 1 VBI data slicer. (i.e. not VDP)
										1	Clears CCAPD_Q Bit	
		GEMD_CLR							0		Do not clear	
									1		Clears GEMD_Q Bit	
		CGMS_CHNGD_CLR						0			Do not clear	
								1			Clears CGMS_CHNGD_Q Bit	
		WSS_CHNGD_CLR					0				Do not clear	
							1				Clears WSS_CHGND_Q Bit	
		SD_FIELD_CHNGD_CLR				0					Do not clear	
						1					Clears SD_FIELD_CHNGD_Q Bit	
		Reserved		0	0						Default set to Zero	
		MPU_STIM_INTRQ_CLR	0								Do not clear	
			1								Clears MPU_STIM_INT_Q Bit	

Table 68: User Map 1 Details Register 0x47 to 0x48

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Comment	Note
0x47 R/W	Interrupt 2 Mask 2	**CCAPD_MSKB2**								0	Masks CCAPD_Q Bit	Note that interrupt in register 0x46 for the CCAP, Gemstar, CGMS and WSS data is using the mode 1 VBI data slicer. (i.e. not VDP)
										1	Unmasks CCAPD_Q Bit	
		GEMD_MSKB2							0		Masks GEMD_Q Bit	
									1		Unmasks GEMD_Q Bit	
		CGMS_CHNGD_MSKB2						0			Masks CGMS_CHNGD_Q Bit	
								1			Unmasks CGMS_CHNGD_Q Bit	
		WSS_CHNGD_MSKB2					0				Masks WSS_CHGND_Q Bit	
							1				Unmasks WSS_CHGND_Q Bit	
		SD_FIELD_CHNGD_MSKB2				0					Masks SD_FIELD_CHNGD_Q	
						1					Unmasks SD_FIELD_CHNGD_Q	
		Reserved		x	x						Set to 0	
		MPU_STIM_INTRQ_MSKB2	0								Masks MPU_STIM_INT_Q Bit	
			1								Unmasks MPU_STIM_INT_Q Bit	
0x48 R/W	Interrupt 1 Mask 2	**CCAPD_MSKB**								0	Masks CCAPD_Q Bit	Note that interrupt in register 0x46 for the CCAP, Gemstar, CGMS and WSS data is using the mode 1 VBI data slicer. (i.e. not VDP)
										1	Unmasks CCAPD_Q Bit	
		GEMD_MSKB							0		Masks GEMD_Q Bit	
									1		Unmasks GEMD_Q Bit	
		CGMS_CHNGD_MSKB						0			Masks CGMS_CHNGD_Q Bit	
								1			Unmasks CGMS_CHNGD_Q Bit	
		WSS_CHNGD_MSKB					0				Masks WSS_CHGND_Q Bit	
							1				Unmasks WSS_CHGND_Q Bit	
		SD_FIELD_CHNGD_MSKB				0					Masks SD_FIELD_CHNGD_Q	
						1					Unmasks SD_FIELD_CHNGD_Q	
		Not used		x	x						Not used	
		MPU_STIM_INTRQ_MSKB	0								Masks MPU_STIM_INT_Q Bit	
			1								Unmasks MPU_STIM_INT_Q Bit	

Table 69: User Map 1 Details Register 0x49 to 0x4A

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x49 Read	Raw Status 3	**SD OP 50Hz**								0	SD 60Hz signal detected at the Output	These bits **cannot** be cleared or masked. Register 4Ah is used for this purpose
										1	SD 50Hz signal detected at the Output	
		SD V LOCK							0		SD Vertical sync Lock not established	
									1		SD Vertical sync Lock established	
		SD_H_LOCK						0			SD Horizontal sync lock not established	
								1			SD Horizontal sync Lock established	
		Not used					x				Not used	
		SCM_LOCK				0					SECAM Lock not established	
		Secam Lock				1					SECAM Lock established	
		[6:5] Reserved		x	x						Not used	
		FL_PLL_LOCKED Indicates the lock status of the PLL (CP)	0								The Pll has not lock to incoming sync	
			1								The PLL has lock to the incoming sync	
0x4A Read	Interrupt Status 3	**SD_OP_CHNG_Q** SD 60/50Hz frame rate at output								0	No change in SD Signal standard detected	Can be used in blue screen mode. Tells the user what standard is being o/p These bits can be cleared and Masked by register 4Bh and 4Ch respectively
										1	A change of SD signal standard has been detected	
		SD V LOCK CHNG Q							0		SD Vertical sync lock not established	
									1		SD Vertical sync Lock established	
		SD_H_LOCK_CHNG_Q						0			SD Horizontal sync lock not established	
								1			SD Horizontal sync Lock established	
		SD_AD_CHNG_Q					0				No change in **AD_RESULT[2:0]** Bits in STATUS 1 register	
							1				**AD_RESULT[2:0]** Bits in STATUS 1 register has changed	
		SCM LOCK CHNG Q				0					No change in SECAM lock status	
						1					SECAM Lock status has changed	
		PAL_SW_LK_CHNG_Q			0						No change in PAL Swinging Burst lock status	
					1						PAL Swinging Burst lock status has changed	
		Reserved		x							Not used	
		FL PLL LOCKED Q	0								No Change in the PLL lock status	
			1								Change in PLL lock status has generated an interrupt	
0x4A Write	Interrupt Clear 3	**SD OP CHNG CLR**								0	Do not Clear	
										1	Clear SD_OP_CHNG_Q Bit	
		SD V LOCK CHNG CLR							0		Do not Clear	
									1		Clear SD_V_LOCK_CHNG_Q Bit	
		SD H LOCK CHNG CLR						0			Do not Clear	
								1			Clear SD_H_LOCK_CHNG_Q Bit	
		SD AD CHNG CLR					0				Do not Clear	
							1				Clear SD_AD_CHNG_Q Bit	
		SCM LOCK CHNG CLR				0					Do not Clear	
						1					Clear SCM_LOCK_CHNG_Q	
		PAL SW LK CHNG CLR			0						Do not Clear	
					1						Clear PAL_SW_LK_CHNG_Q	
		Reserved		0							Set to default	
		FL PLL LOCKED CLR	0								Do not Clear	
			1								Clear FL_PLL_LOCKED_Q	

Table 70: User Map 1 Details Register 0x4B

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x4B R/W	Interrupt 2 Mask 3	**SD_OP_CHNG_MSKB2**								0	Mask SD_OP_CHNG_Q Bit	
										1	Unmask SD_OP_CHNG_Q Bit	
		SD_V_LOCK_CHNG_MSKB2							0		Mask SD_V_LOCK_CHNG_Q Bit	
									1		Unmask V_LOCK_CHNG_Q Bit	
		SD_H_LOCK_CHNG_MSKB2						0			Mask SD_H_LOCK_CHNG_Q Bit	
								1			Unmask SD_H_LOCK_CHNG_Q Bit	
		SD_AD_CHNG_MSKB2					0				Mask SD_AD_CHNG_Q Bit	
							1				Unmask SD_AD_CHNG_Q Bit	
		SCM_LOCK_CHNG_MSKB2				0					Mask SCM_LOCK_CHNG_Q	
						1					Unmask SCM_LOCK_CHNG_Q	
		PAL_SW_LK_CHNG_MSKB2			0						Mask PAL_SW_LK_CHNG_Q bit	
					1						Unmask PAL_SW_LK_CHNG_Q bit	
		Reserved		0							Set to default	
		FL_PLL_LOCKED_MSKB2	0								Mask FL_PLL_LOCKED_Q	
			1								Unmask FL_PLL_LOCKED_Q	

Table 71: User Map 1 Details Register 0x4C to 0x4D

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x4C R/W	Interrupt 1 Mask 3	**SD_OP_CHNG_MSKB**								0	Mask SD_OP_CHNG_Q Bit	
										1	Unmask SD_OP_CHNG_Q Bit	
		SD_V_LOCK_CHNG_MSKB							0		Mask SD_V_LOCK_CHNG_Q Bit	
									1		Unmask V_LOCK_CHNG_Q Bit	
		SD_H_LOCK_CHNG_MSKB						0			Mask SD_H_LOCK_CHNG_Q Bit	
								1			Unmask SD_H_LOCK_CHNG_Q Bit	
		SD_AD_CHNG_MSKB					0				Mask SD_AD_CHNG_Q Bit	
							1				Unmask SD_AD_CHNG_Q Bit	
		SCM_LOCK_CHNG_MSKB				0					Mask SCM_LOCK_CHNG_Q	
						1					Unmask SCM_LOCK_CHNG_Q	
		PAL_SW_LK_CHNG_MSKB			0						Mask PAL_SW_LK_CHNG_Q bit	
					1						Unmask PAL_SW_LK_CHNG_Q bit	
		Reserved		x							Not used	
		FL_PLL_LOCKED_MSKB	0								Mask FL_PLL_LOCKED_Q	
			1								Unmask FL_PLL_LOCKED_Q	
0x4D Read	Raw Status 4	**VDP_CC_AVL**								0	Closed Captioning data not available	
										1	Closed Captioning data available	
		Reserved							x		Not used	
		VDP_CGMS_WSS_AVL						0			CGMS/WSS data not detected/available	
								1			CGMS/WSS data detected/available	
		Reserved					x				Not used	
		VDP_GS_PDC_VPS_UTC_AVL				0					GemStar / PDC / VPS / UTC data is not detected/available	
						1					GemStar / PDC / VPS / UTC data is detected/available	
		Reserved			x							
		VDP_VITC_AVL		0							VITC data is not detected/available	
				1							VITC data is detected/available	
		VDP_TTX_AVL	0								Teletext is not detected/available	
			1								Teletext is detected/available	

Table 72: User Map 1 Details Register 0x4E

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x4E Read	Interrupt Status 4	**VDP_CCAPD_Q**								0	No intterupt has been triggered from this register.	These bits can be cleared and masked / unmasked by registers 0x4F and 0x50 respectively. Note that the interrupt signals in 0x4E are using the VDP VBI dataslicer
										1	Change in Closed Captioning detection has generated an interrupt	
		Reserved							x		Not used	
		VDP_CGMS_WSS_CHNG_Q Please see 0x9C bit 4 (User Sub Map) to determine if interrupt is issued for a change in detected data or for when						0			No interrupt has been generated from this register.	
								1			CGMS / WSS data detection bit has changed and generated an interrupt	
		Reserved					x				Not used	
		VDP_GS_VPS_PDC_UTC_CHNG_Q Please see 0x9C bit 5 (User Sub Map) to determine if interrupt is issued for a change in detected data or for when				0					No interrupt has been generated from this register.	
						1					GemStar / PDC / VPS / UTC detection has changed and generated an interrupt	
		Reserved			x						Not used	
		VDP_VITC_Q		0							No interrupt has been generated from this register.	
				1							VITC detection has changed and generated an interrupt	
		VDP_TTX_AVL_Q	0								No interrupt has been generated from this register.	
			1								Teletext detection has changed and generated an interrupt	
0x4E Write	Interrupt clear 4	**VDP_CCAPD_CLR**								0	Do not Clear	
										1	Clears VDP_CCAPD_Q	
		Reserved							x		Set to 0	
		VDP_CGMS_WSS_CHNG_CLR									Do not Clear	
								0			Clears VDP_CGMS_WSS_CHNG_Q	
		Reserved						1			Not used	
		VDP_GS_VPS_PDC_UTC_CHNG_CLR				0					Do not Clear	
						1					Clears VDP_GS_VPS_PDC_UTC_CHNG_	
		Reserved			x						Reserved	
		VDP_VITC_CLR		0							Do not Clear	
				1							Clears VDP_VITC_Q	
		VDP_TTX_CLR	0								Do not Clear	
			1								Clear VDP_TTX_AVL_Q	

Table 73: User Map 1 Details Register 0x4F to 0x50

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x4F R/W	Interrupt 2 Mask 4	**VDP_CCAPD_MSKB2**								0	Masks VDP_CCAPD_Q	
										1	Unmasks VDP_CCAPD_Q	
		Reserved							x		Not used	
		VDP_CGMS_WSS_CHNG_MSKB2						0			Masks VDP_CGMS_WSS_CHNG_Q	
								1			Unmasks	
		Reserved					x				Not used	
		VDP_GS_VPS_PDC_UTC_CHNG_MSKB2				0					Masks VDP_GS_VPS_PDC_UTC_CHNG_Q	
						1					Unmasks VDP_GS_VPS_PDC_UTC_CHNG_Q	
		Reserved			x						Not used	
		VDP_VITC_MSKB2		0							Masks VDP_VITC_Q	
				1							Unmasks VDP_VITC_Q	
		VDP TTX AVL MSKB2	0								Masks VDP_TTX_AVL_Q	
			1								Unmasks VDP_TTX_AVL_Q	
0x50 R/W	Interrupt 1 Mask 4	**VDP_CCAPD_MSKB**								0	Masks VDP_CCAPD_Q	
										1	Unmasks VDP_CCAPD_Q	
		Reserved							x		Not used	
		VDP_CGMS_WSS_CHNG_MSKB						0			Masks VDP_CGMS_WSS_CHNG_Q	
								1			Unmasks	
		Reserved					x				Not used	
		VDP_GS_VPS_PDC_UTC_CHNG_MSKB				0					Masks VDP_GS_VPS_PDC_UTC_CHNG_Q	
						1					Unmasks VDP_GS_VPS_PDC_UTC_CHNG_Q	
		Reserved			x						Not used	
		VDP_VITC_MSKB		0							Masks VDP_VITC_Q	
				1							Unmasks VDP_VITC_Q	
		VDP TTX AVL MSKB	0								Masks VDP_TTX_AVL_Q	
			1								Unmasks VDP_TTX_AVL_Q	

Table 74: User Map 1 Details Register 0x60

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x60 Read	HDMI_RAW_STATUS_1	**AVI_INFO_RAW** Raw Status bit								0	If No AVI Infoframe has been received within the last 7 Vsyncs. This Bit will reset to zero on the 8th Vsync leading edge following an AVI InfoFrame or after an HDMI reset condition.	An HDMI reset condition includes : -part powered up/ reset -a new TMDS freq is detected
										1	An AVI Infoframe has been received.	
		AUDIO_INFO_RAW Raw Status bit							0		If No Audio Infoframe has been received within the last 3 Vsyncs. This Bit will reset to zero on the 4th Vsync leading edge following an Audio InfoFrame or after an HDMI reset	An HDMI reset condition includes : -part powered up/ reset -a new TMDS freq is detected
									1		An Audio Infoframe has been received.	
		SPD_INFO_RAW Raw Status bit						0			No Source Product Description Infoframe has been received since the last reset condition. This bit reset to zero after an HDMI reset condition.	An HDMI reset condition includes : -part powered up/ reset -a new TMDS freq is detected
								1			Source Product Description Infoframe has been received.	
		MS_INFO_RAW Raw Status bit					0				If No MPEG Source Infoframe has been received within the last 3 Vsyncs, this Bit will reset to zero on the 4th Vsync leading edge or after an HDMI reset condition	All packet detect Bits will go low whenever : The part is powered up or a new TMDS freq is detected
							1				MPEG Source Infoframe has been received.	

Table 75: User Map 1 Details Register 0x60 (Continued)

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x60 Read	HDMI_RAW_STATUS_1	**ACP_PCKT_RAW** Raw Status bit				0					No ACP packet has been received within the last 600ms. This bit will reset to zero after and HDMI reset condition.	An HDMI reset condition includes : -part powered up/ reset -a new TMDS freq is detected
						1					ACP packets have been received.	
		ISRC0_PCKT_RAW Status bit			0						No ISRC0 packets have been received since the last HDMI reset condition.	An HDMI reset condition includes : -part powered up/ reset -a new TMDS freq is detected
					1						ISRC0 packets have been received.	
		ISRC1_PCKT_RAW Status bit.		0							No ISRC1 packets have been received since the last HDMI reset condition.	An HDMI reset condition includes : -part powered up/ reset -a new TMDS freq is detected
				1							ISRC1 packets have been received.	
		DSD_PCKT_RAW Status bit.	0								No DSD packets has been received within the last 10Hsyncs. This Bit will reset to zero on the 11th Hsync leading edge following a DSD packet or if Audio Sample Packet has been received or after an HDMI reset condition.	An HDMI reset condition includes : -part powered up/ reset -a new TMDS freq is detected
			1								DSD packets have been received.	

Table 76: User Map 1 Details Register 0x61 (Read Only)

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x61 Read	HDMI_INT_STATUS_1	**AVI_INFO_ST** Indicates if, AVI_INFO_RAW, has changed or not. This Bit is not active if associated Mask is set.								0	AVI_INFO_RAW has not changed. Interrupt has not been generated.	
										1	AVI_INFO_RAW has changed. Interrupt has been generated.	
		AUDIO_INFO_ST Indicates if, AUDIO_INFO_RAW, has changed or not. This Bit is not active if associated Mask is set.							0		AUDIO_INFO_RAW has not changed. Interrupt has not been generated.	
									1		AUDIO_INFO_RAW has changed. Interrupt has been generated.	
		SPD_INFO_ST Indicates if, SPD_INFO_RAW, has changed or not. This Bit is not active if associated Mask is set.						0			SPD_INFO_RAW has not changed. Interrupt has not been generated.	
								1			SPD_INFO_RAW has changed. Interrupt has been generated.	
		MS_INFO_ST Indicates if, MS_INFO_RAW, has changed or not. This Bit is not active if associated Mask is set.					0				MS_INFO_RAW has not changed. Interrupt has not been generated.	
							1				MS_INFO_RAW has changed. Interrupt has been generated.	
		ACP_PCKT_ST Indicates if, ACP_PCKT_RAW, has changed or not. This Bit is not active if associated Mask is set.				0					ACP_PCKT_RAW has not changed. Interrupt has not been generated.	
						1					ACP_PCKT_RAW has changed. Interrupt has been generated.	
		ISRC0_PCKT_ST Indicates if, ISRC0_PCKT_RAW, has changed or not. This Bit is not active if associated Mask is set.			0						ISRC0_PCKT_RAW has not changed. Interrupt has not been generated.	
					1						ISRC0_PCKT_RAW has changed. Interrupt has been generated.	
		ISRC1_PCKT_ST Indicates if, ISRC1_PCKT_RAW, has changed or not. This Bit is not active if associated Mask is set.		0							ISRC1_PCKT_RAW has not changed. Interrupt has not been generated.	
				1							ISRC1_PCKT_RAW has changed. Interrupt has been generated.	
		DSD_PCKT_ST Indicates if, DSD_PCKT_RAW, has changed or not. This Bit is not active if associated Mask is set.	0								DSD_PCKT_RAW has not changed. Interrupt has not been generated.	
			1								DSD_PCKT_RAW has changed. Interrupt has been generated.	

Table 77: User Map 1 Details Register 0x61 (Write Only)

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x61 Write	HDMI_INT_CLR_1	**AVI_INFO_CLR**								0	Do not clear	
										1	Clears AVI_INFO_ST	
		AUDIO_INFO_CLR							0		Do not clear	
									1		Clears AUDIO_INFO_ST	
		SPD_INFO_CLR						0			Do not clear	
								1			Clears SPD_INFO_ST	
		MS_INFO_CLR					0				Do not clear	
							1				Clears MS_INFO_ST	
		ACP_PCKT_CLR				0					Do not clear	
						1					Clears ACP_PCKT_ST	
		ISRC0_PCKT_CLR			0						Do not clear	
					1						Clears ISRC0_PCKT_ST	
		ISRC1_PCKT_CLR		0							Do not clear	
				1							Clears ISRC1_PCKT_ST	
		DSD_PCKT_CLR	0								Do not clear	
			1								Clears DSD_PCKT_ST	

Table 78: User Map 1 Details Register 0x62 to 0x63

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x62 R/W	HDMI_INT2_MASKB_1 Masks for Interrupt 2	**AVI_INFO_MB2** Mask for AVI_INFO_ST bit								0	Mask	
										1	Unmask	
		AUDIO_INFO_MB2 Mask for AUDIO_INFO_ST bit							0		Mask	
									1		Unmask	
		SPD_INFO_MB2 Mask for SPD_INFO_ST bit						0			Mask	
								1			Unmask	
		MS_INFO_MB2 Mask for MS_INFO_ST bit					0				Mask	
							1				Unmask	
		ACP_PCKT_MB2 Mask for ACP_PCKT_ST bit				0					Mask	
						1					Unmask	
		ISRC0_PCKT_MB2 Mask for ISRC0_PCKT_ST bit			0						Mask	
					1						Unmask	
		ISRC1_PCKT_MB2 Mask for ISRC1_PCKT_ST bit		0							Mask	
				1							Unmask	
		DSD_PCKT_MB2 Mask for DSD_PCKT_ST bit	0								Mask	
			1								Unmask	
0x63 R/W	HDMI_INT1_MASKB_1 Masks for Interrupt 1	**AVI_INFO_MB1** Mask for AVI_INFO_ST bit								0	Mask	
										1	Unmask	
		AUDIO_INFO_MB1 Mask for AUDIO_INFO_ST bit							0		Mask	
									1		Unmask	
		SPD_INFO_MB1 Mask for SPD_INFO_ST bit						0			Mask	
								1			Unmask	
		MS_INFO_MB1 Mask for MS_INFO_ST bit					0				Mask	
							1				Unmask	
		ACP_PCKT_MB1 Mask for ACP_PCKT_ST bit				0					Mask	
						1					Unmask	
		ISRC0_PCKT_MB1 Mask for ISRC0_PCKT_ST bit			0						Mask	
					1						Unmask	
		ISRC1_PCKT_MB1 Mask for ISRC1_PCKT_ST bit		0							Mask	
				1							Unmask	
		DSD_PCKT_MB1 Mask for DSD_PCKT_ST bit	0								Mask	
			1								Unmask	

Table 79: User Map 1 Details Register 0x64 (Read Only)

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x64 Read	HDMI_RAW_STATUS_2	**AUDIO_S_PCKT_RAW** Raw status bit								0	No Audio sample packets has been received within the last 10Hsyncs. This Bit will reset to zero on the 11th Hsync leading edge following an Audio Sample packet or if a DSD Sample Packet has been received or after an HDMI reset condition.	An HDMI reset condition includes : -part powered up/ reset -a new TMDS freq is detected
										1	Audio Sample packets have been received.	
		AUDIO_C_PCKT_RAW Raw status bit							0		No Audio Clock Regeneration packets have been received since the last HDMI reset condition	An HDMI reset condition includes : -part powered up/ reset -a new TMDS freq is detected
									1		Audio Clock Regeneration packets have been received	
		GEN_CTL_PCKT_RAW Raw status bit.						0			No General Control packets have been received since the last HDMI reset condition	An HDMI reset condition includes : -part powered up/ reset -a new TMDS freq is detected
								1			General Control packets have been received.	
		INFO_FR_PCKT_RAW Raw status bit.					0				No Infoframes packet have been received since the last HDMI reset condition.	An HDMI reset condition includes : -part powered up/ reset -a new TMDS freq is detected
							1				Infoframes packet have been received.	
		AV_MUTE_RAW Raw status Bit.				0					No AV Mute raw has been received since last HDMI reset condition	An HDMI reset condition includes : -part powered up/ reset -a new TMDS freq is detected
						1					AV Mute received	
		DE_REGEN_LCK_RAW Status bit. This bit says whether or not the DE regeneration block has locked to the incoming DE signal. Changes whenever DE changes including mode changes and plug/unplug			0						DE regeneration Block has not been locked to the incoming DE signal	
					1						DE regeneration Block has been locked to the incoming DE signal	
		HDMI_ENCRPT_RAW Status bit. This bit says whether the current frame is encrypted or not. It is updated every vsync.		0							Current frame is not been encrypted	
				1							Current frame is encrypted	
		AUDIO_PLL_LCK_RAW Status bit. High if Audio PLL is locked to synthesized audio clock	0								Audio PLL has not been locked to the synthesized audio clock	
			1								Audio PLL has been locked to the synthesized audio clock	

Table 80: User Map 1 Details Register 0x65 (Read Only)

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x65 Read	HDMI_INT_Status_2	**AUDIO_S_PCKT_ST** Indicates if, AUDIO_S_PCKT_RAW, has changed or not. This Bit is not active if associated Mask is set.								0	AUDIO_S_PCKT_RAW has not changed. Interrupt has not been generated	
										1	AUDIO_S_PCKT_RAW has changed. Interrupt has been generated	
		AUDIO_C_PCKT_ST Indicates if, AUDIO_C_PCKT_RAW, has changed or not. This Bit is not active if associated Mask is set.							0		AUDIO_C_PCKT_RAW has not changed. Interrupt has not been generated	
									1		AUDIO_C_PCKT_RAW has changed. Interrupt has been generated	
		GEN_CTL_PCKT_ST Indicates if, GEN_CTL_PCKT_RAW, has changed or not. This Bit is not active if associated Mask is set.						0			GEN_CTL_PCKT_RAW has not changed. Interrupt has not been generated	
								1			GEN_CTL_PCKT_RAW has changed. Interrupt has been generated	
		INFO_FR_PCKT_ST Indicates if, INFO_FR_PCKT_RAW, has changed or not. This Bit is not active if associated Mask is set.					0				INFO_FR_PCKT_RAW has not changed. Interrupt has not been generated	
							1				INFO_FR_PCKT_RAW has changed. Interrupt has been generated	
		AV_MUTE_ST Indicates if, AV_MUTE_RAW, has changed or not. This Bit is not active if associated Mask is set.				0					AV_MUTE_RAW has not changed. Interrupt has not been generated	
						1					AV_MUTE_RAW has changed. Interrupt has been generated	
		DE_REGEN_LCK_ST Indicates if, DE_REGEN_LCK_RAW, has changed or not. This Bit is not active if associated Mask is set.			0						DE_REGEN_LCK_RAW has not changed. Interrupt has not been generated	
					1						DE_REGEN_LCK_RAW has changed. Interrupt has been generated	
		HDMI_ENCRPT_ST Indicates if, HDMI_ENCRPT_RAW, has changed or not. This Bit is not active if associated Mask is set.		0							HDMI_ENCRPT_RAW has not changed. Interrupt has not been generated	
				1							HDMI_ENCRPT_RAW has changed. Interrupt has been generated	
		AUDIO_PLL_LCK_ST Indicates if, AUDIO_PLL_LCK_RAW, has changed or not. This Bit is not active if associated Mask is set.	0								AUDIO_PLL_LCK_RAW has not changed. Interrupt has not been generated	
			1								AUDIO_PLL_LCK_RAW has changed. Interrupt has been generated	

Table 81: User Map 1 Details Register 0x65 (Write Only)

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x65 Write	HDMI_INT_CLR_2	**AUDIO_S_PCKT_CLR**								0	Do not clear	
										1	Clears AUDIO_S_PCKT_ST	
		AUDIO_C_PCKT_CLR							0		Do not clear	
									1		Clears AUDIO_C_PCKT_ST	
		GEN_CTL_PCKT_CLR						0			Do not clear	
								1			Clears GEN_CTL_PCKT_ST	
		INFO_FR_PCKT_CLR					0				Do not clear	
							1				Clears INFO_FR_PCKT_ST	
		AV_MUTE_CLR				0					Do not clear	
						1					Clears AV_MUTE_ST	
		DE_REGEN_LCK_CLR			0						Do not clear	
					1						Clears DE_REGEN_LCK_ST	
		HDMI_ENCRPT_CLR		0							Do not clear	
				1							Clears HDMI_ENCRPT_ST	
		AUDIO_PLL_LCK_CLR	0								Do not clear	
			1								Clears AUDIO_PLL_LCK_ST	

Table 82: User Map 1 Details Register 0x66 to 0x67

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x66 R/W	HDMI_INT2_MASKB_2 Masks for Interrupt 2	**AUDIO_S_PCKT_MB2**								0	Mask	
										1	Unmask	
		AUDIO_C_PCKT_MB2							0		Mask	
									1		Unmask	
		GEN_CTL_PCKT_MB2						0			Mask	
								1			Unmask	
		INFO_FR_PCKT_MB2					0				Mask	
							1				Unmask	
		AV_MUTE_MB2				0					Mask	
						1					Unmask	
		DE_REGEN_LCK_MB2			0						Mask	
					1						Unmask	
		HDMI_ENCPT_MB2		0							Mask	
				1							Unmask	
		AUDIO_PLL_LCK_MB2	0								Mask	
			1								Unmask	
0x67 R/W	HDMI_INT1_MASKB_2 Masks for Interrupt 1	**AUDIO_S_PCKT_MB1**								0	Mask	
										1	Unmask	
		AUDIO_C_PCKT_MB1							0		Mask	
									1		Unmask	
		GEN_CTL_PCKT_MB1						0			Mask	
								1			Unmask	
		INFO_FR_PCKT_MB1					0				Mask	
							1				Unmask	
		AV_MUTE_MB1				0					Mask	
						1					Unmask	
		DE_REGEN_LCK_MB1			0						Mask	
					1						Unmask	
		HDMI_ENCPT_MB1		0							Mask	
				1							Unmask	
		AUDIO_PLL_LCK_MB1	0								Mask	
			1								Unmask	

Table 83: User Map 1 Details Register 0x68

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x68 Read	HDMI_RAW_STATUS_3	**VIDEO_PLL_LCK_RAW** Raw status bit.								0	TMDS PLL is not locked to the incoming HDMI clock.	
										1	TMDS PLL is locked to the incoming HDMI clock.	
		HDMI_MODE_RAW Raw status bit							0		DVI is being received.	
									1		HDMI is being received.	
		AUDIO_CH_MODE_RAW Status bit. Specifies if audio is in stereo or multi-channel.						0			Two-channel audio (could be compressed channel).	
								1			Multi-channel audio (2 4, 6 or 8-channel audio).	
		TMDS_CLK_B_RAW Raw status bit.					0				No TMDS clock detected on Port B	
							1				TMDS clock detected on Port B.	
		TMDS_CLK_A_RAW Raw status bit.				0					No TMDS clock detected on Port A.	
						1					TMDS clock detected on Port A.	
		INTERNAL_MUTE_RAW Raw Status bit			0						Audio is not muted.	
					1						Audio is muted.	
		GAMUT_MDATA_RAW Indicates if Gamut metadata packet received in last Vsync.		0							No Gamut metadata packet received within last Vsync. Reset to zero after an HDMI reset condition.	An HDMI reset condition includes part powered up/reset, and new TMDS freq detected. Refer to HDMI 1.3 spec.
				1							Gamut metadata packet received within last Vsync.	
		V_LOCKED_RAW Indicates if the vertical sync filter has locked and vertical sync parameters in the HDMI Map are valid.	0								Vertical sync filter has not locked and vertical sync parameters are not valid.	This bit is valid and accurate ~50 ms following a resolution change on the input.
			1								Vertical sync filter has locked and vertical sync parameters are valid.	

Table 84: User Map 1 Details Register 0x69 (Read Only)

Sub address	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x69 Read	HDMI_INT_STATUS_3	**VIDEO_PLL_LCK_ST** Indicates if VIDEO_PLL_LCK_RAW has changed or not. This bit is not active if associated mask is set.								0	VIDEO_PLL_LCK_RAW has not changed. Interrupt has not been generated	
										1	VIDEO_PLL_LCK_RAW has changed. Interrupt has been generated	
		HDMI_MODE_ST Indicates if HDMI_MODE_RAW has changed or not. This bit is not active if associated mask is set.							0		HDMI_MODE_RAW has not changed. Interrupt has not been generated	
									1		HDMI_MODE_RAW has changed. Interrupt has been generated	
		AUDIO_CH_MODE_ST Indicates if AUDIO_CH_MODE_RAW has changed or not. This bit is not active if associated mask is set.						0			AUDIO_CH_MODE_RAW has not changed. Interrupt has not been generated	
								1			AUDIO_CH_MODE_RAW has changed. Interrupt has been generated	
		TMDS_CLK_B_ST Indicates if TMDS_CLK_B_RAW has changed or not. This bit is not active if associated mask is set.					0				TMDS_CLK_B_RAW has not changed. Interrupt has not been generated	
							1				TMDS_CLK_B_RAW has changed. Interrupt has been generated	
		TMDS_CLK_A_ST Indicates if TMDS_CLK_A_RAW has changed or not. This bit is not active if associated mask is set.				0					TMDS_CLK_A_RAW has not changed. Interrupt has not been generated	
						1					TMDS_CLK_A_RAW has changed. Interrupt has been generated	
		INTERNAL_MUTE_ST Indicates if INTERNAL_MUTE_RAW has changed or not. This bit is not active if associated mask is set.			0						INTERNAL_MUTE_RAW has not changed. Interrupt has not been generated	
					1						INTERNAL_MUTE_RAW has changed. Interrupt has been generated	
		GAMUT_MDATA_ST Indicates if GAMUT_MDATA_RAW has changed. This bit is not active if associated mask is set.		0							GAMUT_MDATA_RAW has not changed	
				1							GAMUT_MDATA_RAW has changed	
		V_LOCKED_ST Indicates if the vertical sync filter locked status has changed. This bit is not active if the set.	0								No Status change for V_LOCKED	
			1								Status change for V_LOCKED	

Table 85: User Map 1 Details Register 0x69 (Write Only)

Sub address	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x69 Write	HDMI_INT_CLR_3	**VIDEO_PLL_LCK_CLR**								0	Do not clear	
										1	Clears VIDEO_PLL_LCK_ST	
		HDMI_MODE_CLR							0		Do not clear	
									1		Clears HDMI_MODE_ST	
		AUDIO_CH_MODE_CLR						0			Do not clear	
								1			Clears AUDIO_CH_MODE_ST	
		TMDS_CLK_B_CLR					0				Do not clear	
							1				Clears TMDS_CLK_B_ST	
		TMDS_CLK_A_CLR				0					Do not clear	
						1					Clears TMDS_CLK_A_ST	
		INTERNAL_MUTE_CLR			0						Do not clear	
					1						Clears INTERNAL_MUTE_ST. Only applies if MUTE_INT_REAL_STATUS=0	
		GAMUT_MDATA_CLR Clear bit for GAMUT_MDATA_ST.		0							does not clear GAMUT_MDATA	
				1							clears GAMUT_MDATA	
		V_LOCKED_CL Clear bit for V_LOCKED_ST.	0								Do not clear	
			1								Clears V_LOCKED_ST.	

Table 86: User Map 1 Details Register 0x6A to 0x6B

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x6A R/W	HDMI_INT2_MASKB_3 Masks for interrupt 2	**VIDEO_PLL_LCK_MB2** Mask for VIDEO PLL LCK ST bit								0	Mask	
										1	Unmask	
		HDMI_MODE_MB2 Mask for HDMI MOD ST bit							0		Mask	
									1		Unmask	
		AUDIO_CH_MODE_MB2 Mask for AUDIO CH MODE ST bit						0			Mask	
								1			Unmask	
		TMDS_CLK_B_MB2 Mask for TMDS_CLK_B_ST					0				Mask	
							1				Unmask	
		TMDS_CLK_A_MB2 Mask for TMDS_CLK_A_ST				0					Mask	
						1					Unmask	
		INTERNAL MUTE MB2			0						Mask	
					1						Unmask	
		GAMUT_MDATA_MB2 Mask bit for GAMUT_MDATA_ST.		0							Mask	
				1							Unmask	
		V_LOCKED_MB2 Mask bit for V_LOCKED_ST.	0								Mask	
			1								Unmask	
0x6B R/W	HDMI_INT_MASKB 3	**VIDEO_PLL_LCK_MB1** Mask for VIDEO_PLL_LCK_STbit								0	Mask	
										1		
		HDMI_MODE_MB1 Mask for HDMI_MOD_ST bit							0		Mask	
									1		Unmask	
		AUDIO_CH_MODE_MB1 Mask for AUDIO_CH_MODE_ST bit						0			Mask	
								1			Unmask	
		TMDS_CLK_B_MB1 Mask for TMDS_CLK_B_ST					0				Mask	
							1				Unmask	
		TMDS_CLK_A_MB1 Mask for TMDS_CLK_A_ST				0					Mask	
						1					Unmask	
		INTERNAL MUTE MB1			0						Mask	
					1						Unmask	
		GAMUT_MDATA_MB1 Mask bit for GAMUT_MDATA_ST.		0							Mask	
				1							Unmask	
		V_LOCKED_MB1 Mask bit for V_LOCKED_ST.	0								Mask	
			1								Unmask	

Table 87: User Map 1 Details Register 0x6C (Read Only)

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x6C Read	HDMI_INT_STATUS_4	**NEW_AVI_INFO_ST** Indicates if new AVI infoframe received or not. This bit is not active if associated mask is set.								0	No new AVI InfoFrame received	
										1	An AVI InfoFrame with new content received.	
		NEW_AUDIO_INFO_ST Indicates if new Audio Infoframe received or not. This bit is not active if associated mask is set.							0		No new Audio InfoFrame received.	
									1		An audio InfoFrame with new content received.	
		NEW_SPD_INFO_ST Indicates if new SPD Infoframe received or not. This bit is not active if associated mask is set.						0			No new SPD InfoFrame received.	
								1			An SPD InfoFrame with new content received.	
		NEW_MS_INFO_ST Indicates if new MPEG Source Infoframe received or not. This bit is not active if associated mask is set.					0				No new MPEG Source InfoFrame received.	
							1				An MPEG Source InfoFrame with new content received.	
		NEW_ACP_PCKT_ST Indicates if new ACP Packet received or not. This bit is not active if associated mask is set.				0					No new ACP Packet received.	
						1					An ACP Packet with new content received.	
		NEW_ISRC1_PCKT_ST Indicates if new ISRC1 Packet received or not. This bit is not active if associated mask is set.			0						No new ISRC1 Packet received.	
					1						An ISRC1 Packet with new content received	
		NEW_ISRC2_PCKT_ST Indicates if new ISRC2 Packet received or not. This bit is not active if associated mask is set.		0							No new ISRC2 Packet received.	
				1							An ISRC2 Packet with new content received	
		NEW_GAMUT_MDATA_ST Indicates if new Gamut metadata received or changed.	0								No new Gamut metadata packet received or no change has taken place.	Refer to HDMI 1.3 spec.
			1								New Gamut metadata packet received that triggered this interrupt.	

Table 88: User Map 1 Details Register 0x6C (Write Only)

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x6C Write	HDMI_INT_CLR_4	**NEW_AVI_INFO_CLR**								0	Do not clear	
										1	Clears NEW_AVI_INFO_ST and NEW_AVI_INFO_RAW	
		NEW_AUDIO_INFO_CLR							0		Do not clear	
									1		Clears NEW_AUDIO_INFO_ST and NEW_AUDIO_INFO_RAW	
		NEW_SPD_INFO_CLR						0			Do not clear	
								1			Clears NEW_SPD_INFO_ST and NEW_SPD_INFO_RAW	
		NEW_MS_INFO_CLR					0				Do not clear	
							1				Clears NEW_MS_INFO_ST and NEW_MS_INFO_RAW	
		NEW_ACP_PCKT_CLR				0					Do not clear	
						1					Clears NEW_ACP_PCKT_ST and NEW_ACP_PCKT_RAW	
		NEW_ISRC1_PCKT_CLR			0						Do not clear	
					1						Clears NEW_ISRC1_PCKT_ST and NEW_ISRC1_PCKT_RAW	
		NEW_ISRC2_PCKT_CLR		0							Do not clear	
				1							Clears NEW_ISRC2_PCKT_ST and NEW_ISRC2_PCKT_RAW	
		NEW_GAMUT_MDATA_CLR Clear bit for NEW_GAMUT_MDATA_ST	0								Do not clear	
			1								Clears NEW_GAMUT_MDATA_ST and NEW_GAMUT_MDATA_RAW	

Table 89: User Map 1 Details Register 0x6D

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x6D R/W	HDMI_INT2_MASKB_4 Masks for interrupt 2	**NEW_AVI_INFO_MB2** Mask for NEW_AVI_INFO_ST bit								0	Mask	
										1	Unmask	
		NEW_AUDIO_INFO_MB2 Mask for NEW_AUDIO_INFO_ST bit							0		Mask	
									1		Unmask	
		NEW_SPD_INFO_MB2 Mask for NEW_SPD_INFO_ST bit						0			Mask	
								1			Unmask	
		NEW_MS_INFO_MB2 Mask for NEW_MS_INFO_ST_bit					0				Mask	
							1				Unmask	
		NEW_ACP_PCKT_MB2 Mask for NEW_ACP_PACKT_ST bit				0					Mask	
						1					Unmask	
		NEW_ISRC1_PCKT_MB2 Mask for NEW_ISRC1_PCKT_ST bit			0						Mask	
					1						Unmask	
		NEW_ISRC2_PCKT_MB2 Mask for NEW_ISRC2_PCKT_ST bit		0							Mask	
				1							Unmask	
		NEW_GAMUT_MDATA_MB2 Mask bit for NEW_GAMUT_MDATA_ST	0								Mask	
			1								Unmask	

Table 90: User Map 1 Details Register 0x6E

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x6E R/W	HDMI_INT1_MASKB_4 Masks for interrupt 1	**NEW_AVI_INFO_MB1** Mask for NEW_AVI_INFO_ST bit								0	Mask	
										1	Unmask	
		NEW_AUDIO_INFO_MB1 Mask for NEW_AUDIO_INFO_ST bit							0		Mask	
									1		Unmask	
		NEW_SPD_INFO_MB1 Mask for NEW_SPD_INFO_ST bit						0			Mask	
								1			Unmask	
		NEW_MS_INFO_MB1 Mask for NEW_MS_INFO_ST_bit					0				Mask	
							1				Unmask	
		NEW_ACP_PCKT_MB1 Mask for NEW_ACP_PACKT_ST bit				0					Mask	
						1					Unmask	
		NEW_ISRC1_PCKT_MB1 Mask for NEW_ISRC1_PCKT_ST bit			0						Mask	
					1						Unmask	
		NEW_ISRC2_PCKT_MB1 Mask for NEW_ISRC2_PCKT_ST bit		0							Mask	
				1							Unmask	
		NEW_GAMUT_MDATA_MB1 Mask bit for NEW_GAMUT_MDATA_S	0								Mask	
			1								Unmask	

Table 91: User Map 1 Details Register 0x6F (Read Only)

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x6F Read	HDMI_INT_STATUS_5	**AUDIO_PCKT_ERR_ST** Indicates if an uncorrectable error has been detected in the Audio Packets or not. This Bit is not active if associated Mask is set.								0	No uncorrectable error has been detected in the Audio Packets.	
										1	An uncorrectable error as been detected in an Audio Packet.	
		PACKET_ERROR_ST Indicates if an uncorrectable error in Packet header has been detected or not. This Bit is not active if associated Mask is set.							0		No uncorrectable error in Packet header has been detected.	
									1		Un uncorrectable error has been detected in an unknown Packet (Error in the Paket Header)	
		INFOFRAME_ERR_ST Indicates if an uncorrectable error has been detected in the InfoFrame Packets or not. This Bit is not active if associated Mask is set.						0			No uncorrectable error has been detected in the InfoFrame Packets.	
								1			An uncorrectable error has been detected in an InfoFrame Packets.	
		CHANGE_N_ST Indicates if Audio Clock Regeneration N value has changed or not. This Bit is not active if associated Mask is set.					0				Audio Clock Regeneration N value has not changed.	
							1				Audio Clock Regeneration N value has changed.	
		CTS_PASS_THRSH_ST Indicates if CTS changes by more than threshold or not (cf reg 10h HDMI Map). This Bit is not active if associated Mask is set.				0					Audio Clock Regeneration CTS value has not passed the threshold.	
						1					Audio Clock Regeneration CTS value has changes more than threshold	
		Reserved	x	x	x						Audio FIFO has not overflowed.	

Table 92: User Map 1 Details Register 0x6F (Write Only)

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x6F Write	HDMI_INT_CLR_5	**AUDIO_PCKT_ERR_CLR**								0	Do not clear	
										1	Clears AUDIO_PCKT_ERR_ST and AUDIO_PCKT_ERR_RAW	
		PACKET_ERROR_CLR							0		Do not clear	
									1		Clears PACKET_ERROR_ST and PACKET_ERROR_RAW	
		INFOFRAME_ERR_CLR						0			Do not clear	
								1			Clears INFOFRAME_ERR_ST and INFORFRAME_ERR_RAW	
		CHANGE_N_CLR					0				Do not clear	
							1				Clears CHANGE_N_ST and CHANGE_N_RAW	
		CTS_PASS_THRSH_CLR				0					Do not clear	
						1					Clears CTS_PASS_THRSH_ST and CTS_PASS_THRSH_RAW	
		Reserved	0	0	0						Set to 0	

Table 93: User Map 1 Details Register 0x70 to 0x71

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x70 R/W	HDMI_INT2_MASKB_5 Masks for interrupt 2	**AUDIO_PCKT_ERR_MB2** Mask for AUDIO PCKT ERR ST bit								0	Mask	
										1	Unmask	
		PACKET_ERROR_MB2 Mask for PACKET ERROR ST bit							0		Mask	
									1		Unmask	
		INFOFRAME_ERR_MB2 Mask for INFOFRAME ERR ST bit						0			Mask	
								1			Unmask	
		CHANGE_N_MB2 Mask for CHANGE N ST bit					0				Mask	
							1				Unmask	
		CTS_PASS_THRSH_MB2 Mask for CTS PASS THRSH ST bit				0					Mask	
						1					Unmask	
		Reserved	0	0	0						Set to 0	
0x71 R/W	HDMI_INT1_MASKB_5 Masks for interrupt 1	**AUDIO_PCKT_ERR_MB1** Mask for AUDIO PCKT ERR ST bit								0	Mask	
										1	Unmask	
		PACKET_ERROR_MB1 Mask for PACKET ERROR ST bit							0		Mask	
									1		Unmask	
		INFOFRAME_ERR_MB1 Mask for INFOFRAME ERR ST bit						0			Mask	
								1			Unmask	
		CHANGE_N_MB1 Mask for CHANGE N ST bit					0				Mask	
							1				Unmask	
		CTS_PASS_THRSH_MB1 Mask for CTS PASS THRSH ST bit				0					Mask	
						1					Unmask	
		Reserved	0	0	0						Set to 0	

Table 94: User Map 1 Details Register 0x72 (Read Only)

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x72 Read	HDMI_INT_STATUS_6	**FIFO_NEAR_UFLO_ST** Indicates if Audio FIFO has reached low threshold or not (cf reg12h HDMI map). This Bit is not active if associated Mask is set								0	Audio FIFO has not reached low threshold.	
										1	Audio FIFO has reached low threshold.	
		NEW_TMDS_FRQ_ST Indicates if TMDS frequancy has changed by more than tolerance or not (cf reg06h HDMI map). This Bit is not active if associated Mask is							0		TMDS frequancy has not changed by more than tolerance.	
									1		TMDS frequancy has changed by more than tolerance.	
		AUDIO_FLT_LINE_ST Indicates if Audio Sample Packet with flatline bit set has been received or not. This Bit is not active if associated Mask is set						0			Audio Sample Packet with flatline bit set has not been received.	
								1			Audio Sample Packet with flatline bit set has been received.	
		NEW_SAMP_RT_ST Indicates if sampling rate bits of the channel status on audio channel 0 have changed or not. This Bit is not active if associated Mask is set					0				The sampling rate bits of the channel status on audio channel 0 have not changed.	
							1				The sampling rate bits of the channel status on audio channel 0 have changed.	
		PARRITY_ERROR_ST Indicates if parrity error has been detected in the Audio Packets or not. This Bit is not active if associated Mask is set				0					No parrity error has detected in the Audio Packets.	
						1					A parrity error has been detected in an Audio Packet.	
		AKSV_UPDATE_ST Indicate and AKSV update from the HDMI transmitter. This indicates that the transmitter has initiated an authentication.			0						AKSV has not been updated	
					1						AKSV has been updated	
		VCLK_CHNG_ST Indicates if irregular or missing pulse detected in TMDS clock		0							No irregular or missing pulse detected in TMDS	
				1							Irregular or missing pulses detected in TMDS clock triggered this interrupt	
		DEEP_COLOR_CHNG_ST Indicates if deep color mode has changed	0								Deep color mode has not changed.	Refer to HDMI 1.3 spec.
			1								Change in deep color triggered this interrupt.	

Table 95: User Map 1 Details Register 0x72 (Write Only)

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x72 Write	HDMI_INT_CLR_6	**FIFO_NEAR_UFLO_CLR**								0	Do not clear	
										1	Clears FIFO_NEAR_UFLO_ST and FIFO_NEAR_UFLO_RAW	
		NEW TMDS FRQ CLR							0		Do not clear	
									1		Clears NEW_TMDS_FRQ_ST and NEW_TMDS_FRQ_RAW	
		AUDIO FLT LINE CLR						0			Do not clear	
								1			Clears AUDIO_FLT_LINE_ST and AUDIO_FLT_LINE_RAW	
		NEW SAMP RT CLR					0				Do not clear	
							1				Clears NEW_SAMP_RT_ST and NEW_SAMP_RT_RAW	
		PARRITY ERROR CLR				0					Do not clear	
						1					Clears PARRITY_ERROR_ST and PARRITY_ERROR_RAW	
		AKSV_UPDATE_CL			0						Do not clear	
					1						Clears AKSV_UPDATE_ST and AKSV_UPDATE_RAW	
		VCLK_CHNG_CL Clear bit for VCLK_CHNG_ST		0							Do not clear	
				1							Clears VCLK_CHNG_ST and	
		DEEP_COLOR_CHNG_CLR Clear bit for DEEP_COLOR_CHNG_ST	0								Do not clear	
			1								Clears DEEP_COLOR_CHNG_ST	

Table 96: User Map 1 Details Register 0x73 to 0x74

Sub address	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x73 R/W	HDMI_INT2_MASKB_6 Masks for interrupt 2	**FIFO_NEAR_UFLO_M2** Mask for FIFO NEAR UFLO ST bit								0	Mask	
										1	Unmask	
		NEW_TMDS_FRQ_M2 Mask for NEW TMDS FRQ ST bit							0		Mask	
									1		Unmask	
		AUDIO_FLT_LINE_M2 Mask for AUDIO FLT LINE ST bit						0			Mask	
								1			Unmask	
		NEW_SAMP_RT_MB2 Mask for NEW SAMP RT ST bit					0				Mask	
							1				Unmask	
		PARRITY_ERROR_M2 Mask PARRITY_ERROR_ST bit				0					Mask	
						1					Unmask	
		AKSV_UPDATE_M2 Mask for AKSV UPDATE ST			0						Mask	
					1						Unmask	
		VCLK_CHNG_MB2 Mask bit for VCLK CHNG ST		0							Mask	
				1							Unmask	
		DEEP_COLOR_CHNG_MB2 Mask bit for DEEP_COLOR_CHNG_ST	0								Mask	
			1								Unmask	
0x74 R/W	HDMI_INT2_MASKB_6 Masks for interrupt 1	**FIFO_NEAR_UFLO_M1** Mask for FIFO NEAR UFLO ST bit								0	Mask	
										1	Unmask	
		NEW_TMDS_FRQ_M1 Mask for NEW_TMDS_FRQ_ST							0		Mask	
									1		Unmask	
		AUDIO_FLT_LINE_M1 Mask for AUDIO_FLT_LINE_ST bit						0			Mask	
								1			Unmask	
		NEW_SAMP_RT_MB1 Mask for NEW_SAMP_RT_ST bit					0				Mask	
							1				Unmask	
		PARRITY_ERROR_M1 Mask PARRITY_ERROR_ST bit				0					Mask	
						1					Unmask	
		AKSV_UPDATE_M1 Mask for AKSV_UPDATE_ST			0						Mask	
					1						Unmask	
		VCLK_CHNG_MB1 Mask bit for VCLK CHNG ST		0							Mask	
				1							Unmask	
		DEEP_COLOR_CHNG_MB1 Mask bit for DEEP_COLOR_CHNG_ST	0								Mask	
			1								Unmask	

Table 97: User Map 1 Details Register 0x75

Sub address	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x75 R/W	DLL_ON_LLC_PATH	**DLL_ON_LLC_PHASE [4:0]**				0	0	0	0	0	32 phases available for the DLL	
						~	~	~	~	~		
						1	1	1	1	1		
		DLL_ON_LLC_MUX			0						Bypass the DLL	
					1						Mux the DLL output to the LLC output pin	
		DLL_ON_LLC		0							Disable the DLL	
				1							Enable the DLL	
		Reserved	0									

Table 98: User Map 1 Details Register 0x9A to 0x9E

Sub address	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x9A R/W	CP_CONTRAST	**CP_CONTRAST[7:0]** Contrast Adjustment control	1	0	0	0	0	0	0	0	Default gain of 1.0 Gain on Luma Channel (Gain Range 0 to 1.99)	VID_ADJ_EN must be set to 1
0x9B R/W	CP_SATURATION	**CP_SATURATION[7:0]** Satuturation Adjustment control	1	0	0	0	0	0	0	0	Default gain of 1.0 Gain on Chroma Channel (Gain Range 0 to 1.99)	VID_ADJ_EN must be set to 1
0x9C R/W	CP_BRIGHTNESS	**CP_BRIGHTNESS[7:0]** Brightness Adjustment control	0	0	0	0	0	0	0	0	Default Offset of 0 Offset of Luma channel. Register range of -128 to 127 to provide an Brightness range of 508d to -512d	VID_ADJ_EN must be set to 1
0x9D R/W	CP_HUE	**CP_HUE[7:0] Hue** Adjustment control	0	0	0	0	0	0	0	0	Default gain of 1.0 Phase on Chroma Channel (Range 0 to 180 degrees)	VID_ADJ_EN must be set to 1
0x9E R/W	VID_ADJ_BLANK_CTRL	Reserved		0	0	0	0	0	0	0	Reserved	
		VID_ADJ_EN Video Adjustment controls enable	0								Disable Color Controls	
			1								Enable Color Controls	

2.3 User Map 2

Table 99: User Map 2 Details Register 0xEA to 0xEF

Sub address	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0xEA R/W	hidden_slave_address	**RSV_ADDR[7:0]**	0	1	0	0	1	1	0	0	I2C address of the reserved map	
0xEB R/W	uss1_slave_address	**USS1_ADDR[7:0]**	0	1	0	0	0	1	0	0	I2C address of the User Sub Map 1	
0xEC R/W	vdp_slave_address	**VDP_ADDR[7:0]**	0	1	0	0	1	0	0	0	I2C address of theVDP Map (User Map 3)	
0xED R/W	ksv_slave_address	**KSV_ADDR[7:0]**	0	1	1	0	0	1	0	0	I2C address of the KSV Map	
0XEE R/W	edid_slave_address	**EDID_ADDR[7:0]**	0	1	1	0	1	1	0	0	I2C address of the EDID Map	
0xEF R/W	hdmi_slave_address	**ADDR_BIT[7:0]**	1	0	0	1	1	0	0	0	I2C address of the HDMI Map	

2.4 User Map 3 (VDP Map)

Table 100: User Map 3 Details Register 0x3C to 0x3F

Sub address	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x3C Read	VDP_cgms_typeb_data_1	**VDP_cgms_typeb_data[7:0]**	x	x	x	x	x	x	x	x	Decoded byte 1 of CGMS type B data	
0x3D Read	VDP_cgms_typeb_data_2	**VDP_cgms_typeb_data[15:8]**	x	x	x	x	x	x	x	x	Decoded byte 2 of CGMS type B data	
0x3E Read	VDP_cgms_typeb_data_3	**VDP_cgms_typeb_data[23:16]**	x	x	x	x	x	x	x	x	Decoded byte 3 of CGMS type B data	
0x3F Read	VDP_cgms_typeb_data_4	**VDP_cgms_typeb_data[31:24**	x	x	x	x	x	x	x	x	Decoded byte 4 of CGMS type B data	

Table 101: User Map 3 Details Register 0x40 to 0x46

Sub address	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x40 Read	Status Detection Register	**STATUS_CCAP**								0	Closed Captioning is not detected	
										1	Close Captioning is detected	
		STATUS_CCAP_EVEN_FIELD							0		Closed captioning on odd field	
									1		Closed captioning on even field	
		STATUS_WSS_CGMS						0			CGMS/WSS not detected	
								1			CGMS/WSS detected	
		Reserved					0				Reserved	
		STATUS_GS_VPS_PDC_UTC_CGMSTB				0					Gemstar, PDC, VPS, UTC, CGMSTB are not detected	
						1					Gemstar, PDC, VPS, UTC, CGMSTB are detected	
		STATUS_GEMS_TYPE			0						GEMSTAR 1x detected	
					1						GEMSTAR 2x detected	
		STATUS_VITC		0							VITC data has not been detected	
				1							VITC data has been detected	
		STATUS_TTXT	0								Teletext not detected	
			1								Teletext detected	
0x41 Read	VDP CCAP Data 0	**VDP_CCAP_DATA[7:0]**	0	0	0	0	0	0	0	0	Decoded Byte1 of CCAP data	
0x42 Read	VDP CCAP Data 1	**VDP_CCAP_DATA[15:8]**	0	0	0	0	0	0	0	0	Decoded Byte 2 of CCAP data	
0x43 Read	VDP CGMS WSS Data 1	**VDP_CGMS_WSS_DATA[23:16]**	0	0	0	0	0	0	0	0	Decoded CGMS[23:16]	
0x44 Read	VDP CGMS WSS Data 2	**VDP_CGMS_WSS_DATA[15:8]**	0	0	0	0	0	0	0	0	Decoded CGMS[15:8] /WSS[13:8] data	
0x45 Read	VDP CGMS WSS Data 3	**VDP_CGMS_WSS_DATA[7:0]**	0	0	0	0	0	0	0	0	Decoded CGMS[7:0] / WSS[7:0] data	
0x46 Read	VDP WSS Biphase Error Count	**VDP_WSS_BIPHASE_ERROR_COUNT[3:0]**					0	0	0	0	Number of errors encountered while decoding the biphase WSS standard. Each bit is represented by positive or negative transition. If these transitions are not detected by VDP during bit-time, error count is increased.	
		Reserved	x	x	x	x					Reserved	

Table 102: User Map 3 Details Register 0x47 to 0x54

Sub address	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x47 Read	VDP GS VPS UTC CGMSTB Data 0	**VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[7:0]**	0	0	0	0	0	0	0	0	Gemstar, PDC, VPS, UTC, CGMSTB readback register	
0x48 Read	VDP GS VPS UTC CGMSTB Data 1	**VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[15:8]**	0	0	0	0	0	0	0	0	Gemstar, PDC, VPS, UTC, CGMSTB readback register	
0x49 Read	VDP GS VPS UTC CGMSTB Data 2	**VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[23:16]**	0	0	0	0	0	0	0	0	Gemstar, PDC, VPS, UTC, CGMSTB readback register	
0x4A Read	VDP GS VPS UTC CGMSTB Data 3	**VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[31:24]**	0	0	0	0	0	0	0	0	Gemstar, PDC, VPS, UTC, CGMSTB readback register	
0x4B Read	VDP GS VPS UTC CGMSTB Data 4	**VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[39:32]**	0	0	0	0	0	0	0	0	Gemstar, PDC, VPS, UTC, CGMSTB readback register	
0x4C Read	VDP GS VPS UTC CGMSTB Data 5	**VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[47:40]**	0	0	0	0	0	0	0	0	Gemstar, PDC, VPS, UTC, CGMSTB readback register	
0x4D Read	VDP GS VPS UTC CGMSTB Data 6	**VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[55:41]**	0	0	0	0	0	0	0	0	Gemstar, PDC, VPS, UTC, CGMSTB readback register	
0x4E Read	VDP GS VPS UTC CGMSTB Data 7	**VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[63:56]**	0	0	0	0	0	0	0	0	Gemstar, PDC, VPS, UTC, CGMSTB readback register	
0x4F Read	VDP GS VPS UTC CGMSTB Data 8	**VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[71:64]**	0	0	0	0	0	0	0	0	Gemstar, PDC, VPS, UTC, CGMSTB readback register	
0x50 Read	VDP GS VPS UTC CGMSTB Data 9	**VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[79:72]**	0	0	0	0	0	0	0	0	Gemstar, PDC, VPS, UTC, CGMSTB readback register	
0x51 Read	VDP GS VPS UTC CGMSTB Data 10	**VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[87:80]**	0	0	0	0	0	0	0	0	Gemstar, PDC, VPS, UTC, CGMSTB readback register	
0x52 Read	VDP GS VPS UTC CGMSTB Data 11	**VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[95:88]**	0	0	0	0	0	0	0	0	Gemstar, PDC, VPS, UTC, CGMSTB readback register	
0x53 Read	VDP GS VPS UTC CGMSTB Data 12	**VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[103:96]**	0	0	0	0	0	0	0	0	Gemstar, PDC, VPS, UTC, CGMSTB readback register	
0x54 Read	VDP VPS Biphase Error Count	**VDP_VPS_BIPHASE_ERROR_COUNT[7:0]**	0	0	0	0	0	0	0	0	Indicates number of errors encountered while decoding the biphase VPS standard. Each bit is represented by positive or negative transition. If these transitions are not detected by VDP during bit-time, error count is increased.	

Table 103: User Map 3 Details Register 0x55 to 0x60

Sub address	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x55 Read	VDP VITC Data 0	**VDP_VITC_DATA[7:0]**	0	0	0	0	0	0	0	0	VITC readback register	
0x56 Read	VDP VITC Data 1	**VDP_VITC_DATA[15:8]**	0	0	0	0	0	0	0	0	VITC readback register	
0x57 Read	VDP VITC Data 2	**VDP_VITC_DATA[23:16]**	0	0	0	0	0	0	0	0	VITC readback register	
0x58 Read	VDP VITC Data 3	**VDP_VITC_DATA[31:24]**	0	0	0	0	0	0	0	0	VITC readback register	
0x59 Read	VDP VITC Data 4	**VDP_VITC_DATA[39:32]**	0	0	0	0	0	0	0	0	VITC readback register	
0x5A Read	VDP VITC Data 5	**VDP_VITC_DATA[47:40]**	0	0	0	0	0	0	0	0	VITC readback register	
0x5B Read	VDP VITC Data 6	**VDP_VITC_DATA[55:48]**	0	0	0	0	0	0	0	0	VITC readback register	
0x5C Read	VDP VITC Data 7	**VDP_VITC_DATA[63:56]**	0	0	0	0	0	0	0	0	VITC readback register	
0x5D Read	VDP VITC Data 8	**VDP_VITC_DATA[71:64]**	0	0	0	0	0	0	0	0	VITC readback register	
0x5E Read	VDP VITC CALC CRC	**VDP_VITC_CALC_CRC[7:0]**	0	0	0	0	0	0	0	0	VITC readback register	
0x5F	Reserved	Reserved									Reserved	
0x60 R/W	VDP Config 1	**VDP_TTXT_TYPE[1:0]**							0	0	ITU_BT.653-625/50-A	
									0	1	ITU_BT.653-625/50-B(WST) ITU_BT.653-625/60-B	
									1	0	ITU_BT.653-625/50-C(WST) ITU_BT.653-625/60-C or EIA516(NABTS)	
									1	1	ITU_BT.653-625/50-D ITU_BT.653-625/50-D	
		VDP_TTXT_TYPE_MAN_EN						0			User programming of teletext disabled	
								1			User programming of teletext enabled	
		EN_FC_WINDOW_AFTER_					1				Robust - combines scheme1 and	
		CRI					0				Only scheme1	
		SOFT_ERROR_CORRECTI				0					Soft error correction disabled	
		ON_EN				1					Soft error correction enabled	
		Reserved		0	0						Set to 0	
		HAM_ERR_OP_EN	0								Enable hamming code error in the output data	
			1								Disable hamming code error in the output data	

Table 104: User Map 3 Details Register 0x61 to 0x63

Sub address	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x61 R/W	VDP Config 2	**Reserved**				1	0	0	0	0	Set to default	
		NOISE_CLK_DISABLE			0							
					1						Enable noise clock feature for CRI detection	
		Reserved		0							Set to default	
		VDP_CP_CLMP_AVG	0								16 samples are taken for averaging to calculate clamp-levels	
			1								32 samples are taken for averaging to calculate clamp-levels	
0x62 R/W	VDP ADF Config 1	**DID6_2[4:0]** See Comment				1	0	1	0	1	User specified DID sent in the ancillary stream with VBI decoded data	This functionally has not been tested
											ADF enabled	
		ADF_MODE[2:0] See Comment		0	0						Nibble mode (default)	
				0	1						Byte mode, no code restrictions	
				1	0						Byte mode, but 0x00 and 0xFF prevented (0x00->0x01) (0xFF->0xFE)	
				1	1						Reserved	
		ADF_EN See Comment	0								Disable insertion of VBI decoded data into ancillary 656 stream	
			1								Enable insertion of VBI decoded data into ancillary 656 stream	
0x63 R/W	VDP ADF Config 2	**SDID7_2[5:0]** See Comment			1	0	1	0	1	0	User specified SDID sent in the ancillary stream with VBI decoded data	This functionally has not been tested
		Reserved		0							Reserved	
		TOGGLE_ADF See Comment	0								Ancillary data packet is spread across the Y and C data streams	
			1								Ancillary data packet is duplicated across the Y and C data streams	

Table 105: User Map 3 Details Register 0x64 to 0x77

Sub address	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x64 R/W	VDP Man Line 1 21	**VDP_MAN_LINE_1_21[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x65 R/W	VDP Man Line 2 22	**VDP_MAN_LINE_2_22[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x66 R/W	VDP Man Line 3 23	**VDP_MAN_LINE_3_23[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x67 R/W	VDP Man Line 4 24	**VDP_MAN_LINE_4_24[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x68 R/W	VDP Man Line 5 25	**VDP_MAN_LINE_5_25[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x69 R/W	VDP Man Line 6 26	**VDP_MAN_LINE_6_26[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x6A R/W	VDP Man Line 7 27	**VDP_MAN_LINE_7_27[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x6B R/W	VDP Man Line 8 28	**VDP_MAN_LINE_8_28[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x6C R/W	VDP Man Line 9 29	**VDP_MAN_LINE_9_29[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x6D R/W	VDP Man Line 10 30	**VDP_MAN_LINE_10_30[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x6E R/W	VDP Man Line 11 31	**VDP_MAN_LINE_11_31[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x6F R/W	VDP Man Line 12 32	**VDP_MAN_LINE_12_32[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x70 R/W	VDP Man Line 13 33	**VDP_MAN_LINE_13_33[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x71 R/W	VDP Man Line 14 34	**VDP_MAN_LINE_14_34[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x72 R/W	VDP Man Line 15 35	**VDP_MAN_LINE_15_35[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x73 R/W	VDP Man Line 16 36	**VDP_MAN_LINE_16_36[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x74 R/W	VDP Man Line 17 37	**VDP_MAN_LINE_17_37[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x75 R/W	VDP Man Line 18 38	**VDP_MAN_LINE_18_38[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x76 R/W	VDP Man Line 19 39	**VDP_MAN_LINE_19_39[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	
0x77 R/W	VDP Man Line 20 40	**VDP_MAN_LINE_20_40[7:0]**	0	0	0	0	0	0	0	0	Manual VDP Configuration Registers	

Table 106: User Map 3 Details Register 0x78

Sub address	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x78 R/W	VDP Status Clear	**STATUS_CLEAR_CCAP**								0	Not necessary as STATUS_CLEAR_CCAP bit is self clearing	
										1	Refreshes the CCAP readback	
		Reserved							0		Reserved	
		STATUS_CLEAR_WSS_CGMS						0			Not necessary as CGMS/WSS bit is self clearing	
								1			Refreshes the CGMS and WSS readback registers	
		Reserved					0				Set to default	
		STATUS_CLEAR_GS_VPS_PDC_UTC_CGMSTB				0					Not necessary as STATUS_CLEAR_GS_VPS_PDC_UTC_CGMSTB register is self clearing	
						1					Refreshes the STATUS_CLEAR_GS_VPS_PDC_UTC_CGMSTB readback registers	
		Reserved			0						Reserved	
		STATUS_CLEAR_VITC		0							Not necessary as STATUS_CLEAR_VITC register is self clearing	
				1							Refreshes the VITC readback registers	
		STATUS_CLEAR_TXTT	0								Not necessary as STATUS_CLEAR_TXTT register is self clearing	
			1								Refreshes the TTXT readback	

Table 107: User Map 3 Details Register 0x98 to 0x99

Sub address	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x98 R/W	VDP Filter Adaptive slicer Config	**Reserved**						0	0	0	Set to default	
		ADAP2_SI_CONFIG_ENA					0				Disable Peak-Tracking Slicer	
							1				Enable Peak-Tracking Slicer	
		TTX_SEL				0					Disable Teletext Serial Data out	
						1					Enable Teletext Serial Data out enable	
		ADAP1_SL_CONFIG_ENA			0						Disable duty-cycle based slicer	
					1						Enable duty-cycle based slicer	
		Reserved		0							Set to default	
		LOW_DATA_STD_FILTER_EN	0								Disable filter for low data rate	
			1								Enable filter for low data rate	
0x99 R/W	VDP ADAP2 STD EN	**ADAP2_CCAP_STD_EN**								0	CCAP standard not enabled	
										1	Enable CCAP standard	
		Reserved							0		Reserved	
		ADAP2_WSS_CGMS_STD_EN						0			WSS-CGMS standard not enabled	
								1			Enable WSS-CGMS standard	
		ADAP2_VPS_STD_EN					0				VPS standard not enabled	
							1				Enable VPS standard	
		ADAP2_GEMS_STD_EN				0					GEMSTAR-1x,GEMSTAR-2x	
						1					Enable GEMSTAR-1x,GEMSTAR-2x	
		Reserved			0						Reserved	
		ADAP2_VITC_STD_EN		0							VITC standard not enabled	
				1							Enable VITC standard	
		ADAP2_TTXT_STD_EN	0								TTXT standard not enabled	
			1								Enable TTXT standard	

Table 108: User Map 3 Details Register 0x9C

Sub address	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	Comment
0x9C R/W	VDP STATUS CONFIG	**GS_VDP_PDC_UTC_CGMSTB[2:0]**						0	0	0	Gemstar 1x/2x	
								0	0	1	VPS	
								0	1	0	PDC	
								0	1	1	UTC	
								1	0	0	CGMS type B	
								1	0	1	Reserved	
								1	1	0	Reserved	
								1	1	1	Reserved	
		RAW_STATUS_ENABLE					0				Disable raw status and data	
							1				Enable raw status and data	
		WSS_CGMS_CB_CHANGE				0					Disable content based update of WSS, CGMS data	
						1					Enable content based update of WSS, CGMS data	
		GS_VPS_PDC_UTC_CB_CHANGE			0						Disable content based update of VPS, PDC, UTC data	
					1						Enable content based update of UTC, PDC, UTC data	
		Reserved	0	0							Reserved	

2.5 HDMI Map

Table 109: HDMI Map Details Register 0x00 to 0x02

Sub address	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x00 R/W	REGISTER_00H	**HDMI_PORT_SELECT** Manual HMDI port selection. This must be set by the user based on the TMDS clock detect status bits (register 4h, bits 3:2) and system level port priority preference.								0	Port A	
										1	Port B	
		HDCP_ONLY_MODE Used in simultaneous HDMI and CP Mode only							0		HDMI video processing operational	Can be used as a power saving feature in simultaneous HDMI and CP operation
									1		HDMI video processing stopped but HDCP circuitry is enabled and continuously monitoring.	
		[7:2] Reserved	0	0	0	0	0	0			Set to default	
0x01 R/W	REGISTER_01H	**[4:0]** Reserved				0	1	0	0	0	Set to default	
		CLOCK_TERM_PORT_B Termination control for Port B			0						Enable Clock, Channel 0, Channel 1 and Channel 2 terminations of Port B	
					1						Disable Clock, Channel 0, Channel 1 and Channel 2 terminations of Port B	
		CLOCK_TERM_PORT_A Termination control for Port A		0							Enable Clock, Channel 0, Channel 1 and Channel 2 terminations of Port A	
				1							Disable Clock, Channel 0, Channel 1 and Channel 2 terminations of Port A	
		AUDIOPLL_PDN Audio PLL power mode	0								Synthesizer and Analog PLL in normal operation	
			1								Power down the PLL synthesizer and the analog PLL	
0x02 R/W	REGISTER_02H	**MUX_DSD_OUT** I2S /DSD MUX Control								0	Force I2S output	
										1	Force DSD output	
		OVR_AUTO_MUX_DSD_OUT I2S/DSD Automatic mux override							0		Enable automatic muxing between DSD and I2S	
									1		Set DSD/ I2S muxing in manual mode. The active digital audio interface output is set by MUX_DSD_OUT.	
		Reserved	0								Set to 0	
		HDCP_A0 Set the LSB of the address of the HDCP I2C.					0				ALSB low. I2C adress of the HDCP registers is 0x74.	Set to 1 only for a second receiver dual-link configuration
							1				ALSB high. I2C address of the HDCP registers is 0x76.	
		I2S_TRISTATE				0					Normal I2S output	
						1					I2S output and MCLK in high impedance	
		SPDIF_TRISTATE			0						Normal spdif output	
					1						spdif pins in high impedance	
		Reserved	0	0							Set to default	

Table 110: HDMI Map Details Register 0x03

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x03 R/W	REGISTER_03H	**I2SBITWIDTH[4:0]** I2S Bit Width. Set the desired bit width for right justified mode.				0	0	0	0	0		
						0	0	0	0	1		
						0	0	0	1	0		
						0	0	0	1	1		
						0	0	1	0	0		
						0	0	1	0	1		
						0	0	1	1	0		
						0	0	1	1	1		
						0	1	0	0	0		
						0	1	0	0	1		
						0	1	0	1	0		
						0	1	0	1	1		
						0	1	1	0	0		
						0	1	1	0	1		
						0	1	1	1	0		
						0	1	1	1	1		
						1	0	0	0	0		
						1	0	0	0	1		
						1	0	0	1	0		
						1	0	0	1	1		
						1	0	1	0	0		
						1	0	1	0	1		
						1	0	1	1	0		
						1	0	1	1	1		
						1	1	0	0	0	24 bits	
						1	1	0	0	1		
						1	1	0	1	0		
						1	1	0	1	1		
						1	1	1	0	0		
						1	1	1	0	1		
						1	1	1	1	0		
						1	1	1	1	1		
		I2SOUTMODE[1:0] I2S Output Mode		0	0						I2S mode	
				0	1						Right justified	
				1	0						Left justified	
				1	1						Raw IEC60958 mode	
		Reserved	0								Set to 0	

Table 111: HDMI Map Details Register 0x04 to 0x05

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x04 Read	REGISTER_04H	**AUDIO_PLL_LOCKED**								0	Audio PLL has not locked	
										1	Audio PLL has locked	
		VIDEO_PLL_LOCKED							0		TMDS PLL has not locked to incoming TMDS clock	
									1		TMDS PLL has locked to incoming TMDS clock	
		TMDS_PORT_B_ACTIVE Detects a TMDS clock on port B						0			No TDMS clock present on port B	
								1			TDMS clock detected on port B	
		TMDS_PORT_A_ACTIVE Detects a TMDS clock on port A					0				No TDMS clock present on port A	
							1				TDMS clock detected on port A	
		HDCP_KEY_ERROR				0					HDCP keys not rread yet or read error occurred	
						1					Error encounted when reading HDCP keys	
		HDCP_KEYS_READ			0						HDCP keys not read yet or read error may have occurred	
					1						HDCP keys read	
		AV_MUTE. Gives the status of AVMute based on General Control		0							AV not muted	
				1							AV muted	
		Reserved	x								Reserved	
0x05 Read	REGISTER_05H	**HDMI_PIXEL_REPETITION[3:0]** Returns currents HDMI pixel repetition value. The clock and data output automatically de-repeat by this value.					0	0	0	0	1X	
							0	0	0	1	2X	
							0	0	1	0	3X	
							0	0	1	1	4X	
							0	1	0	0	5X	
							0	1	0	1	6X	
							0	1	1	0	7X	
							0	1	1	1	8X	
							1	0	0	0	9X	
							1	0	0	1	10X	
							1	0	1	0	Reserved	
							~	~	~	~	Reserved	
							1	1	1	1	Reserved	
		DVI_VSYNC_POLARITY Returns DVI Vsync polarity				0					Vsync polarity is low active	
						1					Vsync polarity is high active	
		DVI_HSYNC_POLARITY Returns DVI Hsync polarity			0						Hsync polarity is low active	
					1						Hsync polarity is high active	
		HDMI_CONTENT_ENCRYPTED		0							HDCP is not being used	
				1							HDCP decryption is in use	
		HDMI_MODE This bit reports which signal tyoe is currently being received (HDMI or DVI)	0								DVI Mode	
			1								HDMI mode	

Table 112: HDMI Map Details Register 0x06 to 0x08

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x06 Read		**TMDSFREQ[7:0]** Measured Frequency of TMDS input in MHz	x	x	x	x	x	x	x	x	Measured Frequency of TMDS input in MHz	
0x07 Read	REGISTER_07H	**LINE_WIDTH[11:0]** Line Width. Width of the incoming active DE line in pixels.										
		LINE_WIDTH[11:8] See LINE_WIDTH[11:8] above					x	x	x	x		
		DE_REGEN_FILTER_LOCKED				0					DE Regeneration not locked to the incoming DE	
						1					DE Regeneration locked to the incoming DE	
		AUDIO_CHANNEL_MODE			0						Stereo Audio (may be compressed multichannel)	
					1						Multi-Channel Uncompressed Audio (3-8 channels)	
		VERT_FILTER_LOCKED		0							The vertical filter has not locked	
				1							The vertical filter has locked and vertical synchronization parameters are valid for read back	
		Reserved	x									
0x08 Read	LINE WIDTH	**LINE_WIDTH[7:0]** See desciption of LINE_WIDTH[7:0] in Register 0x07	x	x	x	x	x	x	x	x		

Table 113: HDMI Map Details Register 0x09 to 0x10

Sub address	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x09 Read	FIELD 0 HEIGHT MSB	**FIELD_0_HEIGHT[11:0]** Field 0 Height. Height of the active portion of field 0 (Valid only if DE Regeneration is locked)										Height is in lines.
		FIELD_0_HEIGHT[11:8] See FIELD_0_HEIGHT[11:0] above					x	x	x	x		
		[7:5] Reserved	x	x	x	x						
0x0A Read	FIELD 0 HEIGHT	**FIELD_0_HEIGHT[7:0]** See description of FIELD_0_HEIGHT[11:0] in register 0x09	x	x	x	x	x	x	x	x		
0x0B Read	REGISTER_0BH	**FIELD_1_HEIGHT[11:0]** Field 1 Height. Height of the active portion of Field 1.(valid only if DE Regeneration is locked and Interlaced is 1).										Height is in lines
		FIELD_1_HEIGHT[11:8] See FIELD_1_HEIGHT[11:0] above.					x	x	x	x		
		Reserved				x						
		DEEP_COLOR[1:0] Gives information on detected color format currently being processed		0	0						8 bit color per channel	
				0	1						10 bit color per channel (This mode is not supported)	
				1	0						12 bit color per channel	
				1	1						16 bit color per channel (This mode is not supported)	
		Reserved	x									
0x0C Read	FIELD 1 HEIGHT	**FIELD_1_HEIGHT[7:0]** See description of FIELD_1_HEIGHT[11:0] in register 0x0B	x	x	x	x	x	x	x	x		
0x0D R/W		**FREQTOLERANCE[3:0]** Tolerance of the TDMS frequency detection (for interrupt and status bit)					0	1	0	0	Sets the frequency tolerance for the mute mask MT_MSK_VFREQ_CHNG. An audio mute occures if the TMDS frequency changes by more than the tolerance specified by FREQTOLERANCE[3:0]	
		Reserved	0	0	0	0					Set to default	
0x0E R/W	REGISTER_0EH	Reserved	1	0	0	0	1	1	1	1	Set to default	
0x0F R/W	AUDIO MUTE SPEED	**AUDIO_MUTE_SPEED[5:0]** Number of Audio samples per 6dB attenuation			1	1	1	1	1	1	Defines the number audio samples +1, per 6dB attenuation during audio muting.	
		AUDIO_DELAY_LINE_BYPASS Control to enable disable the audio delay line in manual mode.		0							Enable the audio delay line. Only valid if MAN_AUDIO_DL_BYPASS is set to 1.	
				1							Bypass the audio delay line. Only valid if MAN_AUDIO_DL_BYPASS is set to 1.	
		MAN_AUDIO_DL_BYPASS Audio Delay Bypass Manual Enable	0								Audio delay line is automatically bypassed if multichannel audio is received. The audio delay line is automatically enabled if stereo audio is received.	
			1								Override automatic bypass of audio delay line. The audio delay line is bypassed if AUDIO_DELAY_LINE_BYPASS is set to 1. The audio delay line is enabled if AUDIO_DELAY_LINE_BYPASS is set to 0.	
0x10 R/W	HDMI_REG_10H	**CTS_CHANGE_THRESHOLD[5:0]** Set the amounts of LSB's that the CTS can change before a mute/interrupt			0	0	0	1	1	1		
		[7:6] Reserved	0	0							Set to default	

Table 114: HDMI Map Details Register 0x11 to 0x13

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x11 R/W		Reserved	0	0	0	0	0	1	1	1		
0x12 R/W		Reserved	0	0	0	0	0	0	1	0		
0x13 R/W	AUDIO COST MASK	**AC_MSK_VCLK_DET** TMDS Clock Detect Setting this mask causes the audio PLL to coast if TMDS Clock is not detected								0	Disables the mask	
										1	Enables the mask	
		AC_MSK_CHNG_PORT HDMI Port change. Setting this mask causes the audio PLL to coast if TMDS clock is not detected							0		Disables the AC_MSK_CHNG_PORT mask	
									1		Enables the AC_MSK_CHNG_PORT mask	
		AC_MSK_NEW_N -New N. Setting this mask causes the audio PLL to coast if N changes						0			Disables the AC_MSK_NEW_N mask	
								1			Enables the AC_MSK_NEW_N mask	
		AC_MSK_NEW_CTS -New CTS. Setting this mask causesthe audio PLL to coast if CTS changes by more than threshold.					0				Disables the AC_MSK_NEW_CTS mask	
							1				Enables the AC_MSK_NEW_CTS mask	
		AC_MSK_VFREQ_CHNG TMDS Frequency change. Setting this mask causes the audio PLL to coast if TMDS frequancy changes by more than threshold				0					Disables the AC_MSK_VFREQ_CHNG mask	
						1					Enables the AC_MSK_VFREQ_CHNG mask	
		AC_MSK_VPLL_UNLOCK TMDS PLL Unlock. Setting this mask causes the audio PLL to coast if TMDS PLL unlocks.			0						Disables the AC_MSK_VPLL_UNLOCK mask	
					1						Enables the AC_MSK_VPLL_UNLOCK mask	
		AC_MSK_VCLK_CHNG TMDS Clock change- Setting this mask causes the audio PLL to coast if TMDS Clock has any irregular/missing pulses		0							Disables the AC_MSK_VCLK_CHNG mask	
				1							Enables the AC_MSK_VCLK_CHNG mask	
		Reserved	0								Set to default	

Table 115: HDMI Map Details Register 0x14 to 0x15

Sub address	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x14 R/W	MUTE MASK 19_16	**MT_MSK_VCLK_CHNG** TDMS Clock Change.Setting this mute mask causes an audio mute if TMDS Clock has irregular/missing pulses.								0	Disable mute mask MT_MSK_VCLK_CHNG	
										1	Enable mute mask MT_MSK_VCLK_CHNG	
		MT_MSK_PARITY_ERR Parrity Error. Setting this mute mask causes an audio mute if parity bits in the audio samples are not correct.							0		Disable mute mask MT_MSK_VCLK_CHNG	
									1		Enable mute mask MT_MSK_VCLK_CHNG	
		Reserved					1	1			Set to 11	
		MT_MSK_CHNG_DSD_PCM Setting this mute mask causes an audio mute if the audio changes from PCM to DSD and visa versa.				0					Disable mute mask MT_MSK_VCLK_CHNG	
						1					Enable mute mask MT_MSK_VCLK_CHNG	
		MT_MSK_COMPRS_AUD Setting this mute mask causes an audio mute on the I2S interface if the audio is compressed.			0						Disable mute mask MT_MSK_VCLK_CHNG	
					1						Enable mute mask MT_MSK_VCLK_CHNG	
		[7:6] Reserved	0	0							Set to 00	
0x15 R/W	MUTE_MASK 15_8	**Reserved**								0	Set to 0	
										1		
		Reserved							0		Set to 0	
									1			
		MT_MSK_VFREQ_CHNG TMDS Frequency Change. Setting this mute mask causes an audio mute if TMDS Frequency changes by more than the threshold specified by FREQTOLERANCE[3:0].						0			Disable mute mask MT_MSK_VFREQ_CHNG	
								1			Enable mute mask MT_MSK_VFREQ_CHNG	
		MT_MSK_FLATLINE_DET Flatline Det.Setting this mute mask causes an audio mute if flatline bit set in the Audio Packets					0				Disable mute mask MT_MSK_FLATLINE_DET	
							1				Enable mute mask MT_MSK_FLATLINE_DET	
		MT_MSK_SAMP_RT_CHNG Sample Rate change. Setting this mute mask causes an audio mute if the audio sample rate specified in the channel status data of channel 0 has changed.				0					Disable mute mask MT_MSK_SAMP_RT_CHNG	
						1					Enable mute mask MT_MSK_SAMP_RT_CHNG	
		MT_MSK_ACR_NOT_DET ACR Packet Detect. Setting this mute mask causes an audio mute if ACR Packet not received within required time interval			0						Disable mute mask MT_MSK_ACR_NOT_DET	
					1						Enable mute mask MT_MSK_ACR_NOT_DET	
		MT_MSK_VPLL_UNLOCK TMDS PLL Unlock. Setting this mute mask causes an audio mute if TMDS PLL unlocks.		0							Disable mute mask MT_MSK_VPLL_UNLOCK	
				1							Enable mute mask MT_MSK_VPLL_UNLOCK	
		MT_MSK_APLL_UNLOCK Audio OLL Unlock. Setting this mute mask causes an audio mute if Audio PLL unlocks.	0								Disable mute mask MT_MSK_APLL_UNLOCK	
			1								Enable mute mask MT_MSK_APLL_UNLOCK	

Table 116: HDMI Map Details Register 0x16

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x16 R/W	MUTE_MASK_7_0	**MT_MSK_VCLK_DET** TMDS Clock Detect.Setting this mute mask cause an audio mute if the TMDS clock is not detected								0	Disable mute mask MT_MSK_VCLK_DET	
										1	Enable mute mask MT_MSK_VCLK_DET	
		MT_MSK_CHNG_PORT Port Change. Setting this mute mask cause an audio mute if the HDMI active is changed							0		Disable mute mask MT_MSK_CHNG_PORT	
									1		Enable mute mask MT_MSK_CHNG_PORT	
		MT_MSK_APCKT_ECC_ERR Audio Packet ECC error. Setting this mute mask cause an audio mute if an uncorrectable error is detected in the						0			Disable mute mask MT_MSK_APCKT_ECC_ERR	
								1			Enable mute mask MT_MSK_APCKT_ECC_ERR	
		MT_MSK_CHMODE_CHNG Audio Channel Mode change. Setting this mute mask cause an audio mute if the channel mode changes from stereo to multichannel or vica versa.					0				Disable mute mask MT_MSK_CHMODE_CHNG	
							1				Enable mute mask MT_MSK_CHMODE_CHNG	
		MT_MSK_NEW_N New N.Setting this mute mask cause an audio mute if N changes.				0					Disable mute mask MT_MSK_NEW_N	
						1					Enable mute mask MT_MSK_NEW_N	
		MT_MSK_NEW_CTS New CTS. Setting this mute mask cause an audio mute if CTS changes by more than the threshold specified by			0						Disable mute mask MT_MSK_NEW_CTS	
					1						Enable mute mask MT_MSK_NEW_CTS	
		MT_MSK_NOT_HDMIMODE. Causes audio to mute if HDMI Mode bit goes low.		0							Disable mute mask MT_MSK_NOT_HDMIMODE	
				1							Enable mute mask MT_MSK_NOT_HDMIMODE	
		MT_MSK_AVMUTE Setting this mute mask cause an audio mute if AVMute is set by a General Control Packet.	0								Disable mute mask MT_MSK_AVMUTE	
			1								Enable mute mask MT_MSK_AVMUTE	

Table 117: HDMI Map Details Register 0x17

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x17 Read	PACKET DETECTED MSB	**AUDIO_SAMPLE_PCKT_DET** Audio Sample Packet Detection.								0	No Audio sample packet received within the last 10 Hsync. This bit reset to zero on the 11th Hsync leading edge following a Audio packet or if a DSD packet sample packets has been received or after an HDMI reset condition.	HDMI reset condition is: part powerd up/ reset or a new TMDS frequency is detected.
										1	Audio sample packet received	
		ACR_PACKET_DET Audio Clock Regeneration Packet Detection since last HDMI reset condition.							0		No ACR packet received	Refer to bit 0 reg17h for HDMI reset condition
									1		Packet received	
		GC_PACKET_DET General Control Packet Detection the since last HDMI reset condition.						0			No General Control packet reveived.	Refer to bit 0 reg17h for HDMI reset condition
								1			General Control packet received	
		INFOFRAME_PCKT_DET Infoframes Packet Detection since the last HDMI reset condition.					0				No Infoframe packets received	Refer to bit 0 reg17h for HDMI reset condition
							1				High if any Infoframes packets received	
		GAMUT_MDATA_PCKT_DET Indicates if Gamut metadata packet received in last Vsync				0					No Gamut metadata packet received within last Vsync	
						1					Gamut metadata packet received within last Vsync	
		HBR_AUDIO_PCKT_DET Indicates if HBR audio stream packets are being detected.			0						No HBR audio stream packets received	
					1						HBR audio stream packets are being received. This bit is cleared back to 0 on the leading edge of the 11th following 10 hsyncs without any HBR packets.	
		DST_AUDIO_PCKT_DET Indicates if DST audio packets are being detected.		0							No DST audio packets received	
				1							DST audio packets are being received. . This bit is cleared back to 0 on the leading edge of the 11th following 10 hsyncs without any DST packets.	
		Reserved	x									

Table 118: HDMI Map Details Register 0x18

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x18 Read	PACKET DETECTED	**AVI_INFOFRAME_DET** AVI Infoframe Detection								0	No AVI Infoframe has been received within the last 7 Vsyncs. This bit reset to zero on the 8th Vsync leading edge following an AVI InfoFrame or after an HDMI reset condition.	Refer to bit 0 reg17h for HDMI reset condition
										1	An AVI Infoframe has been received.	
		AUDIO_INFOFRAME_DET Audio Infoframe Detection							0		No Audio Infoframe has been received within the last 3 Vsyncs. This bit reset to zero on the 4th Vsync leading edge following an Audio InfoFrame packet or after an HDMI reset condition.	Refer to bit 0 reg17h for HDMI reset condition
									1		An audio Infoframe has been received.	
		SPD_INFOFRAME_DET Source Product Descriptor Infoframe Detection						0			No Source Product Descriptor Infoframe received since the last HDMI reset condition	Refer to bit 0 reg17h for HDMI reset condition
								1			Source Product Descriptor Infoframe received	
		MS_INFOFRAME_DET MPEG Source Infoframe Detection					0				No MPEG Source Infoframe received within the last 3 Vsyncs. This bit reset to zero on the 4th Vsync leading edge following an MPEG Source InfoFrame packet or after an HDMI reset condition.	Refer to bit 0 reg17h for HDMI reset condition
							1				MPEG Source infoframe has been received.	
		ACP_PACKET_DET ACP Packet Detection				0					No ACP Packet received within the last 600ms. This bit reset to zero after an HDMI reset condition.	Refer to bit 0 reg17h for HDMI reset condition
						1					ACP Packet received received.	
		ISRC1_PACKET_DET ISRC1 Packet Detection			0						No ISRC1 Packet received since the last HDMI reset condition	Refer to bit 0 reg17h for HDMI reset condition
					1						ISRC1 Packet received.	
		ISRC2_PACKET_DET ISRC2 Packet Detection		0							No ISRC2 Packet received since the last HDMI reset condition.	Refer to bit 0 reg17h for HDMI reset condition
				1							ISRC2 Packet received.	
		DSD_PACKET_DET DSD Packet Detection since last reset condition.	0								No DSD Packet received within the last 10Hsync. This bit reset to zero on the 11th Hsync leading edge following a DSD packet or if an Audio packet sample packets has been received or after an HDMI reset condition.	Refer to bit 0 reg17h for HDMI reset condition
			1								DSD Packet received.	

Table 119: HDMI Map Details Register 0x19

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x19 Read	PACKET STATUS FLAGS 20_19	**Reserved**								x		
		NEW_TDMS_FREQ New TMDS Frequency							0		TMDS Frequency has not changed by more than tolerance.	Tolerance specified by FREQTOLERANCE[3:0]
									1		TMDS Frequency has changed by more than tolerance. Reset by clearing associated interrupt. (User Map1 REG B2 BIT 1)	
		FLATLINE_BIT_SET						0			No audio sample packet has been received with a flatline.	
								1			Audio Sample Packet with flatline has been received. Reset by clearing associated interrupt. (User Map1 REG B2 BIT 2)	
		SAMP_RT_CHNG Audio sample rate change in Channel Status (of channel 0)					0				No sample rate change occurred.	
							1				Audio sample rate in Channel Status ahs channged (for channel 0 only). Reset by clearing associated interrupt. (User Map1 REG B2 BIT 3)	
		AUDIO_PARITY_ERR Audio Parity Error				0					No audio parity has been detected.	
						1					Audio parity error is detected. Reset by clearing associated interrupt. (User Map1 REG B2 BIT 4)	
		[7:5] Reserved	x	x	x							

Table 120: HDMI Map Details Register 0x1A

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x1A Read	PACKET STATUS FLAG 15_8	**ERR_IN_AUDIO_PCKT** Error in Audio Sample Packet								0	No uncorrectable error has been detected in an audio sample packet.	
										1	An uncorrectable error has been detected in an Audio Sample Packet. Reset by clearing associated interrupt. (User Map1 REG AF BIT 0)	
		ERR_IN_UNKNOWN_PCKT Error in unknown Packet							0		No uncorrectable error has been detected in an audio sample packet.	
									1		Uncorrectable error has been detected in an unknown packet (error was in the packet header). Reset by clearing associated interrupt.(User Map1 REG AF BIT 1)	
		ERR_IN_INFOFRAME_PCKT Error in Infoframe Packet						0			No uncorrectable infoframe error has been detected.	
								1			Uncorrectable error has been detected in an Infoframe Packet. Reset by clearing associated interrupt. (User Map1 REG AF BIT 2)	
		NEW_N					0				No change in N has been detected.	
							1				N has changed. Reset by clearing associated interrupt. (User Map1 REG AF BIT 3)	
		NEW_CTS				0					No detected change in CTS.	
						1					CTS has changed by more than threshold specified in reg 10h. Reset by clearing associated interrupt. (User Map1 REG AF BIT 4)	
		Reserved	x	x	x							

Table 121: HDMI Map Details Register 0x1B

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x1B Read	PACKET STATUS FLAG 7_0	**NEW_AVI_INFOFRAME**								0	An AVI Infoframe with new contents has not been received.	
										1	An AVI Infoframe with new contents has been received. Reset by clearing associated interrupt. (User Map1 REG AC BIT 0)	
		NEW_AUDIO_INFOFRAME							0		An Audio Infoframe with new contents has not been received.	
									1		An Audio Infoframe with new contents has been received. Reset by clearing associated interrupt. (User Map1 REG AC BIT 1)	
		NEW_SPD_INFOFRAME New Source Product Descriptor Infoframe						0			A Source Product Descriptor infoframe with new contents has not been received.	
								1			A Source Product Descriptor infoframe with new contents has been received. Reset by clearing associated interrupt. (User Map1 REG AC BIT 2)	
		NEW_MS_INFOFRAME New MPEG Source Infoframe					0				A new MPEG Source Infoframe has not been received.	
							1				A new MPEG Source Infoframe has been received. Reset by clearing associated interrupt. (User Map1 REG AC BIT 3)	
		NEW_ACP_PCKT New ACP Packet				0					An ACP Packet with new contents has been not received.	
						1					An ACP Packet with new contents has been received. Reset by clearing associated register. (User Map1 REG AC BIT 4)	
		NEW_ISRC1_PCKT New ISRC1 Packet			0						An ISRC1 Packet with new content has not been received.	
					1						An ISRC1 Packet with new content has been received. Reset by clearing associated interrupt. (User Map1 REG AC BIT 5)	
		NEW_ISRC2_PCKT New ISRC2 Packet		0							An ISRC2 Packet with new content has not been received.	
				1							An ISRC2 Packet with new content has been received. Reset by clearing associated interrupt. (User Map1 REG AC BIT 6)	
		NEW_GAMUT_MDATA_PCKT Indicates if Gamut metadata received or change taken place	0								No new Gamut metadata packet received or changed.	
			1								Updated Gamut metadata packet received or a change has taken place.	

Table 122: HDMI Map Details Register 0x1C

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x1C R/W	REGISTER 1CH	**MCLKFS_N[2:0].** Frequency divider from MCKCKOUT to main clock for the audio processing block.						0	0	0	MCLKOUT=128Fs	fs is the audio sampling frequency
								0	0	1	MCLKOUT=256Fs	
								0	1	0	MCLKOUT=384Fs	
								0	1	1	MCLKOUT=512Fs	
								1	0	0	MCLKOUT=640Fs	
								1	0	1	MCLKOUT=768Fs	
								1	1	0	MCLKOUT=896Fs	
								1	1	1	MCLKOUT=1024Fs	
		MCLKPLL_N[2:0] Post devider for Mclck from PLL. Used to devide output back down after PLL multiplication			0	0	0				1X	
					0	0	1				1/2X	
					0	1	0				1/3X	
					0	1	1				1/4X	
					1	0	0				1/5X	
					1	0	1				1/6X	
					1	1	0				1/7X	
					1	1	1				1/8X	
		MCLKPLLEN Analog Audio PLL enable		0							Disable the audio analog PLL	
				1							Enable the audio analog PLL	
		Reserved	0								Set to default	

Table 123: HDMI Map Details Register 0x1D to 0x25

Subadress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x1D R/W		**NOT_AUTO_UNMUTE**								0	Allow audio to unmute automatically in a manner defined by WAIT_UNMUTE[1:0], when there are no mute conditions set.	
										1	Prevent audio from unmuting automatically	
		WAIT_UNMUTE[1:0] Delayed auto unmute						0	0		Don't immplement a delay before unmuting.	
								0	1		Unmute 500 Msec after all mute conditions become inactive	
								1	0		Unmute 1 sec after all mute conditions become inactive	
								1	1		Unmute 2.6 sec after all mute condition become inactive.	
		MUTE_AUDIO Both Mute and Umutting are ramped to prevent pops or clicks					0				Normal Audio	
							1				Force Audio Mute	
		Reserved				0					Set to default	
		UP_CONVERSION_MODE			0						Repeat Cr/Cb values	
					1						Interpolate Cr/Cb values	
		[7:6] Reserved	0	0							Set to default	
0x1E Read	TOTAL_LINE_WIDTH_MSB	**TOTAL_LINE_WIDTH[11:0]** Line Width. Number of active pixels per line.										
		TOTAL_LINE_WIDTH[11:8] See TOTAL_LINE_WIDTH[11:0] above					x	x	x	x		
		[7:4] Reserved	x	x	x	x						
0x1F Read	TOTAL_LINE_WIDTH_LSB	**TOTAL_LINE_WIDTH[7:0]** See TOTAL_LINE_WIDTH[11:0] in register 0x1E	x	x	x	x	x	x	x	x		
0x20 Read	HSYNC_FRONT_PORCH_MSB	**HSYNC_FRONT_PORCH[9:0]** Hsync Front Porch. HSYNC front porch width in unit of unique pixels (Valid only if DE regeneration is locked).										
		HSYNC_FRONT_PORCH[9:8] See HSYNC_FRONT_PORCH[9:0] above							x	x		
		[7:2] Reserved	x	x	x	x	x	x				
0x21 Read	HSYNC_FRONT_PORCH	**HSYNC_FRONT_PORCH7:0]** See HSYNC_FRONT_PORCH[9:0] in register 0x20	x	x	x	x	x	x	x	x		
0x22 Read	HSYNC_PULSE_WIDTH_MSB	HSYNC_PULSE_WIDTH[9:0] HSync Pulse Width. HSYNC width in unit of unique pixels (Valid only if DE regeneration is locked).										
		HSYNC_PULSE_WIDTH[9:8] See HSYNC_PULSE_WIDTH[9:0] above							x	x		
		[7:2] Reserved	x	x	x	x	x	x				
0x23 Read	HSYNC_PULSE_WIDTH	**HSYNC_PULSE_WIDTH[7:0]** See HSYNC_PULSE_WIDTH[9:0] in register 0x22	x	x	x	x	x	x	x	x		
0x24 Read	HSYNC_BACK_PORCH_MSB	**HSYNC_BACK_PORCH[9:0]** HSync Back Porch. HSYNC back porch width in unit of unique pixels (Valid only if DE regeneration is locked).										
		HSYNC_BACK_PORCH[9:8] See HSYNC_BACK_PORCH[9:8] above							x	x		
		[7:2] Reserved	x	x	x	x	x	x				
0x25 Read	HSYNC_BACK_PORCH	**HSYNC_BACK_PORCH[7:0]** See HSYNC_BACK_PORCH[7:0] in register 0x24	x	x	x	x	x	x	x	x		

Table 124: HDMI Map Details Register 0x26 to 0x2F

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x26 Read	FIELD0_TOTAL_HEIGHT_MSB	**FIELD0_TOTAL_HEIGHT[9:0]** Field 0 Height. Total number of lines in field 0 (Valid only if Vertical filter is locked).										
		FIELD0_TOTAL_HEIGHT[9:8] See FIELD0_TOTAL_HEIGHT[9:0] above.				x	x	x	x	x		
		[7:5] Reserved	x	x	x							
0x27 Read	FIELD0_TOTAL_HEIGHT	**FIELD0_TOTAL_HEIGHT[7:0]** See FIELD0_TOTAL_HEIGHT[9:0] in register 0x26	x	x	x	x	x	x	x	x		
0x28 Read	FIELD1_TOTAL_HEIGHT_MSB	**FIELD1_TOTAL_HEIGHT[9:0]** Field 1 Height. Total number of lines in field 1 (Valid only if Vertical fileter is locked).										
		FIELD1_TOTAL_HEIGHT[9:8] See FIELD1_TOTAL_HEIGHT[9:0] above.				x	x	x	x	x		
		[7:5] Reserved	x	x	x							
0x29 Read	FIELD1_TOTAL_HEIGHT	**FIELD1_TOTAL_HEIGHT[7:0]** See FIELD1_TOTAL_HEIGHT[9:0] in register 0x28	x	x	x	x	x	x	x	x		
0x2A Read	FIELD0_VS_FRONT_PORCH_MSB	**FIELD0_VS_FRONT_PORCH[9:0].** VSync front porch width in field 0. Unit is unique pixel.(Valid only if Vertical filter is locked).										
		FIELD0_VS_FRONT_PORCH[9:8] See FIELD0_VS_FRONT_PORCH[9:0] above.				x	x	x	x	x		
		[7:5] Reserved	x	x	x							
0x2B Read	FIELD0_VS_FRONT_PORCH	**FIELD0_VS_FRONT_PORCH[7:0]** See FIELD0_VS_FRONT_PORCH[9:0] in register 0x2A	x	x	x	x	x	x	x	x		
0x2C Read	FIELD1_VS_FRONT_PORCH_MSB	**FIELD1_VS_FRONT_PORCH[9:0]** VSync front porch width in field 1. Unit is unique pixel.(Valid only if Vertical filter is locked).										
		FIELD1_VS_FRONT_PORCH[9:8] See FIELD1_VS_FRONT_PORCH[9:0] above.				x	x	x	x	x		
		[7:5] Reserved	x	x	x							
0x2D Read	FIELD1_VS_FRONT_PORCH	**FIELD1_VS_FRONT_PORCH[7:0]** See FIELD1_VS_FRONT_PORCH[9:0] in register 0x2C	x	x	x	x	x	x	x	x		
0x2E Read	FIELD0_VS_PULSE_WIDTH_MSB	**FIELD0_VS_PULSE_WIDTH[9:0]** VSync width in field 0. Unit is unique pixel.(Valid only if Vertical filter is locked).										
		FIELD0_VS_PULSE_WIDTH[9:8] See FIELD0_VS_PULSE_WIDTH[9:0] above				x	x	x	x	x		
		[7:5] Reserved	x	x	x							
0x2F Read	FIELD0_VS_PULSE_WIDTH	**FIELD0_VS_PULSE_WIDTH[7:0]** See FIELD0_VS_PULSE_WIDTH[9:0] in register 0x2E	x	x	x	x	x	x	x	x		

Table 125: HDMI Map Details Register 0x30 to 0x35

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x30 Read	FIELD1_VS_PULSE_WIDTH_MSB	**FIELD1_VS_PULSE_WIDTH[9:0]** VSync width in field 1. Unit is unique pixel.(Valid only if Vertical filter is locked).										
		FIELD1_VS_PULSE_WIDTH[9:8] See FIELD1_VS_PULSE_WIDTH[9:0] above				x	x	x	x	x		
		[7:5] Reserved	x	x	x							
0x31 Read	FIELD1_VS_PULSE_WIDTH	**FIELD1_VS_PULSE_WIDTH[7:0]** See FIELD1_VS_PULSE_WIDTH[9:0] in register 0x30	x	x	x	x	x	x	x	x		
0x32 Read	FIELD0_VS_BACK_PORCH_MSB	**FIELD0_VS_BACK_PORCH[9:0]** VSync back porch width in field 0. Unit is unique pixels. (Valid only if Vertical filter is locked).										
		FIELD0_VS_BACK_PORCH[9:8] See FIELD0_VS_BACK_PORCH[9:0] above				x	x	x	x	x		
		[7:5] Reserved	x	x	x							
0x33 Read	FIELD0_VS_BACK_PORCH	**FIELD0_VS_BACK_PORCH[7:0]** See FIELD0_VS_BACK_PORCH[9:0] in register 0x32	x	x	x	x	x	x	x	x		
0x34 Read	FIELD1_VS_BACK_PORCH_MSB	**FIELD1_VS_BACK_PORCH[9:0]** VSync back porch width in field 1. Unit is unique pixels. (Valid only if Vertical filter is locked).										
		FIELD1_VS_BACK_PORCH[9:8] See FIELD1_VS_BACK_PORCH[9:8] above				x	x	x	x	x		
		[7:5] Reserved	x	x	x							
0x35 Read	FIELD1_VS_BACK_PORCH	**FIELD1_VS_BACK_PORCH[7:0]** See FIELD1_VS_BACK_PORCH[9:0] in register 0x34	x	x	x	x	x	x	x	x		

Table 126: HDMI Map Details Register 0x36 to 0x41

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x36 Read	CHANNEL STATUS DATA 0	**CHANNEL_STATUS_DATA_0[7:0]** Byte 0 of channel Status data for channel audio 0										
		CHANNEL_STATUS_DATA_0[7:0] See CHANNEL_STATUS_DATA_0[7:0] above	x	x	x	x	x	x	x	x		
0x37 Read	CHANNEL STATUS DATA 1	**CHANNEL_STATUS_DATA_1[7:0]** Byte 1 of channel Status data for channel audio 0										
		CHANNEL_STATUS_DATA_1[7:0] See CHANNEL_STATUS_DATA_1[7:0] above	x	x	x	x	x	x	x	x		
0x38 Read	CHANNEL STATUS DATA 2	**CHANNEL_STATUS_DATA_2[7:0]** Byte 2 of channel Status data for channel audio 0										
		CHANNEL_STATUS_DATA_2[7:0] See CHANNEL_STATUS_DATA_2[7:0] above	x	x	x	x	x	x	x	x		
0x39 Read	CHANNEL STATUS DATA 3	**CHANNEL_STATUS_DATA_3[7:0]** Byte 3 of channel Status data for channel audio 0										
		CHANNEL_STATUS_DATA_3[7:0] See CHANNEL_STATUS_DATA_3[7:0] above	x	x	x	x	x	x	x	x		
0x3A Read	CHANNEL STATUS DATA 4	**CHANNEL_STATUS_DATA_4[3:0]** Byte 4 of channel Status data for channel audio 0										
		CHANNEL_STATUS_DATA_4[3:0] See CHANNEL_STATUS_DATA_4[3:0] above					x	x	x	x		
		[7:4] Reserved	x	x	x	x						
0x3C R/W	PLL DIVIDER	**[3:0]** Reserved					0	0	1	0	Set to default	
		PLL_DIVIDER[3:0] See PLL_DIVIDER[11:0] in register 0x3B	0	1	0	0						
0x3D R/W	REGISTER 3DH	**[7:0]** Reserved	0	0	1	0	0	0	0	0	Set to default	
0x3E R/W	REGISTER 3EH	**[7:0]** Reserved	0	0	1	1	0	1	0	1	Set to default	
0x3F R/W	REGISTER 3FH	**[7:0]** Reserved	0	1	1	0	0	0	1	1	Set to default	
0x40 R/W	REGISTER 40H	Reserved	0	0	0	0	0	0	0	0	Set to default	
0x41 R/W	REGISTER 41H	**DEREP_N[3:0]** Control the pixel repetition manually.					x	x	x	x	DEREP_N+1 indicates the pixel and clock discard factor	DEREP_N_Override must be set to enable manual control of pixel repetition
		DEREP_N_OVERRIDE Control to set manual control over pixel repetition				0					Automatic detection and processing of pixel repetition using AVI InfoFrames.	
						1					Enables manual setting of pixel repet	
		Reserved	0	1	0						Set to default	

Table 127: HDMI Map Details Register 0x42 to 0x4C

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x42 Read	REGISTER 42H	**[7:0]** Reserved	x	x	x	x	x	x	x	x	Reserved	
0x43 R/W	REGISTER 43H	**[7:0]** Reserved	0	0	0	1	1	1	1	1	Set to default	
0x44 R/W	REGISTER 44H	**[7:0]** Reserved	0	0	0	0	0	0	0	0	Set to default	
0x45 R/W	REGISTER_45H	**[7:0]** Reserved	0	0	0	0	0	0	0	0	Set to default	
0x46 R/W	REGISTER_46H	**[7:0]** Reserved	1	0	0	0	1	1	1	1	Set to default	
0x47 R/W	REGISTER_47H	**[7:0]** Reserved	0	0	0	0	0	0	0	0	Set to default	
0x48 R/W	REGISTER_48H	**[7:0]** Reserved	0	0	0	0	0	0	0	0	Set to default	
0x49 Read	REGISTER_49H	**[7:0]** Reserved	x	x	x	x	x	x	x	x		
0x4A Read	REGISTER_4AH	**[7:0]** Reserved	x	x	x	x	x	x	x	x		
0x4B Read	REGISTER_4BH	**[7:0]** Reserved	x	x	x	x	x	x	x	x		
0x4C Read	REGISTER_4CH	**[7:0]** Reserved	0	1	0	0	0	1	1	1	Set to default	

Table 128: HDMI Map Details Register 0x4D to 0x4F

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x4D R/W	REGISTER_4DH	**[7:0]** Reserved	0	0	0	0	0	0	0	0	Set to default	
0x4E R/W	REGISTER_4EH	**[7:0]** Reserved	0	0	1	1	0	1	0	1	Set to default	
0x4F R/W	REGISTER_4FH	**[7:0]** Reserved	0	1	1	0	0	0	1	1	Set to default	

Table 129: HDMI Map Details Register 0x50

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x50 Write	Register 0x50	**Reserved**								0		
		CS_COPYWRITE_FORCE Controls the Channel status copy write that is passed to SPDIF output.							0		Does not change the channel status copyright bit that is passed to SPDIF	
									1		Asserts channel copyright bit before it is passed to the SPDIF output	
		Reserved	0	0	0	0	0	0			Set to default	

Table 130: HDMI Map Details Register 0x5A to 0x5F

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x5A Write	Register 0x5A	**AUDIO_PLL_RESET** Reset the audio PLL synthetizer. Self clearing bit.								0		
										1	Reset the audio PLL synthetizer	Setting this bit will send a changeN signal to the audio PLL and cause an audio mute if ChangeN mute Mask bit is set.
		PACKET_DET_RESET. Reset the packet audio block. Self clearing bit.							0			
									1			
		[7:2] Reseved	0	0	0	0	0	0			Set to 0	
0x5B Read	CTS_REG1	CTS[19:0] CTS value for audio clock regeneration (CTS)										
		CTS[19:12] See CTS[19:0] above	x	x	x	x	x	x	x	x		
0x5C Read	CTS_REG2	**CTS[11:4]** See CTS[19:0] in register 0x7B	x	x	x	x	x	x	x	x		
0x5D Read	CTS_REG3_N-REG1	**N[19:0]** N value for audio clock regeneration (ACR)										
		N[19:16] See N[19:] above					x	x	x	x		
		CTS[3:0] See CTS[19:0] in register 0x7B	x	x	x	x						
0x5E	N-REG2	**N[15:8]** See N[19:0] in register 0x7D	x	x	x	x	x	x	x	x		
0x5F	N-REG3	**N[7:0]** See N[19:0] in register 0x7D	x	x	x	x	x	x	x	x		

Table 131: HDMI Map Details Register 0x60 to 0x7F

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x60 Read	GAMUT_METADATA_BODY_0	**GBD_0.7** to **GBD_0.0** Gamut metadata byte 0										
0x61 Read	GAMUT_METADATA_BODY_1	**GBD_1.7** to **GBD_1.0** Gamut metadata byte 1										
0x62 Read	GAMUT_METADATA_BODY_2	**GBD_2.7** to **GBD_2.0** Gamut metadata byte 2										
0x63 Read	GAMUT_METADATA_BODY_3	**GBD_3.7** to **GBD_3.0** Gamut metadata byte 3										
0x64 Read	GAMUT_METADATA_BODY_4	**GBD_4.7** to **GBD_4.0** Gamut metadata byte 4										
0x65 Read	GAMUT_METADATA_BODY_5	**GBD_5.7** to **GBD_5.0** Gamut metadata byte 5										
0x66 Read	GAMUT_METADATA_BODY_6	**GBD_6.7** to **GBD_6.0** Gamut metadata byte 6										
0x67		**Not used**										
0x68 Read	GAMUT_METADATA_BODY_7	**GBD_7.7** to **GBD_7.0** Gamut metadata byte 7										
0x69 Read	GAMUT_METADATA_BODY_8	**GBD_8.7** to **GBD_8.0** Gamut metadata byte 8										
0x6A Read	GAMUT_METADATA_BODY_9	**GBD_9.7** to **GBD_9.0** Gamut metadata byte 9										
0x6B Read	GAMUT_METADATA_BODY_10	**GBD_10.7** to **GBD_10.0** Gamut metadata byte 10										
0x6C Read	GAMUT_METADATA_BODY_11	**GBD_11.7** to **GBD_11.0** Gamut metadata byte 11										
0x6D Read	GAMUT_METADATA_BODY_12	**GBD_12.7** to **GBD_12.0** Gamut metadata byte 12										
0x6E Read	GAMUT_METADATA_BODY_13	**GBD_13.7** to **GBD_13.0** Gamut metadata byte 13										
0x6F		**Not used**										
0x70 Read	GAMUT_METADATA_BODY_14	**GBD_14.7** to **GBD_14.0** Gamut metadata byte 14										
0x71 Read	GAMUT_METADATA_BODY_15	**GBD_15.7** to **GBD_15.0** Gamut metadata byte 15										
0x72 Read	GAMUT_METADATA_BODY_16	**GBD_16.7** to **GBD_16.0** Gamut metadata byte 16										
0x73 Read	GAMUT_METADATA_BODY_17	**GBD_17.7** to **GBD_17.0** Gamut metadata byte 17										
0x74 Read	GAMUT_METADATA_BODY_18	**GBD_18.7** to **GBD_18.0** Gamut metadata byte 18										
0x75 Read	GAMUT_METADATA_BODY_19	**GBD_19.7** to **GBD_19.0** Gamut metadata byte 19										
0x76 Read	GAMUT_METADATA_BODY_20	**GBD_20.7** to **GBD_20.0** Gamut metadata byte 20										
0x77		**Not used**										
0x78 Read	GAMUT_METADATA_BODY_21	**GBD_21.7** to **GBD_21.0** Gamut metadata byte 21										
0x79 Read	GAMUT_METADATA_BODY_22	**GBD_22.7** to **GBD_22.0** Gamut metadata byte 22										
0x7A Read	GAMUT_METADATA_BODY_23	**GBD_23.7** to **GBD_23.0** Gamut metadata byte 23										
0x7B Read	GAMUT_METADATA_BODY_24	**GBD_24.7** to **GBD_24.0** Gamut metadata byte 24										
0x7C Read	GAMUT_METADATA_BODY_25	**GBD_25.7** to **GBD_25.0** Gamut metadata byte 25										
0x7D Read	GAMUT_METADATA_BODY_26	**GBD_26.7** to **GBD_26.0** Gamut metadata byte 26										
0x7E Read	GAMUT_METADATA_BODY_27	**GBD_27.7** to **GBD_27.0** Gamut metadata byte 27										
0x7F		**Not used**										

Table 132: HDMI Map Details Register 0x80 to 0x84

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x80 Read	AVI_INF_VERS	**AVI_INF_VERS[7:0]** Infoframe Version Number	x	x	x	x	x	x	x	x	For interpretation of the infoframe version number refer 861D specification.	For more details on the AVI infoframe refer to the 861D specification
0x81 Read	AVI_DATA_BYTE_1	**S[1:0]** Scan Information							0	0	No Data	
									0	1	Overscanned (television)	
									1	0	Underscanned (Computer)	
									1	1	Reserved	
		B[1:0] Bar Information					0	0			Bar Data not valid	
							0	1			Vert. Bar Info valid	
							1	0			Horiz. Bar info Valid	
							1	1			Vert. and Horiz. Bar Info Valid	
		A Active Format Information				0					No Data	
						1					Active Format Information valid	
		Y[1:0] RGB or YCbCr		0	0						RGB	
				0	1						YCbCr 4:2:2	
				1	0						YCbCr 4:4:4	
				1	1						Reserved	
		Reserved	x								Reserved	
0x82 Read	AVI_INF_BYTE_2	**R[3:0]** Active Format Aspect Ratio					1	0	0	0	Same as picture aspect Ratio	
							1	0	0	1	4:3 (Center)	
							1	0	1	0	16:9 (Center)	
							1	0	1	1	14:9 (Center)	
							-	-	-	-	All other values per DVB AFD active format field in ETSI[3]	
		M[1:0] Picture Aspect Ratio			0	0					No Data	
					0	1					4:3	
					1	0					16:9	
					1	1					Reserved	
		C[1:0] Colorimetry	0	0							No Data	
			0	1							SMPTE 170M, ITU601	
			1	0							ITU709	
			1	1							Extended colorimetry information valid (colorimetry indicated in bits EC0, EC2,EC2)	
0x83 Read	AVI_INF_BYTE_3	**SC[1:0]** Non-uniform Picture scaling							0	0	No known non-unifrom scaling	
									0	1	Picture has been scaled horizontally	
									1	0	Picture has been scaled vertically	
									1	1	Picture has been scaled horizontally and vertically	
		Q[1:0] RGB Quantization Range					0	0			Default (depends on video format)	
							0	1			Limited Range	
							1	0			Full Range	
							1	1			Reserved	
		EC[2:0] Extended colorimetry		0	0	0					$xvYCC_{601}$	
				0	0	1					$xvYCC_{709}$	
				-	-	-					all other values reserved	
		ITC IT Content	0								No data	
			1								IT Content	
0x84 Read	AVI_INF_BYTE_4	**VIC[6:0]** Video Identification code		x	x	x	x	x	x	x	This is for Infoframe format version 2. This is not in version1	
			x								Reserved	

Table 133: HDMI Map Details Register 0x85 to 0x8E

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x85 Read	AVI_INF_BYTE_5	**PR[3:0]** indicates to the DTV Monitor how many repetitions of each unique pixel are transmitted for the optional (2880)x480i or (2880)x576/288p formats					0	0	0	0	No repetition (i.e., pixel sent once)	
							0	0	0	1	pixel sent 2 times (i.e., repeated once)	
							0	0	1	0	pixel sent 3 times	
							0	0	1	1	pixel sent 4 times	
							0	1	0	0	pixel sent 5 times	
							0	1	0	1	pixel sent 6 times	
							0	1	1	0	pixel sent 7 times	
							0	1	1	1	pixel sent 8 times	
							1	0	0	0	pixel sent 9 times	
							1	0	0	1	pixel sent 10 times	
							~	~	~	~	Reserved	
							1	1	1	1		
			x	x	x	x					Reserved	
0x86 Read	AVI_INF_BYTE_6	**LINE_END_LSB[7:0]** Line Number of Start of Bottom Bar (lower 8 Bits)	x	x	x	x	x	x	x	x		
0x88 Read	AVI_INF_BYTE_7	**LINE_END_MSB[7:0]** Line Number of Start of Bottom Bar (upper 8 Bits)	x	x	x	x	x	x	x	x		
0x89 Read	AVI_INF_BYTE_8	**LINE_START_LSB[7:0]** Line Number of End of Top Bar (lower 8 Bits)	x	x	x	x	x	x	x	x		
0x8A Read	AVI_INF_BYTE_9	**LINE_START_MSB[7:0]** Line Number of End of Top Bar (upper 8 Bits)	x	x	x	x	x	x	x	x		
0x8B Read	AVI_INF_BYTE_10	**PIXEL_END_LSB[7:0]** Pixel Number of Start of Right Bar (lower 8 Bits)	x	x	x	x	x	x	x	x		
0x8C Read	AVI_INF_BYTE_11	**PIXEL_END_MSB[7:0]** Pixel Number of Start of Right Bar (upper 8 Bits)	x	x	x	x	x	x	x	x		
0x8D Read	AVI_INF_BYTE_12	**PIXEL_START_LSB[7:0]** Pixel Number of End of Left Bar (lower 8 Bits)	x	x	x	x	x	x	x	x		
0x8E Read	AVI_INF_BYTE_13	**PIXEL_START_MSB[7:0]** Pixel Number of End of Left Bar (upper 8 Bits)	x	x	x	x	x	x	x	x		

Table 134: HDMI Map Details Register 0x90 to 0x93

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x90 Read	AUDIO_INF_VERS	**AUDIO_INF_VERS[7:0] Audio Infofr**	x	x	x	x	x	x	x	x		
0x91 Read	AUDIO_INF_BYTE_1	**CC[2:0]** Audio Channel Count						0	0	0	Refer to Stream Header	
								0	0	1	2ch	
								0	1	0	3ch	
								0	1	1	4ch	
								1	0	0	5ch	
								1	0	1	6ch	
								1	1	0	7ch	
								1	1	1	8ch	
							x				Reserved	
		CT[3:0] Audio Coding Type	0	0	0	0					Refer to Stream Header	
			0	0	0	1					IEC60958PCM	
			0	0	1	0					AC-3	
			0	0	1	1					MPEG1(Layers 1 & 2)	
			0	1	0	0					MP3 (MPEG1 Layer3)	
			0	1	0	1					MPEG2 (multichannel)	
			0	1	1	0					AAC	
			0	1	1	1					DTS	
			1	0	0	0					ATRAC	
			~	~	~	~					Reserved	
			1	1	1	1						
0x92 Read	AUDIO_INF_BYTE_2	**SS[1:0]** Sample Size							0	0	Refer to stream header	
									0	1	16 Bit	
									1	0	20 Bit	
									1	1	24 bit	
		SF[2:0] Sampling Frequency				0	0	0			Refer to Stream header	
						0	0	1			32KHz	
						0	1	0			44.1KHz (CD)	
						0	1	1			48KHz	
						1	0	0			88.2KHZ	
						1	0	1			96KHz	
						1	1	0			176.4KHz	
						1	1	1			192KHz	
			x	x	x						Reserved	
0x93 Read	AUDIO_INF_BYTE_3	**AUDIO_INF_BYTE_3[7:0]** Format depends on coding type (i.e.,Data Byte 1)	x	x	x	x	x	x	x	x		

Table 135: HDMI Map Details Register 0x94

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting								Comment
0x94 Read	AUDIO_INF_BYTE_4	**CA[7:0]** contains information that describes how various speaker locations are allocated to transmission channels	CA								Channel Number								
											8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	
			0	0	0	0	0	0	0	0	-	-	-	-	-	-	FR	FL	
			0	0	0	0	0	0	0	1	-	-	-	-	-	E	FR	FL	
			0	0	0	0	0	0	1	0	-	-	-	-	FC	-	FR	FL	
			0	0	0	0	0	0	1	1	-	-	-	-	FC	E	FR	FL	
			0	0	0	0	0	1	0	0	-	-	-	RC	-	-	FR	FL	
			0	0	0	0	0	1	0	1	-	-	-	RC	-	E	FR	FL	
			0	0	0	0	0	1	1	0	-	-	-	RC	FC	-	FR	FL	
			0	0	0	0	0	1	1	1	-	-	-	RC	FC	E	FR	FL	
			0	0	0	0	1	0	0	0	-	-	RR	RL	-	-	FR	FL	
			0	0	0	0	1	0	0	1	-	-	RR	RL	-	E	FR	FL	
			0	0	0	0	1	0	1	0	-	-	RR	RL	FC	-	FR	FL	
			0	0	0	0	1	0	1	1	-	-	RR	RL	FC	E	FR	FL	
			0	0	0	0	1	1	0	0	-	RC	RR	RL	-	-	FR	FL	
			0	0	0	0	1	1	0	1	-	RC	RR	RL	-	E	FR	FL	
			0	0	0	0	1	1	1	0	-	RC	RR	RL	FC	-	FR	FL	
			0	0	0	0	1	1	1	1	-	RC	RR	RL	FC	E	FR	FL	
			0	0	0	1	0	0	0	0	RR	RLC	RR	RL	-	-	FR	FL	
			0	0	0	1	0	0	0	1	RR	RLC	RR	RL	-	E	FR	FL	
			0	0	0	1	0	0	1	0	RR	RLC	RR	RL	FC	-	FR	FL	
			0	0	0	1	0	0	1	1	RR	RLC	RR	RL	FC	E	FR	FL	
			0	0	0	1	0	1	0	0	FRC	FLC	-	-	-	-	FR	FL	
			0	0	0	1	0	1	0	1	FRC	FLC	-	-	-	E	FR	FL	
			0	0	0	1	0	1	1	0	FRC	FLC	-	-	FC	-	FR	FL	
			0	0	0	1	0	1	1	1	FRC	FLC	-	-	FC	E	FR	FL	
			0	0	0	1	1	0	0	0	FRC	FLC	-	RC	-	-	FR	FL	
			0	0	0	1	1	0	0	1	FRC	FLC	-	RC	-	E	FR	FL	
			0	0	0	1	1	0	1	0	FRC	FLC	-	RC	FC	-	FR	FL	
			0	0	0	1	1	0	1	1	FRC	FLC	-	RC	FC	E	FR	FL	
			0	0	0	1	1	1	0	0	FRC	FLC	RR	RL	-	-	FR	FL	
			0	0	0	1	1	1	0	1	FRC	FLC	RR	RL	-	E	FR	FL	
			0	0	0	1	1	1	1	0	FRC	FLC	RR	RL	FC	-	FR	FL	
			0	0	0	1	1	1	1	1	FRC	FLC	RR	RL	FC	E	FR	FL	
			~1	~1	~1	~1	~1	~1	~1	~1	Reserved								

Table 136: HDMI Map Details Register 0x95

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x95 Read	AUDIO_INF_BYTE_5							x	x	x	Reserved	
		LSV[3:0] Level Shift Value		0	0	0	0				0dB	
				0	0	0	1				1dB	
				0	0	1	0				2dB	
				0	0	1	1				3dB	
				0	1	0	0				4dB	
				0	1	0	1				5dB	
				0	1	1	0				6dB	
				0	1	1	1				7dB	
				1	0	0	0				8dB	
				1	0	0	1				9dB	
				1	0	1	0				10dB	
				1	0	1	1				11dB	
				1	1	0	0				12dB	
				1	1	0	1				13dB	
				1	1	1	0				14dB	
				1	1	1	1				15dB	
		DM_INH Down-mix Inhibit Flag. Describes whether the down mixed stereo output is permitted or not	0								Permitted or no information about any assertion of this	
			1								Prohibited	

Speaker Placement	
FL	Front Left
FC	Front Center
FR	Front Right
FLC	Front Left Center
FRC	Front Right Center
RL	Rear Left
RC	Rear Center
RR	Rear Right
RLC	Rear Left Center
RRC	Rear Right Center
LFE	Low Frequency Effect

Table 137: HDMI Map Details Register 0x98 to 0xB4

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x98 Read	SOURCE_PROD_INF_VERS	**SOURCE_PROD_INF_VERS[7:0]** Source Product Infoframe version Number	x	x	x	x	x	x	x	x		
0x99 Read	SOURCE_PROD_INF_BYTE_1	**VN1[7:0]** Vendor Name Character 1 VN1 (7Bit ASCII code)	x	x	x	x	x	x	x	x		
0x9A Read	SOURCE_PROD_INF_BYTE_2	**VN2[7:0]** Vendor Name Character 2 VN2	x	x	x	x	x	x	x	x		
0x9B Read	SOURCE_PROD_INF_BYTE_3	**VN3[7:0]** Vendor Name Character 3 VN3	x	x	x	x	x	x	x	x		
0x9C Read	SOURCE_PROD_INF_BYTE_4	**VN4[7:0]** Vendor Name Character 4 VN4	x	x	x	x	x	x	x	x		
0x9D Read	SOURCE_PROD_INF_BYTE_5	**VN5[7:0]** Vendor Name Character 5 VN5	x	x	x	x	x	x	x	x		
0x9E Read	SOURCE_PROD_INF_BYTE_6	**VN6[7:0]** Vendor Name Character 6 VN6	x	x	x	x	x	x	x	x		
0xA0 Read	SOURCE_PROD_INF_BYTE_7	**VN7[7:0]** Vendor Name Character 7 VN7	x	x	x	x	x	x	x	x		
0xA1 Read	SOURCE_PROD_INF_BYTE_8	**VN8[7:0]** Vendor Name Character 8 VN8	x	x	x	x	x	x	x	x		
0xA2 Read	SOURCE_PROD_INF_BYTE_9	**PD1[7:0]** Product Description Character 1 PD1 (7-bit ASCII code)	x	x	x	x	x	x	x	x		
0xA3 Read	SOURCE_PROD_INF_BYTE_10	**PD2[7:0]** Product Description Character 2 PD2	x	x	x	x	x	x	x	x		
0xA4 Read	SOURCE_PROD_INF_BYTE_11	**PD3[7:0]** Product Description Character 3 PD3	x	x	x	x	x	x	x	x		
0xA5 Read	SOURCE_PROD_INF_BYTE_12	**PD4[7:0]** Product Description Character 4 PD4	x	x	x	x	x	x	x	x		
0xA6 Read	SOURCE_PROD_INF_BYTE_13	**PD5[7:0]** Product Description Character 5 PD5	x	x	x	x	x	x	x	x		
0xA8 Read	SOURCE_PROD_INF_BYTE_14	**PD6[7:0]** Product Description Character 6 PD6	x	x	x	x	x	x	x	x		
0xA9 Read	SOURCE_PROD_INF_BYTE_15	**PD7[7:0]** Product Description Character 7 PD7	x	x	x	x	x	x	x	x		
0xAA Read	SOURCE_PROD_INF_BYTE_16	**PD8[7:0]** Product Description Character 8 PD8	x	x	x	x	x	x	x	x		
0xAB Read	SOURCE_PROD_INF_BYTE_17	**PD9[7:0]** Product Description Character 9 PD9	x	x	x	x	x	x	x	x		
0xAC Read	SOURCE_PROD_INF_BYTE_18	**PD10[7:0]** Product Description Character 10 PD10	x	x	x	x	x	x	x	x		
0xAD Read	SOURCE_PROD_INF_BYTE_19	**PD11[7:0]** Product Description Character 11 PD11	x	x	x	x	x	x	x	x		
0xAE Read	SOURCE_PROD_INF_BYTE_20	**PD12[7:0]** Product Description Character 12 PD12	x	x	x	x	x	x	x	x		
0xB0 Read	SOURCE_PROD_INF_BYTE_21	**PD13[7:0]** Product Description Character 13 PD13	x	x	x	x	x	x	x	x		
0xB1 Read	SOURCE_PROD_INF_BYTE_22	**PD14[7:0]** Product Description Character 14 PD14	x	x	x	x	x	x	x	x		
0xB2 Read	SOURCE_PROD_INF_BYTE_23	**PD15[7:0]** Product Description Character 15 PD15	x	x	x	x	x	x	x	x		
0xB3 Read	SOURCE_PROD_INF_BYTE_24	**PD16[7:0]** Product Description Character 16 PD16	x	x	x	x	x	x	x	x		
0xB4 Read	SOURCE_PROD_INF_BYTE_25	SOURCE_DEV_INF[7:0] code classifies the source device	Code								Source Device Information	
			0	0	0	0	0	0	0	0	unknown	
			0	0	0	0	0	0	0	1	Digital STB	
			0	0	0	0	0	0	1	0	DVD	
			0	0	0	0	0	0	1	1	D-VHS	
			0	0	0	0	0	1	0	0	HDD Video	
			0	0	0	0	0	1	0	1	DVC	
			0	0	0	0	0	1	1	0	DSC	
			0	0	0	0	0	1	1	1	Video CD	
			0	0	0	0	1	0	0	0	Game	
			0	0	0	0	1	0	0	1	PC General	
			~	~	~	~	~	~	~	~	Reserved	
			1	1	1	1	1	1	1	1		

Table 138: HDMI Map Details Register 0xB8 to 0xBD

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0xB8 Read	MPEG_SOURCE INF VERS	**MPEG_SOURCE_INF_VERS[7:0]** MPEG source Infoframe Version	x	x	x	x	x	x	x	x		
0xB9 Read	MPEG_SOURCE INF_BYTE_1	**MB0[7:0]** MB#0 (MPEG Bit Rate: Hz Lower -> Upper)	x	x	x	x	x	x	x	x		
0xBA Read	MPEG_SOURCE INF_BYTE_2	**MB1[7:0]** MB#1	x	x	x	x	x	x	x	x		
0xBB Read	MPEG_SOURCE INF_BYTE_3	**MB2[7:0]** MB#2	x	x	x	x	x	x	x	x		
0xBC Read	MPEG_SOURCE INF_BYTE_4	**MB3[7:0]** MB#3 (Upper Byte	x	x	x	x	x	x	x	x		
0xBD Read	MPEG_SOURCE INF_BYTE_5								0	0	Unknown (No Data)	
									0	1	I Picture	
									1	0	B Picture	
									1	1	P Picture	
							x	x			Reserved	
		FR Field Repeat (for 3:2 pull-down)				0					New field (picture)	
						1					Repeated Field	
			x	x	x						Reserved	

Table 139: HDMI Map Details Register 0xC0 to 0xD6

Subadress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0xC0 Read	ACP_TYPE	**ACP_TYPE[7:0]** This defines which Audio content protection is used	Type									
			0	0	0	0	0	0	0	0	Generic Audio	
			0	0	0	0	0	0	0	1	IEC 60958-Identified Audio	
			0	0	0	0	0	0	1	0	DVD-Audio	
			0	0	0	0	0	0	1	1	Reserved for super Audio CD	
			~1	~1	~1	~1	~1	~1	~1	~1	Reserved	
0xC1 Read	ACP_PACKET_BYTE_0	**ACP_PB0[7:0]** Audio content protection Packet Byte 0	x	x	x	x	x	x	x	x		
0xC2 Read	ACP_PACKET_BYTE_1	**ACP_PB1[7:0]** Audio content protection Packet Byte 1	x	x	x	x	x	x	x	x		
0xC3 Read	ACP_PACKET_BYTE_2	**ACP_PB2[7:0]** Audio content protection Packet Byte 2	x	x	x	x	x	x	x	x		
0xC4 Read	ACP_PACKET_BYTE_3	**ACP_PB3[7:0]** Audio content protection Packet Byte 3	x	x	x	x	x	x	x	x		
0xC5 Read	ACP_PACKET_BYTE_4	**ACP_PB4[7:0]** Audio content protection Packet Byte 4	x	x	x	x	x	x	x	x		
0xC6 Read	ACP_PACKET_BYTE_5	**ACP_PB5[7:0]** Audio content protection Packet Byte 5	x	x	x	x	x	x	x	x		
0xC8 Read	ACP_PACKET_BYTE_6	**ACP_PB6[7:0]** Audio content protection Packet Byte 6	x	x	x	x	x	x	x	x		
0xC9 Read	ACP_PACKET_BYTE_7	**ACP_PB7[7:0]** Audio content protection Packet Byte 7	x	x	x	x	x	x	x	x		
0xCA Read	ACP_PACKET_BYTE_8	**ACP_PB8[7:0]** Audio content protection Packet Byte 8	x	x	x	x	x	x	x	x		
0xCB Read	ACP_PACKET_BYTE_9	**ACP_PB9[7:0]** Audio content protection Packet Byte 9	x	x	x	x	x	x	x	x		
0xCC Read	ACP_PACKET_BYTE_10	**ACP_PB10[7:0]** Audio content protection Packet Byte 10	x	x	x	x	x	x	x	x		
0xCD Read	ACP_PACKET_BYTE_11	**ACP_PB11[7:0]** Audio content protection Packet Byte 11	x	x	x	x	x	x	x	x		
0xCE Read	ACP_PACKET_BYTE_12	**ACP_PB12[7:0]** Audio content protection Packet Byte 12	x	x	x	x	x	x	x	x		
0xD0 Read	ACP_PACKET_BYTE_13	**ACP_PB13[7:0]** Audio content protection Packet Byte 0	x	x	x	x	x	x	x	x		
0xD1 Read	ACP_PACKET_BYTE_14	**ACP_PB14[7:0]** Audio content protection Packet Byte 1	x	x	x	x	x	x	x	x		
0xD2 Read	ACP_PACKET_BYTE_15	**ACP_PB15[7:0]** Audio content protection Packet Byte 2	x	x	x	x	x	x	x	x		
0xD3 Read	ACP_PACKET_BYTE_16	**ACP_PB16[7:0]** Audio content protection Packet Byte 3	x	x	x	x	x	x	x	x		
0xD4 Read	ACP_PACKET_BYTE_17	**ACP_PB17[7:0]** Audio content protection Packet Byte 4	x	x	x	x	x	x	x	x		
0xD5 Read	ACP_PACKET_BYTE_18	**ACP_PB18[7:0]** Audio content protection Packet Byte 5	x	x	x	x	x	x	x	x		
0xD6 Read	ACP_PACKET_BYTE_19	**ACP_PB19[7:0]** Audio content protection Packet Byte 6	x	x	x	x	x	x	x	x		

Table 140: HDMI Map Details Register 0xD8 to 0xEA

Subadress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0xD8 Read	ISRC1_INF	**ISRC1_STATUS[2:0]** These bits define where the ISRC track the samples are : at least 2 transmissions of '001' occur at the beginning of the track, while in the middle of the track continuous transmission of '010'occurs folowed by at least 2 transmissions of '100' near the end of the track.						x	x	x		
					x	x	x				Reserved	
		ISRC1_VALID This bit is an indication of wheher ISRC1 packet bytes are valid		0							ISRC1 status bits and PBs not valid	
				1							ISRC1 status bits and PBs valid	
		ISRC1_CONTINUED This bit indicates that a continuation of the 16 ISRC1 packet bytes (an ISRC2 packet) is being transmitted	x								This bit indicates that a continuation of the 16 ISRC1 packet bytes (an ISRC2 packet) is being transmitted	
0xD9 Read	ISRC1_PACKET_BYTE_0	**ISRC1_PB0[7:0]** ISRC1 Packet Byte0	x	x	x	x	x	x	x	x		
0xDA Read	ISRC1_PACKET_BYTE_1	**ISRC1_PB1[7:0]** ISRC1 Packet Byte1	x	x	x	x	x	x	x	x		
0xDB Read	ISRC1_PACKET_BYTE_2	**ISRC1_PB2[7:0]** ISRC1 Packet Byte2	x	x	x	x	x	x	x	x		
0xDC Read	ISRC1_PACKET_BYTE_3	**ISRC1_PB3[7:0]** ISRC1 Packet Byte3	x	x	x	x	x	x	x	x		
0xDD Read	ISRC1_PACKET_BYTE_4	**ISRC1_PB4[7:0]** ISRC1 Packet Byte4	x	x	x	x	x	x	x	x		
0xDE Read	ISRC1_PACKET_BYTE_5	**ISRC1_PB5[7:0]** ISRC1 Packet Byte5	x	x	x	x	x	x	x	x		
0xE0 Read	ISRC1_PACKET_BYTE_6	**ISRC1_PB6[7:0]** ISRC1 Packet Byte6	x	x	x	x	x	x	x	x		
0xE1 Read	ISRC1_PACKET_BYTE_7	**ISRC1_PB7[7:0]** ISRC1 Packet Byte7	x	x	x	x	x	x	x	x		
0xE2 Read	ISRC1_PACKET_BYTE_8	**ISRC1_PB8[7:0]** ISRC1 Packet Byte8	x	x	x	x	x	x	x	x		
0xE3 Read	ISRC1_PACKET_BYTE_9	**ISRC1_PB9[7:0]** ISRC1 Packet Byte9	x	x	x	x	x	x	x	x		
0xE4 Read	ISRC1_PACKET_BYTE_10	**ISRC1_PB10[7:0]** ISRC1 Packet Byte10	x	x	x	x	x	x	x	x		
0xE5 Read	ISRC1_PACKET_BYTE_11	**ISRC1_PB11[7:0]** ISRC1 Packet Byte11	x	x	x	x	x	x	x	x		
0xE6 Read	ISRC1_PACKET_BYTE_12	**ISRC1_PB12[7:0]** ISRC1 Packet Byte12	x	x	x	x	x	x	x	x		
0xE8 Read	ISRC1_PACKET_BYTE_13	**ISRC1_PB13[7:0]** ISRC1 Packet Byte13	x	x	x	x	x	x	x	x		
0xE9 Read	ISRC1_PACKET_BYTE_14	**ISRC1_PB14[7:0]** ISRC1 Packet Byte14	x	x	x	x	x	x	x	x		
0xEA Read	ISRC1_PACKET_BYTE_15	**ISRC1_PB15[7:0]** ISRC1 Packet Byte15	x	x	x	x	x	x	x	x		

Table 141: HDMI Map Details Register 0xEB to 0xFE

Subadress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0xEB Read	ISRC2_PACKET_BYTE_0	**ISRC2_PB0[7:0]** ISRC2 Packet Byte0	x	x	x	x	x	x	x	x	This is transmitted only when the ISRC-Continue bit (register 0xC8 bit 7) is set to 1	
0xEC Read	ISRC2_PACKET_BYTE_1	**ISRC2_PB1[7:0]** ISRC2 Packet Byte1	x	x	x	x	x	x	x	x		
0xED Read	ISRC2_PACKET_BYTE_2	**ISRC2_PB2[7:0]** ISRC2 Packet Byte2	x	x	x	x	x	x	x	x		
0xEE Read	ISRC2_PACKET_BYTE_3	**ISRC2_PB3[7:0]** ISRC2 Packet Byte3	x	x	x	x	x	x	x	x		
0xF0 Read	ISRC2_PACKET_BYTE_4	**ISRC2_PB4[7:0]** ISRC2 Packet Byte4	x	x	x	x	x	x	x	x		
0xF1 Read	ISRC2_PACKET_BYTE_5	**ISRC2_PB5[7:0]** ISRC2 Packet Byte5	x	x	x	x	x	x	x	x		
0xF2 Read	ISRC2_PACKET_BYTE_6	**ISRC2_PB6[7:0]** ISRC2 Packet Byte6	x	x	x	x	x	x	x	x		
0xF3 Read	ISRC2_PACKET_BYTE_7	**ISRC2_PB7[7:0]** ISRC2 Packet Byte7	x	x	x	x	x	x	x	x		
0xF4 Read	ISRC2_PACKET_BYTE_8	**ISRC2_PB8[7:0]** ISRC2 Packet Byte8	x	x	x	x	x	x	x	x		
0xF5 Read	ISRC2_PACKET_BYTE_9	**ISRC2_PB9[7:0]** ISRC2 Packet Byte9	x	x	x	x	x	x	x	x		
0xF6 Read	ISRC2_PACKET_BYTE_10	**ISRC2_PB10[7:0]** ISRC2 Packet Byte10	x	x	x	x	x	x	x	x		
0xF8 Read	ISRC2_PACKET_BYTE_11	**ISRC2_PB11[7:0]** ISRC2 Packet Byte11	x	x	x	x	x	x	x	x		
0xF9 Read	ISRC2_PACKET_BYTE_12	**ISRC2_PB12[7:0]** ISRC2 Packet Byte12	x	x	x	x	x	x	x	x		
0xFA Read	ISRC2_PACKET_BYTE_13	**ISRC2_PB13[7:0]** ISRC2 Packet Byte13	x	x	x	x	x	x	x	x		
0xFB Read	ISRC2_PACKET_BYTE_14	**ISRC2_PB14[7:0]** ISRC2 Packet Byte14	x	x	x	x	x	x	x	x		
0xFC Read	ISRC2_PACKET_BYTE_15	**ISRC2_PB15[7:0]** ISRC2 Packet Byte15	x	x	x	x	x	x	x	x		
0xFD Read	ISRC2_PACKET_BYTE_16	**ISRC2_PB16[7:0]** ISRC2 Packet Byte16	x	x	x	x	x	x	x	x		
0xFE Read	ISRC2_PACKET_BYTE_17	**ISRC2_PB17[7:0]** ISRC2 Packet Byte17	x	x	x	x	x	x	x	x		

2.6 Repeater KSV Map

Table 142: Repeater KSV Map Details Register 0x00 to 0x1E

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x00 Read	BKSV_0	BSKV[39:0] HDCP Receiver KSV										
		BSKV[7:0] See BSKV[39:0] above	x	x	x	x	x	x	x	x		
0x01 Read	BKSV_1	**BSKV[15:0]** See BSKV[15:0] above	x	x	x	x	x	x	x	x		
0x02 Read	BKSV_2	**BSKV[23:16]** See BSKV[39:0] above	x	x	x	x	x	x	x	x		
0x03 Read	BKSV_3	**BSKV[31:24]** see BSKV[39:0] above	x	x	x	x	x	x	x	x		
0x04 Read	BKSV_4	**BSKV[39:32]** See BSKV[39:0] above	x	x	x	x	x	x	x	x		
0x08 Read	Ri_0	Ri[15:0] Link verification response Ri.										
		Ri[7:0] See Ri[15:0] above	x	x	x	x	x	x	x	x		
0x09 Read	Ri_1	**Ri[15:8]** See Ri[15:0] above	x	x	x	x	x	x	x	x		
0x0A Read	Ri_1	Pj[7:0] Enhanced Link Verification Response Pj'										
		Pj[7:0] See Pj[7:0] above	x	x	x	x	x	x	x	x		
0x10 R/W	AKSV_0	ASKV[39:0] HDCP Transmitter KSV										
		ASKV[7:0] See ASKV[39:0] above	0	0	0	0	0	0	0	0		
0x11 R/W	AKSV_1	**ASKV[15:8]** See ASKV[39:0] above	0	0	0	0	0	0	0	0		
0x12 R/W	AKSV_2	**ASKV[23:16]** See ASKV[39:0] above	0	0	0	0	0	0	0	0		
0x13 R/W	AKSV_3	**ASKV[31:24]** See ASKV[39:0] above	0	0	0	0	0	0	0	0		
0x14 R/W	AKSV_4	**ASKV[39:32]** See ASKV[39:0] above	0	0	0	0	0	0	0	0		
0x15 R/W	Ainfo	Ainfo[7:0] Ainfo Register										
		Ainfo[7:0] See Ainfo[7:0] above	0	0	0	0	0	0	0	0		
0x18 R/W	AN_0	AN[63:0] Session random number An										
		AN[7:0] See AN[63:0] above	0	0	0	0	0	0	0	0		
0x18 R/W	AN_1	**AN[15:8]** See AN[63:0] above	0	0	0	0	0	0	0	0		
0x19 R/W	AN_2	**AN[23:16]** See AN[63:0] above	0	0	0	0	0	0	0	0		
0x1A R/W	AN_3	**AN[31:24]** See AN[63:0] above	0	0	0	0	0	0	0	0		
0x1B R/W	AN_4	**AN[39:32]** See AN[63:0] above	0	0	0	0	0	0	0	0		
0x1C R/W	AN_5	**AN[47:40]** See AN[63:0] above	0	0	0	0	0	0	0	0		
0x1D R/W	AN_6	**AN[55:48]** See AN[63:0] above	0	0	0	0	0	0	0	0		
0x1E R/W	AN_7	**AN[63:56]** See AN[63:0] above	0	0	0	0	0	0	0	0		

Table 143: Repeater KSV Map Details Register 0x20 to 0x33

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x20 R/W	SHA_A_0	SHA_A[31:0] H0 part of SHA-1 has value V'										
		SHA_A[7:0] See SHA_A[39:0] above	0	0	0	0	0	0	0	0		
0x21 R/W	SHA_A_1	**SHA_A[15:8]** See SHA_A[39:0] above	0	0	0	0	0	0	0	0		
0x22 R/W	SHA_A_2	**SHA_A[23:16]** See SHA_A[39:0] above	0	0	0	0	0	0	0	0		
0x23 R/W	SHA_A_3	**SHA_A[31:24]** See SHA_A[39:0] above	0	0	0	0	0	0	0	0		
0x24 R/W	SHA_B_0	SHA_B[31:0] H1 part of SHA-1 has value V'										
		SHA_B[7:0] See SHA_B[39:0] above	0	0	0	0	0	0	0	0		
0x25 R/W	SHA_B_1	**SHA_B[15:8]** See SHA_B[39:0] above	0	0	0	0	0	0	0	0		
0x26 R/W	SHA_B_2	**SHA_B[23:16]** See SHA_B[39:0] above	0	0	0	0	0	0	0	0		
0x27 R/W	SHA_B_3	**SHA_B[31:24]** See SHA_B[39:0] above	0	0	0	0	0	0	0	0		
0x28 R/W	SHA_C_0	SHA_C[31:0] H2 part of SHA-1 has value V'										
		SHA_C[7:0] See SHA_C[39:0] above	0	0	0	0	0	0	0	0		
0x29 R/W	SHA_C_1	**SHA_C[15:8]** See SHA_C[39:0] above	0	0	0	0	0	0	0	0		
0x2A R/W	SHA_C_2	**SHA_C[23:16]** See SHA_C[39:0] above	0	0	0	0	0	0	0	0		
0x2B R/W	SHA_C_3	**SHA_C[31:24]** See SHA_C[39:0] above	0	0	0	0	0	0	0	0		
0x2C R/W	SHA_D_0	SHA_D[31:0] H3 part of SHA-1 has value V'										
		SHA_C[7:0] See SHA_C[39:0] above	0	0	0	0	0	0	0	0		
0x2D R/W	SHA_D_1	**SHA_D[15:8]** See SHA_D[39:0] above	0	0	0	0	0	0	0	0		
0x2E R/W	SHA_D_2	**SHA_D[23:16]** See SHA_D[39:0] above	0	0	0	0	0	0	0	0		
0x2F R/W	SHA_D_3	**SHA_D[31:24]** See SHA_D[39:0] above	0	0	0	0	0	0	0	0		
0x30 R/W	SHA_E_0	SHA_E[31:0] H0 part of SHA-1 has value V'										
		SHA_E[7:0] See SHA_E[39:0] above	0	0	0	0	0	0	0	0		
0x31 R/W	SHA_E_1	**SHA_E[15:8]** See SHA_E[39:0] above	0	0	0	0	0	0	0	0		
0x32 R/W	SHA_E_2	**SHA_E[23:16]** See SHA_E[39:0] above	0	0	0	0	0	0	0	0		
0x33 R/W	SHA_E_3	**SHA_E[31:24]** See SHA_E[39:0] above	0	0	0	0	0	0	0	0		

Table 144: Repeater KSV Map Details Register 0x40 to 0x76

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x40 R/W	Bcaps	**Bcaps[7:0]** Bcaps value	0	0	0	0	0	0	0	0		
0x41 R/W	BStatus_0	BStatus[15:0] Bstatus value										
		BStatus[7:0] See BStatus[15:0] above	0	0	0	0	0	0	0	0		
0x42 R/W	BStatus_1	**BStatus[15:8]** See BStatus[15:0] above	0	0	0	0	0	0	0	0		
0x70 R/W	SPA_PortB_1	SPA_PortB[15:0] Source Physical Address of HDMI port B										This register is used to configure the internal EDID of PortB
		SPA_PortB[7:0] See SPA_PortB[15:0] above	0	0	0	0	0	0	0	0		
0x71 R/W	SPA_PortB_2	**SPA_PortB[15:8]** See SPA_PortB[15:0] above	0	0	0	0	0	0	0	0		
0x72 R/W	SPA_Location	**SPA_Location[7:0]** Location of the source physical address in the internal EDID of Port B	0	0	0	0	0	0	0	0		This register is used to configure the internal EDID of PortB
0x73 R/W	CTRL_BITS	**KSV_List_Ready** This bit must be set when KSV list has been updated in Repeater mode.								0	Set to 0 if KSV list is not ready	
										1	Set to 1 if KSV list is ready	
		EDID_A_Enable Internal EDID enable for Port A							0		Disable internal EDID for Port A	
									1		Enable Internal EDID for Port A	
		EDID_BA_Enable Internal EDID enable for Port B						0			Disable internal EDID for Port B	
								1			Enable Internal EDID for Port B	
		Reserved	0	0	0	0	0				Set to default	
0x76 R/W	PortB_Chsum	PortB_Chsum[7:0] CEA timing extension cheksum for internal EDI of Port B										This register is used to configure the internal EDID of PortB
		PortB_Chksum[7:0] See PortB_Chksum[7:0] above	0	0	0	0	0	0	0	0		

Table 145: Repeater KSV Map Details Register 0x80 to 0x93

Subadress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x80 R/W	KSV0_B0	KSV0[39:0] KSV0 of KSV list										
		KSV0[7:0] See KSV0[39:0] above	0	0	0	0	0	0	0	0		
0x81 R/W	KSV0_B1	**KSV0[15:8]** See KSV0[39:0] above	0	0	0	0	0	0	0	0		
0x82 R/W	KSV0_B2	**KSV0[23:16]** See KSV0[39:0] above	0	0	0	0	0	0	0	0		
0x83 R/W	KSV0_B3	**KSV0[31:24]** See KSV0[39:0] above	0	0	0	0	0	0	0	0		
0x84 R/W	KSV0_B4	**KSV0[39:32]** See KSV0[39:0] above	0	0	0	0	0	0	0	0		
0x85 R/W	KSV1_B0	KSV1[39:0] KSV1 of KSV list										
		KSV1[7:0] See KSV1[39:0] above	0	0	0	0	0	0	0	0		
0x86 R/W	KSV1_B1	**KSV1[15:8]** See KSV1[39:0] above	0	0	0	0	0	0	0	0		
0x87 R/W	KSV1_B2	**KSV1[23:16]** See KSV1[39:0] above	0	0	0	0	0	0	0	0		
0x88 R/W	KSV1_B3	**KSV1[31:24]** See KSV1[39:0] above	0	0	0	0	0	0	0	0		
0x89 R/W	KSV1_B4	**KSV1[39:32]** See KSV1[39:0] above	0	0	0	0	0	0	0	0		
0x8A R/W	KSV2_B0	KSV2[39:0] KSV2 of KSV list										
		KSV2[7:0] See KSV2[39:0] above	0	0	0	0	0	0	0	0		
0x8B R/W	KSV2_B1	**KSV2[15:8]** See KSV2[39:0] above	0	0	0	0	0	0	0	0		
0x8C R/W	KSV2_B2	**KSV2[23:16]** See KSV2[39:0] above	0	0	0	0	0	0	0	0		
0x8D R/W	KSV2_B3	**KSV2[31:24]** See KSV2[39:0] above	0	0	0	0	0	0	0	0		
0x8E R/W	KSV2_B4	**KSV2[39:32]** See KSV2[39:0] above	0	0	0	0	0	0	0	0		
0x8F R/W	KSV3_B0	KSV3[39:0] KSV3 of KSV list										
		KSV3[7:0] See KSV3[39:0] above	0	0	0	0	0	0	0	0		
0x90 R/W	KSV3_B1	**KSV3[15:8]** See KSV3[39:0] above	0	0	0	0	0	0	0	0		
0x91 R/W	KSV3_B2	**KSV3[23:16]** See KSV3[39:0] above	0	0	0	0	0	0	0	0		
0x92 R/W	KSV3_B3	**KSV3[31:24]** See KSV3[39:0] above	0	0	0	0	0	0	0	0		
0x93 R/W	KSV3_B4	**KSV3[39:32]** See KSV3[39:0] above	0	0	0	0	0	0	0	0		

Table 146: Repeater KSV Map Details Register 0x94 to 0xA7

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x94 R/W	KSV4_B0	KSV4[39:0] KSV4 of KSV list										
		KSV4[7:0] See KSV4[39:0] above	0	0	0	0	0	0	0	0		
0x95 R/W	KSV4_B1	**KSV4[15:8]** See KSV4[39:0] above	0	0	0	0	0	0	0	0		
0x96 R/W	KSV4_B2	**KSV4[23:16]** See KSV4[39:0] above	0	0	0	0	0	0	0	0		
0x97 R/W	KSV4_B3	**KSV4[31:24]** See KSV4[39:0] above	0	0	0	0	0	0	0	0		
0x98 R/W	KSV4_B4	**KSV4[39:32]** See KSV4[39:0] above	0	0	0	0	0	0	0	0		
0x99 R/W	KSV5_B0	KSV5[39:0] KSV5 of KSV list										
		KSV5[7:0] See KSV5[39:0] above	0	0	0	0	0	0	0	0		
0x9A R/W	KSV5_B1	**KSV5[15:8]** See KSV5[39:0] above	0	0	0	0	0	0	0	0		
0x9B R/W	KSV5_B2	**KSV[23:16]** See KSV5[39:0] above	0	0	0	0	0	0	0	0		
0x9C R/W	KSV5_B3	**KSV5[31:24]** See KSV5[39:0] above	0	0	0	0	0	0	0	0		
0x9D R/W	KSV5_B4	**KSV5[39:32]** See KSV5[39:0] above	0	0	0	0	0	0	0	0		
0x9E R/W	KSV6_B0	KSV6[39:0] KSV6 of KSV list										
		KSV6[7:0] See KSV6[39:0] above	0	0	0	0	0	0	0	0		
0x9F R/W	KSV6_B1	**KSV6[15:8]** See KSV6[39:0] above	0	0	0	0	0	0	0	0		
0xA0 R/W	KSV6_B2	**KSV6[23:16]** See KSV6[39:0] above	0	0	0	0	0	0	0	0		
0xA1 R/W	KSV6_B3	**KSV6[31:24]** See KSV6[39:0] above	0	0	0	0	0	0	0	0		
0xA2 R/W	KSV6_B4	**KSV6[39:32]** See KSV6[39:0] above	0	0	0	0	0	0	0	0		
0xA3 R/W	KSV7_B0	KSV7[39:0] KSV7 of KSV list										
		KSV7[7:0] See KSV7[39:0] above	0	0	0	0	0	0	0	0		
0xA4 R/W	KSV7_B1	**KSV7[15:8]** See KSV7[39:0] above	0	0	0	0	0	0	0	0		
0xA5 R/W	KSV7_B2	**KSV7[23:16]** See KSV7[39:0] above	0	0	0	0	0	0	0	0		
0xA6 R/W	KSV7_B3	**KSV7[31:24]** See KSV7[39:0] above	0	0	0	0	0	0	0	0		
0xA7 R/W	KSV7_B4	**KSV7[39:32]** See KSV7[39:0] above	0	0	0	0	0	0	0	0		

Table 147: Repeater KSV Map Details Register 0xA8 to 0xBB

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0xA8 R/W	KSV8_B0	KSV8[39:0] KSV8 of KSV list										
		KSV8[7:0] See KSV8[39:0] above	0	0	0	0	0	0	0	0		
0xA9 R/W	KSV8_B1	**KSV8[15:8]** See KSV8[39:0] above	0	0	0	0	0	0	0	0		
0xAA R/W	KSV8_B2	**KSV8[23:16]** See KSV8[39:0] above	0	0	0	0	0	0	0	0		
0xAB R/W	KSV8_B3	**KSV8[31:24]** See KSV8[39:0] above	0	0	0	0	0	0	0	0		
0xAC R/W	KSV8_B4	**KSV8[39:32]** See KSV8[39:0] above	0	0	0	0	0	0	0	0		
0xAD R/W	KSV9_B0	KSV9[39:0] KSV9 of KSV list										
		KSV9[7:0] See KSV9[39:0] above	0	0	0	0	0	0	0	0		
0xAE R/W	KSV9_B1	**KSV9[15:8]** See KSV9[39:0] above	0	0	0	0	0	0	0	0		
0xAF R/W	KSV9_B2	**KSV9[23:16]** See KSV9[39:0] above	0	0	0	0	0	0	0	0		
0xB0 R/W	KSV9_B3	**KSV9[31:24]** See KSV9[39:0] above	0	0	0	0	0	0	0	0		
0xB1 R/W	KSV9_B4	**KSV9[39:32]** See KSV9[39:0] above	0	0	0	0	0	0	0	0		
0xB2 R/W	KSV10_B0	KSV10[39:0] KSV10 of KSV list										
		KSV10[7:0] See KSV10[39:0] above	0	0	0	0	0	0	0	0		
0xB3 R/W	KSV10_B1	**KSV10[15:8]** See KSV10[39:0] above	0	0	0	0	0	0	0	0		
0xB4 R/W	KSV10_B2	**KSV10[23:16]** See KSV10[39:0] above	0	0	0	0	0	0	0	0		
0xB5 R/W	KSV10_B3	**KSV10[31:24]** See KSV10[39:0] above	0	0	0	0	0	0	0	0		
0xB6 R/W	KSV10_B4	**KSV10[39:32]** See KSV10[39:0] above	0	0	0	0	0	0	0	0		
0xB7 R/W	KSV11_B0	KSV11[39:0] KSV11 of KSV list										
		KSV11[7:0] See KSV11[39:0] above	0	0	0	0	0	0	0	0		
0xB8 R/W	KSV11_B1	**KSV11[15:8]** See KSV11[39:0] above	0	0	0	0	0	0	0	0		
0xB9 R/W	KSV11_B2	**KSV11[23:16]** See KSV11[39:0] above	0	0	0	0	0	0	0	0		
0xBA R/W	KSV11_B3	**KSV11[31:24]** See KSV11[39:0] above	0	0	0	0	0	0	0	0		
0xBB R/W	KSV11_B4	**KSV11[39:32]** See KSV11[39:0] above	0	0	0	0	0	0	0	0		

Table 148: Repeater KSV Map Details Register 0xBC to 0xCF

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0xBC R/W	KSV12_B0	KSV12[39:0] KSV12 of KSV list										
		KSV12[7:0] See KSV12[39:0] above	0	0	0	0	0	0	0	0		
0xBD R/W	KSV12_B1	**KSV12[15:8]** See KSV12[39:0] above	0	0	0	0	0	0	0	0		
0xBE R/W	KSV12_B2	**KSV12[23:16]** See KSV12[39:0] above	0	0	0	0	0	0	0	0		
0xBF R/W	KSV12_B3	**KSV12[31:24]** See KSV12[39:0] above	0	0	0	0	0	0	0	0		
0xC0 R/W	KSV12_B4	**KSV12[39:32]** See KSV12[39:0] above	0	0	0	0	0	0	0	0		
0xC1 R/W	KSV13_B0	KSV13[39:0] KSV13 of KSV list										
		KSV13[7:0] See KSV13[39:0] above	0	0	0	0	0	0	0	0		
0xC2 R/W	KSV13_B1	**KSV[15:8]** See KSV[39:0] above	0	0	0	0	0	0	0	0		
0xC3 R/W	KSV13_B2	**KSV13[23:16]** See KSV13[39:0] above	0	0	0	0	0	0	0	0		
0xC4 R/W	KSV13_B3	**KSV13[31:24]** See KSV13[39:0] above	0	0	0	0	0	0	0	0		
0xC5 R/W	KSV13_B4	**KSV13[39:32]** See KSV13[39:0] above	0	0	0	0	0	0	0	0		
0xC6 R/W	KSV14_B0	KSV14[39:0] KSV14 of KSV list										
		KSV14[7:0] See KSV14[39:0] above	0	0	0	0	0	0	0	0		
0xC7 R/W	KSV14_B1	**KSV14[15:8]** See KSV14[39:0] above	0	0	0	0	0	0	0	0		
0xC8 R/W	KSV14_B2	**KSV14[23:16]** See KSV14[39:0] above	0	0	0	0	0	0	0	0		
0xC9 R/W	KSV14_B3	**KSV14[31:24]** See KSV14[39:0] above	0	0	0	0	0	0	0	0		
0xCA R/W	KSV14_B4	**KSV14[39:32]** See KSV14[39:0] above	0	0	0	0	0	0	0	0		
0xCB R/W	KSV15_B0	KSV15[39:0] KSV15 of KSV list										
		KSV15[7:0] See KSV15[39:0] above	0	0	0	0	0	0	0	0		
0xCC R/W	KSV15_B1	**KSV15[15:8]** See KSV15[39:0] above	0	0	0	0	0	0	0	0		
0xCD R/W	KSV15_B2	**KSV15[23:16]** See KSV15[39:0] above	0	0	0	0	0	0	0	0		
0xCD R/W	KSV15_B3	**KSV15[31:24]** See KSV15[39:0] above	0	0	0	0	0	0	0	0		
0xCF R/W	KSV15_B4	**KSV15[39:32]** See KSV15[39:0] above	0	0	0	0	0	0	0	0		

Table 149: Repeater KSV Map Details Register 0xD0 to 0xE3

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0xD0 R/W	KSV16_B0	KSV16[39:0] KSV16 of KSV list										
		KSV16[7:0] See KSV16[39:0] above	0	0	0	0	0	0	0	0		
0xD1 R/W	KSV16_B1	**KSV16[15:8]** See KSV16[39:0] above	0	0	0	0	0	0	0	0		
0xD2 R/W	KSV16_B2	**KSV16[23:16]** See KSV16[39:0] above	0	0	0	0	0	0	0	0		
0xD3 R/W	KSV16_B3	**KSV16[31:24]** See KSV16[39:0] above	0	0	0	0	0	0	0	0		
0xD4 R/W	KSV16_B4	**KSV16[39:32]** See KSV16[39:0] above	0	0	0	0	0	0	0	0		
0xD5 R/W	KSV17_B0	KSV17[39:0] KSV17 of KSV list										
		KSV17[7:0] See KSV17[39:0] above	0	0	0	0	0	0	0	0		
0xD6 R/W	KSV17_B1	**KSV[15:8]** See KSV[39:0] above	0	0	0	0	0	0	0	0		
0xD7 R/W	KSV17_B2	**KSV17[23:16]** See KSV17[39:0] above	0	0	0	0	0	0	0	0		
0xD8 R/W	KSV17_B3	**KSV17[31:24]** See KSV17[39:0] above	0	0	0	0	0	0	0	0		
0xD9 R/W	KSV17_B4	**KSV17[39:32] See KSV17[39:0] above**	0	0	0	0	0	0	0	0		
0xDA R/W	KSV18_B0	KSV18[39:0] KSV18 of KSV list										
		KSV18[7:0] See KSV18[39:0] above	0	0	0	0	0	0	0	0		
0xDB R/W	KSV18_B1	**KSV18[15:8]** See KSV18[39:0] above	0	0	0	0	0	0	0	0		
0xDC R/W	KSV18_B2	**KSV18[23:16]** See KSV18[39:0] above	0	0	0	0	0	0	0	0		
0xDD R/W	KSV18_B3	**KSV18[31:24]** See KSV18[39:0] above	0	0	0	0	0	0	0	0		
0xDE R/W	KSV18_B4	**KSV18[39:32]** See KSV18[39:0] above	0	0	0	0	0	0	0	0		
0xDF R/W	KSV19_B0	KSV19[39:0] KSV19 of KSV list										
		KSV19[7:0] See KSV19[39:0] above	0	0	0	0	0	0	0	0		
0xE0 R/W	KSV19_B1	**KSV19[15:8]** See KSV19[39:0] above	0	0	0	0	0	0	0	0		
0xE1 R/W	KSV19_B2	**KSV19[23:16]** See KSV19[39:0] above	0	0	0	0	0	0	0	0		
0xE2 R/W	KSV19_B3	**KSV19[31:24]** See KSV19[39:0] above	0	0	0	0	0	0	0	0		
0xE3 R/W	KSV19_B4	**KSV19[39:32]** See KSV19[39:0] above	0	0	0	0	0	0	0	0		

Table 150: Repeater KSV Map Details Register 0xE4 to 0xF7

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0xE4 R/W	KSV20_B0	KSV20[39:0] KSV20 of KSV list										
		KSV20[7:0] See KSV20[39:0] above	0	0	0	0	0	0	0	0		
0xE5 R/W	KSV20_B1	**KSV20[15:8]** See KSV20[39:0] above	0	0	0	0	0	0	0	0		
0xE6 R/W	KSV20_B2	**KSV20[23:16]** See KSV20[39:0] above	0	0	0	0	0	0	0	0		
0xE7 R/W	KSV20_B3	**KSV20[31:24]** See KSV20[39:0] above	0	0	0	0	0	0	0	0		
0xE8 R/W	KSV20_B4	**KSV20[39:32]** See KSV20[39:0] above	0	0	0	0	0	0	0	0		
0xE9 R/W	KSV21_B0	KSV21[39:0] KSV21 of KSV list										
		KSV21[7:0] See KSV21[39:0] above	0	0	0	0	0	0	0	0		
0xEA R/W	KSV21_B1	**KSV[15:8]** See KSV[39:0] above	0	0	0	0	0	0	0	0		
0xEB R/W	KSV21_B2	**KSV21[23:16]** See KSV21[39:0] above	0	0	0	0	0	0	0	0		
0xEC R/W	KSV21_B3	**KSV21[31:24]** See KSV21[39:0] above	0	0	0	0	0	0	0	0		
0xED R/W	KSV21_B4	**KSV21[39:32]** See KSV21[39:0] above	0	0	0	0	0	0	0	0		
0xEE R/W	KSV22_B0	KSV22[39:0] KSV22 of KSV list										
		KSV22[7:0] See KSV22[39:0] above	0	0	0	0	0	0	0	0		
0xEF R/W	KSV22_B1	**KSV22[15:8]** See KSV22[39:0] above	0	0	0	0	0	0	0	0		
0xF0 R/W	KSV22_B2	**KSV22[23:16]** See KSV22[39:0] above	0	0	0	0	0	0	0	0		
0xF1 R/W	KSV22_B3	**KSV22[31:24]** See KSV22[39:0] above	0	0	0	0	0	0	0	0		
0xF2 R/W	KSV22_B4	**KSV22[39:32]** See KSV22[39:0] above	0	0	0	0	0	0	0	0		
0xF3 R/W	KSV23_B0	KSV23[39:0] KSV23 of KSV list										
		KSV23[7:0] See KSV23[39:0] above	0	0	0	0	0	0	0	0		
0xF4 R/W	KSV23_B1	**KSV23[15:8]** See KSV23[39:0] above	0	0	0	0	0	0	0	0		
0xF5 R/W	KSV23_B2	**KSV23[23:16]** See KSV23[39:0] above	0	0	0	0	0	0	0	0		
0xF6 R/W	KSV23_B3	**KSV23[31:24]** See KSV23[39:0] above	0	0	0	0	0	0	0	0		
0xF7 R/W	KSV23_B4	**KSV23[39:32]** See KSV23[39:0] above	0	0	0	0	0	0	0	0		

List of Tables

Document Revision History

Version	Date	Changes
Rev. 0	November 2007	Initial
Rev. A	February 2008	**User Map 1** - Added Reg. 0x9E description to global register map (Table 3)
Rev. B	July 2009	Updated Table 2. Register 0xC5 name.
		Updated Table 3. Added register 0x4D description. Added the following bits: 0x4E [7]
		Removed duplicate description in Table 37.
		Table 69 updated. Description of FL_PLL_LOCKED
		Table 84 updated. Description of GAMUT_MDATA_ST
		Table 86 updated. V_LOCKED_MB1
		Added bit 0 of HDMI_INT_MASKB_3 to Table 86
		Added bit 5 to register 0x70 of Table 93
		Table 95 updated. Updated description of AKSV_UPDSTE_CLR
		Table 96 updated.
		Correction to Table 125. Description of FIELD1_VS_BACK_PORCH
		Correction to Table 133. Description of LINE_START_MSB
		Typo corrected in Table 138
		Table 139 ACP descriptions (0xC2 – 0xD6) corrected
Rev. C	May 2010	Removed confidential references
Rev. D	June 2010	Added copyright

