HDMI Audio Settings for the AD9880 (and derivatives)

To fully support all audio modes for all video resolutions up to 1080p, it is necessary to adjust certain audio-related registers from their power-on default values. Table 1 describes these registers and gives the recommended settings.

Table1: AD9880 Audio Register Settings

Register	Bits	Recommended Setting		Function	Comments
		All Modes / Optimized 1080p	Optimized VGA/480p		
0x01	7:0	0x00	0x00	PLL Divisor (MSB's)	The analog video PLL is also used for the audio clock circuit when in HDMI mode. This is done automatically.
0x02	7:4	0x40	0x40	PLL Divisor (LSB's)	
0x03	7:6	01	01	VCO Range	
	5:3	010	010	Charge Pump Current	
	2	1	**0**[2]	PLL Enable	In HDMI mode, this bit enables a lower frequency to be used for audio MCLK generation
0x25	5:4	01	01	Output Drive Strength	Medium-low setting reduces system noise
0x34	5	1	1	Audio Frequency Select	0 = 1.25x clock 1 = 2.5x clock
	4	0	0	Audio Frequency Mode Override	0 = low freq. mode of Audio PLL set automatically 1= low freq. mode set by 0x34[5]
0x58	7	1	1	PLL Enable	This enables the analog PLL to be used for audio MCLK generation
	6:4	001	**011**	MCLK PLL Divisor	001 = /2 011 = /4
	3	0	0	N/CTS Disable	The N and CTS values should always be enabled
	2:0	001	001	MCLK Sampling Frequency	000 = 128*Fs 001 = 256*Fs 010 = 384*Fs 011 = 512*Fs

Notes: 1. The audio PLL must be "reset" by writing 0x00 to R0x7F upon every mode change.
2. Differences from the "all modes" recommendation are in red.

AD9880 Audio MCLK Generation