# ADV7181C Interrupts

The goal of this document is to describe how to set up the ADV7181C on the EVAL-ADV7181CEBZ evaluation board to generate interrupts when the input signal gets plugged in, plugged out, and when the input resolution changes.

## Example 1: CVBS Input

In this example, a CVBS signal is provided to the ADV7181C evaluation board. The signal is an NTSC signal and is plugged in initially.

1. Run the following recommended CVBS script from ADV7181C_ADV7181C@_ADV7341-VER.3.2c.txt:

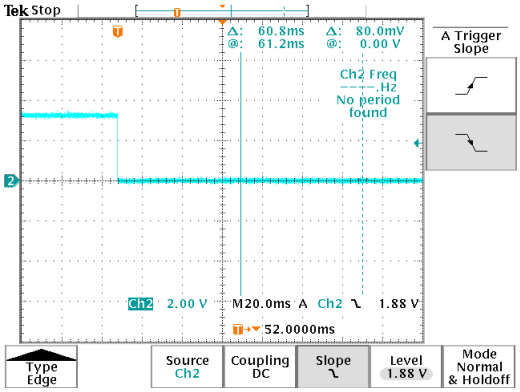
```
:AUTODETECT CVBS IN NTSC/PAL/SECAM, 8-Bit 422 encoder:
42 00 00 ; CVBS IN
42 03 0C ; 8 Bit Mode
42 04 77 ; Enable SFL
42 17 41 ; select SH1
42 1D 47 ; Enable 28MHz Crystal
42 31 02 ; Clears NEWAV_MODE, SAV/EAV  to suit ADV video encoders
42 3A 17 ; Set Latch Clock & power down ADC 1 & ADC2 & ADC3
42 3B 81 ; Enable internal Bias
42 3D A2 ; MWE Enable Manual Window, Colour Kill Threshold to 2
42 3E 6A ; BLM optimisation
42 3F A0 ; BGB
42 86 0B ; Enable stdi_line_count_mode
42 F3 01 ; Enable Anti Alias Filter on ADC0
42 F9 03 ; Set max v lock range
42 0E 80 ; ADI Recommended Setting
42 52 46 ; ADI Recommended Setting
42 54 00 ; ADI Recommended Setting
42 7F FF ; ADI Recommended Setting
42 81 30 ; ADI Recommended Setting
42 90 C9 ; ADI Recommended Setting
42 91 40 ; ADI Recommended Setting
42 92 3C ; ADI Recommended Setting
42 93 CA ; ADI Recommended Setting
42 94 D5 ; ADI Recommended Setting
42 B1 FF ; ADI Recommended Setting
42 B6 08 ; ADI Recommended Setting
42 C0 9A ; ADI Recommended Setting
42 CF 50 ; ADI Recommended Setting
42 D0 4E ; ADI Recommended Setting
42 D1 B9 ; ADI Recommended Setting
42 D6 DD ; ADI Recommended Setting
42 D7 E2 ; ADI Recommended Setting
42 E5 51 ; ADI Recommended Setting
42 F6 3B ; ADI Recommended Setting
42 0E 00 ; ADI Recommended Setting
56 17 02 ; Software Reset
56 00 FC ; Power up all DAcs and PLL
56 01 80 ; SD only mode, Data input on Y-bus
56 80 10 ; SSAF Luma filter enabled, NTSC mode
56 82 c9 ; Step control on, pixel data valid, pedestal on, PrPb SSAF on,CVBS/YC out.
56 84 06 ; RTCO/SFL Enable
56 88 00 ; 8 bit input enabled
56 87 20 ; Encoder PAL/NTSC auto-detect enabled
End
```

2. Enter the User Sub Map 1 and configure the interrupts:

```
42 0E 20 ; Enter User Sub Map
42 40 C1 ; Interrupt active until cleared, Drive Low when Active
42 44 03 ; Unmask SD_LOCK_Q and SD_UNLOCK_Q
42 43 83 ; Clear SD_LOCK_Q and SD_UNLOCK_Q
42 4C 81 ; Unmask SD_OP_CHNG_Q
42 4B C1 ; Clear SD_OP_CHNG_Q
42 0E 00 ; Exit User Sub Map
```

3. **Unplug CVBS source signal**

**→ Interrupt happens: INT signal goes Low and remains Low**




4. Read the Interrupt Status registers:

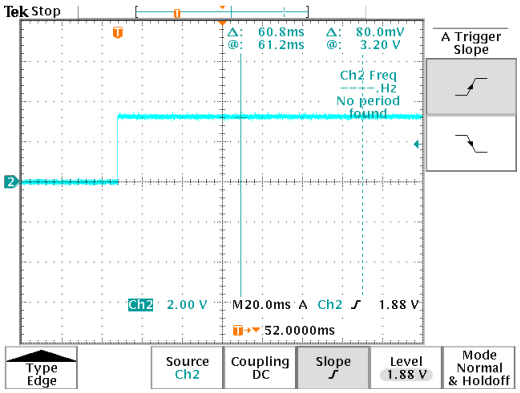
```
42 0E 20 ; Enter User Sub Map
```

Value in Register 0x42 is 0x02, meaning SD_UNLOCK_Q went High.

5. Clear Interrupt

```
42 43 80 ; Unclear SD_LOCK_Q and SD_UNLOCK_Q
42 43 83 ; Clear SD_LOCK_Q and SD_UNLOCK_Q
42 0E 00 ; Exit User Sub Map
```

**→ INT goes back High and remains High**



6. **Plug CVBS source signal**

**→ Interrupt happens: INT signal goes Low and remains Low**

7. Read the Interrupt Status registers:

```
42 0E 20 ; Enter User Sub Map
```

Value in Register 0x42 is 0x01, meaning SD_LOCK_Q went High.

8. Clear Interrupt

```
42 43 80 ; Unclear SD_LOCK_Q and SD_UNLOCK_Q
42 43 83 ; Clear SD_LOCK_Q and SD_UNLOCK_Q
42 0E 00 ; Exit User Sub Map
```

**→ INT goes back High and remains High**

9. **Change Source standard from NTSC to PAL**

**→ Interrupt happens: INT signal goes Low and remains Low**

10. Read the Interrupt Status registers:

```
42 0E 20 ; Enter User Sub Map
```

Value in Register 0x4A is 0x01, meaning SD_OP_CHNG_Q went High.

11. Clear Interrupt

```
42 4B C0 ; Unclear SD_OP_CHNG_Q
42 43 C1 ; Clear SD_OP_CHNG_Q
42 0E 00 ; Exit User Sub Map
```

**→ INT goes back High and remains High**

**Example 2: Component Input**

In this example, a YPrPb signal is provided to the ADV7181C evaluation board. The signal is a 480p signal and is plugged in initially.

1. Run one of the recommended 480p script from ADV7181C_ADV7181C@_ADV7341-VER.3.2c.txt, for example:

```
:525p/60Hz YPrPb In 20Bit 422 EAV/SAV Encoder:
42 05 01 ; PRIM_MODE = 001b COMP
42 06 06 ; VID_STD for 525P 2x1
42 C3 46 ; ADC1 to Ain4, ADC0 to Ain6,
42 C4 B5 ; ADC2 to Ain5 and enables manual override of mux
42 1D 47 ; Enable 28.63636MHz crystal
42 3A 11 ; Set Latch Clock 01b. Power down ADC3.
```

```
42 3B 81 ; Enable Internal Bias
42 3C 53 ; PLL QPUMP to 011b
42 6B 81 ; 422 20bit out
42 C9 00 ; SDR mode
42 73 CF ; Enable Manual Gain and set CH_A gain
42 74 A3 ; Set CH_A and CH_B Gain - 0FAh
42 75 E8 ; Set CH_B and CH_C Gain
42 76 FA ; Set CH_C Gain
42 7B 1E ; Enable EAV and SAV Codes.
42 85 19 ; Turn off SSPD and force SOY
42 86 0B ; Enable STDI Line Count Mode
42 8A B0 ; Manual VCO Range=01
42 BF 06 ; Blue Screen Free Run Colour
42 C0 40 ; default color
42 C1 F0 ; default color
42 C2 80 ; Default color
42 C5 01 ;
42 0E 80 ; ADI recommended sequence
42 52 46 ; ADI recommended sequence
42 54 00 ; ADI recommended sequence
42 57 01 ; ADI recommended sequence
42 F6 3B ; ADI Recommended Setting
42 0E 00 ; ADI recommended sequence
56 17 02 ; Software Reset
56 00 1C ; Power up DACs and PLL
56 02 21 ; YPbPr out / Rev.3 operation 861B
56 01 10 ; ED/HD-SDR only mode
56 30 04 ; 525p@60 Frame rate, EAV/SAV
56 31 01 ; H54X enabled, Pixel data valid
56 33 6D ; PrPb SSAF, Sync filter enabled, 422 enabled
56 39 20 ; ED/HD 861B Timing
End
```

2. Enter the User Sub Map 1 and configure the interrupts:

```
42 0E 20 ; Enter User Sub Map
42 40 C1 ; Interrupt active until cleared, Drive Low when Active
42 44 1C ; Unmask STDI_DVALID_Q, CP_LOCK_Q and CP_UNLOCK_Q
42 43 9C ; Clear STDI_DVALID_Q, CP_LOCK_Q and CP_UNLOCK_Q
42 0E 00 ; Exit User Sub Map
```

3. **Unplug Y signal from source**

**→ Interrupt happens: INT signal goes Low and remains Low**

4. Read the Interrupt Status registers:

```
42 0E 20 ; Enter User Sub Map
```

Value in Register 0x42 is 0x18, meaning CP_UNLOCK_Q and STDI_DVALID_Q went High.

5. Clear Interrupt

```
42 43 80 ; Unclear STDI_DVALID_Q, CP_LOCK_Q and CP_UNLOCK_Q
42 43 9C ; Clear STDI_DVALID_Q, CP_LOCK_Q and CP_UNLOCK_Q
42 0E 00 ; Exit User Sub Map
```

**→ INT goes back High and remains High**

6. **Plug Y signal from source back**

**→ Interrupt happens: INT signal goes Low and remains Low**

7. Read the Interrupt Status registers:

```
42 0E 20 ; Enter User Sub Map
```

Value in Register 0x42 is 0x14, meaning CP_LOCK_Q and STDI_DVALID_Q went High.

8. Clear Interrupt

```
42 43 80 ; Unclear STDI_DVALID_Q, CP_LOCK_Q and CP_UNLOCK_Q
42 43 9C ; Clear STDI_DVALID_Q, CP_LOCK_Q and CP_UNLOCK_Q
42 0E 00 ; Exit User Sub Map
```

**→ INT goes back High and remains High**

9. **Change Source standard from 480p to 1080i60**

**→ Interrupt happens: INT signal goes Low and remains Low**

10. Read the Interrupt Status registers:

```
42 0E 20 ; Enter User Sub Map
```

Value in Register 0x42 is 0x18, meaning CP_UNLOCK_Q and STDI_DVALID_Q went High.

11. Clear Interrupt

```
42 43 80 ; Unclear STDI_DVALID_Q, CP_LOCK_Q and CP_UNLOCK_Q
42 43 9C ; Clear STDI_DVALID_Q, CP_LOCK_Q and CP_UNLOCK_Q
42 0E 00 ; Exit User Sub Map
```

**→ INT goes back High and remains High**