225 MHz High Performance HDMI Transmitter with CEC

ADV7510

FEATURES

General
- Incorporates HDMI (v.1.3 with Deep Color, x.v.Color)
- 225 MHz supports 12-bit Deep Color operation in all video formats up to 1080p
- Supports Gamut Metadata Packet transmission
- Integrated CEC buffer/controller
- Compatible with DVI v.1.0, and HDCP v.1.3
- Video/audio inputs accept logic levels from 1.8 V to 3.3 V

Digital video
- Programmable two-way color space converter
- Supports RGB, YCbCr, and DDR
- Supports ITU656-based embedded syncs
- Auto input video format timing detection (CEA-861-D)

Digital audio
- Supports standard S/PDIF for stereo LPCM or compressed audio up to 192 kHz
- 8-channel uncompressed LPCM I²S audio up to 192 kHz

Special features for easy system design
- On-chip MPU with I²C master to perform HDCP operations and EDID reading operations
- 5 V tolerant I²C and HPD I/Os, no extra device needed
- No audio master clock needed for supporting S/PDIF and I²S
- On-chip MPU reports HDMI events through interrupts and registers

FUNCTIONAL BLOCK DIAGRAM

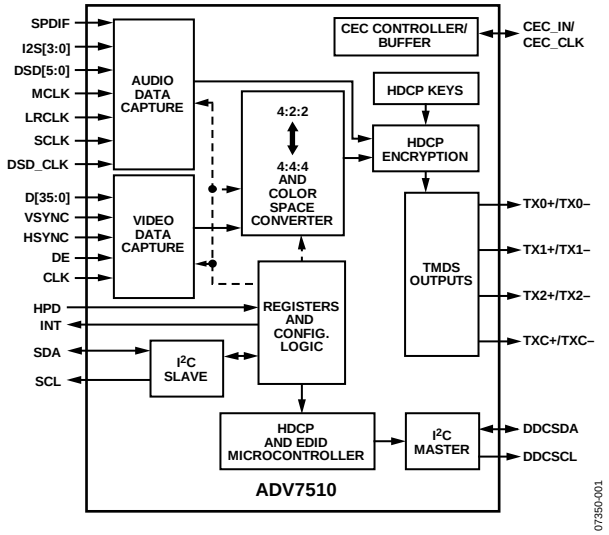

Figure 1.

GENERAL DESCRIPTION

The ADV7510 is a 225 MHz High Definition Multimedia Interface (HDMI™) transmitter, which is ideal for home entertainment products including DVD players/recorders, digital set top boxes, A/V receivers, gaming consoles, and PCs.

The digital video interface contains an HDMI and a DVI v.1.0-compatible transmitter, and supports all HDTV formats (including 1080p with 12-bit Deep Color). The ADV7510 also supports x.v.Color™, high bit rate audio, digital theater sound (DTS), and programmable AVI InfoFrames features.

With the inclusion of HDCP, the ADV7510 allows the secure transmission of protected content as specified by the HDCP v.1.3 protocol.

The ADV7510 supports both S/PDIF and 8-channel I²S audio. Its high fidelity 8-channel I²S can transmit either stereo or 7.1 surround audio up to 768 kHz. The S/PDIF can carry compressed audio including Dolby® Digital, DTS®, and THX®.

Fabricated in an advanced CMOS process, the ADV7510 is provided in a 100-lead LQFP surface-mount plastic package and is specified over the −25°C to +85°C temperature range.

Rev. Sp0

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REVISION HISTORY

10/08—Revision Sp0: Initial Version

ABSOLUTE MAXIMUM RATINGS

Table 1.

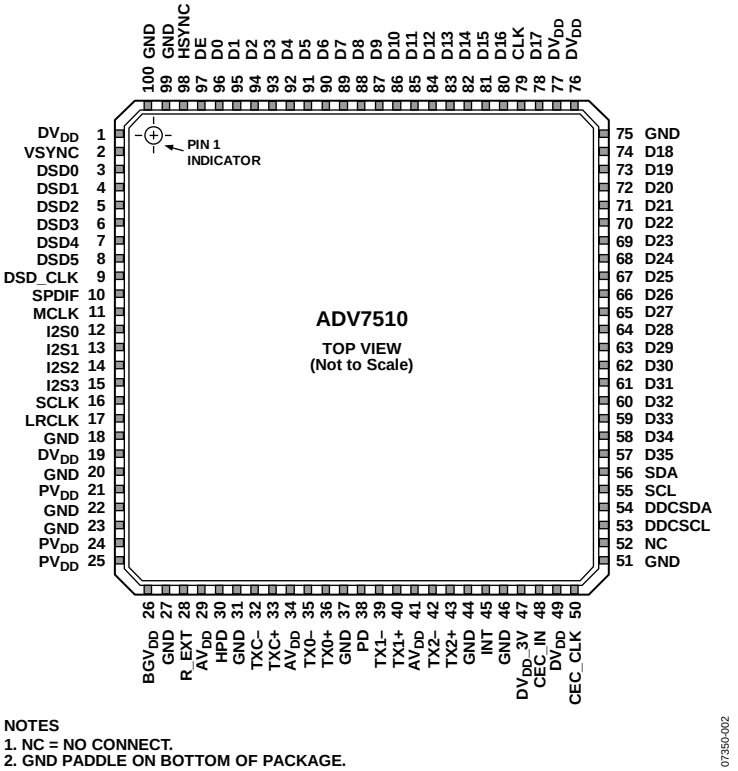
Parameter	Rating
Digital Inputs (SDA, SCL, DDCSDA, DDCSCL, HPD, CEC_IN, CEC_CLK, PD)	−0.3 V to +5.5 V
Audio/Video Digital Inputs (DSD[5:0], MCLK, SPDIF, I2S[3:0], SCLK, HSYNC, DE, VSYNC)	−0.3 V to +3.6 V
Digital Output Current	20 mA
Operating Temperature Range	−40°C to +100°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT.
2. GND PADDLE ON BOTTOM OF PACKAGE.

Figure 2. Pin Configuration

Table 2. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 19, 49, 76, 77	DV_{DD}	Power	1.8 V Power Supply. These pins should be filtered and as quiet as possible.
2	VSYNC	Input	Vertical Sync Input.
3 to 8	DSD[5:0]	Input	DSD Audio Data Inputs.
9	DSD_CLK	Input	DSD Clock Input.
10	SPDIF	Input	S/PDIF (Sony/Philips Digital Interface) Audio Input.
11	MCLK	Input	Audio Reference Clock Input.
12 to 15	I2S[3:0]	Input	I^2S Audio Data Inputs. These represent the eight channels of audio (two per input) available through I^2S.
16	SCLK	Input	I^2S Audio Clock Input.
17	LRCLK	Input	Left/Right Channel Signal Input.
18, 20, 22, 23, 27, 31, 37, 44, 46, 51, 75, 99, 100	GND	Power	Ground.
21, 24, 25	PV_{DD}	Power	1.8 V PLL Power Supply.
26	BGV_{DD}	Power	Band Gap Power Supply.
28	R_EXT	Input	This pin sets the internal reference currents.
29, 34, 41	AV_{DD}	Power	1.8 V Power Supply for TMDS Outputs.
30	HPD	Input	Hot Plug Detect Signal Input.
32, 33	TXC–, TXC+	Differential output	Differential TMDS Clock Output.
35, 36	TX0–, TX0+	Differential output	Differential TMDS Output Channel 0.
38	PD	Input	Power-Down Control and I^2C® Address Selection.

Pin No.	Mnemonic	Type	Description
39, 40	TX1−, TX1+	Differential output	Differential TMDS Output Channel 1.
42, 43	TX2−, TX2+	Differential output	Differential TMDS Output Channel 2.
45	INT	Output	Interrupt Signal Output.
47	DV_{DD}_3V	Power	3.3 V Power Supply.
48	CEC_IN	Input/output	CEC Data Signal.
50	CEC_CLK	Input	The CEC clock is a crystal from 1 MHz to 100 MHz.
52	NC	No connect	No Connect.
53	DDCSCL	Control	Serial Port Data Clock to Sink.
54	DDCSDA	Control	Serial Port Data I/O to Sink.
55	SCL	Control	Serial Port Data Clock Input.
56	SDA	Control	Serial Port Data I/O.
57 to 74, 78, 80 to 96	D[35:0]	Input	Video Data Input.
97	DE	Input	Data Enable Signal Input for Digital Video.
98	HSYNC	Input	Horizontal Sync Input.

APPLICATIONS INFORMATION

DESIGN RESOURCES

Analog Devices, Inc., evaluation kits, reference design schematics, hardware and software guides, and other support documentation is available under NDA from ATV_VideoTX_apps@analog.com.

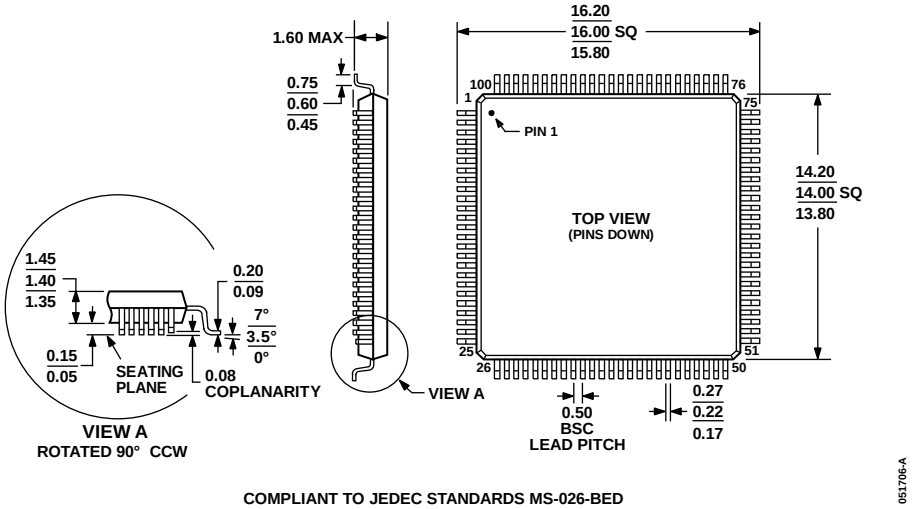
Other references include the following:

EIA/CEA-861-D, a technical specifications document, describes audio and video InfoFrames, as well as the E-EDID structure for HDMI. It is available from Consumer Electronics Association (CEA).

High-Definition Multimedia Interface Specification Version 1.3, a defining document for HDMI v.1.3, and the *High-Definition Multimedia Interface Compliance Test Specification Version 1.3a* are available from HDMI Licensing, LLC.

High-Bandwidth Digital Content Protection System Revision 1.3, the defining technical specifications document for the HDCP v.1.3, is available from Digital Content Protection, LLC.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BED

Figure 3. 100-Lead Low Profile Quad Flat Package [LQFP]
(ST-100)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADV7510BSTZ-225[1]	−25°C to +85°C	100-Lead Low Profile Quad Flat Package (LQFP)	ST-100
ADV7510/PCBZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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