ANALOG DEVICES

ADV7180
Schematic Check List

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Rev. A

Rev.A

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Rev.A – Initial Revision 10/2013

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1. Introduction

This document is intended as design check list to assist with the design of ADV7180 systems. This document should to be used with the ADV7180 datasheets and reference schematics. Please refer to the datasheet for details on all blocks.

2. Note on Pin Numbers

Note that the ADV7180 is available in a number of different models. In this document these models are organized into four groups: 32 lead models, 40 lead models, 48 lead models and 64 lead models. Each group contains ADV7180 models that have the same pinout. See the ordering guide of the ADV7180 datasheet for more information.

The tables below state which ADV7180 models are in which group.

Group	Model
32 Lead Models	ADV7180BCP32Z ADV7180BCP32Z-RL ADV7180KCP32Z ADV7180KCP32Z-RL ADV7180WBCP32Z ADV7180WBCP32Z-RL
40 Lead Models	ADV7180BCPZ ADV7180BCPZ-REEL ADV7180WBCPZ ADV7180WBCPZ-REEL
48 Lead Models	ADV7180BST48Z ADV7180BST48Z-RL ADV7180KST48Z ADV7180KST48Z-RL ADV7180WBST48Z ADV7180WBST48Z-RL
64 Lead Models	ADV7180BSTZ ADV7180BSTZ-REEL ADV7180WBSTZ ADV7180WBSTZ-REEL

3. Check List

3.1 Control and Misc. pins

* Note these pins can operate at the logic level of the DVDDIO voltage supply. Therefore these pins can operate at a 3.3 Volt or 1.8 Volt logic level. Note that if the 1.8V logic level is used then the drive strength for all digital outputs need to be set to maximum. See Global Pin Control section of the ADV7180 datasheet.

Name	Pin number				Logic Level	I/O Mode	To Check	✓
	32 lead models	40lead models	48 lead models	64 lead models				
SDATA	27	33	39	53	DVDDIO*	Digital Bi-directional	I^2C Data - Connect to CPU/System I2C bus. External pull-up required to DVDDIO for normal I2C operation (Typ: 4.7k ohm)	
SCL	28	34	40	54		Digital Input	I^2C Clock - Connect to CPU/System I2C bus. External pull-up required to DVDDIO for normal I^2C operation (Typ: 4.7k ohm)	
$\overline{\text{RESET}}$	25	31	37	51		Digital Input	Reset (Active Low) – Drive high (to DVDDIO) to take the device out of reset	
$\overline{\text{PWRDWN}}$	n/a	18	21	29		Digital Input	Powerdown (Active Low) – Drive high (to DVDDIO) to take the device out of powerdown mode.	
ALSB	26	32	38	52		Digital Input	Sets I^2C base address of the ADV7180 - Pull to DVDDIO or ground through a ≥4.7k ohm resistor. Low = Base address 0x40 High = Base address 0x42	
$\overline{\text{INTRQ}}$	32	38	46	1		Digital Output	Interrupt output – connect to downstream CPU/FPGA. Pull up to DVDDIO through a ≥4.7k ohm resistor. If not used this pin can be left unconnected.	

3.2 Analog Video Inputs

Name	Pin Number				Logic Level	Description	To Check	✓
	32 lead models	40lead models	48 lead models	64 lead models				
$A_{IN}1$	19	23	26	35	n/a	ANALOG Video INPUT	Analog Video Input- A 36Ω/39Ω resistor divider network and a 100 nF AC coupling capacitor are required. If not used this pin can be left floating or connected directly to ground.	
$A_{IN}2$	23	29	27	36			Analog Video Input- A 36Ω/39Ω resistor divider network and a 100 nF AC coupling capacitor are required. If not used this pin can be left floating or connected directly to ground.	
$A_{IN}3$	24	30	33	46			Analog Video Input- A 36Ω/39Ω resistor divider network and a 100 nF AC coupling capacitor are required. If not used this pin can be left floating or connected directly to ground.	
$A_{IN}4$	n/a	n/a	34	47			Analog Video Input- A 36Ω/39Ω resistor divider network and a 100 nF AC coupling capacitor are required. If not used this pin can be left floating or connected directly to ground.	
Ain 5	n/a	n/a	35	48			Analog Video Input- A 36Ω/39Ω resistor divider network and a 100 nF AC coupling capacitor are required. If not used this pin can be left floating or connected directly to ground.	
Ain 6	n/a	n/a	36	49			Analog Video Input- A 36Ω/39Ω resistor divider network and a 100 nF AC coupling capacitor are required. If not used this pin can be left floating or connected directly to ground.	

3.3 Digital Video Outputs

* Note these pins can operate at the logic level of the DVDDIO voltage supply. Therefore these pins can operate at a 3.3 Volt or 1.8 Volt logic level. Note that if the 1.8V logic level is used then the drive strength for digital outputs and I^2C input/ouptuts need to be set to maximum. See Global Pin Control section of the ADV7180 datasheet.

Name	Pin Number				Logic Level	I/O Mode	To Check	✓
	32 lead models	40lead models	48 lead models	64 lead models				
P0	16	17	22	26	DVDDIO *	Digital Video Outputs	Digital video outputs – connect to downstream device. A 33Ω series resistor should be inserted close to the ADV7180.	
P1	15	16	20	25				
P2	10	10	12	19				
P3	9	9	11	18				
P4	8	8	10	17				
P5	7	7	9	16				
P6	6	6	8	15				
P7	5	5	7	14				
P8	n/a	n/a	n/a	8				
P9	n/a	n/a	n/a	7				
P10	n/a	n/a	n/a	6				
P11	n/a	n/a	n/a	5				
P12	n/a	n/a	n/a	62				
P13	n/a	n/a	n/a	61				
P14	n/a	n/a	n/a	60				
P15	n/a	n/a	n/a	59				
LLC	11	11	14	20	DVDDIO*	Digital Output	27 MHz line locked clock – connect to downstream device. A 33Ω series resistor should be inserted close to the ADV7180.	

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Name	Pin Number				Logic Level	I/O Mode	To Check	✓
	32 lead models	40lead models	48 lead models	64 lead models				
HS	1	39	47	2	DVDDIO*	Digital Output	Horizontal synchronization signal. A 33Ω series resistor should be inserted close to the ADV7180. This output can be connected to the downstream devices, however this output is optional. If not used this pin can be left floating.	
VS/FIELD	31	37	45	n/a	DVDDIO*	Digital Output	Vertical synchronization/ Field synchronization signal. A 33Ω series resistor should be inserted close to the ADV7180. This output can be connected to the downstream devices, however this output is optional. If not used this pin can be left floating.	
VS	n/a	n/a	n/a	64	DVDDIO*	Digital Output	Vertical synchronization signal. A 33Ω series resistor should be inserted close to the ADV7180. This output can be connected to the downstream devices, however this output is optional. If not used this pin can be left floating.	
FIELD	n/a	n/a	n/a	63	DVDDIO*	Digital Output	Field synchronization signal. A 33Ω series resistor should be inserted close to the ADV7180. This output can be connected to the downstream devices, however this output is optional. If not used this pin can be left floating.	
SFL	4	2	3	9	DVDDIO*	Digital Output	Color subcarrier frequency lock synchronization signal. A 33Ω series resistor should be inserted close to the ADV7180. This output can be connected to the downstream devices, such as analog devices' video encoders. However this output is optional and if not used this pin can be left floating.	

3.4 Voltage Reference Pins

Name	Pin Number				Logic Level	I/O Mode	To Check	✓
	32 lead models	40lead models	48 lead models	64 lead models				
VREFP	20	25	29	38	1.8V	Output	Voltage Reference Outputs. A single 100 nF capacitor should be placed between the VREFP and VREFN pins. The 100 nF capacitor should be placed close to the ADV7180 and on the same side of the PCB as the ADV7180.	
VREFN	21	26	30	39	1.8V	Output		

3.5 External Loop Filter

Name	Pin Number				Logic Level	I/O Mode	To Check	✓
	32 lead models	40lead models	48 lead models	64 lead models				
ELFP	17	19	24	30	PVDD	Input	An external loop filter circuit needs to be connected to the ELFP pin. See Figure 1 below and 'Typical Circuit Connection' section of the ADV7180 datasheet. The external loop filter should be placed close to the ADV7180 and on the same side of the PCB as the ADV7180.	

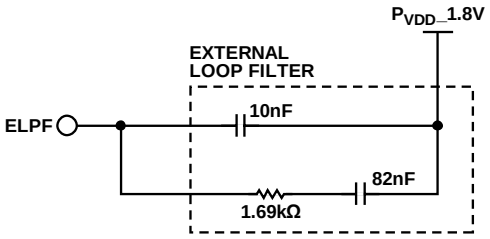

Figure 1. External Loop Filter Required on the ELFP Pin

3.6 Clock Pins

Name	Pin Number				Logic Level	Description	To Check	✓
	32 lead models	40lead models	48 lead models	64 lead models				
XTAL1	12	12	16	21	1.8V	Outputs 1.8V to external crystal.	<u>For Crystal Sources</u>: • This pin should be connected to the 1.8V 28.63636 MHz (+/- 50ppm) fundamental crystal. • A 1 MΩ resistor should be placed between the XTAL1 and XTAL pins. • See datasheet of the crystal for a description of the additional resistor / capacitor setup needed. <u>For Oscillator Sources</u>: This pin should be left not connected. <u>Note</u>: The crystal/ oscillator and associated circuitry should be located close to, and on the same side of the PCB, as the ADV7180.	
XTAL	13	13	17	22	1.8V	Input for crystal or clock oscillator	<u>For Crystal Sources</u>: • This pin should be connected to the 1.8V 28.63636 MHz (+/- 50ppm) fundamental crystal. • A 1 MΩ resistor should be placed between the XTAL1 and XTAL pins. • See datasheet of the crystal for a description of the additional resistor / capacitor setup needed. <u>For Oscillator Sources</u>: • The output from the 1.8V 28.63636 MHz clock oscillator should be fed into this pin. <u>Note1</u>: The crystal/ oscillator and associated circuitry should be located close to, and on the same side of the PCB, as the ADV7182 or ADV7280. <u>Note2</u>: An additional I^2C write is needed in order for the ADV7182 / ADV7280 to operate with a clock oscillator source instead of a crystal source. Write 0x04 to register 0x13 in the User Main Map.	

3.7 Power and Ground

Name	Pin Numbers				Logic Level	Description	To Check	✓
	32 lead models	40lead models	48 lead models	64 lead models				
AVDD	22	27	31	40	1.8V	Power	A 1.8V supply should be connected to the AVDD pin through a filter circuit and a decoupling circuit. Filter Circuit: The filter circuit should be placed close to the supply. The recommended filter circuit consists of these element in this order. • A parallel 220uF capacitor between the supply and ground, • A series ferrite bead, • And another parallel 33uF parallel capacitor to ground. Decoupling Circuit: The decoupling circuit should be placed close to the AVDD pin of the ADV7180. The recommended decoupling circuit consists of these elements in this order. • A parallel 100nF parallel capacitor between the supply and ground. • And another 10nF parallel capacitor between the supply and ground	
PVDD	18	20	25	31	1.8V	Power	A 1.8V supply should be connected to the PVDD pin through a filter circuit and a decoupling circuit. Filter Circuit: The filter circuit should be placed close to the supply. The recommended filter circuit consists of these element in this order. • A parallel 220uF capacitor between the supply and ground, • A series ferrite bead, • And another parallel 33uF parallel capacitor to ground. Decoupling Circuit: The decoupling circuit should be placed close to the PVDD pin of the ADV7180. The recommended decoupling circuit consists of these elements in this order. • A parallel 100nF parallel capacitor between the supply and ground. • And another 10nF parallel capacitor between the supply and ground.	

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Name	Pin Numbers							
	32 lead models	40lead models	48 lead models	64 lead models	Logic Level	Description	To Check	✓
DVDD	14,30	14,36	18, 44	23, 58	1.8V	Power	A 1.8V supply should be connected to the DVDD pins through a filter circuit and a decoupling circuit. Filter Circuit: The filter circuit should be placed close to the supply. The recommended filter circuit consists of these element in this order. • A parallel 220uF capacitor between the supply and ground, • A series ferrite bead, • And another parallel 33uF parallel capacitor to ground. Decoupling Circuit: Two decoupling circuits are required. One decoupling circuit should be placed close to each DVDD pin of the ADV7180. It is recommended that each decoupling circuit consists of these elements in this order. • A parallel 100nF parallel capacitor between the supply and ground. • And another 10nF parallel capacitor between the supply and ground	
DVDDIO	3	1, 4	2, 4	4, 11	1.8V or 3.3V	Power	The DVDDIO can be set to 1.8V or 3.3V. The 3.3V or 1.8V supply should be connected to the DVDDIO pin after a filter circuit and a decoupling circuit. Filter Circuit: The filter circuit should be placed close to the supply. The recommended filter circuit consists of these element in this order. • A parallel 220uF capacitor between the supply and ground, • A series ferrite bead, • And another parallel 33uF parallel capacitor to ground. Decoupling Circuit: The decoupling circuit should be placed close to the DVDDIO pin of the ADV7180. The recommended decoupling circuit consists of these elements in this order. • A parallel 100nF parallel capacitor between the supply and ground. • And another 10nF parallel capacitor between the supply and ground	

Name	Pin Numbers				Logic Level	Description	To Check	✓
	32 lead models	40lead models	48 lead models	64 lead models				
DGND	2, 29	3, 15, 35, 40	1, 13, 19, 43	3, 10, 24, 57		Ground	All DGND pins, AGND pins and the exposed back paddle should be connected together to a common ground plane.	
AGND	n/a	21, 24, 28	23, 28, 32	32, 37, 43		Ground		
EPAD	Exposed Back Paddle	Exposed Back Paddle	n/a	n/a		Ground		

3.8 Miscellaneous

Name	Pin Numbers				Logic Level	Description	To Check	✓
	32 lead models	40lead models	48 lead models	64 lead models				
TEST_0	n/a	22	n/a	34		Used for internal testing	Connect to the common ground plane	
NC	n/a	n/a	15, 48	27, 28, 33, 41, 42, 44, 45, 50		Not connected	These pins are not connected internally. These pins can be left floating.	
GPO0	n/a	n/a	5	12		General purpose output	These pins can be configured to drive high and so control downstream devices. The use of these pins is optional. If not used then these pins can be left floating.	
GPO1	n/a	n/a	6	13		General purpose output		
GPO2	n/a	n/a	41	55		General purpose output		
GPO3	n/a	n/a	42	56		General purpose output		