ADV7802 External Memory Test

The ADV7802 contains a BIST (Built in Self-Test) for the external memory. This test can be used to test the operation of the external memory interface. It checks the connections between the ADV7802 and external memory. The test is controlled through I2C and the test result can be read back through registers within the ADV7802.

Test Operation
The memory BIST test generates an LFSR sequence of numbers which is output to the external memory. This sequence is read back for the external memory to check for errors. This test is internally generated and does not need any external inputs applied. It can also be carried out in circuit. It is recommended that a hardware reset is carried out before the memory BIST test is executed.

Test Setup

The following writes should be carried out in this order:

```
82 12 00   ;     Disable TBC, DNR, 3DYC (for now)
42 2B 8D ;     DLL Phase Adjust
42 19 1C  ;     DLL Phase Adjust
42 2B 00  ;     DLL Phase Adjust
42 60 40   ;     Memory Reset
42 2A 10  ;     Memory Test Initialisation Write
42 7C 1D ;     Memory Test Initialisation Write
42 7D 00  ;     Memory Test Initialisation Write
42 7E 1A ;     Memory Test Initialisation Write
```

Wait 10ms

```
42 D9 D5 ;     Enable Memory BIST Test
82 12 05   ;     Enable 3D Comb and Frame TBC
```

Test Results
IO Map Register 0xDB [4] – Test has completed.
IO Map Register 0xDB [5] – Failed if this bit is 1

Once the memory test is initialised, the test will run continuously until the ADV7802 receives a hardware reset. The completed bit will be set once a single memory transaction has been completed, but the test will run continuously. Once the test reports a failure, the pass/fail bit is latched high will not be reset until the ADV7802 is reset or the complete test is run again. It is recommended that a hardware reset is carried out after the memory BIST test is executed before the ADV7802 is configured in a standard mode