AD9984 Clamping and Auto-Offset Settings for 480i

When operating in 480i (or 576i) mode with macrovision, "extra" data is transmitted on the horizontal back porch during both the front and back vertical "porch". This is illustrated in figure 1. The placement of these data pulses relative to the Hsync pulse is in the clamping region. This is illustrated in figure 2.

What this means is that Coast needs to be extended further in both directions so that the Clamp Placement and Duration can be set to "normal" settings. On the evaluation bard this amounted to settings of 7 and 15, respectively for the pre and post coast registers. This allows the user to set the clamp placement and duration registers back to "standard" settings that can be used in most other video modes. If the user is using an external clamp signal, they should ensure that it is not applied during these times (during the last 6 Hsyncs before Vsync or during the first 14 Hsyncs after Vsync).

Figure 3 shows the proper clamping times for this mode.

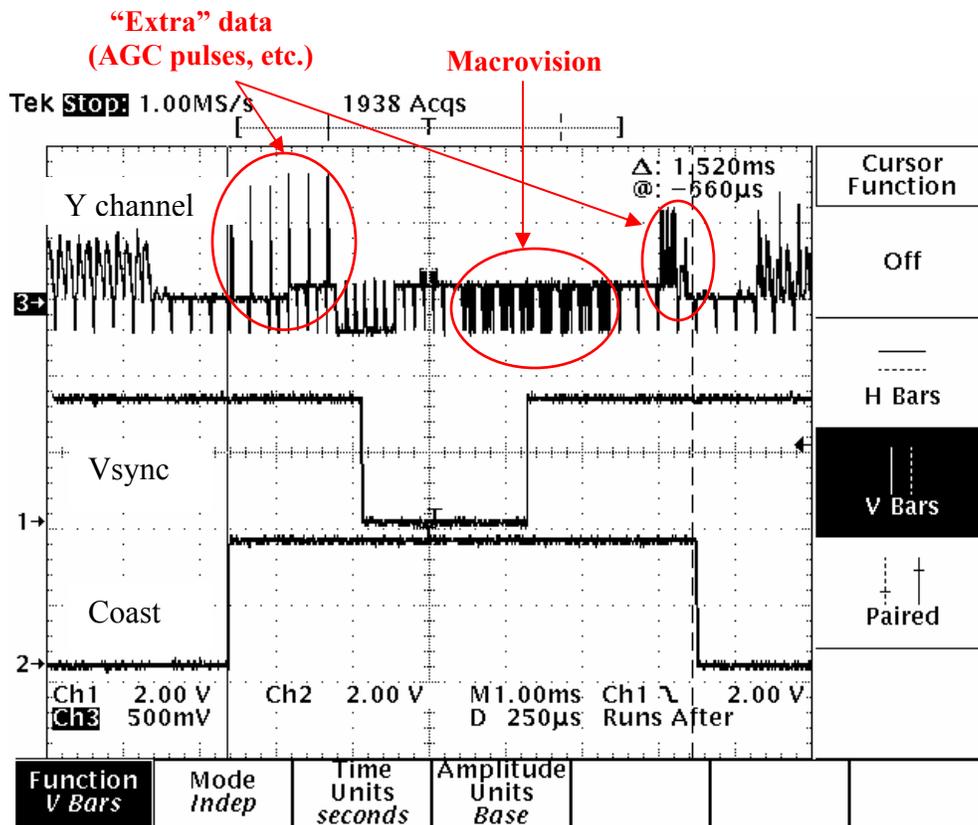## Figure 1: 480i video signal (Y) with macrovision
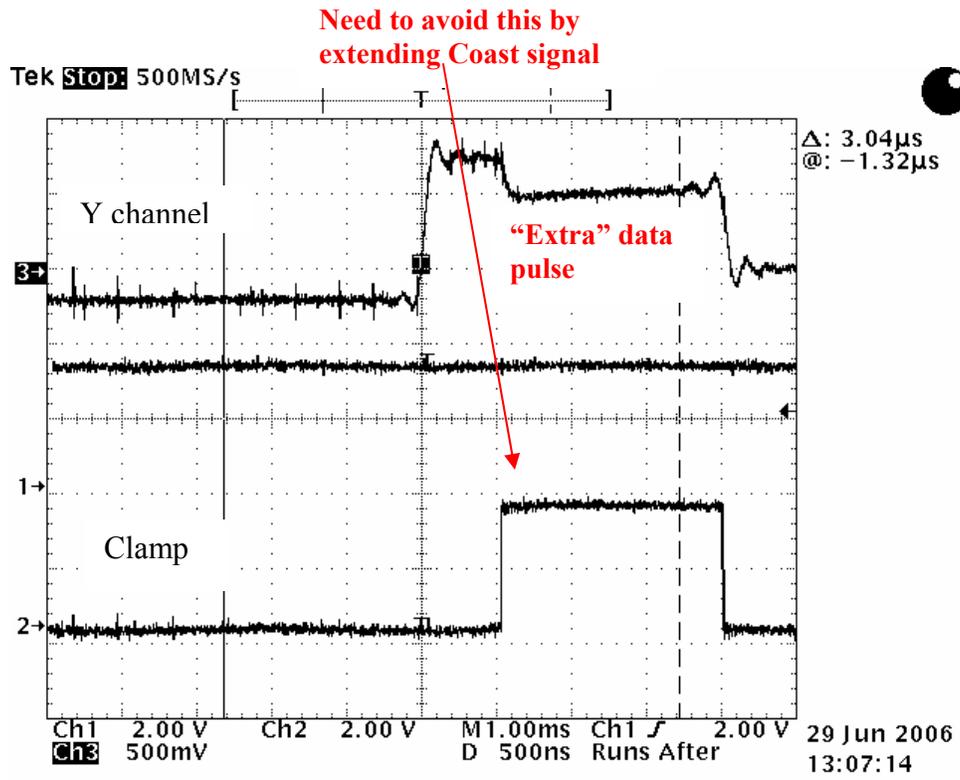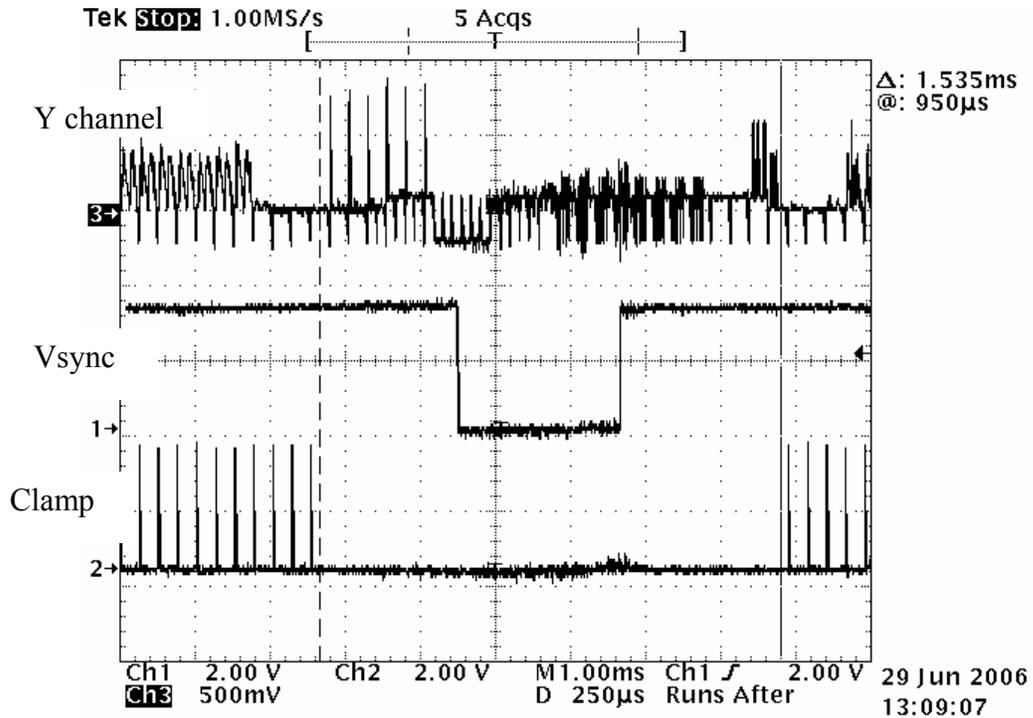
Figure 2: Clamping region relative to "extra" pulses

Need to avoid this by
extending Coast signal

Tek **Stop** 500MS/s

Y channel

3→

"Extra" data
pulse

Δ: 3.04μs
@: −1.32μs

1→

Clamp

2→

| Ch1 | 2.00 V | Ch2 | 2.00 V | M1.00ms | Ch1 ƒ | 2.00 V | 29 Jun 2006 |
| Ch3 | 500mV | | | D 500ns | Runs After | | 13:07:14 |

Figure 3: Clamp signal applied properly for 480i

Tek **Stop** 1.00MS/s   5 Acqs

Y channel

3→

Δ: 1.535ms
@: 950μs

Vsync

1→

Clamp

2→

| Ch1 | 2.00 V | Ch2 | 2.00 V | M1.00ms | Ch1 ƒ | 2.00 V | 29 Jun 2006 |
| Ch3 | 500mV | | | D 250μs | Runs After | | 13:09:07 |

Recommended Settings:

Register	Bits	Recommended Setting	Function	Comments
0x16	7:0	0x08	Pre-Coast	These settings assume the use of internal coast function
0x17	7:0	**0x0C**	Post-Coast	
0x19	7:0	0x08	Clamp Placement	Longer clamp duration improves the clamp accuracy
0x1A	7:0	**0x14**	Clamp Duration	
0x1B	5	1	Auto-Offset Enable	'1' turns on auto-offset
	4:3	10	Auto-Offset Update Mode	'10' allows update every 64 clamp cycles
0x20	2	1	PLL Sync Filter Enable	Set the PLL to use filtered Hsync
	1	1	SP Sync Filter Enable	Set the Sync Processor to use filtered Hsync
	0	1	Post Filter Enable	Enables filtering for auto-offset algorithm

It is further recommended that the AO circuit be put into "hold" (0x2C[4] = 1) mode after approximately 0.5 seconds in order to eliminate any small amount of "flashing" that can be caused by noise on the analog input.