Advantiv™
Analog Devices

ADV7441A/AD9388A

Register Settings

Recommendations

Rev. P

May 2012

About This Document

This document describes the ADI register setting recommendations and adjustments for the ADV7441A and the AD9388A . This document must be used in conjunction with the devices' corresponding Hardware Manual and Software Manual.

Revision History

Revision	Date	Changes
Rev. 0	10/06/2007	Initial
Rev. A	28/01/2008	Added Sections 1.3.12 and 1.3.13
Rev. B	06/02/2008	Added Section 2.3.4
Rev. C	08/02/2008	Added Sections 1.3.14 and 1.3.15 Removed initialisation settings in Section 1.1 for the KSV registers in the Repeater Map – Section 1.3.15 now describes this recommendation in more details. Updated Table 8 in Section 1.3.5.3
Rev. D	12/02/2008	Title and content of Section 1.3.3 changed (recommendation of an audio PLL reset on a change of TMDS clock changed to recommendation of an audio PLL reset upon reception of an ACR packet). Corrected the bit position of the deglitch filter in Section 2.3.4. Added list of figures. Added list of tables.
Rev. E	28/02/2008	Updated Section 1.3.12. An audio synthesiser reset is recommended after the optimization setting of the audio synthesiser.
Rev. F	14/03/2008	Added Section 3.1
		Updated Figure 1
Rev. G	29/05/2008	Added Section 2.3.5
Rev. H	10/06/2008	Updated Section 2.3.5
Rev. I	25/11/2008	Added Section 2.3.2 and 2.3.3
Rev. J	12/06/2009	Added CP Color Control adjustments section
Rev. K	21/09/2009	Added AGC and Embedded Sync section
Rev. L	07/05/2010	Removed disclaimer
Rev. M	24/06/2010	Added copyright
Rev. N	03/02/2012	Updated Section 1.3.12
Rev. P	14/05/2012	Updated Section 1.3.12

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1. HDMI Receiver Register Settings

1.1. Initialization Settings for HDMI Mode

ADI recommends that these register setting are programmed to set the part correctly in HDMI mode.

User Map

42 05 06	Set Prim Mode to HDMI – for automatic mode
42 C8 08	Set digital fine clamp setting for HDMI Mode

HDMI Map

6A 10 1F	ADI Recommendation for CTS Change Threshold

1.2. Standard Dynamic Settings for HDMI Mode

The following standard register setting adjustments are required for the best performance in HDMI mode.

1.2.1. Primary Mode and Video Standard Settings

The Primary Mode register (User Map, Reg 0x05 bit [3:0]) has three HDMI modes:

- SD HDMI mode (0x04)
- ED/HD HDMI mode (0x05)
- Automatic/graphics HDMI mode (0x06)

The Primary Mode (User Map, Reg 0x05 bit [3:0]), Video Standard (User Map, Reg 0x06 bit [3:0]), and Vertical Frequency (User Map, Reg 0x06 bit [7:5]) registers must be set as follows:

- If free run is not enabled, the Primary Mode setting must be set to Automatic Mode 0x06, the Video Standard setting must be set to default 0x02, and the Vertical Frequency setting must be set to default 0x00.
- If free run is enabled, the Primary Mode setting, the Video Standard and Vertical Frequency registers must be set according to the required resolution for free run.

1.2.2. Bcaps Setting

1.2.2.1. Bcaps Register Bit 1

The ADV7441A/AD9338A does not support the Enhanced Link Verification feature defined in the HDCP specifications. This feature must be disabled by setting bit 1 of the Bcaps register to 0.

Table 1. Recommended Setting for Bcaps Register Bit 1

Bcaps Register Location	Bit Position	Setting Recommendation
KSV/Repeater Map, Reg 0x40	1	0

1.2.2.2. Bcaps Register Bit 7

The MSB of the Bcaps register must be set according to Table 2 to ensure optimum interconnectivity between the ADV7441A/AD9338A and HDMI transmitters.

Table 2. Recommended Setting for Bcaps Register Bit 7

Bcaps Register Location	Bit Position	Setting Condition	Setting Recommendation
KSV/Repeater Map, Reg 0x40	7	ADV7441A/AD9338A has been implemented in a DVI receiver mode	0
KSV/Repeater Map, Reg 0x40	7	ADV7441A/AD9338A has been implemented in a HDMI receiver mode	1

1.2.3. Audio Mute Mask Settings

The audio mute masks are used to configure the audio mute feature of the ADV7441A/AD9338A. The optimum mute mask setting resulting from the evaluation of the ADV7441A/AD9338A is shown in Table 3. Refer to the Datasheet Manual for additional detail on the audio mute feature.

Table 3. Settings Recommendation for Audio Mute Masks

Item	Mute Mask	Register Location	Setting Recommendation
1	MT_MSK_COMPRS_AUD	0x14 [5]	Setting for mute mask is function of design application
2	MT_MSK_CHNG_DSD_PCM	0x14 [4]	Setting for mute mask is function of design application
3	MT_MSK_PARITY_ERR	0x14 [1]	This mute mask should always be set to 1

Item	Mute Mask	Register Location	Setting Recommendation
4	MT_MSK_VCLK_CHNG	0x14 [0]	This mute mask should always be set to 1
5	MT_MSK_APLL_UNLOCK	0x15 [7]	This mute mask should always be set to 1
6	MT_MSK_VPLL_UNLOCK	0x15 [6]	This mute mask should always be set to 1
7	MT_MSK_ACR_NOT_DET	0x15 [5]	This mute mask should always be set to 1
8	MT_MSK_SAMP_RT_CHNG	0x15 [4]	This mute mask should be set to 0
9	MT_MSK_FLATLINE_DET	0x15 [3]	Setting for mute mask is function of design application
10	MT_MSK_VFREQ_CHNG	0x15 [2]	This mute mask should be set to 1
13	MT_MSK_AVMUTE	0x16 [7]	Setting for mute mask is function of design application
14	MT_MSK_NOT_HDMIMODE	0x16 [6]	This mute mask should be set to 1
15	MT_MSK_NEW_CTS	0x16 [5]	This mute mask should be set to 1
16	MT_MSK_NEW_N	0x16 [4]	This mute mask should be set to 1
17	MT_MSK_CHMODE_CHNG	0x16 [3]	This mute mask should be set to 1
18	MT_MSK_APCKT_ECC_ERR	0x16 [2]	This mute mask should be set to 1
19	MT_MSK_CHNG_PORT	0x16 [1]	Setting for mute mask is function of design application
20	MT_MSK_VCLK_DET	0x16 [0]	This mute mask should be set to 1

1.2.4. Drive Strength Setting

The drive strength for data, clock, and synchronization signals must be programmed according to the pixel frequency. Refer to Sections 6.3.4, 6.3.5, and 6.3.6 of the Datasheet Manual.

1.3. Dynamic Settings for HDMI Mode

The following sections detail the register setting adjustments recommended for optimal performance.

1.3.1. Forcing HDMI Mode for HDMI Inputs

The register FORCE_HDMI (HDMI Map, Reg 0x45, bit 6) must be set according to the HDMI_Mode register (HDMI Map, Reg 0x05, bit 7):

- If HDMI_Mode = 1, set FORCE_HDMI to 1
- If HDMI_Mode = 0, set FORCE_HDMI to 0

Note that this configuration is needed only to ensure that the ADV7441A/AD9388A mutes properly when a mute condition has occurred.

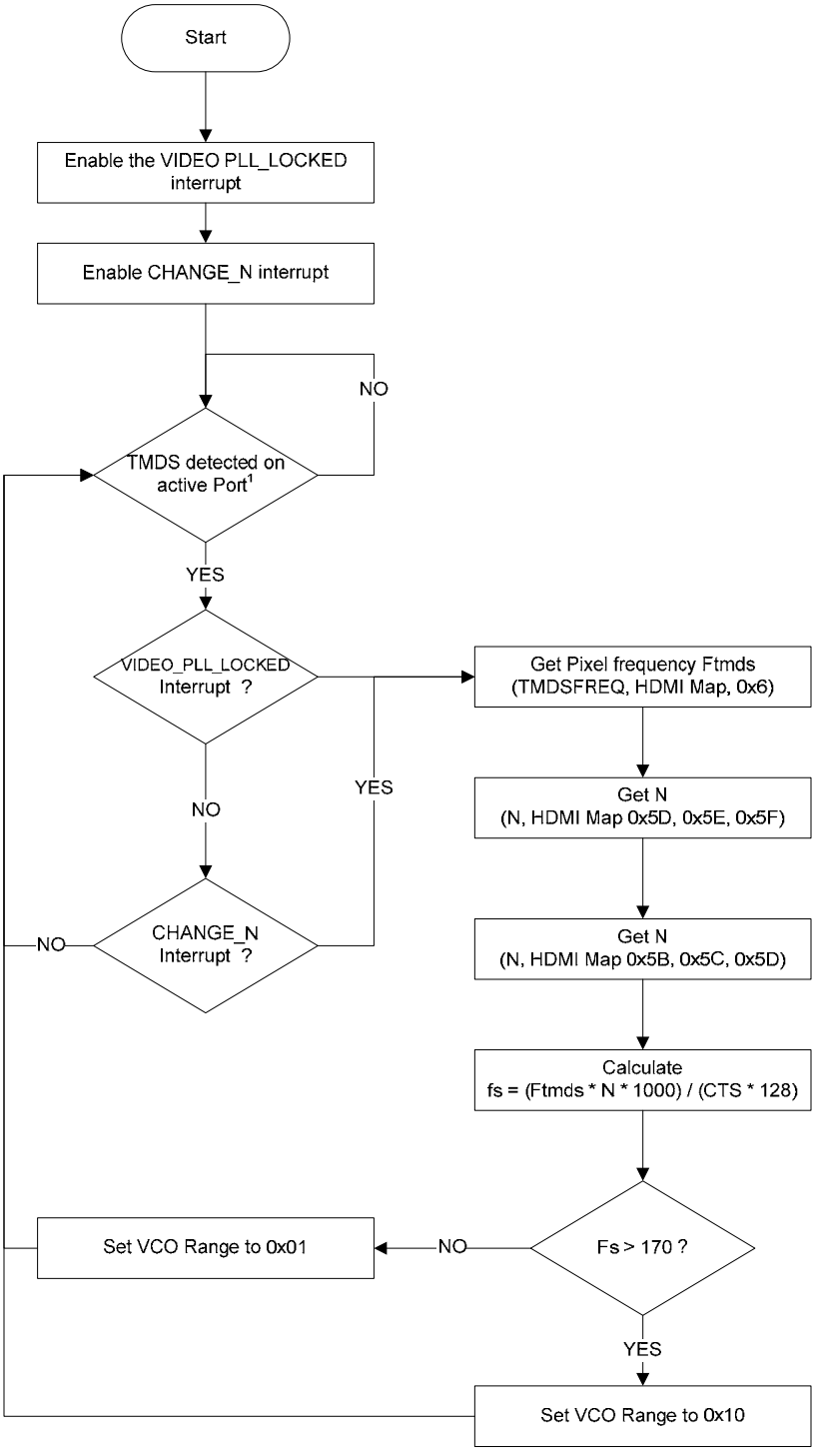
1.3.2. Audio PLL Settings

The VCO range (HDMI Map, Reg 0x3D bit [7:6]) must be manually programmed to 0x10 when the audio sampling frequency (Fs) is 192 KHz and the master clock (MCLK) is programmed for 128fs.The default value of VCO range, 0x01, is suitable for all other cases.

Table 4 details the recommended VCO range setting for the analog audio PLL. Figure 2 shows the firmware function that can be implemented to update the Audio PLL VCO range. Refer to the Datasheet Manual for full programming details of the analog audio PLL.

Table 4. Recommended VCO Range Settings for Analog Audio PLL

	Audio Sampling Frequency						
Multiple of Fs	**32kHz**	**44.1kHz**	**48kHz**	**88.2kHz**	**96kHz**	**176.4kHz**	**192kHz**
128	0x1	0x1	0x1	0x1	0x1	0x2	0x2
256	0x1	0x1	0x1	0x1	0x1	N/A	N/A
384	0x1	0x1	0x1	N/A	N/A	N/A	N/A
512	0x1	0x1	0x1	N/A	N/A	N/A	N/A

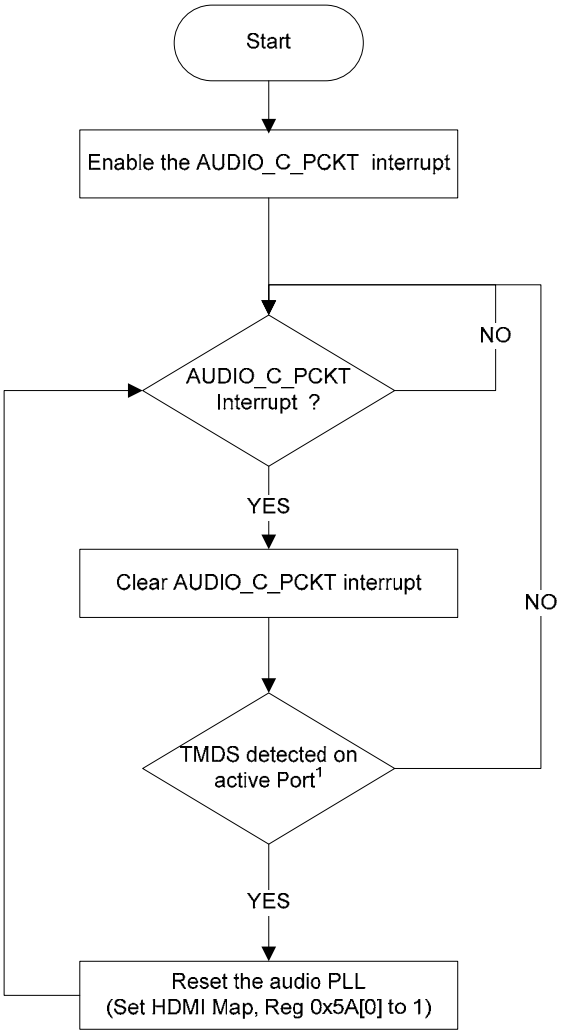


Note: 1. TMDS_CLK_A_RAW (User Map 1 Reg 0x68[4]) or/and TMDS_CLK_B_RAW (User Map 1 Reg 0x68[3]) may be used to verify TMDS activity on the active TMDS Port. The active TMDS port is selected via HDMI_PORT_SELECT (HDMI Map Reg 0x00[0])

Figure 2. Algorithm for Updating VCO Range According to Audio Sampling Frequency

1.3.3. Audio PLL Reset on Reception of ACR Packet

It is recommended to reset the audio PLL upon reception of an Audio Clock Regeneration (ACR) packet. The algorithm shown in Figure 3 can be implemented in the display controller for this purpose.



Note: 1. TMDS_CLK_A_RAW (User Map 1 Reg 0x68[4]) or/and TMDS_CLK_B_RAW (User Map 1 Reg 0x68[3]) may be used to verify TMDS activity on the active TMDS Port. The active TMDS port is selected via HDMI_PORT_SELECT (HDMI Map Reg 0x00[0])

Figure 3. Algorithm for Resetting Audio PLL Upon Reception of ACR packet

1.3.4. Audio PLL Reset on Change of CTS

Some sources update the audio clock regeneration (ACR) packet in a non standard manner on a change of the sample rate. These sources update the ACR packet in two steps:

1. The first ACR packet contains a non standard N and CTS pair.
2. The second ACR packet contains a standard N and CTS pair.

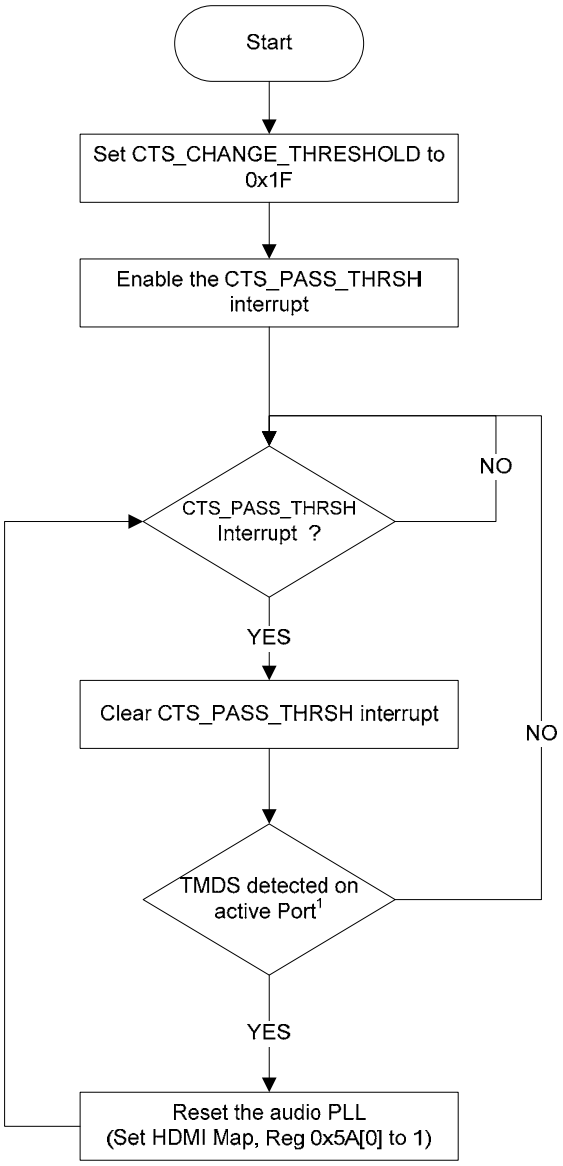
This non standard way of updating the ACR packets upsets the audio processing engine of the ADV7441A/AD9388A and, as a result, the audio synthesizer does not reset correctly.

It is possible to make sure that the audio PLL synthesizer is properly reset by manually resetting the PLL as follows if CTS passes a predefined threshold:

1. Set the desired CTS threshold (HDMI Map, Reg 0x10 bit [5:0]). ADI recommends using a threshold value of 0x1F.
2. Reset the audio PLL synthesizer when CTS passes the CTS threshold.

There are two possible ways for the display controller to know if CTS has passed the threshold:

- The ADV7441A/AD9388A can be configured to generate an interrupt if the CTS passes the threshold by setting CTS_PASS_THRS_M1 (User Map 1, Reg 0x71 bit 4) or CTS_PASS_THRS_M2 (User Map 1, Reg 0x70 bit 4). Refer to the Datasheet Manual for additional details on programming interrupts.
- The display controller can read back the NEW_CTS register status (HDMI Map, Reg 0x1A bit 4) to check if CTS has passed the threshold.



Note: 1. TMDS_CLK_A_RAW (User Map 1 Reg 0x68[4]) or/and TMDS_CLK_B_RAW (User Map 1 Reg 0x68[3]) may be used to verify TMDS activity on the active TMDS Port. The active TMDS port is selected via HDMI_PORT_SELECT (HDMI Map Reg 0x00[0])

Figure 4. Algorithm for Resetting Audio PLL on Change of CTS

1.3.5. HDMI Interrupts Validity Checking Process

Each HDMI interrupts has a set of conditions that must be taken into account for validation in the display firmware. When the ADV7441A/AD9388A interrupts the display controller for an HDMI interrupt, it must check that all validity conditions for that interrupt are met before processing that interrupt.

The HDMI interrupts can be subdivided into three groups according to their corresponding validity conditions. The following sub-sections detail the validity conditions for each of the three groups of HDMI interrupts.

Table 5. HDMI Interrupts in User Map 1 Categorised into Three Groups

Bit Position / Register Address	7	6	5	4	3	2	1	0
0x61	3	3	3	3	3	3	3	3
0x65	2	3	3	3	3	3	3	3
0x69	3	3	2	1	1	3	3	2
0x6C	3	3	3	3	3	3	3	3
0x6F	3	3	3	3	3	3	3	3
0x72	3	3	2	3	3	3	3	3

1.3.5.1. Group 1 HDMI Interrupts

The interrupts listed in Table 6 are valid irrespective of the mode in which the ADV7441A/AD9388A is configured, that is:

- SD-M mode (PRIM_MODE set to 0x0)
- COMP mode (PRIM_MODE set to 0x1)
- GR mode (PRIM_MODE set to 0x10)
- HDMI mode (PRIM_MODE set to values 0x100, 0x101, or 0x110)

Table 6. HDMI Interrupts Group 1

Interrupts	User Map 1 Location
TMDS_CLK_A_ST	Reg 0x69 bit 4
TMDS_CLK_B_ST	Reg 0x69 bit 3

1.3.5.2. Group 2 HDMI Interrupts

The interrupts listed in Table 7 are valid on the condition that the ADV7441A/AD9388A is configured in HMDI mode.

Table 7. HDMI Interrupts Group 2

Interrupts	**User Map 1 Location**
AUDIO_PLL_LCK_ST	Reg 0x65 bit 7
INTERNAL_MUTE_ST	Reg 0x69 bit 5
VIDEO_PLL_LCK_ST	Reg 0x69 bit 0
AKSV_UPDATE_ST	Reg 0x73 bit 5

1.3.5.3. Group 3 HDMI Interrupts

The interrupts listed in Table 8 are valid under the following conditions:

- The ADV7441A/AD9388A is configured in HDMI mode
- TMDS_PORT_A_ACTIVE is set to 1 (HDMI Map, Reg 0x4 bit 2) if Port A is the active HDMI port
- TMDS_PORT_B_ACTIVE is set to 1 (HDMI Map, Reg 0x4 bit 3) if Port B is the active HDMI port
- VIDEO_PLL_LOCKED is set to 1 (HDMI Map, Reg 0x4 bit 1)

Table 8. HDMI Interrupts Group 3

Interrupts	**User Map 1 Location**
DSD_PCKT_ST	Reg 0x61 bit 7
ISRC2_PCKT_ST	Reg 0x61 bit 6
ISRC1_PCKT_ST	Reg 0x61 bit 5
ACP_PCKT_ST	Reg 0x61 bit 4
MS_INFO_ST	Reg 0x61 bit 3
SPD_INFO_ST	Reg 0x61 bit 2
AUDIO_INFO_ST	Reg 0x61 bit 1
AVI_INFO_ST	Reg 0x61 bit 0
HDMI_ENCRPT_ST	Reg 0x65 bit 6
AV_MUTE_ST	Reg 0x65 bit 4

Interrupts	User Map 1 Location
INFO_FR_PCKT_ST	Reg 0x65 bit 3
GEN_CTL_PCKT_ST	Reg 0x65 bit 2
AUDIO_C_PCKT_ST	Reg 0x65 bit 1
AUDIO_S_PCKT_ST	Reg 0x65 bit 0
AUDIO_CH_MD_ST	Reg 0x68 bit 2
HDMI_MODE_ST	Reg 0x68 bit 1
V_LOCKED_ST	Reg 0x69 bit 6
GAMUT_MDATA_ST	Reg 0x69 bit 6
NEW_GAMUT_MDATA_ST	Reg 0x6C bit 7
NEW_ISRC2_PCKT_ST	Reg 0x6C bit 6
NEW_ISRC1_PCKT_ST	Reg 0x6C bit 5
NEW_ACP_PCKT_ST	Reg 0x6C bit 4
NEW_MS_INFO_ST	Reg 0x6C bit 3
NEW_SPD_INFO_ST	Reg 0x6C bit 2
NEW_AUDIO_INFO_ST	Reg 0x6C bit 1
NEW_AVI_INFO_ST	Reg 0x6C bit 0
CTS_PASS_THRSH_ST	Reg 0x6F bit 4
CHANGE_N_ST	Reg 0x6F bit 3
INFOFRAME_ERR_ST	Reg 0x6F bit 2
PACKET_ERROR_ST	Reg 0x6F bit 1
AUDIO_PCKT_ERR_ST	Reg 0x6F bit 0
DEEP_COLOR_CHNG_ST	Reg 0x72 bit 7
VCLK_CHNG_ST	Reg 0x72 bit 6
PARRITY_ERROR_ST	Reg 0x72 bit 4
NEW_SAMP_RT_ST	Reg 0x72 bit 3
AUDIO_FLT_LINE_ST	Reg 0x72 bit 2
NEW_TMDS_FRQ_ST	Reg 0x72 bit 1

1.3.6. Support for DVI Sources Outputting Pixel Repeated Data

Some DVI sources use a pixel repetition scheme in order to transmit video format that have pixel below 25 MHz, for example, 480i or 576i format. As DVI does not support InfoFrames, these non standard sources cannot provide the pixel repetition factor information to the sink.

It is possible to support DVI sources outputting pixel repeated data by manually setting the pixel repetition settings and the decoder will discard the repeated pixels appropriately and provide the required clock**.**

- DEPER_N_OVERRIDE (HDMI Map, Reg 0x41 bit 4) set to 1 enables manual setting of the pixel repetition field
- DEREP_N[3:0] (HDMI Map Reg 0x41 bit[3:0]) sets the pixel repetition value. The value set here is used to derepeat the pixel data and clock when DEPER_N_OVERRIDE is set high.

In HDMI mode, pixel repetition is handled automatically by the receiver based on the supplied InfoFrame. Therefore, in HDMI mode, DEREP_N_OVERRIDE should be set to the default of 0.

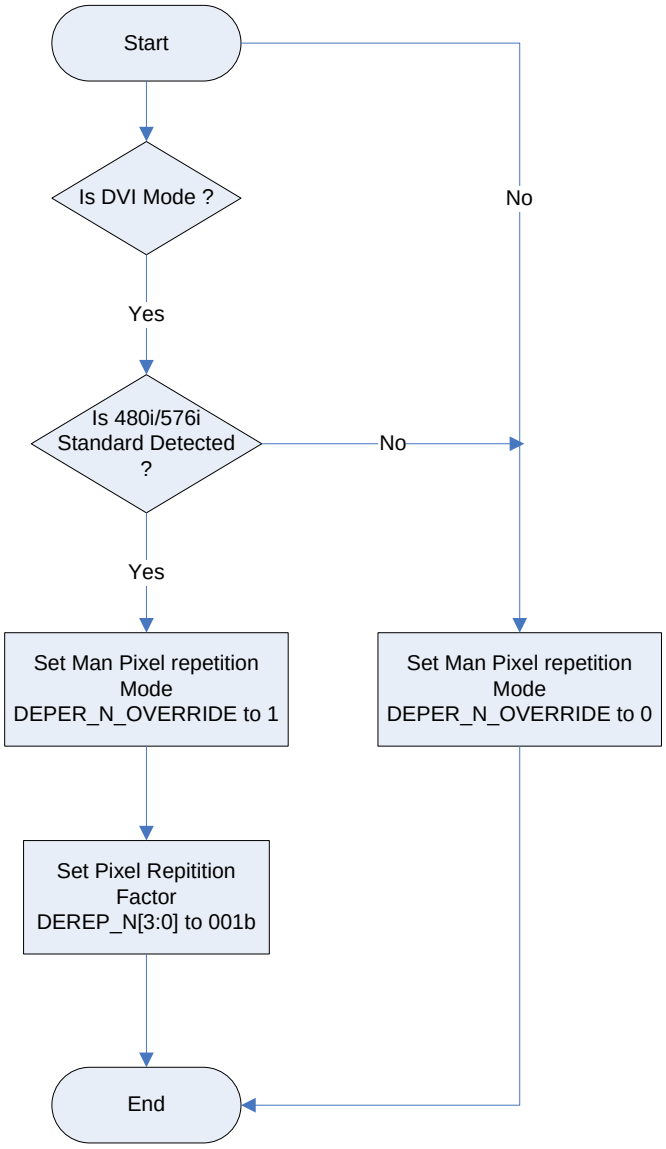


Figure 5. Example Implementation for DVI Pixel Repetition

1.3.7. Recommended Equalizer Settings

For optimal equalizer performance, ADI recommends the following settings for the equalizer based on the TMDS frequency:

- TMDS frequency < 160 MHz

  User Map 2
  62 F0 10 ADI Recommended Write
  62 F1 0F ADI Recommended Write
  62 F4 20 ADI Recommended Write

- TMDS frequency > 160 MHz

User Map 2
62 F0 30 ADI Recommended Write
62 F1 0F ADI Recommended Write
62 F4 A0 ADI Recommended Write

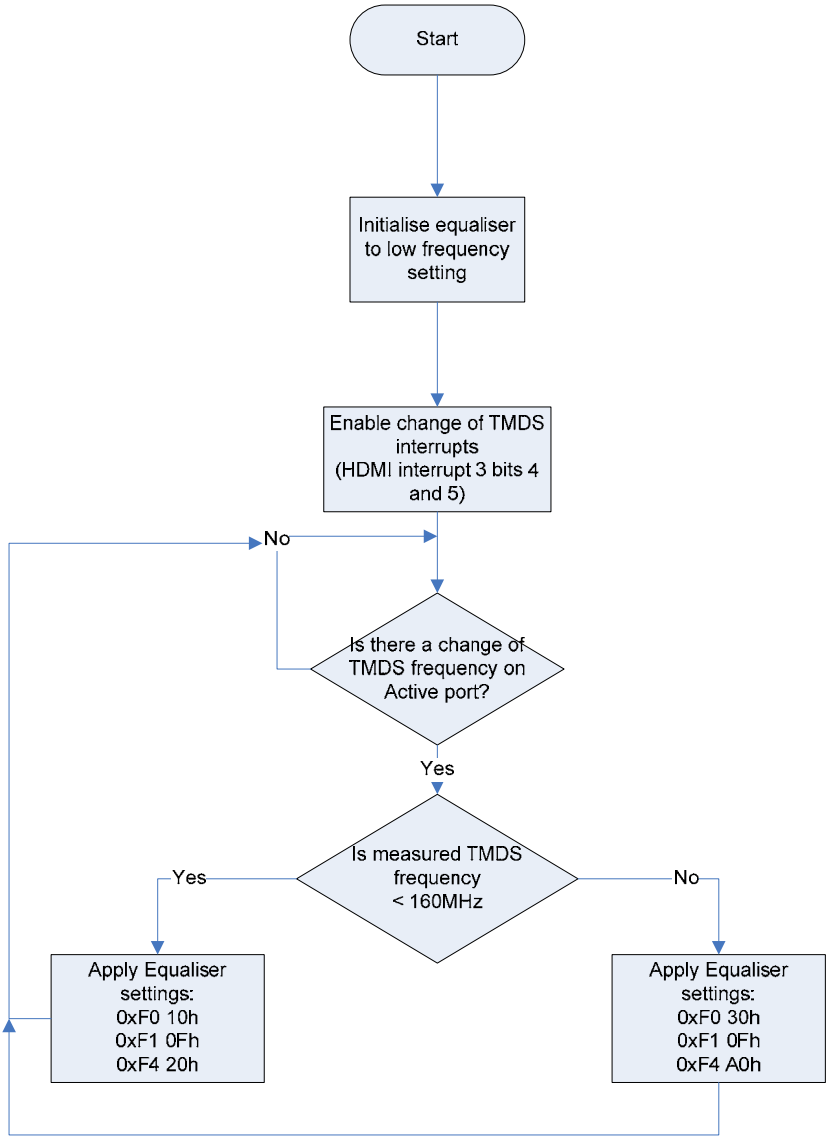


Figure 6. Adjusting Equaliser Settings

1.3.8. Clamp, Gain and Offset Settings

The CP core provides the designer with the gain, clamp and offset controls which can be used to modify digital data output from the HDMI core. Equation 1 outlines the channel input/output relationship in the CP core. For simplicity, the case where Color Space Conversion (CSC) is applied is not considered in Equation 1.

$$Y_{OUT} = [A\_GAIN \cdot (Y_{IN} - A\_CLAMP)] + A\_OFFSET$$
$$U_{OUT} = [B\_GAIN \cdot (U_{IN} - B\_CLAMP)] + B\_OFFSET$$
$$V_{OUT} = [C\_GAIN \cdot (V_{IN} - C\_CLAMP)] + C\_OFFSET$$

Equation 1. CP core channel input/output relationship with no CSC.

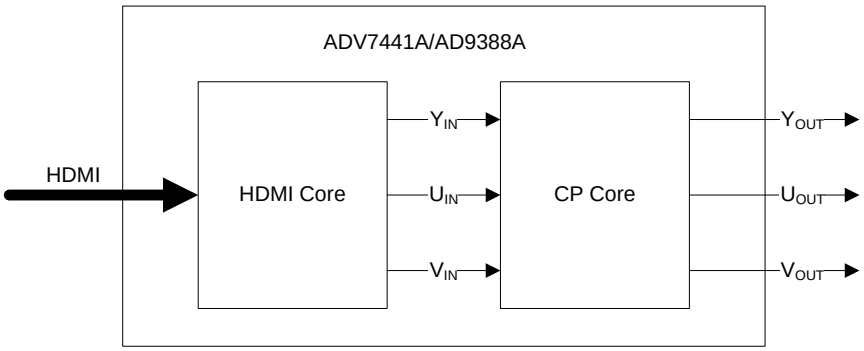


Figure 7. HDMI and CP Cores in ADV7441A/AD9388A

Setting the gain to unity, the clamp and offset to zero allows for transfer of un-gained and un-scaled data from the from the HDMI core, through the CP core, to the output pixel bus. The settings below are recommended for all ranges of the input signal and output signal is one must obey one of the following cases

- Input range is [0…255] and output range is [0…255]
- Input range is [16…235] and output range is [16…235]

- Set CP_OP_656 to ‘0’(User Map, Reg 0x6B bit 4). This disables the saturator block in the CP core and allows for full range [0:255] support.
- Set User Map, Reg 0x6C bit 4 to ‘1’ to enable measurement of clamp values on all channels output from the HDMI section to the CP core.
- Set CLMP_A_MAN should be set as per Table 4 (User Map, Reg 0x6C bit 7).
- Set CLMP_BC_MAN should be set as per Table 4 (User Map, Reg 0x6C bit 6).
- Set GAIN_MAN to ‘1’ (User Map, Reg 0x73, bit 7).
- Set AGC_MODE_MAN to ‘1’ (User Map, Reg 0x73, bit 6).

- Set A_GAIN should be set as per Table 4 (User Map, Reg 0x73, 0x74).
- Set B_GAIN should be set as per Table 4 (User Map, Reg 0x74, 0x75).
- Set C_GAIN should be set as per Table 4 (User Map, Reg 0x75, 0x76).
- Set A_OFFSET should be set as per Table 4 (User Map, Reg 0x77, 0x78).
- Set B_OFFSET should be set as per Table 4 (User Map, Reg 0x78, 0x79).
- Set C_OFFSET should be set as per Table 4 (User Map, Reg 0x79, 0x7A).

Table 9. Gain, Clamp and Offset Register Settings

Register Name	Register Address (in User Map)	RGB in RGB out	YPrPb in RGB out	YPrBb in YPrPb out	RGB in YPrPb out
CLMP_A_MAN	Reg 0x6C bit 7	0	0	0	0
CLMP_BC_MAN	Reg 0x6C bit 6	0	0	0	0
User Map Reg 0x6C bit 4	Reg 0x6C bit 4	1	1	1	1
GAIN_MAN	Reg 0x73 bit 7	1	1	1	1
AGC_MODE_MAN	Reg 0x73 bit 6	1	1	1	1
A_GAIN[9:0]	Reg 0x73, 0x74	0x100	0x100	0x100	0x100
B_GAIN[9:0]	Reg 0x74, 0x75	0x100	0x100	0x100	0x100
C_GAIN[9:0]	Reg 0x75, 0x76	0x100	0x100	0x100	0x100
A_OFFSET[9:0]	Reg 0x77, 0x78	0x0*	0x40	0x40	0x0*
B_OFFSET[9:0]	Reg 0x78, 0x79	0x0*	0x40	0x200*	0x200*
C_OFFSET[9:0]	Reg 0x79, 0x7A	0x0*	0x40	0x200*	0x200*
CSC_COEFF_SEL	Reg 0x68 bit[7:4]	0xF	0xF	0xF	0xF
RGB_OUT	Reg 0x68 bit 1	1	1	0	0
CP_OP_656_SEL	Reg 0x6A bit 4	0	0	0	0

*0x3FF may also be used.

1.3.9. Clamp, Gain and Offset Settings for [16…235] Input, [0…255] Output

Table 10 provides recommended setting for the case where the range of the input signal is [16…235] and the required range of the output signal is [0...255].

Table 10. Settings for [16…235] Input, [0…255] Output

Register Name	Register Address (in User Map)	RGB in RGB out	YPrPb in RGB out	YPrPb in YPrPb out	RGB in YPrPb out
CLMP_A_MAN	Reg 0x6C bit 7	1	0	0	1
CLMP_BC_MAN	Reg 0x6C bit 6	1	0	0	1
CLMP_A	Reg 0x6C[3:0], Reg0x6D	0x100	0x000	0x000	0x100
CLMP_B	Reg 0x6E, Reg 0x6F[7:4]	0x100	0x000	0x000	0x800
CLMP_C	Reg 0x6F[3:0], Reg0x70	0x100	0x000	0x000	0x800
User Map Reg 0x6C bit 4	Reg 0x6C bit 4	1	1	1	1
CSC_COEFF_SEL	Reg 0x68 bit[7:4]	0xF	0xF	0xF	0xF
RGB_OUT	Reg 0x68 bit 1	1	1	0	0
CP_OP_656_SEL	Reg 0x6A bit 4	0	0	0	0

1.3.10. Clamp, Gain and Offset Settings for [0…255] Input, [16…235] Output

Table 11 provides recommended setting for the case where the range of the input signal is [0…255] and the required range of the output signal is [16...235].

Table 11. Settings for [0…255] Input, [16…235] Output

Register Name	Register Address (in User Map)	RGB in RGB out	YPrPb in RGB out	YPrPb in YPrPb out	RGB in YPrPb out
CLMP_A_MAN	Reg 0x6C bit 7	0	1	1	0
CLMP_BC_MAN	Reg 0x6C bit 6	0	1	1	0
CLMP_A	Reg 0x6C[3:0], Reg0x6D	0x000	0x000	0x000	0x000
CLMP_B	Reg 0x6E, Reg 0x6F[7:4]	0x000	0x000	0x800	0x000
CLMP_C	Reg 0x6F[3:0], Reg0x70	0x000	0x000	0x800	0x000
User Map Reg 0x6C bit 4	Reg 0x6C bit 4	1	1	1	1
GAIN_MAN	Reg 0x73 bit 7	1#	1	1	1#
AGC_MODE_MAN	Reg 0x73 bit 6	1#	1	1	1#
A_GAIN[9:0]	Reg 0x73, 0x74	0x0DC	0x0DC	0x0DC	0x0DC
B_GAIN[9:0]	Reg 0x74, 0x75	0x0DC	0x0DC	0x0DC	0x0DC
C_GAIN[9:0]	Reg 0x75, 0x76	0x0DC	0x0DC	0x0DC	0x0DC
A_OFFSET[9:0]	Reg 0x77, 0x78	0x40*	0x40*	0x40*	0x40*
B_OFFSET[9:0]	Reg 0x78, 0x79	0x40*	0x40*	0x200*	0x200*
C_OFFSET[9:0]	Reg 0x79, 0x7A	0x40*	0x40*	0x200*	0x200*
CSC_COEFF_SEL	Reg 0x68 bit[7:4]	0xF	0xF	0xF	0xF
RGB_OUT	Reg 0x68 bit 1	1	1	0	0
CP_OP_656_SEL	Reg 0x6A bit 4	1	1	1	1

*0x3FF may also be used. # Zero may also be used

1.3.11. Data Enable Output for Pixel Repetition

For a HDMI input through the CP core using video format 2880 x 480 interlaced with pixel repetition read back HDMI_PIXEL_REPETITION (HDMI Map Reg 0x5[3:0]) set to a value strictly less than four, the decoder was found to emit no Data Enable Signal (pin 16). This can be rectified by setting User Map, reg 0xB7[6] to 1’b1.

1.3.12. Audio Synthesizer Settings for 1080p59/1080p60 Video Input

When the input TMDS frequency is higher than 147.8MHz (i.e. for video resolutions equal or higher than 1080p59/1080p60), the following register write must be performed

HDMI Map

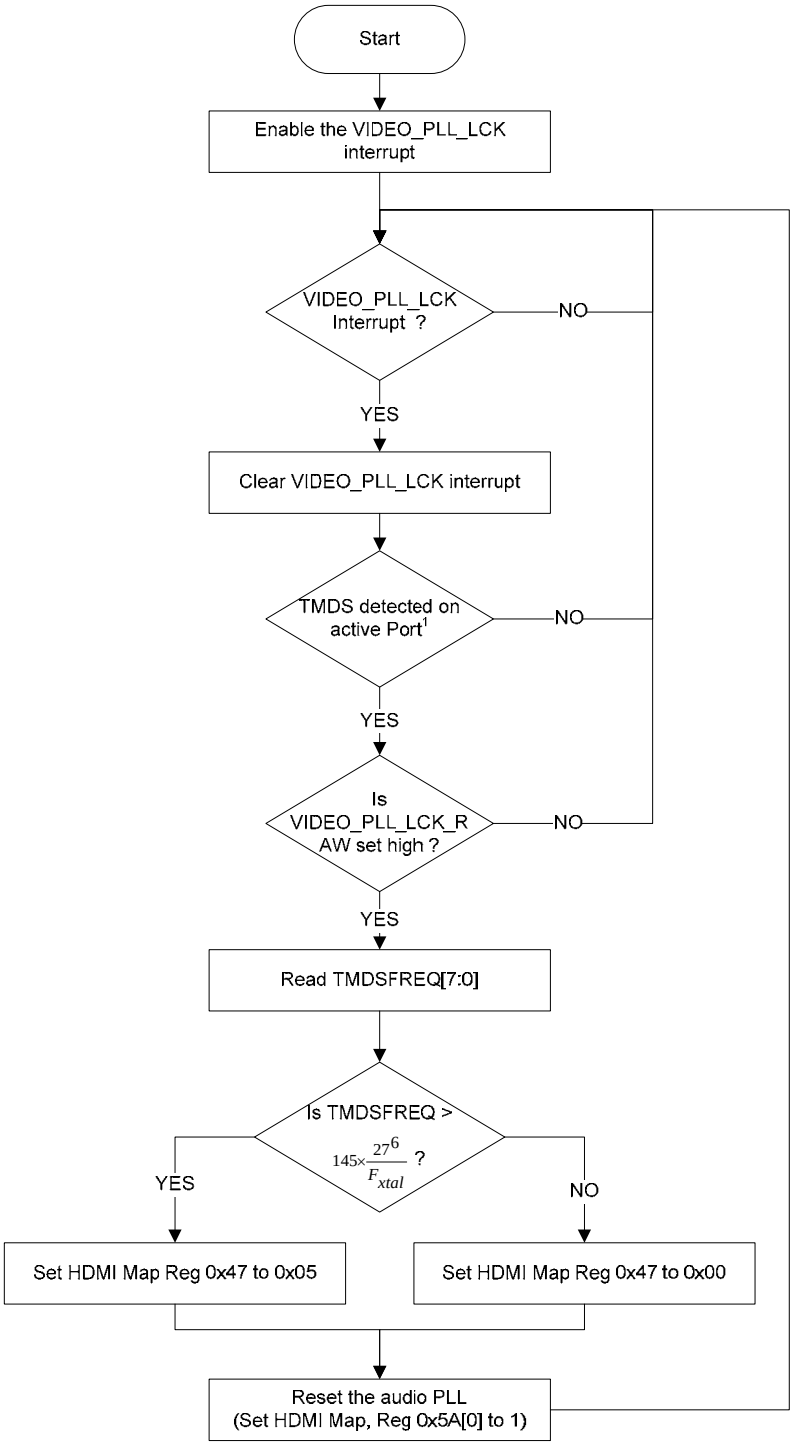
6A 47 05	ADI Recommended Write (Audio Synthesizer Optimization)
6A 5A 01	Reset the audio synthesiser

Following a change to an input video resolution below 147.8 (i.e. for video resolutions below 1080p59/1080p60) the follow register write must be performed:

HDMI Map

6A 47 00	ADI Recommended Write (Audio Synthesizer Optimization)
6A 5A 01	Reset the audio synthesiser

The algorithm shown in Figure 8 can be implemented in order to optimize the configuration of the Audio Synthesiser according to the TMDS clock Frequency.



Note: 1. TMDS_CLK_A_RAW (User Map 1 Reg 0x68[4]) or/and TMDS_CLK_B_RAW (User Map 1 Reg 0x68[3]) may be used to verify TMDS activity on the active TMDS Port. The active TMDS port is selected via HDMI_PORT_SELECT (HDMI Map Reg 0x00[0])
2. Fxtal is the Frequency of the external clock driving the part. Fxtal is typically 28.63636 MHz

Figure 8. Algorithm for Optimising Audio Synthesiser

1.3.13. Front and Back Porch Adjustment

The front and back porch positioning of the video output from the AD9388A/ADV7441A is misaligned by 1 pixel. In order to fix this misalignment it is necessary to move the DE signal by one pixel. This is achieved by the following settings:

User Map
DE_H_START (Reg 0x8B, 0x8D) = 0x01
DE_H_END (Reg 0x8B, 0x8C) = 0x01

Performing these writes causes a shift in the picture positioning and therefore an adjustment in the picture positioning is required. This is achieved by the following settings:

User Map
42 BF A2 Subtract 1 clock from HCount

These settings must be used for all HDMI input video.

1.3.14. Level Sensitive Versus Edge Sensitive Interrupts

The HDMI interrupt can be classified in the following 2 groups as shown in Table 12:

- Level Sensitive Interrupts
- Edge Sensitive Interrupts

The next 2 sub-sections detail these 2 categories.

Table 12. HDMI Interrupts Categorised in Level Versus Edge Sensitive Groups

Bit Position / Register Address	7	6	5	4	3	2	1	0
0x61	Level Sensitive Interrupts							
0x65								
0x69								
0x6C	Edge Sensitive Interrupts							
0x6F								
0x72								

1.3.14.1. Level Sensitive Interrupts

The interrupts in this group are triggered when the value of their corresponding 'raw status signal' change from 0 to 1 or from 1 to 0.

The raw status signal of a level sensitive interrupts is usually stored in the register preceding the register where the interrupt status is stored. Also not that the raw status of the HDMI interrupts stored in User Map 1, are also duplicated in the HDMI Map.

For example, AVI_INFO_ST is an interrupt status located in User Map 1, Reg 0x61[0]. The raw status corresponding to AVI_INFO_ST is AVI_INFO_RAW located in User Map, Reg 0x61 [0]. The AVI_INFO_RAW bit from the User Map 1 is duplicated in the HDMI Map as AVI_INFOFRAME_DET in Reg 0x18[0].

The HDMI level sensitive interrupts are enabled for the Interrupt pin INT1 or INT 2 by setting a relevant bit mask. For example, the interrupt for AVI_INFO_ST can be enabled as follows:

- On interrupt pin INT1
  by setting AVI_INFO_MB1 to 1 (in User Map 1, Reg 0x63 [0])

- On interrupt pin INT2
  by setting AVI_INFO_MB2 to 1 (in User Map 1, Reg 0x62 [0])

1.3.14.2. Edge Sensitive Interrupts

The interrupts is this group are triggered when the value of their corresponding raw status signal goes from 0 to 1.

The edge sensitive interrupt statuses are all located in the User Map 1. The raw status signals, available for some of the edge sensitive interrupts, are located in the HDMI Map in Reg 0x19 to 0x1B.

An edge sensitive interrupts are enabled by setting its corresponding mask. Note that a edge sensitive interrupt must be cleared at least once in order to correctly trigger. For example, the interrupt corresponding to NEW_AVI_INFO_ST can be enabled as follows:

- On interrupt pin INT1
  Set NEW_AVI_INFO_MB1 to 1 (in User Map 1, Reg 0x6E [0])
  Set NEW_AVI_INFO_CLR to 1 (in User Map 1, Reg 0x6C [0])

- On interrupt pin INT2
  Set NEW_AVI_INFO_MB2 to 1 (in User Map 1, Reg 0x6D [0])
  Set NEW_AVI_INFO_CLR to 1 (in User Map 1, Reg 0x6C [0])

1.3.15. Clearing the KSV List

The KSV registers located at address 0x80 to 0xF7 in Repeater Map are stored in RAM. These registers are only cleared to 0 when the part is powered up. Note that the KSV registers are not reset when the part is reset by a hardware reset or by a software reset. The processor controlling the AD9388A/ADV7441A can reset all the KSV registers with the following rights

64 80 00	Set all KSV registers in KSV FIFO to 0
64 81 00	Set all KSV registers in KSV FIFO to 0
…	Set all KSV registers in KSV FIFO to 0
64 F7 00	Set all KSV registers in KSV FIFO to 0

2. Digitizer Recommended Register Settings

2.1. Recommended Settings for All Digitizer Modes

ADI recommends that these register settings are programmed for all digitizer modes:

42 C8 08 Set Digital Fine Clamp setting for HDMI Mode

2.2. Standard Dynamic Settings for Digitizer Modes

The following standard register setting adjustments are required for best performance and are dependant on the video format currently being received by the digitizer:

- Primary Mode (User Map, Reg 0x05 bit [3:0]) and Video Standard (User Map, Reg 0x06 bit [3:0]) should be set as per Table 36 of the Datasheet Manual for each mode.
- Automatic setting of the PLL charge pump current should be enabled (User Map, Reg 0x47 bit [1]) and VCO range (User Map, Reg 0x47 bit [3]). Alternatively, these can be set manually via PLL_QPump[3:0] (User Map, Reg 0x3C bit[2:0]) and VCO_RANGE[1:0] (User Map, Reg 0x8A). Refer to Table 11 and Table 12 of the Datasheet Manual for each mode.
- For HD standards at 50 Hz, 30 Hz, 25 Hz, and 24 Hz, the correct Vertical Frequency setting must be set via CP_V_FREQ (User Map, Reg 0x06 bit [7:5]).
- The drive strength for data, clock, and synchronization signals must be programmed according to the pixel frequency.

2.3. Dynamic Settings for Optimal Performance

2.3.1. 1080p at 24/25/30 Hz

1080p 24 Hz, 25 Hz, and 30 Hz cannot be supported directly with the Primary Mode Video standard and Vertical Frequency for 1080p. It can be supported indirectly using the settings for 1080i and by forcing the interlaced bit to false.

The following settings are required for 1080p at 24 Hz:

User Map
42 05 01 PRIM_MODE = 001b COMP mode
42 06 4C VID_STD = 01100b for 1080i 60Hz 1x1. CP_V_FREQ = 010b for 30 Hz
42 91 10 Set interlaced bit to LO for 1080p

The following settings are required for 1080p at 25 Hz:

User Map
42 05 01 PRIM_MODE = 001b COMP mode
42 06 6C VID_STD = 01100b for 1080i60Hz 1x1. V_FREQ = 011b for 25 Hz
42 91 10 Set interlaced bit to LO for 1080p

The following settings are required for 1080p at 24Hz:

User Map
42 05 01 PRIM_MODE = 001b COMP mode
42 06 8C VID_STD = 01100b for 1080i60Hz 1x1, V_FREQ = 100b for 24 Hz
42 91 10 Set interlaced bit to LO for 1080p

2.3.2. 720p at 30Hz

The ADV7441A/AD9388A supports 720p as defined by the SMPTE 296M standard. In order to support 720p at 30Hz the following writes must be performed within the standard script.

- Set **cp_i2c_vsync_id_range** (0xB7[6], User Map) to 1'b1.
- Set **CP_V_FREQ** (0x06[7:5], User Map) to 3'b010.

Note: 720p at 24/25Hz cannot be supported by the ADV7441A/AD9388A.

2.3.3. 525p & 625p

When inputting 525p and 625p component formats with embedded syncs the following write is recommended to improve HS jitter.

4E F6 3B

2.3.4. Australian 1080i/ 1250i Detection

The ADV7441A/AD9388A supports 1250i/Australian 1080i as defined by the SMPTE 295M standard. However, the Standard Identification (STDI) block will not flag that the signal applied is an interlaced version of the standard. The STDI interlaced bit will not be set to 1.

The CP core does distinguish between the interlaced and progressive standard when the video standard is programmed for the 1250i/Australian 1080i standard. By using the CP_FORCED_INTERLACED bit, it can be detected whether or not the input is progressive.

Table 13 and Figure 9 provide details on how interlace detection can be done via the CP core.

Table 13. STDI and CP Interlaced Bits for 1250i/Australian 1080i Video Standard

VID_STD Setting	Applied Input	INTERLACED (STDI Readback)	CP_FORCED_INTERLACED (CP_Readback)	CP_INTERLACED (CP Readback)
01110b (1250i)	1250p	0	1	1
	1250i	0	0	1

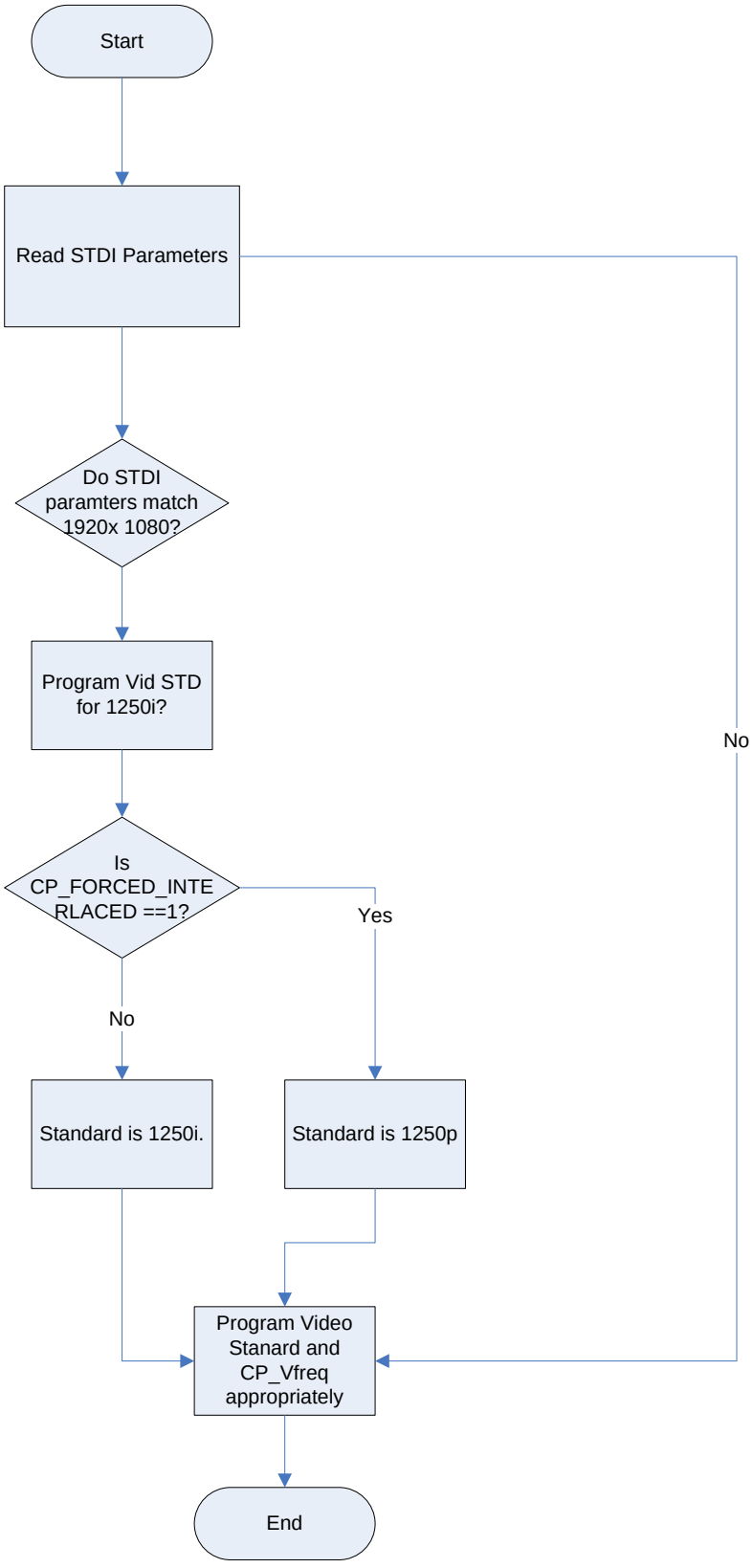


Figure 9. Algorithm for Distinguishing 1250i/Australian 1080i

2.3.5. Support for Interlaced Graphics Standards

The ADV7441A/AD9388A can be configured for video standards that are supported by the Primary Mode and Video Standard controls. The auto graphics mode is used to support these standards. Refer to the Hardware Manual for the list of modes supported by Primary Mode and Video Standard controls, and for a more detailed description of the auto graphics mode.

For interlaced graphics standards, the auto graphics mode can also be used but this requires an additional write in order to configure the Vsync correctly for interlaced standards. The additional write is as follows:

User Map
42 B7 17 ADI Recommended Write

The following script is an example configuration of an interlaced graphics mode (1024x768@ 43i) for the AD9388A/ADV7441A evaluation board.

RGB 1024x768 _@ 43 Auto Graphics 44.900 MHz Out through DAC

42 03 0C	Disable TOD
42 05 02	Prim_Mode =010b for automatic graphics mode
42 06 07	VID_STD=00111b for automatic graphics mode
42 1D 40	Disable TRI_LLC
42 3C A8	SOG Sync level for attenuated sync
42 47 0A	Enable Automatic PLL_Qpump and VCO Range
42 68 F2	Auto CSC , RGB Out
42 7B 1D	TURN OFF EAV & SAV CODES
42 F4 3F	Max Drive Strength
42 B7 17	ADI Recommended Write
42 87 E4	Enable Manual PLL Divider Ratio
42 88 F0	Set PLL Divider Ratio to 1264d
42 8F 03	Set Free Run Line Length to 815d
42 90 2F	Set Free Run Line Length
42 AB 33	Set Line Count Max 817d
42 AC 10	Set Line Count Max
42 91 50	Set interlaced bit

2.3.6. Support of Narrow Hsync and Vsync Pulses

The SPPD block is preceded with a deglitch filter that removes Hsync and Vsync pulses narrower than 7 clock periods of the external crystal oscillator. Thus with an external crystal oscillator of 28.63636 MHz frequency, pulses narrower than 0.27us will be filtered out by the deglitch filter. It is possible bypass the deglitch filter so that the DUT can correctly process video input that have narrow Hsync pulses with the settings outlined below. Note that the deglitch filter control value cannot read back as is located in the write-only function register 0x5 of the User Map.

- Enabling the deglitch filter (default configuration)
  Set User Map, Reg 0xB5 to 0x0

- Disabling the deglitch filter
  Set User Map, Reg 0xB5 to 0x8

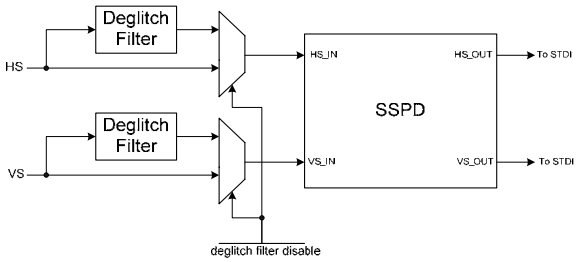


Figure 9. Syncs path showing the deglitch filter

2.3.7. Outputting CEA-861 Compliant Synchronization

2.3.7.1. Vsync Pulse

The following write is required to output a Vsync pulse width that is compliant with the CEA-861 specification for 1920x1080i and 720x480p resolutions

- Force Vsync output to be consistent with the 861 specification
  Set User Map, Reg 0xB7[3] to 1

Note that User Map, Reg 0xB7 is a write-only register with default value 0x13.

2.3.7.2. HS Signal

The following write are recommended to output a Hsync signal compliant to the 861 specification for 720x480p

- Set the fields END_HS[9:0] and START_HS[9:0]
  Set END_HS[9:0] to 0x3FD
  Set START_HS[9:0] to 0x3FE

Note that the field END_HS[9:0] and START_HS[9:0] are located in the User Map as follows

- END_HS[9:8], User Map Reg 0x7C[1:0]
- END_HS[7:0], User Map Reg 0x7C[7:0]
- START_HS[9:8], User Map Reg 0x7C[3:2]
- START_HS[9:8], User Map Reg 0x7E[1:0]

3. CP Core

3.1. CSC Pixel Shift

When setting CP_CSC_EN to 1 (User Map, Reg 0x69 [4]) A single pixel shift to the right was observed. This pixel misalignment can be fixed by setting:

User Map
DE_H_START (Reg 0x8B, 0x8D) = 0x01
DE_H_END (Reg 0x8B, 0x8C) = 0x01

3.2. CP Color Control Adjustments

The ADV7441A & AD9388A have a color control feature that can adjust the brightness, contrast, saturation, and hue properties. This feature can only be applied when the CP_CSC is directly implementing one of the following color space conversions:

• YUV to YUV
• RGB to YUV
• YUV to RGB

The CP color control block is enabled by setting **CP_CSC_EN,** User Map, Address 0x69, [4] = 1'b1 & leaving **VID_ADJ_EN (CP),** User Map 1, Address 0x9E, [7] to its default value of 1'b1.

Registers 0x9A, 0x9B, 0x9C & 0x9D control contrast, saturation, brightness & hue respectively. In the case where the input color space is YPbPr and the output format is RGB there is an issue with the brightness adjustment register 0x9C.

It should not be used for brightness adjustments in this mode. Instead the channel offset registers should be used to control brightness.

A_OFFSET[9:0] Channel A Offset (CP), User Map, Address 0x77, [5:0]; Address 0x78, [7:4]

B_OFFSET[9:0] Channel B Offset (CP), User Map, Address 0x78, [3:0]; Address 0x79, [7:2]

C_OFFSET[9:0] Channel C Offset (CP), User Map, Address 0x79, [1:0]; Address 0x7A, [7:0]

3.3. Automatic Gain Control with Embedded Synchronization Signals

The CP section contains an AGC block. The AGC measures the depth of the horizontal synchronization pulse on channel A to calculate the gain to be applied. In cases where no embedded synchronization is preset, the video gain must be set manually.

When processing analog component video with synchronization signals present on all channels the CP CSC should be enabled by setting CP_CSC_EN, User Map, Address 0x69, [4] = 1’b1. HSD_CHA[9:0], HSD_CHB[9:0] and HSD_CHC[9:0] can be used to decide if a sync signal is present on a given channel.