

ADV7850 REGISTER MAP DOCUMENTATION

Documentation of the Register Maps

SOFTWARE MANUAL

RevA

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1 REGISTER TABLES

1.1 ADDR 40(IO)

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x01	0x00		rw	adc_hdmi_simult_mode	-	-	-	-	-	-	-
0x07	0x40	io_reg_07	rw	sync_ch_auto_mode	sync_ch1_priority	sync_ch1_hs_sel[1]	sync_ch1_hs_sel[0]	sync_ch1_vs_sel[1]	sync_ch1_vs_sel[0]	sync_ch1_emb_sync_sel[1]	sync_ch1_emb_sync_sel[0]
0x08	0x14	io_reg_08	rw	-	-	sync_ch2_hs_sel[1]	sync_ch2_hs_sel[0]	sync_ch2_vs_sel[1]	sync_ch2_vs_sel[0]	sync_ch2_emb_sync_sel[1]	sync_ch2_emb_sync_sel[0]
0x0B	0x00		rw	-	-	-	-	-	-	core_pdn	xtal_pdn
0x0C	0x60	io_reg_0c	rw	-	-	power_down	-	-	-	-	-
0x11	0x00		rw	-	-	ch1 dly sel[1]	ch1 dly sel[0]	ch2 dly sel[1]	ch2 dly sel[0]	ch3 dly sel[1]	ch3 dly sel[0]
0x12	0x00	io_reg_12	r	sel_sync_channel	-	-	cp_std_interlaced	cp_interlaced	cp_prog_parm_for_int	cp_force_interlaced	cp_non_std_video
0x13	0x00	io_reg_13	r	-	-	-	-	-	-	cp_current_sync_src[1]	cp_current_sync_src[0]
0x15	0xBE	io_reg_15	rw	-	-	-	tri_audio	-	-	-	-
0x1B	0x00	hdmi tx reset	sc	tx_soft_reset	-	-	-	-	-	-	-
0x1C	0xBF	spi configuration_1	rw	-	-	vdp data packet size[5]	vdp data packet size[4]	vdp data packet size[3]	vdp data packet size[2]	vdp data packet size[1]	vdp data packet size[0]
0x1D	0x00	spi readback	r	-	-	-	-	-	-	vdp spi master busy	vdp spi slave busy
0x1E	0x2E	spi configuration_2	rw	spi config[1]	spi config[0]	-	vdp_dedicated_intr_en	spi master clock sel[1]	spi master clock sel[0]	vdp_intr_active_low	-
0x20	0x00	hpa_reg1	rw	hpa_man_value_a	hpa_man_value_b	hpa_man_value_c	hpa_man_value_d	hpa_tristate_a	hpa_tristate_b	hpa_tristate_c	hpa_tristate_d
0x21	0x00	hpa_reg2	r	-	-	-	-	hpa_status_port_a	hpa_status_port_b	hpa_status_port_c	hpa_status_port_d
0x22	0x16		rw	-	-	line_cnt_for_vdp_intr[5]	line_cnt_for_vdp_intr[4]	line_cnt_for_vdp_intr[3]	line_cnt_for_vdp_intr[2]	line_cnt_for_vdp_intr[1]	line_cnt_for_vdp_intr[0]
0x2C	0x00	hpa_reg3	rw	-	-	-	-	-	-	-	tx_hpd_override
0x3F	0x00	int status	r	-	-	-	-	-	tx_intrq_raw	intrq_raw	intrq2_raw
0x40	0x00	int1_configuration	rw	intrq_dur_sel[1]	intrq_dur_sel[0]	-	store_unmasked_irqs	-	mpu_stim_intrq	intrq_op_sel[1]	intrq_op_sel[0]
0x41	0x30	int2_configuration	rw	intrq2_dur_sel[1]	intrq2_dur_sel[0]	cp_lock_unlock_edge_sel	stdi_data_valid_edge_sel	en_umask_raw_intrq2	int2_en	intrq2_op_sel[1]	intrq2_op_sel[0]
0x42	0x00	raw_status_1	r	sspd_rslt_chngd_raw	mv_ps_det_raw	-	stdi_data_valid_raw	cp_unlock_raw	cp_lock_raw	-	afe_interrupt_raw
0x43	0x00	interrupt_status_1	r	sspd_rslt_chngd_st	mv_ps_det_st	-	stdi_data_valid_st	cp_unlock_st	cp_lock_st	-	afe_interrupt_st
0x44	0x00	interrupt_clear_1	sc	sspd_rslt_chngd_clr	mv_ps_det_clr	-	stdi_data_valid_clr	cp_unlock_clr	cp_lock_clr	-	afe_interrupt_clr
0x45	0x00	interrupt2_maskb_1	rw	sspd_rslt_chngd_mb2	mv_ps_det_mb2	-	stdi_data_valid_mb2	cp_unlock_mb2	cp_lock_mb2	-	afe_interrupt_mb2

ADD	DEF	REGISTERNAME	ACC	7	6	5	4	3	2	1	0
0x46	0x00	interrupt_maskb_1	rw	sspd_rslt_chngd_mb1	mv_ps_det_mb1	-	stdi_data_valid_mb1	cp_unlock_mb1	cp_lock_mb1	-	afe_interrupt_mb1
0x47	0x00	raw_status_2	r	mpu_stim_intrq_raw	mv_agc_det_raw	mv_cs_det_raw	-	-	cp_cgms_chngd_raw	-	-
0x48	0x00	interrupt_status_2	r	mpu_stim_intrq_st	mv_agc_det_st	mv_cs_det_st	-	-	cp_cgms_chngd_st	-	-
0x49	0x00	interrupt_clear_2	sc	mpu_stim_intrq_clr	mv_agc_det_clr	mv_cs_det_clr	-	-	cp_cgms_chngd_clr	-	-
0x4A	0x00	interrupt2_maskb_2	rw	mpu_stim_intrq_mb2	mv_agc_det_mb2	mv_cs_det_mb2	-	-	cp_cgms_chngd_mb2	-	-
0x4B	0x00	interrupt_maskb_2	rw	mpu_stim_intrq_mb1	mv_agc_det_mb1	mv_cs_det_mb1	-	-	cp_cgms_chngd_mb1	-	-
0x51	0x00	raw_status_4	r	ttxt_avl_raw	vitc_avl_raw	gs_data_type_raw	gs_pdc_vps_utc_avl_raw	-	cgms_wss_avl_raw	ccap_even_field_raw	ccap_avl_raw
0x52	0x00	interrupt_status_4	r	ttxt_avl_st	vitc_avl_st	gs_data_type_st	gs_pdc_vps_utc_avl_st	-	cgms_wss_avl_st	ccap_even_field_st	ccap_avl_st
0x53	0x00	interrupt_clear_4	sc	ttxt_avl_clr	vitc_avl_clr	gs_data_type_clr	gs_pdc_vps_utc_avl_clr	-	cgms_wss_avl_clr	ccap_even_field_clr	ccap_avl_clr
0x54	0x00	interrupt2_maskb_4	rw	ttxt_avl_mb2	vitc_avl_mb2	gs_data_type_mb2	gs_pdc_vps_utc_avl_mb2	-	cgms_wss_avl_mb2	ccap_even_field_mb2	ccap_avl_mb2
0x55	0x00	interrupt_maskb_4	rw	ttxt_avl_mb1	vitc_avl_mb1	gs_data_type_mb1	gs_pdc_vps_utc_avl_mb1	-	cgms_wss_avl_mb1	ccap_even_field_mb1	ccap_avl_mb1
0x5B	0x00	raw_status_6	r	cp_lock_ch2_raw	cp_unlock_ch2_raw	stdi_dvalid_ch2_raw	sspd_rslt_chngd_ch2_raw	cp_lock_ch1_raw	cp_unlock_ch1_raw	stdi_dvalid_ch1_raw	sspd_rslt_chngd_ch1_raw
0x5C	0x00	interrupt_status_6	r	cp_lock_ch2_st	cp_unlock_ch2_st	stdi_dvalid_ch2_st	sspd_rslt_chngd_ch2_st	cp_lock_ch1_st	cp_unlock_ch1_st	stdi_dvalid_ch1_st	sspd_rslt_chngd_ch1_st
0x5D	0x00	interrupt_clear_6	sc	cp_lock_ch2_clr	cp_unlock_ch2_clr	stdi_dvalid_ch2_clr	sspd_rslt_chngd_ch2_clr	cp_lock_ch1_clr	cp_unlock_ch1_clr	stdi_dvalid_ch1_clr	sspd_rslt_chngd_ch1_clr
0x5E	0x00	interrupt2_maskb_6	rw	cp_lock_ch2_mb2	cp_unlock_ch2_mb2	stdi_dvalid_ch2_mb2	sspd_rslt_chngd_ch2_mb2	cp_lock_ch1_mb2	cp_unlock_ch1_mb2	stdi_dvalid_ch1_mb2	sspd_rslt_chngd_ch1_mb2
0x5F	0x00	interrupt_maskb_6	rw	cp_lock_ch2_mb1	cp_unlock_ch2_mb1	stdi_dvalid_ch2_mb1	sspd_rslt_chngd_ch2_mb1	cp_lock_ch1_mb1	cp_unlock_ch1_mb1	stdi_dvalid_ch1_mb1	sspd_rslt_chngd_ch1_mb1
0x60	0x00	hdmi lvl raw status 1	r	isrc2_pckt_raw	isrc1_pckt_raw	acp_pckt_raw	vs_info_raw	ms_info_raw	spd_info_raw	audio_info_raw	avi_info_raw
0x61	0x00	hdmi lvl int status 1	r	isrc2_pckt_st	isrc1_pckt_st	acp_pckt_st	vs_info_st	ms_info_st	spd_info_st	audio_info_st	avi_info_st
0x62	0x00	hdmi lvl int clr 1	sc	isrc2_pckt_clr	isrc1_pckt_clr	acp_pckt_clr	vs_info_clr	ms_info_clr	spd_info_clr	audio_info_clr	avi_info_clr
0x63	0x00	hdmi lvl int2 maskb 1	rw	isrc2_pckt_mb2	isrc1_pckt_mb2	acp_pckt_mb2	vs_info_mb2	ms_info_mb2	spd_info_mb2	audio_info_mb2	avi_info_mb2
0x64	0x00	hdmi lvl int maskb 1	rw	isrc2_pckt_mb1	isrc1_pckt_mb1	acp_pckt_mb1	vs_info_mb1	ms_info_mb1	spd_info_mb1	audio_info_mb1	avi_info_mb1
0x65	0x00	hdmi lvl raw status 2	r	cs_data_valid_raw	internal_mute_raw	av_mute_raw	audio_ch_md_raw	hdmi_mode_raw	gen_ctl_pckt_raw	audio_c_pckt_raw	gamut_mdata_raw
0x66	0x00	hdmi lvl int status 2	r	cs_data_valid_st	internal_mute_st	av_mute_st	audio_ch_md_st	hdmi_mode_st	gen_ctl_pckt_st	audio_c_pckt_st	gamut_mdata_st
0x67	0x00	hdmi lvl int clr 2	sc	cs_data_valid_clr	internal_mute_clr	av_mute_clr	audio_ch_md_clr	hdmi_mode_clr	gen_ctl_pckt_clr	audio_c_pckt_clr	gamut_mdata_clr

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x68	0x00	hdmi lvl int2 maskb 2	rw	cs_data_valid_mb2	internal_mute_mb2	av_mute_mb2	audio_ch_md_mb2	hdmi_mode_mb2	gen_ctl_pckt_mb2	audio_c_pckt_mb2	gamut_mdata_mb2
0x69	0x00	hdmi lvl int maskb 2	rw	cs_data_valid_mb1	internal_mute_mb1	av_mute_mb1	audio_ch_md_mb1	hdmi_mode_mb1	gen_ctl_pckt_mb1	audio_c_pckt_mb1	gamut_mdata_mb1
0x6A	0x00	hdmi lvl raw status 3	r	tmdsppll_lck_a_raw	tmdsppll_lck_b_raw	tmdsppll_lck_c_raw	tmdsppll_lck_d_raw	tmds_clk_a_raw	tmds_clk_b_raw	tmds_clk_c_raw	tmds_clk_d_raw
0x6B	0x00	hdmi lvl int status 3	r	tmdsppll_lck_a_st	tmdsppll_lck_b_st	tmdsppll_lck_c_st	tmdsppll_lck_d_st	tmds_clk_a_st	tmds_clk_b_st	tmds_clk_c_st	tmds_clk_d_st
0x6C	0x00	hdmi lvl int clr 3	sc	tmdsppll_lck_a_clr	tmdsppll_lck_b_clr	tmdsppll_lck_c_clr	tmdsppll_lck_d_clr	tmds_clk_a_clr	tmds_clk_b_clr	tmds_clk_c_clr	tmds_clk_d_clr
0x6D	0x00	hdmi lvl int2 maskb 3	rw	tmdsppll_lck_a_mb2	tmdsppll_lck_b_mb2	tmdsppll_lck_c_mb2	tmdsppll_lck_d_mb2	tmds_clk_a_mb2	tmds_clk_b_mb2	tmds_clk_c_mb2	tmds_clk_d_mb2
0x6E	0x00	hdmi lvl int maskb 3	rw	tmdsppll_lck_a_mb1	tmdsppll_lck_b_mb1	tmdsppll_lck_c_mb1	tmdsppll_lck_d_mb1	tmds_clk_a_mb1	tmds_clk_b_mb1	tmds_clk_c_mb1	tmds_clk_d_mb1
0x6F	0x00	hdmi lvl raw status 4	r	hdmi_encrypt_a_raw	hdmi_encrypt_b_raw	hdmi_encrypt_c_raw	hdmi_encrypt_d_raw	cable_det_a_raw	cable_det_b_raw	cable_det_c_raw	cable_det_d_raw
0x70	0x00	hdmi lvl int status 4	r	hdmi_encrypt_a_st	hdmi_encrypt_b_st	hdmi_encrypt_c_st	hdmi_encrypt_d_st	cable_det_a_st	cable_det_b_st	cable_det_c_st	cable_det_d_st
0x71	0x00	hdmi lvl int clr 4	sc	hdmi_encrypt_a_clr	hdmi_encrypt_b_clr	hdmi_encrypt_c_clr	hdmi_encrypt_d_clr	cable_det_a_clr	cable_det_b_clr	cable_det_c_clr	cable_det_d_clr
0x72	0x00	hdmi lvl int2 maskb 4	rw	hdmi_encrypt_a_mb2	hdmi_encrypt_b_mb2	hdmi_encrypt_c_mb2	hdmi_encrypt_d_mb2	cable_det_a_mb2	cable_det_b_mb2	cable_det_c_mb2	cable_det_d_mb2
0x73	0x00	hdmi lvl int maskb 4	rw	hdmi_encrypt_a_mb1	hdmi_encrypt_b_mb1	hdmi_encrypt_c_mb1	hdmi_encrypt_d_mb1	cable_det_a_mb1	cable_det_b_mb1	cable_det_c_mb1	cable_det_d_mb1
0x74	0x00	hdmi lvl raw status 5	r	-	-	-	-	-	video_3d_raw	v_locked_raw	de_regen_lck_raw
0x75	0x00	hdmi lvl int status 5	r	-	-	-	-	-	video_3d_st	v_locked_st	de_regen_lck_st
0x76	0x00	hdmi lvl int clr 5	sc	-	-	-	-	-	video_3d_clr	v_locked_clr	de_regen_lck_clr
0x77	0x00	hdmi lvl int2 maskb 5	rw	-	-	-	-	-	video_3d_mb2	v_locked_mb2	de_regen_lck_mb2
0x78	0x00	hdmi lvl int maskb 5	rw	-	-	-	-	-	video_3d_mb1	v_locked_mb1	de_regen_lck_mb1
0x79	0x00	hdmi edg raw status 1	r	new_isrc2_pckt_raw	new_isrc1_pckt_raw	new_acp_pckt_raw	new_vs_info_raw	new_ms_info_raw	new_spd_info_raw	new_audio_info_raw	new_avi_info_raw
0x7A	0x00	hdmi edg int status 1	r	new_isrc2_pckt_st	new_isrc1_pckt_st	new_acp_pckt_st	new_vs_info_st	new_ms_info_st	new_spd_info_st	new_audio_info_st	new_avi_info_st
0x7B	0x00	hdmi edg int clr 1	sc	new_isrc2_pckt_clr	new_isrc1_pckt_clr	new_acp_pckt_clr	new_vs_info_clr	new_ms_info_clr	new_spd_info_clr	new_audio_info_clr	new_avi_info_clr
0x7C	0x00	hdmi edg int2 maskb 1	rw	new_isrc2_pckt_mb2	new_isrc1_pckt_mb2	new_acp_pckt_mb2	new_vs_info_mb2	new_ms_info_mb2	new_spd_info_mb2	new_audio_info_mb2	new_avi_info_mb2
0x7D	0x00	hdmi edg int maskb 1	rw	new_isrc2_pckt_mb1	new_isrc1_pckt_mb1	new_acp_pckt_mb1	new_vs_info_mb1	new_ms_info_mb1	new_spd_info_mb1	new_audio_info_mb1	new_avi_info_mb1
0x7E	0x00	hdmi edg raw status 2	r	fifo_near_ovfl_raw	fifo_underflo_raw	fifo_overflo_raw	cts_pass_thrsh_raw	change_n_raw	packet_error_raw	audio_pckt_err_raw	new_gamut_mdata_raw
0x7F	0x00	hdmi edg int status 2	r	fifo_near_ovfl_st	fifo_underflo_st	fifo_overflo_st	cts_pass_thrsh_st	change_n_st	packet_error_st	audio_pckt_err_st	new_gamut_mdata_st

ADD	DEF	REGISTERNAME	ACC	7	6	5	4	3	2	1	0
0x80	0x00	hdmi edg int clr 2	sc	fifo_near_ovfl_clr	fifo_underflo_clr	fifo_overflo_clr	cts_pass_thrsh_clr	change_n_clr	packet_error_clr	audio_pckt_err_clr	new_gamut_mdat_a_clr
0x81	0x00	hdmi edg int2 maskb 2	rw	fifo_near_ovfl_mb2	fifo_underflo_mb2	fifo_overflo_mb2	cts_pass_thrsh_mb2	change_n_mb2	packet_error_mb2	audio_pckt_err_mb2	new_gamut_mdat_a_mb2
0x82	0x00	hdmi edg int maskb 2	rw	fifo_near_ovfl_mb1	fifo_underflo_mb1	fifo_overflo_mb1	cts_pass_thrsh_mb1	change_n_mb1	packet_error_mb1	audio_pckt_err_mb1	new_gamut_mdat_a_mb1
0x83	0x00	hdmi edg raw status 3	r	deep_color_chng_raw	vclk_chng_raw	audio_mode_chng_raw	parity_error_raw	new_samp_rt_raw	audioflt_line_raw	new_tmnds_frq_raw	fifo_near_uflora_w
0x84	0x00	hdmi edg status 3	r	deep_color_chng_st	vclk_chng_st	audio_mode_chng_st	parity_error_st	new_samp_rt_st	audioflt_line_st	new_tmnds_frq_st	fifo_near_uflora_st
0x85	0x00	hdmi edg int clr 3	sc	deep_color_chng_clr	vclk_chng_clr	audio_mode_chng_clr	parity_error_clr	new_samp_rt_clr	audioflt_line_clr	new_tmnds_frq_clr	fifo_near_uflora_clr
0x86	0x00	hdmi edg int2 maskb 3	rw	deep_color_chng_mb2	vclk_chng_mb2	audio_mode_chng_mb2	parity_error_mb2	new_samp_rt_mb2	audioflt_line_mb2	new_tmnds_frq_mb2	fifo_near_uflora_mb2
0x87	0x00	hdmi edg int maskb 3	rw	deep_color_chng_mb1	vclk_chng_mb1	audio_mode_chng_mb1	parity_error_mb1	new_samp_rt_mb1	audioflt_line_mb1	new_tmnds_frq_mb1	fifo_near_uflora_mb1
0x88	0x00	hdmi edg raw status 4	r	ms_inf_cks_err_raw	spd_inf_cks_err_raw	aud_inf_cks_err_raw	avi_inf_cks_err_raw	aksv_update_a_raw	aksv_update_b_raw	aksv_update_c_raw	aksv_update_d_raw
0x89	0x00	hdmi edg status 4	r	ms_inf_cks_err_st	spd_inf_cks_err_st	aud_inf_cks_err_st	avi_inf_cks_err_st	aksv_update_a_st	aksv_update_b_st	aksv_update_c_st	aksv_update_d_st
0x8A	0x00	hdmi edg int clr 4	sc	ms_inf_cks_err_clr	spd_inf_cks_err_clr	aud_inf_cks_err_clr	avi_inf_cks_err_clr	aksv_update_a_clr	aksv_update_b_clr	aksv_update_c_clr	aksv_update_d_clr
0x8B	0x00	hdmi edg int2 maskb 4	rw	ms_inf_cks_err_mb2	spd_inf_cks_err_mb2	aud_inf_cks_err_mb2	avi_inf_cks_err_mb2	aksv_update_a_mb2	aksv_update_b_mb2	aksv_update_c_mb2	aksv_update_d_mb2
0x8C	0x00	hdmi edg int maskb 4	rw	ms_inf_cks_err_mb1	spd_inf_cks_err_mb1	aud_inf_cks_err_mb1	avi_inf_cks_err_mb1	aksv_update_a_mb1	aksv_update_b_mb1	aksv_update_c_mb1	aksv_update_d_mb1
0x8D	0x00	hdmi edg raw status 5	r	ri_expired_a_raw	ri_expired_b_raw	ri_expired_c_raw	ri_expired_d_raw	-	-	bg_meas_done_raw	vs_inf_cks_err_raw
0x8E	0x00	hdmi edg status 5	r	ri_expired_a_st	ri_expired_b_st	ri_expired_c_st	ri_expired_d_st	-	-	bg_meas_done_st	vs_inf_cks_err_st
0x8F	0x00	hdmi edg int clr 5	sc	ri_expired_a_clr	ri_expired_b_clr	ri_expired_c_clr	ri_expired_d_clr	-	-	bg_meas_done_clr	vs_inf_cks_err_clr
0x90	0x00	hdmi edg int2 maskb 5	rw	ri_expired_a_mb2	ri_expired_b_mb2	ri_expired_c_mb2	ri_expired_d_mb2	-	-	bg_meas_done_mb2	vs_inf_cks_err_mb2
0x91	0x00	hdmi edg int maskb 5	rw	ri_expired_a_mb1	ri_expired_b_mb1	ri_expired_c_mb1	ri_expired_d_mb1	-	-	bg_meas_done_mb1	vs_inf_cks_err_mb1
0x9C	0x00	sdp_raw_status	r	-	-	-	-	sdp_std_changed_raw	-	sdp_burst_locked_raw	sdp_video_detected_raw
0x9D	0x00	sdp_interrupt_status	r	-	-	-	-	sdp_std_changed_st	-	sdp_burst_locked_st	sdp_video_detected_st
0x9E	0x00	sdp_interrupt_clear	sc	-	-	-	-	sdp_std_changed_clr	-	sdp_burst_locked_clr	sdp_video_detected_clr
0x9F	0x00	sdp_interrupt2_maskb	rw	-	-	-	-	sdp_std_changed_mb2	-	sdp_burst_locked_mb2	sdp_video_detected_mb2
0xA0	0x00	sdp_interrupt_maskb	rw	-	-	-	-	sdp_std_changed_mb1	sdp_fifo_crisis_mb1	sdp_burst_locked_mb1	sdp_video_detected_mb1

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xAC	0x0F	arc_tx_powerdown	rw	-	-	-	-	arc_pwrn_d[1]	arc_pwrn_c[1]	arc_pwrn_b[1]	arc_pwrn_a[1]
0xAD	0x00	arc_tx_control_1	rw	inv_spdif_in_d	inv_spdif_in_c	inv_spdif_in_b	inv_spdif_in_a	zero_spdif_in_d	zero_spdif_in_c	zero_spdif_in_b	zero_spdif_in_a
0xAE	0x06	arc_tx_control_2	rw	-	-	-	-	-	arc_tx_ampl[2]	arc_tx_ampl[1]	arc_tx_ampl[0]
0xE1	0x00	identification code_1	r	rd_info[15]	rd_info[14]	rd_info[13]	rd_info[12]	rd_info[11]	rd_info[10]	rd_info[9]	rd_info[8]
0xE2	0x00	identification code_2	r	rd_info[7]	rd_info[6]	rd_info[5]	rd_info[4]	rd_info[3]	rd_info[2]	rd_info[1]	rd_info[0]
0xE4	0x00		rw	-	-	-	-	-	-	clock polarity	clock phase
0xE7	0x00	audio_codec_slave_address	rw	audio_codec_slave_addr[6]	audio_codec_slave_addr[5]	audio_codec_slave_addr[4]	audio_codec_slave_addr[3]	audio_codec_slave_addr[2]	audio_codec_slave_addr[1]	audio_codec_slave_addr[0]	-
0xEB	0x00	xmem_gamma_slave_address	rw	xmem_gamma_slave_addr[6]	xmem_gamma_slave_addr[5]	xmem_gamma_slave_addr[4]	xmem_gamma_slave_addr[3]	xmem_gamma_slave_addr[2]	xmem_gamma_slave_addr[1]	xmem_gamma_slave_addr[0]	-
0xEC	0x00	vfe_slave_address	rw	vfe_slave_addr[6]	vfe_slave_addr[5]	vfe_slave_addr[4]	vfe_slave_addr[3]	vfe_slave_addr[2]	vfe_slave_addr[1]	vfe_slave_addr[0]	-
0xF0	0x00	tx_edid_slave_address	rw	tx_edid_slave_addr[6]	tx_edid_slave_addr[5]	tx_edid_slave_addr[4]	tx_edid_slave_addr[3]	tx_edid_slave_addr[2]	tx_edid_slave_addr[1]	tx_edid_slave_addr[0]	-
0xF1	0x00	sdp_slave_address	rw	sdp_slave_addr[6]	sdp_slave_addr[5]	sdp_slave_addr[4]	sdp_slave_addr[3]	sdp_slave_addr[2]	sdp_slave_addr[1]	sdp_slave_addr[0]	-
0xF2	0x00	sdp_io_slave_address	rw	sdp_io_slave_addr[6]	sdp_io_slave_addr[5]	sdp_io_slave_addr[4]	sdp_io_slave_addr[3]	sdp_io_slave_addr[2]	sdp_io_slave_addr[1]	sdp_io_slave_addr[0]	-
0xF5	0x00	infoframe_slave_address	rw	infoframe_slave_addr[6]	infoframe_slave_addr[5]	infoframe_slave_addr[4]	infoframe_slave_addr[3]	infoframe_slave_addr[2]	infoframe_slave_addr[1]	infoframe_slave_addr[0]	-
0xF8	0x00	afe_slave_address	rw	afe_slave_addr[6]	afe_slave_addr[5]	afe_slave_addr[4]	afe_slave_addr[3]	afe_slave_addr[2]	afe_slave_addr[1]	afe_slave_addr[0]	-
0xF9	0x00	ksv_slave_address	rw	ksv_slave_addr[6]	ksv_slave_addr[5]	ksv_slave_addr[4]	ksv_slave_addr[3]	ksv_slave_addr[2]	ksv_slave_addr[1]	ksv_slave_addr[0]	-
0xFA	0x00	edid_slave_address	rw	edid_slave_addr[6]	edid_slave_addr[5]	edid_slave_addr[4]	edid_slave_addr[3]	edid_slave_addr[2]	edid_slave_addr[1]	edid_slave_addr[0]	-
0xFB	0x00	hdmi_slave_address	rw	hdmi_slave_addr[6]	hdmi_slave_addr[5]	hdmi_slave_addr[4]	hdmi_slave_addr[3]	hdmi_slave_addr[2]	hdmi_slave_addr[1]	hdmi_slave_addr[0]	-
0xFD	0x00	cp_slave_address	rw	cp_slave_addr[6]	cp_slave_addr[5]	cp_slave_addr[4]	cp_slave_addr[3]	cp_slave_addr[2]	cp_slave_addr[1]	cp_slave_addr[0]	-
0xFE	0x00	vdp_slave_address	rw	vdp_slave_addr[6]	vdp_slave_addr[5]	vdp_slave_addr[4]	vdp_slave_addr[3]	vdp_slave_addr[2]	vdp_slave_addr[1]	vdp_slave_addr[0]	-
0xFF	0x00	io_reg_ff	sc	main_reset	-	vdp_reset	-	sdp_reset	sdp_mem_reset	-	-

1.2 ADDR 4C (AFE)

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x0F	adc powerdown control	rw	-	-	-	-	pdn_adc3	pdn_adc2	pdn_adc1	pdn_adc0
0x01	0x07	afe powerdown	rw	-	-	-	-	-	-	pdn_aout2	pdn_aout1
0x02	0x00	input mux control_1	rw	adc_switch_man	emb_sync_sel_man_en	-	-	-	ain_sel[2]	ain_sel[1]	ain_sel[0]
0x03	0x00	input mux control_2	rw	adc0_sw_man[3]	adc0_sw_man[2]	adc0_sw_man[1]	adc0_sw_man[0]	adc1_sw_man[3]	adc1_sw_man[2]	adc1_sw_man[1]	adc1_sw_man[0]
0x04	0x00	input mux control_3	rw	adc2_sw_man[3]	adc2_sw_man[2]	adc2_sw_man[1]	adc2_sw_man[0]	adc3_sw_man[3]	adc3_sw_man[2]	adc3_sw_man[1]	adc3_sw_man[0]
0x05	0x00	anti-alias filter enable	rw	-	-	-	-	aa_filter_en3	aa_filter_en2	aa_filter_en1	aa_filter_en0
0x06	0x00	anti-alias filter calibration	rw	-	-	aa_filt_high_bw[1]	-	-	-	-	-
0x07	0x00	anti-alias filter bandwidth	rw	aa_filt_high_bw[0]	aa_filt_prog_bw[1]	aa_filt_prog_bw[0]	-	-	-	-	-
0x14	0x00	fast blank	rw	-	-	-	-	fb_select[3]	fb_select[2]	fb_select[1]	fb_select[0]
0x15	0x0A	sync stripper	rw	emb_sync_1_sel_man[1]	emb_sync_1_sel_man[0]	emb_sync_2_sel_man[1]	emb_sync_2_sel_man[0]	sync1_filter_sel[1]	sync1_filter_sel[0]	sync2_filter_sel[1]	sync2_filter_sel[0]
0x16	0x98	sync slicer level	rw	-	-	-	slice_level[4]	slice_level[3]	slice_level[2]	slice_level[1]	slice_level[0]
0x17	0x00	trilevel interrupt enable 1	rw	tri1_int_maskb[1]	tri1_int_maskb[0]	tri2_int_maskb[1]	tri2_int_maskb[0]	tri3_int_maskb[1]	tri3_int_maskb[0]	tri4_int_maskb[1]	tri4_int_maskb[0]
0x18	0x00	trilevel interrupt enable 2	rw	tri5_int_maskb[1]	tri5_int_maskb[0]	tri6_int_maskb[1]	tri6_int_maskb[0]	tri7_int_maskb[1]	tri7_int_maskb[0]	tri8_int_maskb[1]	tri8_int_maskb[0]
0x19	0x00	trilevel interrupt clear 1	sc	tri1_int_clear[1]	tri1_int_clear[0]	tri2_int_clear[1]	tri2_int_clear[0]	tri3_int_clear[1]	tri3_int_clear[0]	tri4_int_clear[1]	tri4_int_clear[0]
0x1A	0x00	trilevel interrupt clear 2	sc	tri5_int_clear[1]	tri5_int_clear[0]	tri6_int_clear[1]	tri6_int_clear[0]	tri7_int_clear[1]	tri7_int_clear[0]	tri8_int_clear[1]	tri8_int_clear[0]
0x1B	0x00	trilevel interrupt status 1	r	tri1_int_status[1]	tri1_int_status[0]	tri2_int_status[1]	tri2_int_status[0]	tri3_int_status[1]	tri3_int_status[0]	tri4_int_status[1]	tri4_int_status[0]
0x1C	0x00	trilevel interrupt status 2	r	tri5_int_status[1]	tri5_int_status[0]	tri6_int_status[1]	tri6_int_status[0]	tri7_int_status[1]	tri7_int_status[0]	tri8_int_status[1]	tri8_int_status[0]
0x1D	0x6D	tri1 slice control	rw	-	tri1_slicer_pwrdsn	tri1_bilevel_slice_en	tri1_upper_slice_level[2]	tri1_upper_slice_level[1]	tri1_upper_slice_level[0]	tri1_lower_slice_level[1]	tri1_lower_slice_level[0]
0x1E	0x6D	tri2 slice control	rw	-	tri2_slicer_pwrdsn	tri2_bilevel_slice_en	tri2_upper_slice_level[2]	tri2_upper_slice_level[1]	tri2_upper_slice_level[0]	tri2_lower_slice_level[1]	tri2_lower_slice_level[0]
0x1F	0x6D	tri3 slice control	rw	-	tri3_slicer_pwrdsn	tri3_bilevel_slice_en	tri3_upper_slice_level[2]	tri3_upper_slice_level[1]	tri3_upper_slice_level[0]	tri3_lower_slice_level[1]	tri3_lower_slice_level[0]
0x20	0x6D	tri4 slice control	rw	-	tri4_slicer_pwrdsn	tri4_bilevel_slice_en	tri4_upper_slice_level[2]	tri4_upper_slice_level[1]	tri4_upper_slice_level[0]	tri4_lower_slice_level[1]	tri4_lower_slice_level[0]
0x21	0x6D	tri5 slice control	rw	-	tri5_slicer_pwrdsn	tri5_bilevel_slice_en	tri5_upper_slice_level[2]	tri5_upper_slice_level[1]	tri5_upper_slice_level[0]	tri5_lower_slice_level[1]	tri5_lower_slice_level[0]
0x22	0x6D	tri6 slice control	rw	-	tri6_slicer_pwrdsn	tri6_bilevel_slice_en	tri6_upper_slice_level[2]	tri6_upper_slice_level[1]	tri6_upper_slice_level[0]	tri6_lower_slice_level[1]	tri6_lower_slice_level[0]
0x23	0x6D	tri7 slice control	rw	-	tri7_slicer_pwrdsn	tri7_bilevel_slice_en	tri7_upper_slice_level[2]	tri7_upper_slice_level[1]	tri7_upper_slice_level[0]	tri7_lower_slice_level[1]	tri7_lower_slice_level[0]

Addr 4C (AFE)

ADV7850 Register Map

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x24	0x6D	tri8 slice control	rw	-	tri8_slicer_pwrn	tri8_bilevel_slice_en	tri8_upper_slice_level[2]	tri8_upper_slice_level[1]	tri8_upper_slice_level[0]	tri8_lower_slice_level[1]	tri8_lower_slice_level[0]
0x27	0x00	tri-inputs level readback_1	r	tri1_readback[1]	tri1_readback[0]	tri2_readback[1]	tri2_readback[0]	tri3_readback[1]	tri3_readback[0]	tri4_readback[1]	tri4_readback[0]
0x28	0x00	tri-inputs level readback_2	r	tri5_readback[1]	tri5_readback[0]	tri6_readback[1]	tri6_readback[0]	tri7_readback[1]	tri7_readback[0]	tri8_readback[1]	tri8_readback[0]
0x2C	0x00	input mux control_4	rw	vout2_sel[3]	vout2_sel[2]	vout2_sel[1]	vout2_sel[0]	vout1_sel[3]	vout1_sel[2]	vout1_sel[1]	vout1_sel[0]

1.3 ADDR A8 (MEMORY)

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x11	0x12	ddr2 controller config_12	rw	sdram_size[3]	sdram_size[2]	sdram_size[1]	sdram_size[0]	-	-	-	-
0x28	0x00	ext mem control_7	rw	rw_ctrl_oe	ddr2_ck_oe	-	-	-	-	mem_rw_ctrl_drv_str[1]	mem_rw_ctrl_drv_str[0]
0x2B	0x29	ddr2 controller config_19	rw	-	-	-	-	-	mem_sm_reset	-	-
0x37	0xAA	ext mem control_9	rw	ck_drv_str[7]	ck_drv_str[6]	ck_drv_str[5]	ck_drv_str[4]	ck_drv_str[3]	ck_drv_str[2]	ck_drv_str[1]	ck_drv_str[0]
0x38	0x55	ext mem control_10	rw	dqs_drv_str[7]	dqs_drv_str[6]	dqs_drv_str[5]	dqs_drv_str[4]	dqs_drv_str[3]	dqs_drv_str[2]	dqs_drv_str[1]	dqs_drv_str[0]
0x39	0x55	ext mem control_11	rw	dqs_drv_str[7]	dqs_drv_str[6]	dqs_drv_str[5]	dqs_drv_str[4]	dqs_drv_str[3]	dqs_drv_str[2]	dqs_drv_str[1]	dqs_drv_str[0]

1.4 ADDR 44 (CP)

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x0B	0x00	csc_coeff_rb_1	r	rb_csc_scale[1]	rb_csc_scale[0]	-	rb_a4[12]	rb_a4[11]	rb_a4[10]	rb_a4[9]	rb_a4[8]
0x0C	0x00	csc_coeff_rb_2	r	rb_a4[7]	rb_a4[6]	rb_a4[5]	rb_a4[4]	rb_a4[3]	rb_a4[2]	rb_a4[1]	rb_a4[0]
0x0D	0x00	csc_coeff_rb_3	r	-	rb_a3[12]	rb_a3[11]	rb_a3[10]	rb_a3[9]	rb_a3[8]	rb_a3[7]	rb_a3[6]
0x0E	0x00	csc_coeff_rb_4	r	rb_a3[5]	rb_a3[4]	rb_a3[3]	rb_a3[2]	rb_a3[1]	rb_a3[0]	rb_a2[12]	rb_a2[11]
0x0F	0x00	csc_coeff_rb_5	r	rb_a2[10]	rb_a2[9]	rb_a2[8]	rb_a2[7]	rb_a2[6]	rb_a2[5]	rb_a2[4]	rb_a2[3]
0x10	0x00	csc_coeff_rb_6	r	rb_a2[2]	rb_a2[1]	rb_a2[0]	rb_a1[12]	rb_a1[11]	rb_a1[10]	rb_a1[9]	rb_a1[8]
0x11	0x00	csc_coeff_rb_7	r	rb_a1[7]	rb_a1[6]	rb_a1[5]	rb_a1[4]	rb_a1[3]	rb_a1[2]	rb_a1[1]	rb_a1[0]
0x12	0x00	csc_coeff_rb_8	r	-	-	-	rb_b4[12]	rb_b4[11]	rb_b4[10]	rb_b4[9]	rb_b4[8]
0x13	0x00	csc_coeff_rb_9	r	rb_b4[7]	rb_b4[6]	rb_b4[5]	rb_b4[4]	rb_b4[3]	rb_b4[2]	rb_b4[1]	rb_b4[0]
0x14	0x00	csc_coeff_rb_10	r	-	rb_b3[12]	rb_b3[11]	rb_b3[10]	rb_b3[9]	rb_b3[8]	rb_b3[7]	rb_b3[6]
0x15	0x00	csc_coeff_rb_11	r	rb_b3[5]	rb_b3[4]	rb_b3[3]	rb_b3[2]	rb_b3[1]	rb_b3[0]	rb_b2[12]	rb_b2[11]
0x16	0x00	csc_coeff_rb_12	r	rb_b2[10]	rb_b2[9]	rb_b2[8]	rb_b2[7]	rb_b2[6]	rb_b2[5]	rb_b2[4]	rb_b2[3]
0x17	0x00	csc_coeff_rb_13	r	rb_b2[2]	rb_b2[1]	rb_b2[0]	rb_b1[12]	rb_b1[11]	rb_b1[10]	rb_b1[9]	rb_b1[8]
0x18	0x00	csc_coeff_rb_14	r	rb_b1[7]	rb_b1[6]	rb_b1[5]	rb_b1[4]	rb_b1[3]	rb_b1[2]	rb_b1[1]	rb_b1[0]
0x19	0x00	csc_coeff_rb_15	r	-	-	-	rb_c4[12]	rb_c4[11]	rb_c4[10]	rb_c4[9]	rb_c4[8]
0x1A	0x00	csc_coeff_rb_16	r	rb_c4[7]	rb_c4[6]	rb_c4[5]	rb_c4[4]	rb_c4[3]	rb_c4[2]	rb_c4[1]	rb_c4[0]
0x1B	0x00	csc_coeff_rb_17	r	-	rb_c3[12]	rb_c3[11]	rb_c3[10]	rb_c3[9]	rb_c3[8]	rb_c3[7]	rb_c3[6]
0x1C	0x00	csc_coeff_rb_18	r	rb_c3[5]	rb_c3[4]	rb_c3[3]	rb_c3[2]	rb_c3[1]	rb_c3[0]	rb_c2[12]	rb_c2[11]
0x1D	0x00	csc_coeff_rb_19	r	rb_c2[10]	rb_c2[9]	rb_c2[8]	rb_c2[7]	rb_c2[6]	rb_c2[5]	rb_c2[4]	rb_c2[3]
0x1E	0x00	csc_coeff_rb_20	r	rb_c2[2]	rb_c2[1]	rb_c2[0]	rb_c1[12]	rb_c1[11]	rb_c1[10]	rb_c1[9]	rb_c1[8]
0x1F	0x00	csc_coeff_rb_21	r	rb_c1[7]	rb_c1[6]	rb_c1[5]	rb_c1[4]	rb_c1[3]	rb_c1[2]	rb_c1[1]	rb_c1[0]
0x22	0x00	hs_pos_cntrl_1	rw	-	-	-	cp_start_hs[12]	cp_start_hs[11]	cp_start_hs[10]	cp_start_hs[9]	cp_start_hs[8]
0x23	0x00	hs_pos_cntrl_2	rw	cp_start_hs[7]	cp_start_hs[6]	cp_start_hs[5]	cp_start_hs[4]	cp_start_hs[3]	cp_start_hs[2]	cp_start_hs[1]	cp_start_hs[0]
0x24	0x00	hs_pos_cntrl_3	rw	-	-	-	cp_end_hs[12]	cp_end_hs[11]	cp_end_hs[10]	cp_end_hs[9]	cp_end_hs[8]
0x25	0x00	hs_pos_cntrl_4	rw	cp_end_hs[7]	cp_end_hs[6]	cp_end_hs[5]	cp_end_hs[4]	cp_end_hs[3]	cp_end_hs[2]	cp_end_hs[1]	cp_end_hs[0]
0x26	0x00	de_pos_cntrl_1	rw	-	-	-	cp_start_sav[12]	cp_start_sav[11]	cp_start_sav[10]	cp_start_sav[9]	cp_start_sav[8]
0x27	0x00	de_pos_cntrl_2	rw	cp_start_sav[7]	cp_start_sav[6]	cp_start_sav[5]	cp_start_sav[4]	cp_start_sav[3]	cp_start_sav[2]	cp_start_sav[1]	cp_start_sav[0]
0x28	0x00	de_pos_cntrl_3	rw	-	-	-	cp_start_eav[12]	cp_start_eav[11]	cp_start_eav[10]	cp_start_eav[9]	cp_start_eav[8]
0x29	0x00	de_pos_cntrl_4	rw	cp_start_eav[7]	cp_start_eav[6]	cp_start_eav[5]	cp_start_eav[4]	cp_start_eav[3]	cp_start_eav[2]	cp_start_eav[1]	cp_start_eav[0]
0x2A	0x00	de_pos_cntrl_5	rw	cp_start_vbi_r[11]	cp_start_vbi_r[10]	cp_start_vbi_r[9]	cp_start_vbi_r[8]	cp_start_vbi_r[7]	cp_start_vbi_r[6]	cp_start_vbi_r[5]	cp_start_vbi_r[4]
0x2B	0x00	de_pos_cntrl_6	rw	cp_start_vbi_r[3]	cp_start_vbi_r[2]	cp_start_vbi_r[1]	cp_start_vbi_r[0]	cp_end_vbi_r[11]	cp_end_vbi_r[10]	cp_end_vbi_r[9]	cp_end_vbi_r[8]
0x2C	0x00	de_pos_cntrl_7	rw	cp_end_vbi_r[7]	cp_end_vbi_r[6]	cp_end_vbi_r[5]	cp_end_vbi_r[4]	cp_end_vbi_r[3]	cp_end_vbi_r[2]	cp_end_vbi_r[1]	cp_end_vbi_r[0]
0x2D	0x00	de_pos_cntrl_8	rw	cp_start_vbi_even_r[11]	cp_start_vbi_even_r[10]	cp_start_vbi_even_r[9]	cp_start_vbi_even_r[8]	cp_start_vbi_even_r[7]	cp_start_vbi_even_r[6]	cp_start_vbi_even_r[5]	cp_start_vbi_even_r[4]
0x2E	0x00	de_pos_cntrl_9	rw	cp_start_vbi_even_r[3]	cp_start_vbi_even_r[2]	cp_start_vbi_even_r[1]	cp_start_vbi_even_r[0]	cp_end_vbi_even_r[11]	cp_end_vbi_even_r[10]	cp_end_vbi_even_r[9]	cp_end_vbi_even_r[8]
0x2F	0x00	de_pos_cntrl_10	rw	cp_end_vbi_even_r[7]	cp_end_vbi_even_r[6]	cp_end_vbi_even_r[5]	cp_end_vbi_even_r[4]	cp_end_vbi_even_r[3]	cp_end_vbi_even_r[2]	cp_end_vbi_even_r[1]	cp_end_vbi_even_r[0]
0x30	0x00	de_pos_adj_1	rw	de_v_start_r[3]	de_v_start_r[2]	de_v_start_r[1]	de_v_start_r[0]	de_v_end_r[3]	de_v_end_r[2]	de_v_end_r[1]	de_v_end_r[0]
0x31	0x00	de_pos_adj_2	rw	de_v_start_even_r[3]	de_v_start_even_r[2]	de_v_start_even_r[1]	de_v_start_even_r[0]	de_v_end_even_r[3]	de_v_end_even_r[2]	de_v_end_even_r[1]	de_v_end_even_r[0]
0x3A	0x80	contrast_cntrl	rw	cp_contrast[7]	cp_contrast[6]	cp_contrast[5]	cp_contrast[4]	cp_contrast[3]	cp_contrast[2]	cp_contrast[1]	cp_contrast[0]
0x3B	0x80	saturation_cntrl	rw	cp_saturation[7]	cp_saturation[6]	cp_saturation[5]	cp_saturation[4]	cp_saturation[3]	cp_saturation[2]	cp_saturation[1]	cp_saturation[0]
0x3C	0x00	brightness_cntrl	rw	cp_brightness[7]	cp_brightness[6]	cp_brightness[5]	cp_brightness[4]	cp_brightness[3]	cp_brightness[2]	cp_brightness[1]	cp_brightness[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x3D	0x00	hue_cntrl	rw	cp_hue[7]	cp_hue[6]	cp_hue[5]	cp_hue[4]	cp_hue[3]	cp_hue[2]	cp_hue[1]	cp_hue[0]
0x3E	0x00	vid_adj_0	rw	vid_adj_en	-	-	-	-	cp_mode_gain_adj_en	alt_sat_uv_man	alt_sat_uv
0x40	0x5C	cp_pre_gain_cntrl	rw	cp_mode_gain_adj[7]	cp_mode_gain_adj[6]	cp_mode_gain_adj[5]	cp_mode_gain_adj[4]	cp_mode_gain_adj[3]	cp_mode_gain_adj[2]	cp_mode_gain_adj[1]	cp_mode_gain_adj[0]
0x41	0x02	sync_det_cntrl_ch_2_1	rw	ch2_pol_man_en	ch2_pol_vs	ch2_pol_hscs	ch2_sync_src[1]	ch2_sync_src[0]	ch2_trig_sspd	ch2_sspd_cont	ch2_sspd_pp_en
0x42	0x3B	sync_det_cntrl_ch_2_2	rw	-	-	-	-	-	ch2_trig_stdi	ch2_stdi_cont	-
0x43	0xD4	sync_det_cntrl_ch_2_3	rw	-	-	ch2_fl_fr_threshold[2]	ch2_fl_fr_threshold[1]	ch2_fl_fr_threshold[0]	ch2_f_run_thr[2]	ch2_f_run_thr[1]	ch2_f_run_thr[0]
0x46	0x00	sync_det_cntrl_ch_2_6	rw	ch2_fr_field_lenh[11]	ch2_fr_field_lenh[10]	ch2_fr_field_lenh[9]	ch2_fr_field_lenh[8]	ch2_fr_field_lenh[7]	ch2_fr_field_lenh[6]	ch2_fr_field_lenh[5]	ch2_fr_field_lenh[4]
0x47	0x00	sync_det_cntrl_ch_2_7	rw	ch2_fr_field_lenh[3]	ch2_fr_field_lenh[2]	ch2_fr_field_lenh[1]	ch2_fr_field_lenh[0]	-	ch2_fr_II[10]	ch2_fr_II[9]	ch2_fr_II[8]
0x48	0x00	sync_det_cntrl_ch_2_8	rw	ch2_fr_II[7]	ch2_fr_II[6]	ch2_fr_II[5]	ch2_fr_II[4]	ch2_fr_II[3]	ch2_fr_II[2]	ch2_fr_II[1]	ch2_fr_II[0]
0x49	0x00	sync_det_cntrl_ch_2_rb_1	r	ch2_stdi_dvalid	ch2_stdi_intlcd	ch2_bl[13]	ch2_bl[12]	ch2_bl[11]	ch2_bl[10]	ch2_bl[9]	ch2_bl[8]
0x4A	0x00	sync_det_cntrl_ch_2_rb_2	r	ch2_bl[7]	ch2_bl[6]	ch2_bl[5]	ch2_bl[4]	ch2_bl[3]	ch2_bl[2]	ch2_bl[1]	ch2_bl[0]
0x4B	0x00	sync_det_cntrl_ch_2_rb_3	r	ch2_lcvs[4]	ch2_lcvs[3]	ch2_lcvs[2]	ch2_lcvs[1]	ch2_lcvs[0]	ch2_lcf[11]	ch2_lcf[10]	ch2_lcf[9]
0x4C	0x00	sync_det_cntrl_ch_2_rb_4	r	ch2_lcf[8]	ch2_lcf[7]	ch2_lcf[6]	ch2_lcf[5]	ch2_lcf[4]	ch2_lcf[3]	ch2_lcf[2]	ch2_lcf[1]
0x4D	0x00	sync_det_cntrl_ch_2_rb_5	r	ch2_lcf[0]	-	-	ch2_fcl[12]	ch2_fcl[11]	ch2_fcl[10]	ch2_fcl[9]	ch2_fcl[8]
0x4E	0x00	sync_det_cntrl_ch_2_rb_6	r	ch2_fcl[7]	ch2_fcl[6]	ch2_fcl[5]	ch2_fcl[4]	ch2_fcl[3]	ch2_fcl[2]	ch2_fcl[1]	ch2_fcl[0]
0x4F	0x00	sync_det_cntrl_ch_2_rb_7	r	ch2_sspd_dvalid	ch2_vs_act	ch2_cur_pol_vs	ch2_hs_act	ch2_cur_pol_hs	ch2_rs_active	ch2_cur_sync_src[1]	ch2_cur_sync_src[0]
0x52	0x40	csc_coefs_1	rw	csc_scale[1]	csc_scale[0]	-	a4[12]	a4[11]	a4[10]	a4[9]	a4[8]
0x53	0x00	csc_coefs_2	rw	a4[7]	a4[6]	a4[5]	a4[4]	a4[3]	a4[2]	a4[1]	a4[0]
0x54	0x00	csc_coefs_3	rw	-	a3[12]	a3[11]	a3[10]	a3[9]	a3[8]	a3[7]	a3[6]
0x55	0x00	csc_coefs_4	rw	a3[5]	a3[4]	a3[3]	a3[2]	a3[1]	a3[0]	a2[12]	a2[11]
0x56	0x00	csc_coefs_5	rw	a2[10]	a2[9]	a2[8]	a2[7]	a2[6]	a2[5]	a2[4]	a2[3]
0x57	0x08	csc_coefs_6	rw	a2[2]	a2[1]	a2[0]	a1[12]	a1[11]	a1[10]	a1[9]	a1[8]
0x58	0x00	csc_coefs_7	rw	a1[7]	a1[6]	a1[5]	a1[4]	a1[3]	a1[2]	a1[1]	a1[0]
0x59	0x00	csc_coefs_8	rw	-	-	-	b4[12]	b4[11]	b4[10]	b4[9]	b4[8]
0x5A	0x00	csc_coefs_9	rw	b4[7]	b4[6]	b4[5]	b4[4]	b4[3]	b4[2]	b4[1]	b4[0]
0x5B	0x00	csc_coefs_10	rw	-	b3[12]	b3[11]	b3[10]	b3[9]	b3[8]	b3[7]	b3[6]
0x5C	0x01	csc_coefs_11	rw	b3[5]	b3[4]	b3[3]	b3[2]	b3[1]	b3[0]	b2[12]	b2[11]
0x5D	0x00	csc_coefs_12	rw	b2[10]	b2[9]	b2[8]	b2[7]	b2[6]	b2[5]	b2[4]	b2[3]
0x5E	0x00	csc_coefs_13	rw	b2[2]	b2[1]	b2[0]	b1[12]	b1[11]	b1[10]	b1[9]	b1[8]
0x5F	0x00	csc_coefs_14	rw	b1[7]	b1[6]	b1[5]	b1[4]	b1[3]	b1[2]	b1[1]	b1[0]
0x60	0x00	csc_coefs_15	rw	-	-	-	c4[12]	c4[11]	c4[10]	c4[9]	c4[8]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x61	0x00	csc_coeffs_16	rw	c4[7]	c4[6]	c4[5]	c4[4]	c4[3]	c4[2]	c4[1]	c4[0]
0x62	0x20	csc_coeffs_17	rw	-	c3[12]	c3[11]	c3[10]	c3[9]	c3[8]	c3[7]	c3[6]
0x63	0x00	csc_coeffs_18	rw	c3[5]	c3[4]	c3[3]	c3[2]	c3[1]	c3[0]	c2[12]	c2[11]
0x64	0x00	csc_coeffs_19	rw	c2[10]	c2[9]	c2[8]	c2[7]	c2[6]	c2[5]	c2[4]	c2[3]
0x65	0x00	csc_coeffs_20	rw	c2[2]	c2[1]	c2[0]	c1[12]	c1[11]	c1[10]	c1[9]	c1[8]
0x66	0x00	csc_coeffs_21	rw	c1[7]	c1[6]	c1[5]	c1[4]	c1[3]	c1[2]	c1[1]	c1[0]
0x67	0x00	emb_sync_status	rw	-	-	emb_sync_on_all	-	-	-	-	-
0x68	0xF0	csc_decim_cntrl	rw	csc_coeff_sel[3]	csc_coeff_sel[2]	csc_coeff_sel[1]	csc_coeff_sel[0]	-	-	-	-
0x69	0x04	vid_adj_1	rw	-	-	-	man_cp_csc_en	-	eia_861_compliance	-	-
0x6C	0x10	clmp_cntrl_1	rw	clmp_a_man	clmp_bc_man	clmp_freeze	-	clmp_a[11]	clmp_a[10]	clmp_a[9]	clmp_a[8]
0x6D	0x00	clmp_cntrl_2	rw	clmp_a[7]	clmp_a[6]	clmp_a[5]	clmp_a[4]	clmp_a[3]	clmp_a[2]	clmp_a[1]	clmp_a[0]
0x6E	0x00	clmp_cntrl_3	rw	clmp_b[11]	clmp_b[10]	clmp_b[9]	clmp_b[8]	clmp_b[7]	clmp_b[6]	clmp_b[5]	clmp_b[4]
0x6F	0x00	clmp_cntrl_4	rw	clmp_b[3]	clmp_b[2]	clmp_b[1]	clmp_b[0]	clmp_c[11]	clmp_c[10]	clmp_c[9]	clmp_c[8]
0x70	0x00	clmp_cntrl_5	rw	clmp_c[7]	clmp_c[6]	clmp_c[5]	clmp_c[4]	clmp_c[3]	clmp_c[2]	clmp_c[1]	clmp_c[0]
0x71	0x00	gain_cntrl_1	rw	agc_tar[9]	agc_tar[8]	agc_tar_man	agc_freeze	hs_norm	agc_tim[2]	agc_tim[1]	agc_tim[0]
0x72	0x00	gain_cntrl_2	rw	agc_tar[7]	agc_tar[6]	agc_tar[5]	agc_tar[4]	agc_tar[3]	agc_tar[2]	agc_tar[1]	agc_tar[0]
0x73	0x10	gain_cntrl_3	rw	gain_man	agc_mode_man	a_gain[9]	a_gain[8]	a_gain[7]	a_gain[6]	a_gain[5]	a_gain[4]
0x74	0x04	gain_cntrl_4	rw	a_gain[3]	a_gain[2]	a_gain[1]	a_gain[0]	b_gain[9]	b_gain[8]	b_gain[7]	b_gain[6]
0x75	0x01	gain_cntrl_5	rw	b_gain[5]	b_gain[4]	b_gain[3]	b_gain[2]	b_gain[1]	b_gain[0]	c_gain[9]	c_gain[8]
0x76	0x00	gain_cntrl_6	rw	c_gain[7]	c_gain[6]	c_gain[5]	c_gain[4]	c_gain[3]	c_gain[2]	c_gain[1]	c_gain[0]
0x77	0xFF	offset_cntrl_1	rw	-	-	a_offset[9]	a_offset[8]	a_offset[7]	a_offset[6]	a_offset[5]	a_offset[4]
0x78	0xFF	offset_cntrl_2	rw	a_offset[3]	a_offset[2]	a_offset[1]	a_offset[0]	b_offset[9]	b_offset[8]	b_offset[7]	b_offset[6]
0x79	0xFF	offset_cntrl_3	rw	b_offset[5]	b_offset[4]	b_offset[3]	b_offset[2]	b_offset[1]	b_offset[0]	c_offset[9]	c_offset[8]
0x7A	0xFF	offset_cntrl_4	rw	c_offset[7]	c_offset[6]	c_offset[5]	c_offset[4]	c_offset[3]	c_offset[2]	c_offset[1]	c_offset[0]
0x7C	0xC0	sync_cntrl_1	rw	cp_inv_hs	cp_inv_vs	-	cp_inv_de	start_hs[9]	start_hs[8]	end_hs[9]	end_hs[8]
0x7D	0x00	sync_cntrl_2	rw	end_hs[7]	end_hs[6]	end_hs[5]	end_hs[4]	end_hs[3]	end_hs[2]	end_hs[1]	end_hs[0]
0x7E	0x00	sync_cntrl_3	rw	start_hs[7]	start_hs[6]	start_hs[5]	start_hs[4]	start_hs[3]	start_hs[2]	start_hs[1]	start_hs[0]
0x7F	0x00	sync_cntrl_4	rw	start_vs[3]	start_vs[2]	start_vs[1]	start_vs[0]	end_vs[3]	end_vs[2]	end_vs[1]	end_vs[0]
0x81	0xC0	noise_calib_1	rw	meas_wl[1]	meas_wl[0]	-	gr_av_bl_en	meas_ws[11]	meas_ws[10]	meas_ws[9]	meas_ws[8]
0x82	0x04	noise_calib_2	rw	meas_ws[7]	meas_ws[6]	meas_ws[5]	meas_ws[4]	meas_ws[3]	meas_ws[2]	meas_ws[1]	meas_ws[0]
0x83	0x00	cp_reg_83	rw	isd_thr[7]	isd_thr[6]	isd_thr[5]	isd_thr[4]	isd_thr[3]	isd_thr[2]	isd_thr[1]	isd_thr[0]
0x84	0x0C	sync_det_cntrl_ch_1_1	rw	cp_gain_filt[3]	cp_gain_filt[2]	cp_gain_filt[1]	cp_gain_filt[0]	-	-	ch1_sspd_pp_en	ifsd_avg
0x85	0x03	sync_det_cntrl_ch_1_2	rw	ch1_pol_man_en	ch1_pol_vs	ch1_pol_hscs	ch1_sync_src[1]	ch1_sync_src[0]	ch1_trig_sspd	ch1_sspd_cont	-
0x86	0x0B	sync_det_cntrl_ch_1_3	rw	-	-	-	-	-	ch1_trig_stdi	ch1_stdi_cont	-
0x87	0x00	de_pos_adj_4	rw	-	-	de_v_start_even[5]	de_v_start_even[4]	de_v_start_even[3]	de_v_start_even[2]	de_v_start_even[1]	de_v_start_even[0]
0x88	0x00	de_pos_adj_5	rw	-	-	de_v_end_even[5]	de_v_end_even[4]	de_v_end_even[3]	de_v_end_even[2]	de_v_end_even[1]	de_v_end_even[0]
0x89	0x00	sync_cntrl_6	rw	start_vs_even[3]	start_vs_even[2]	start_vs_even[1]	start_vs_even[0]	end_vs_even[3]	end_vs_even[2]	end_vs_even[1]	end_vs_even[0]
0x8A	0x20	clmp_cntrl_6	rw	ignr_clmp_vs_mar_end[4]	ignr_clmp_vs_mar_end[3]	ignr_clmp_vs_mar_end[2]	ignr_clmp_vs_mar_end[1]	ignr_clmp_vs_mar_end[0]	-	-	ignr_clmp_vs_mar_start[4]
0x8B	0x40	de_pos_adj_6	rw	ignr_clmp_vs_mar_start[3]	ignr_clmp_vs_mar_start[2]	ignr_clmp_vs_mar_start[1]	ignr_clmp_vs_mar_start[0]	de_h_start[9]	de_h_start[8]	de_h_end[9]	de_h_end[8]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x8C	0x00	de_pos_adj_7	rw	de_h_end[7]	de_h_end[6]	de_h_end[5]	de_h_end[4]	de_h_end[3]	de_h_end[2]	de_h_end[1]	de_h_end[0]
0x8D	0x00	de_pos_adj_8	rw	de_h_start[7]	de_h_start[6]	de_h_start[5]	de_h_start[4]	de_h_start[3]	de_h_start[2]	de_h_start[1]	de_h_start[0]
0x8F	0x00	sync_det_cntrl_ch 1_4_1	rw	-	-	-	-	-	ch1_fr_II[10]	ch1_fr_II[9]	ch1_fr_II[8]
0x90	0x00	sync_det_cntrl_ch 1_4_2	rw	ch1_fr_II[7]	ch1_fr_II[6]	ch1_fr_II[5]	ch1_fr_II[4]	ch1_fr_II[3]	ch1_fr_II[2]	ch1_fr_II[1]	ch1_fr_II[0]
0x91	0x40	vid_adj_2	rw	man_parm	interlaced	-	-	-	-	-	-
0x98	0x00	de_pos_adj_9	rw	-	-	de_v_start[5]	de_v_start[4]	de_v_start[3]	de_v_start[2]	de_v_start[1]	de_v_start[0]
0x99	0x00	de_pos_adj_10	rw	-	-	de_v_end[5]	de_v_end[4]	de_v_end[3]	de_v_end[2]	de_v_end[1]	de_v_end[0]
0x9A	0x00	vs_pos_cntrl_1	rw	-	-	cp_start_vs[5]	cp_start_vs[4]	cp_start_vs[3]	cp_start_vs[2]	cp_start_vs[1]	cp_start_vs[0]
0x9B	0x00	vs_pos_cntrl_2	rw	-	-	cp_end_vs[5]	cp_end_vs[4]	cp_end_vs[3]	cp_end_vs[2]	cp_end_vs[1]	cp_end_vs[0]
0x9C	0x00	vs_pos_cntrl_3	rw	-	cp_start_vs_even[10]	cp_start_vs_even[9]	cp_start_vs_even[8]	cp_start_vs_even[7]	cp_start_vs_even[6]	cp_start_vs_even[5]	cp_start_vs_even[4]
0x9D	0x00	vs_pos_cntrl_4	rw	cp_start_vs_even[3]	cp_start_vs_even[2]	cp_start_vs_even[1]	cp_start_vs_even[0]	-	cp_end_vs_even[10]	cp_end_vs_even[9]	cp_end_vs_even[8]
0x9E	0x00	vs_pos_cntrl_5	rw	cp_end_vs_even[7]	cp_end_vs_even[6]	cp_end_vs_even[5]	cp_end_vs_even[4]	cp_end_vs_even[3]	cp_end_vs_even[2]	cp_end_vs_even[1]	cp_end_vs_even[0]
0x9F	0x00	fld_pos_cntrl_1	rw	cp_start_f_odd[10]	cp_start_f_odd[9]	cp_start_f_odd[8]	cp_start_f_odd[7]	cp_start_f_odd[6]	cp_start_f_odd[5]	cp_start_f_odd[4]	cp_start_f_odd[3]
0xA0	0x00	fld_pos_cntrl_2	rw	cp_start_f_odd[2]	cp_start_f_odd[1]	cp_start_f_odd[0]	cp_start_f_even[1 0]	cp_start_f_even[9]	cp_start_f_even[8]	cp_start_f_even[7]	cp_start_f_even[6]
0xA1	0x00	fld_pos_cntrl_3	rw	cp_start_f_even[5]	cp_start_f_even[4]	cp_start_f_even[3]	cp_start_f_even[2]	cp_start_f_even[1]	cp_start_f_even[0]	-	-
0xA3	0x00	sync_det_cntrl_ch 1_rb_1	r	-	-	-	-	ch1_lcf[11]	ch1_lcf[10]	ch1_lcf[9]	ch1_lcf[8]
0xA4	0x00	sync_det_cntrl_ch 1_rb_2	r	ch1_lcf[7]	ch1_lcf[6]	ch1_lcf[5]	ch1_lcf[4]	ch1_lcf[3]	ch1_lcf[2]	ch1_lcf[1]	ch1_lcf[0]
0xA5	0x00	vbi_pos_cntrl_1	rw	cp_start_vbi[11]	cp_start_vbi[10]	cp_start_vbi[9]	cp_start_vbi[8]	cp_start_vbi[7]	cp_start_vbi[6]	cp_start_vbi[5]	cp_start_vbi[4]
0xA6	0x00	vbi_pos_cntrl_2	rw	cp_start_vbi[3]	cp_start_vbi[2]	cp_start_vbi[1]	cp_start_vbi[0]	cp_end_vbi[11]	cp_end_vbi[10]	cp_end_vbi[9]	cp_end_vbi[8]
0xA7	0x00	vbi_pos_cntrl_3	rw	cp_end_vbi[7]	cp_end_vbi[6]	cp_end_vbi[5]	cp_end_vbi[4]	cp_end_vbi[3]	cp_end_vbi[2]	cp_end_vbi[1]	cp_end_vbi[0]
0xA8	0x00	vbi_pos_cntrl_4	rw	cp_start_vbi_even [11]	cp_start_vbi_even [10]	cp_start_vbi_even [9]	cp_start_vbi_even [8]	cp_start_vbi_even [7]	cp_start_vbi_even [6]	cp_start_vbi_even [5]	cp_start_vbi_even [4]
0xA9	0x00	vbi_pos_cntrl_5	rw	cp_start_vbi_even [3]	cp_start_vbi_even [2]	cp_start_vbi_even [1]	cp_start_vbi_even [0]	cp_end_vbi_even[11]	cp_end_vbi_even[10]	cp_end_vbi_even[9]	cp_end_vbi_even[8]
0xAA	0x00	vbi_pos_cntrl_6	rw	cp_end_vbi_even[7]	cp_end_vbi_even[6]	cp_end_vbi_even[5]	cp_end_vbi_even[4]	cp_end_vbi_even[3]	cp_end_vbi_even[2]	cp_end_vbi_even[1]	cp_end_vbi_even[0]
0xAB	0x00	sync_det_cntrl_ch 1_4	rw	cp_lcount_max[11]	cp_lcount_max[10]	cp_lcount_max[9]	cp_lcount_max[8]	cp_lcount_max[7]	cp_lcount_max[6]	cp_lcount_max[5]	cp_lcount_max[4]
0xAC	0x00	sync_det_cntrl_ch 1_5	rw	cp_lcount_max[3]	cp_lcount_max[2]	cp_lcount_max[1]	cp_lcount_max[0]	-	-	-	-
0xB1	0x00	sync_det_cntrl_ch 1_rb_3	r	ch1_stdv_dvalid	ch1_stdv_intlcd	ch1_bl[13]	ch1_bl[12]	ch1_bl[11]	ch1_bl[10]	ch1_bl[9]	ch1_bl[8]
0xB2	0x00	sync_det_cntrl_ch 1_rb_4	r	ch1_bl[7]	ch1_bl[6]	ch1_bl[5]	ch1_bl[4]	ch1_bl[3]	ch1_bl[2]	ch1_bl[1]	ch1_bl[0]
0xB3	0x00	sync_det_cntrl_ch 1_rb_5	r	ch1_lcv[4]	ch1_lcv[3]	ch1_lcv[2]	ch1_lcv[1]	ch1_lcv[0]	-	-	-

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xB5	0x00	sync_det_cntrl_ch1_rb_6	r	ch1_sspd_dvalid	ch1_vs_act	ch1_cur_pol_vs	ch1_hs_act	ch1_cur_pol_hs	ch1_rs_active	ch1_cur_sync_src[1]	ch1_cur_sync_src[0]
0xB8	0x00	sync_det_cntrl_ch1_rb_6_1	r	-	-	-	ch1_fcl[12]	ch1_fcl[11]	ch1_fcl[10]	ch1_fcl[9]	ch1_fcl[8]
0xB9	0x00	sync_det_cntrl_ch1_rb_6_2	r	ch1_fcl[7]	ch1_fcl[6]	ch1_fcl[5]	ch1_fcl[4]	ch1_fcl[3]	ch1_fcl[2]	ch1_fcl[1]	ch1_fcl[0]
0xBA	0x01	hdmi_cp_cntrl_1	rw	-	-	-	-	-	-	hdmi_frun_mode	hdmi_frun_en
0xBE	0x04	dly_adj	rw	dly_a	dly_b	dly_c	-	-	-	hcount_align_adj[4]	hcount_align_adj[3]
0xBF	0x12	fr_color_sel_1	rw	hcount_align_adj[2]	hcount_align_adj[1]	hcount_align_adj[0]	-	-	cp_def_col_man_val	cp_def_col_auto	cp_force_freerun
0xC0	0x00	fr_color_sel_2	rw	def_col_cha[7]	def_col_cha[6]	def_col_cha[5]	def_col_cha[4]	def_col_cha[3]	def_col_cha[2]	def_col_cha[1]	def_col_cha[0]
0xC1	0x00	fr_color_sel_3	rw	def_col_chb[7]	def_col_chb[6]	def_col_chb[5]	def_col_chb[4]	def_col_chb[3]	def_col_chb[2]	def_col_chb[1]	def_col_chb[0]
0xC2	0x00	fr_color_sel_4	rw	def_col_chc[7]	def_col_chc[6]	def_col_chc[5]	def_col_chc[4]	def_col_chc[3]	def_col_chc[2]	def_col_chc[1]	def_col_chc[0]
0xC5	0x91	dfc_clmp_cntrl	rw	clamp_avg_fctr[1]	clamp_avg_fctr[0]	-	-	-	-	-	-
0xC6	0x00	clmp_pos_cntrl_1	rw	cp_anvc_pos_start[7]	cp_anvc_pos_start[6]	cp_anvc_pos_start[5]	cp_anvc_pos_start[4]	cp_anvc_pos_start[3]	cp_anvc_pos_start[2]	cp_anvc_pos_start[1]	cp_anvc_pos_start[0]
0xC7	0x00	clmp_pos_cntrl_2	rw	cp_anvc_pos_duration[7]	cp_anvc_pos_duration[6]	cp_anvc_pos_duration[5]	cp_anvc_pos_duration[4]	cp_anvc_pos_duration[3]	cp_anvc_pos_duration[2]	cp_anvc_pos_duration[1]	cp_anvc_pos_duration[0]
0xC8	0x00	clmp_pos_cntrl_3	rw	cp_dfc_pos_start[7]	cp_dfc_pos_start[6]	cp_dfc_pos_start[5]	cp_dfc_pos_start[4]	cp_dfc_pos_start[3]	cp_dfc_pos_start[2]	cp_dfc_pos_start[1]	cp_dfc_pos_start[0]
0xC9	0x2C	clmp_pos_cntrl_4	rw	cp_anvc_pos_start[12]	cp_dfc_pos_start[12]	-	-	-	-	-	dis_auto_param_buff
0xCA	0x00	clmp_pos_cntrl_5	rw	cp_anvc_pos_start[11]	cp_anvc_pos_start[10]	cp_anvc_pos_start[9]	cp_anvc_pos_start[8]	cp_dfc_pos_start[11]	cp_dfc_pos_start[10]	cp_dfc_pos_start[9]	cp_dfc_pos_start[8]
0xCB	0x60	hdmi_cp_cntrl_2	rw	-	-	-	-	-	-	hdmi_cp_lock_threshold[1]	hdmi_cp_lock_threshold[0]
0xDA	0x00	peak_white_agc_cntrl_1	rw	-	-	-	-	-	-	pw_win_man	pw_show_win
0xDB	0x19	peak_white_agc_cntrl_2	rw	pw_vb[7]	pw_vb[6]	pw_vb[5]	pw_vb[4]	pw_vb[3]	pw_vb[2]	pw_vb[1]	pw_vb[0]
0xDC	0x64	peak_white_agc_cntrl_3	rw	pw_vl[7]	pw_vl[6]	pw_vl[5]	pw_vl[4]	pw_vl[3]	pw_vl[2]	pw_vl[1]	pw_vl[0]
0xDD	0x12	peak_white_agc_cntrl_4	rw	pw_hb[11]	pw_hb[10]	pw_hb[9]	pw_hb[8]	pw_hb[7]	pw_hb[6]	pw_hb[5]	pw_hb[4]
0xDE	0xC5	peak_white_agc_cntrl_5	rw	pw_hb[3]	pw_hb[2]	pw_hb[1]	pw_hb[0]	pw_hl[11]	pw_hl[10]	pw_hl[9]	pw_hl[8]
0xDF	0x78	peak_white_agc_cntrl_6	rw	pw_hl[7]	pw_hl[6]	pw_hl[5]	pw_hl[4]	pw_hl[3]	pw_hl[2]	pw_hl[1]	pw_hl[0]
0xE0	0x00	status_0_1	r	-	hdmi_cp_autoparm_locked	hdmi_autoparm_ts[1]	hdmi_autoparm_ts[0]	-	-	cp_agc_gain[9]	cp_agc_gain[8]
0xE1	0x00	status_0_2	r	cp_agc_gain[7]	cp_agc_gain[6]	cp_agc_gain[5]	cp_agc_gain[4]	cp_agc_gain[3]	cp_agc_gain[2]	cp_agc_gain[1]	cp_agc_gain[0]
0xE2	0x00	noise_calib_rb	r	noise[7]	noise[6]	noise[5]	noise[4]	noise[3]	noise[2]	noise[1]	noise[0]
0xE3	0x00	cp_reg_e3	r	-	-	-	calib[10]	calib[9]	calib[8]	ifsd[8]	isd[8]
0xE4	0x00		r	isd[7]	isd[6]	isd[5]	isd[4]	isd[3]	isd[2]	isd[1]	isd[0]
0xE5	0x00	cp_reg_e5	r	ifsd[7]	ifsd[6]	ifsd[5]	ifsd[4]	ifsd[3]	ifsd[2]	ifsd[1]	ifsd[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xE6	0x00	cp_reg_e6	r	calib[7]	calib[6]	calib[5]	calib[4]	calib[3]	calib[2]	calib[1]	calib[0]
0xE7	0x00	hsync_depth_rb_1	r	-	-	hsd_chc[9]	hsd_chc[8]	hsd_chb[9]	hsd_chb[8]	hsd_cha[9]	hsd_cha[8]
0xE8	0x00	hsync_depth_rb_2	r	hsd_cha[7]	hsd_cha[6]	hsd_cha[5]	hsd_cha[4]	hsd_cha[3]	hsd_cha[2]	hsd_cha[1]	hsd_cha[0]
0xE9	0x00	hsync_depth_rb_3	r	hsd_chb[7]	hsd_chb[6]	hsd_chb[5]	hsd_chb[4]	hsd_chb[3]	hsd_chb[2]	hsd_chb[1]	hsd_chb[0]
0xEA	0x00	hsync_depth_rb_4	r	hsd_chc[7]	hsd_chc[6]	hsd_chc[5]	hsd_chc[4]	hsd_chc[3]	hsd_chc[2]	hsd_chc[1]	hsd_chc[0]
0xEB	0x00	hsync_depth_rb_5	r	-	-	-	-	hsd_fb[11]	hsd_fb[10]	hsd_fb[9]	hsd_fb[8]
0xEC	0x00	hsync_depth_rb_6	r	hsd_fb[7]	hsd_fb[6]	hsd_fb[5]	hsd_fb[4]	hsd_fb[3]	hsd_fb[2]	hsd_fb[1]	hsd_fb[0]
0xED	0x00	peak_white_rb_1	r	-	-	pkv_cha[9]	pkv_cha[8]	pkv_chb[9]	pkv_chb[8]	pkv_chc[9]	pkv_chc[8]
0xEE	0x00	peak_white_rb_2	r	pkv_cha[7]	pkv_cha[6]	pkv_cha[5]	pkv_cha[4]	pkv_cha[3]	pkv_cha[2]	pkv_cha[1]	pkv_cha[0]
0xEF	0x00	peak_white_rb_3	r	pkv_chb[7]	pkv_chb[6]	pkv_chb[5]	pkv_chb[4]	pkv_chb[3]	pkv_chb[2]	pkv_chb[1]	pkv_chb[0]
0xF0	0x00	peak_white_rb_4	r	pkv_chc[7]	pkv_chc[6]	pkv_chc[5]	pkv_chc[4]	pkv_chc[3]	pkv_chc[2]	pkv_chc[1]	pkv_chc[0]
0xF3	0xD4	sync_det_cntrl_ch1_6	rw	-	-	ch1_fl_fr_threshold[2]	ch1_fl_fr_threshold[1]	ch1_fl_fr_threshold[0]	ch1_f_run_thr[2]	ch1_f_run_thr[1]	ch1_f_run_thr[0]
0xF4	0x00	csc_coeff_sel_rb	r	csc_coeff_sel_rb[3]	csc_coeff_sel_rb[2]	csc_coeff_sel_rb[1]	csc_coeff_sel_rb[0]	-	-	-	-
0xF5	0x00	vid_adj_3	rw	-	-	-	wd_timer_dis	dig_sync_deglitch_reduce	dig_sync_deglitch_reduce_man	bypass_std1_locking	bypass_std2_locking
0xFF	0x00	cp_reg_ff	r	mv_ps_det	mv_agc_det	-	cp_free_run	-	-	-	-

1.5 ADDR 48 (VDP)

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x3C	0x00	vdp_cgms_typeb_data_1	r	vdp_cgms_typeb_data[7]	vdp_cgms_typeb_data[6]	vdp_cgms_typeb_data[5]	vdp_cgms_typeb_data[4]	vdp_cgms_typeb_data[3]	vdp_cgms_typeb_data[2]	vdp_cgms_typeb_data[1]	vdp_cgms_typeb_data[0]
0x3D	0x00	vdp_cgms_typeb_data_2	r	vdp_cgms_typeb_data[15]	vdp_cgms_typeb_data[14]	vdp_cgms_typeb_data[13]	vdp_cgms_typeb_data[12]	vdp_cgms_typeb_data[11]	vdp_cgms_typeb_data[10]	vdp_cgms_typeb_data[9]	vdp_cgms_typeb_data[8]
0x3E	0x00	vdp_cgms_typeb_data_3	r	vdp_cgms_typeb_data[23]	vdp_cgms_typeb_data[22]	vdp_cgms_typeb_data[21]	vdp_cgms_typeb_data[20]	vdp_cgms_typeb_data[19]	vdp_cgms_typeb_data[18]	vdp_cgms_typeb_data[17]	vdp_cgms_typeb_data[16]
0x3F	0x00	vdp_cgms_typeb_data_4	r	vdp_cgms_typeb_data[31]	vdp_cgms_typeb_data[30]	vdp_cgms_typeb_data[29]	vdp_cgms_typeb_data[28]	vdp_cgms_typeb_data[27]	vdp_cgms_typeb_data[26]	vdp_cgms_typeb_data[25]	vdp_cgms_typeb_data[24]
0x40	0x00	vdp_status	r	vdp_status_ttxt	vdp_status_vitc	vdp_status_gems_type	vdp_status_gs_vps_pdc_utc_cgmstb	-	vdp_status_wss_cgms	vdp_status_ccap_even_field	vdp_status_ccap
0x41	0x00	vdp_ccap_data_1	r	vdp_ccap_data[7]	vdp_ccap_data[6]	vdp_ccap_data[5]	vdp_ccap_data[4]	vdp_ccap_data[3]	vdp_ccap_data[2]	vdp_ccap_data[1]	vdp_ccap_data[0]
0x42	0x00	vdp_ccap_data_2	r	vdp_ccap_data[15]	vdp_ccap_data[14]	vdp_ccap_data[13]	vdp_ccap_data[12]	vdp_ccap_data[11]	vdp_ccap_data[10]	vdp_ccap_data[9]	vdp_ccap_data[8]
0x43	0x00	vdp_cgms_wss_data_1	r	vdp_cgms_wss_data[23]	vdp_cgms_wss_data[22]	vdp_cgms_wss_data[21]	vdp_cgms_wss_data[20]	vdp_cgms_wss_data[19]	vdp_cgms_wss_data[18]	vdp_cgms_wss_data[17]	vdp_cgms_wss_data[16]
0x44	0x00	vdp_cgms_wss_data_2	r	vdp_cgms_wss_data[15]	vdp_cgms_wss_data[14]	vdp_cgms_wss_data[13]	vdp_cgms_wss_data[12]	vdp_cgms_wss_data[11]	vdp_cgms_wss_data[10]	vdp_cgms_wss_data[9]	vdp_cgms_wss_data[8]
0x45	0x00	vdp_cgms_wss_data_3	r	vdp_cgms_wss_data[7]	vdp_cgms_wss_data[6]	vdp_cgms_wss_data[5]	vdp_cgms_wss_data[4]	vdp_cgms_wss_data[3]	vdp_cgms_wss_data[2]	vdp_cgms_wss_data[1]	vdp_cgms_wss_data[0]
0x47	0x00	vdp_gs_vps_pdc_utc_cgmstb_data_1	r	vdp_gs_vps_pdc_utc_cgmstb_data[7]	vdp_gs_vps_pdc_utc_cgmstb_data[6]	vdp_gs_vps_pdc_utc_cgmstb_data[5]	vdp_gs_vps_pdc_utc_cgmstb_data[4]	vdp_gs_vps_pdc_utc_cgmstb_data[3]	vdp_gs_vps_pdc_utc_cgmstb_data[2]	vdp_gs_vps_pdc_utc_cgmstb_data[1]	vdp_gs_vps_pdc_utc_cgmstb_data[0]
0x48	0x00	vdp_gs_vps_pdc_utc_cgmstb_data_2	r	vdp_gs_vps_pdc_utc_cgmstb_data[15]	vdp_gs_vps_pdc_utc_cgmstb_data[14]	vdp_gs_vps_pdc_utc_cgmstb_data[13]	vdp_gs_vps_pdc_utc_cgmstb_data[12]	vdp_gs_vps_pdc_utc_cgmstb_data[11]	vdp_gs_vps_pdc_utc_cgmstb_data[10]	vdp_gs_vps_pdc_utc_cgmstb_data[9]	vdp_gs_vps_pdc_utc_cgmstb_data[8]
0x49	0x00	vdp_gs_vps_pdc_utc_cgmstb_data_3	r	vdp_gs_vps_pdc_utc_cgmstb_data[23]	vdp_gs_vps_pdc_utc_cgmstb_data[22]	vdp_gs_vps_pdc_utc_cgmstb_data[21]	vdp_gs_vps_pdc_utc_cgmstb_data[20]	vdp_gs_vps_pdc_utc_cgmstb_data[19]	vdp_gs_vps_pdc_utc_cgmstb_data[18]	vdp_gs_vps_pdc_utc_cgmstb_data[17]	vdp_gs_vps_pdc_utc_cgmstb_data[16]
0x4A	0x00	vdp_gs_vps_pdc_utc_cgmstb_data_4	r	vdp_gs_vps_pdc_utc_cgmstb_data[31]	vdp_gs_vps_pdc_utc_cgmstb_data[30]	vdp_gs_vps_pdc_utc_cgmstb_data[29]	vdp_gs_vps_pdc_utc_cgmstb_data[28]	vdp_gs_vps_pdc_utc_cgmstb_data[27]	vdp_gs_vps_pdc_utc_cgmstb_data[26]	vdp_gs_vps_pdc_utc_cgmstb_data[25]	vdp_gs_vps_pdc_utc_cgmstb_data[24]
0x4B	0x00	vdp_gs_vps_pdc_utc_cgmstb_data_5	r	vdp_gs_vps_pdc_utc_cgmstb_data[39]	vdp_gs_vps_pdc_utc_cgmstb_data[38]	vdp_gs_vps_pdc_utc_cgmstb_data[37]	vdp_gs_vps_pdc_utc_cgmstb_data[36]	vdp_gs_vps_pdc_utc_cgmstb_data[35]	vdp_gs_vps_pdc_utc_cgmstb_data[34]	vdp_gs_vps_pdc_utc_cgmstb_data[33]	vdp_gs_vps_pdc_utc_cgmstb_data[32]
0x4C	0x00	vdp_gs_vps_pdc_utc_cgmstb_data_6	r	vdp_gs_vps_pdc_utc_cgmstb_data[47]	vdp_gs_vps_pdc_utc_cgmstb_data[46]	vdp_gs_vps_pdc_utc_cgmstb_data[45]	vdp_gs_vps_pdc_utc_cgmstb_data[44]	vdp_gs_vps_pdc_utc_cgmstb_data[43]	vdp_gs_vps_pdc_utc_cgmstb_data[42]	vdp_gs_vps_pdc_utc_cgmstb_data[41]	vdp_gs_vps_pdc_utc_cgmstb_data[40]
0x4D	0x00	vdp_gs_vps_pdc_utc_cgmstb_data_7	r	vdp_gs_vps_pdc_utc_cgmstb_data[55]	vdp_gs_vps_pdc_utc_cgmstb_data[54]	vdp_gs_vps_pdc_utc_cgmstb_data[53]	vdp_gs_vps_pdc_utc_cgmstb_data[52]	vdp_gs_vps_pdc_utc_cgmstb_data[51]	vdp_gs_vps_pdc_utc_cgmstb_data[50]	vdp_gs_vps_pdc_utc_cgmstb_data[49]	vdp_gs_vps_pdc_utc_cgmstb_data[48]
0x4E	0x00	vdp_gs_vps_pdc_utc_cgmstb_data_8	r	vdp_gs_vps_pdc_utc_cgmstb_data[63]	vdp_gs_vps_pdc_utc_cgmstb_data[62]	vdp_gs_vps_pdc_utc_cgmstb_data[61]	vdp_gs_vps_pdc_utc_cgmstb_data[60]	vdp_gs_vps_pdc_utc_cgmstb_data[59]	vdp_gs_vps_pdc_utc_cgmstb_data[58]	vdp_gs_vps_pdc_utc_cgmstb_data[57]	vdp_gs_vps_pdc_utc_cgmstb_data[56]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x4F	0x00	vdp_gs_vps_pdc_UTC_cgmstb_data_9	r	vdp_gs_vps_pdc_UTC_cgmstb_data[71]	vdp_gs_vps_pdc_UTC_cgmstb_data[70]	vdp_gs_vps_pdc_UTC_cgmstb_data[69]	vdp_gs_vps_pdc_UTC_cgmstb_data[68]	vdp_gs_vps_pdc_UTC_cgmstb_data[67]	vdp_gs_vps_pdc_UTC_cgmstb_data[66]	vdp_gs_vps_pdc_UTC_cgmstb_data[65]	vdp_gs_vps_pdc_UTC_cgmstb_data[64]
0x50	0x00	vdp_gs_vps_pdc_UTC_cgmstb_data_10	r	vdp_gs_vps_pdc_UTC_cgmstb_data[79]	vdp_gs_vps_pdc_UTC_cgmstb_data[78]	vdp_gs_vps_pdc_UTC_cgmstb_data[77]	vdp_gs_vps_pdc_UTC_cgmstb_data[76]	vdp_gs_vps_pdc_UTC_cgmstb_data[75]	vdp_gs_vps_pdc_UTC_cgmstb_data[74]	vdp_gs_vps_pdc_UTC_cgmstb_data[73]	vdp_gs_vps_pdc_UTC_cgmstb_data[72]
0x51	0x00	vdp_gs_vps_pdc_UTC_cgmstb_data_11	r	vdp_gs_vps_pdc_UTC_cgmstb_data[87]	vdp_gs_vps_pdc_UTC_cgmstb_data[86]	vdp_gs_vps_pdc_UTC_cgmstb_data[85]	vdp_gs_vps_pdc_UTC_cgmstb_data[84]	vdp_gs_vps_pdc_UTC_cgmstb_data[83]	vdp_gs_vps_pdc_UTC_cgmstb_data[82]	vdp_gs_vps_pdc_UTC_cgmstb_data[81]	vdp_gs_vps_pdc_UTC_cgmstb_data[80]
0x52	0x00	vdp_gs_vps_pdc_UTC_cgmstb_data_12	r	vdp_gs_vps_pdc_UTC_cgmstb_data[95]	vdp_gs_vps_pdc_UTC_cgmstb_data[94]	vdp_gs_vps_pdc_UTC_cgmstb_data[93]	vdp_gs_vps_pdc_UTC_cgmstb_data[92]	vdp_gs_vps_pdc_UTC_cgmstb_data[91]	vdp_gs_vps_pdc_UTC_cgmstb_data[90]	vdp_gs_vps_pdc_UTC_cgmstb_data[89]	vdp_gs_vps_pdc_UTC_cgmstb_data[88]
0x53	0x00	vdp_gs_vps_pdc_UTC_cgmstb_data_13	r	vdp_gs_vps_pdc_UTC_cgmstb_data[103]	vdp_gs_vps_pdc_UTC_cgmstb_data[102]	vdp_gs_vps_pdc_UTC_cgmstb_data[101]	vdp_gs_vps_pdc_UTC_cgmstb_data[100]	vdp_gs_vps_pdc_UTC_cgmstb_data[99]	vdp_gs_vps_pdc_UTC_cgmstb_data[98]	vdp_gs_vps_pdc_UTC_cgmstb_data[97]	vdp_gs_vps_pdc_UTC_cgmstb_data[96]
0x55	0x00	vdp_vitc_data_1	r	vdp_vitc_data[7]	vdp_vitc_data[6]	vdp_vitc_data[5]	vdp_vitc_data[4]	vdp_vitc_data[3]	vdp_vitc_data[2]	vdp_vitc_data[1]	vdp_vitc_data[0]
0x56	0x00	vdp_vitc_data_2	r	vdp_vitc_data[15]	vdp_vitc_data[14]	vdp_vitc_data[13]	vdp_vitc_data[12]	vdp_vitc_data[11]	vdp_vitc_data[10]	vdp_vitc_data[9]	vdp_vitc_data[8]
0x57	0x00	vdp_vitc_data_3	r	vdp_vitc_data[23]	vdp_vitc_data[22]	vdp_vitc_data[21]	vdp_vitc_data[20]	vdp_vitc_data[19]	vdp_vitc_data[18]	vdp_vitc_data[17]	vdp_vitc_data[16]
0x58	0x00	vdp_vitc_data_4	r	vdp_vitc_data[31]	vdp_vitc_data[30]	vdp_vitc_data[29]	vdp_vitc_data[28]	vdp_vitc_data[27]	vdp_vitc_data[26]	vdp_vitc_data[25]	vdp_vitc_data[24]
0x59	0x00	vdp_vitc_data_5	r	vdp_vitc_data[39]	vdp_vitc_data[38]	vdp_vitc_data[37]	vdp_vitc_data[36]	vdp_vitc_data[35]	vdp_vitc_data[34]	vdp_vitc_data[33]	vdp_vitc_data[32]
0x5A	0x00	vdp_vitc_data_6	r	vdp_vitc_data[47]	vdp_vitc_data[46]	vdp_vitc_data[45]	vdp_vitc_data[44]	vdp_vitc_data[43]	vdp_vitc_data[42]	vdp_vitc_data[41]	vdp_vitc_data[40]
0x5B	0x00	vdp_vitc_data_7	r	vdp_vitc_data[55]	vdp_vitc_data[54]	vdp_vitc_data[53]	vdp_vitc_data[52]	vdp_vitc_data[51]	vdp_vitc_data[50]	vdp_vitc_data[49]	vdp_vitc_data[48]
0x5C	0x00	vdp_vitc_data_8	r	vdp_vitc_data[63]	vdp_vitc_data[62]	vdp_vitc_data[61]	vdp_vitc_data[60]	vdp_vitc_data[59]	vdp_vitc_data[58]	vdp_vitc_data[57]	vdp_vitc_data[56]
0x5D	0x00	vdp_vitc_data_9	r	vdp_vitc_data[71]	vdp_vitc_data[70]	vdp_vitc_data[69]	vdp_vitc_data[68]	vdp_vitc_data[67]	vdp_vitc_data[66]	vdp_vitc_data[65]	vdp_vitc_data[64]
0x5E	0x00	vdp_vitc_calc_crc	r	vdp_vitc_calc_crc[7]	vdp_vitc_calc_crc[6]	vdp_vitc_calc_crc[5]	vdp_vitc_calc_crc[4]	vdp_vitc_calc_crc[3]	vdp_vitc_calc_crc[2]	vdp_vitc_calc_crc[1]	vdp_vitc_calc_crc[0]
0x60	0x08	vdp_config_1	rw	-	-	-	-	en_fc_window_after_cri_det	vdp_ttxt_type_man_en	vdp_ttxt_type[1]	vdp_ttxt_type[0]
0x61	0x18	vdp_config_2	rw	vdp_cp_clmp_avg	-	noise_clk_disable	auto_detect_gem	-	-	vitc_strip_sync_disable	biphase_decode_disable
0x64	0x00	vdp_man_line_1_21	rw	vdp_man_line_1_21[7]	vdp_man_line_1_21[6]	vdp_man_line_1_21[5]	vdp_man_line_1_21[4]	vdp_man_line_1_21[3]	vdp_man_line_1_21[2]	vdp_man_line_1_21[1]	vdp_man_line_1_21[0]
0x65	0x00	vdp_man_line_2_22	rw	vdp_man_line_2_22[7]	vdp_man_line_2_22[6]	vdp_man_line_2_22[5]	vdp_man_line_2_22[4]	vdp_man_line_2_22[3]	vdp_man_line_2_22[2]	vdp_man_line_2_22[1]	vdp_man_line_2_22[0]
0x66	0x00	vdp_man_line_3_23	rw	vdp_man_line_3_23[7]	vdp_man_line_3_23[6]	vdp_man_line_3_23[5]	vdp_man_line_3_23[4]	vdp_man_line_3_23[3]	vdp_man_line_3_23[2]	vdp_man_line_3_23[1]	vdp_man_line_3_23[0]
0x67	0x00	vdp_man_line_4_24	rw	vdp_man_line_4_24[7]	vdp_man_line_4_24[6]	vdp_man_line_4_24[5]	vdp_man_line_4_24[4]	vdp_man_line_4_24[3]	vdp_man_line_4_24[2]	vdp_man_line_4_24[1]	vdp_man_line_4_24[0]
0x68	0x00	vdp_man_line_5_25	rw	vdp_man_line_5_25[7]	vdp_man_line_5_25[6]	vdp_man_line_5_25[5]	vdp_man_line_5_25[4]	vdp_man_line_5_25[3]	vdp_man_line_5_25[2]	vdp_man_line_5_25[1]	vdp_man_line_5_25[0]
0x69	0x00	vdp_man_line_6_26	rw	vdp_man_line_6_26[7]	vdp_man_line_6_26[6]	vdp_man_line_6_26[5]	vdp_man_line_6_26[4]	vdp_man_line_6_26[3]	vdp_man_line_6_26[2]	vdp_man_line_6_26[1]	vdp_man_line_6_26[0]
0x6A	0x00	vdp_man_line_7_27	rw	vdp_man_line_7_27[7]	vdp_man_line_7_27[6]	vdp_man_line_7_27[5]	vdp_man_line_7_27[4]	vdp_man_line_7_27[3]	vdp_man_line_7_27[2]	vdp_man_line_7_27[1]	vdp_man_line_7_27[0]
0x6B	0x00	vdp_man_line_8_28	rw	vdp_man_line_8_28[7]	vdp_man_line_8_28[6]	vdp_man_line_8_28[5]	vdp_man_line_8_28[4]	vdp_man_line_8_28[3]	vdp_man_line_8_28[2]	vdp_man_line_8_28[1]	vdp_man_line_8_28[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x6C	0x00	vdp_man_line_9_29	rw	vdp_man_line_9_29[7]	vdp_man_line_9_29[6]	vdp_man_line_9_29[5]	vdp_man_line_9_29[4]	vdp_man_line_9_29[3]	vdp_man_line_9_29[2]	vdp_man_line_9_29[1]	vdp_man_line_9_29[0]
0x6D	0x00	vdp_man_line_10_30	rw	vdp_man_line_10_30[7]	vdp_man_line_10_30[6]	vdp_man_line_10_30[5]	vdp_man_line_10_30[4]	vdp_man_line_10_30[3]	vdp_man_line_10_30[2]	vdp_man_line_10_30[1]	vdp_man_line_10_30[0]
0x6E	0x00	vdp_man_line_11_31	rw	vdp_man_line_11_31[7]	vdp_man_line_11_31[6]	vdp_man_line_11_31[5]	vdp_man_line_11_31[4]	vdp_man_line_11_31[3]	vdp_man_line_11_31[2]	vdp_man_line_11_31[1]	vdp_man_line_11_31[0]
0x6F	0x00	vdp_man_line_12_32	rw	vdp_man_line_12_32[7]	vdp_man_line_12_32[6]	vdp_man_line_12_32[5]	vdp_man_line_12_32[4]	vdp_man_line_12_32[3]	vdp_man_line_12_32[2]	vdp_man_line_12_32[1]	vdp_man_line_12_32[0]
0x70	0x00	vdp_man_line_13_33	rw	vdp_man_line_13_33[7]	vdp_man_line_13_33[6]	vdp_man_line_13_33[5]	vdp_man_line_13_33[4]	vdp_man_line_13_33[3]	vdp_man_line_13_33[2]	vdp_man_line_13_33[1]	vdp_man_line_13_33[0]
0x71	0x00	vdp_man_line_14_34	rw	vdp_man_line_14_34[7]	vdp_man_line_14_34[6]	vdp_man_line_14_34[5]	vdp_man_line_14_34[4]	vdp_man_line_14_34[3]	vdp_man_line_14_34[2]	vdp_man_line_14_34[1]	vdp_man_line_14_34[0]
0x72	0x00	vdp_man_line_15_35	rw	vdp_man_line_15_35[7]	vdp_man_line_15_35[6]	vdp_man_line_15_35[5]	vdp_man_line_15_35[4]	vdp_man_line_15_35[3]	vdp_man_line_15_35[2]	vdp_man_line_15_35[1]	vdp_man_line_15_35[0]
0x73	0x00	vdp_man_line_16_36	rw	vdp_man_line_16_36[7]	vdp_man_line_16_36[6]	vdp_man_line_16_36[5]	vdp_man_line_16_36[4]	vdp_man_line_16_36[3]	vdp_man_line_16_36[2]	vdp_man_line_16_36[1]	vdp_man_line_16_36[0]
0x74	0x00	vdp_man_line_17_37	rw	vdp_man_line_17_37[7]	vdp_man_line_17_37[6]	vdp_man_line_17_37[5]	vdp_man_line_17_37[4]	vdp_man_line_17_37[3]	vdp_man_line_17_37[2]	vdp_man_line_17_37[1]	vdp_man_line_17_37[0]
0x75	0x00	vdp_man_line_18_38	rw	vdp_man_line_18_38[7]	vdp_man_line_18_38[6]	vdp_man_line_18_38[5]	vdp_man_line_18_38[4]	vdp_man_line_18_38[3]	vdp_man_line_18_38[2]	vdp_man_line_18_38[1]	vdp_man_line_18_38[0]
0x76	0x00	vdp_man_line_19_39	rw	vdp_man_line_19_39[7]	vdp_man_line_19_39[6]	vdp_man_line_19_39[5]	vdp_man_line_19_39[4]	vdp_man_line_19_39[3]	vdp_man_line_19_39[2]	vdp_man_line_19_39[1]	vdp_man_line_19_39[0]
0x77	0x00	vdp_man_line_20_40	rw	vdp_man_line_20_40[7]	vdp_man_line_20_40[6]	vdp_man_line_20_40[5]	vdp_man_line_20_40[4]	vdp_man_line_20_40[3]	vdp_man_line_20_40[2]	vdp_man_line_20_40[1]	vdp_man_line_20_40[0]
0x78	0x00	vdp_status_clear	sc	status_clear_ttxt	status_clear_vitc	-	status_clear_gems_vps	-	status_clear_wss_cgms	-	status_clear_ccap
0x98	0x88	vdp_filter_adaptive_slicer_config	rw	low_data_std_filter_en	-	adap1_sl_config_en	-	adap2_sl_config_en	-	-	-
0x99	0xDD	vdp_adap2_std_en	rw	adap2_ttxt_std_en	adap2_vitc_std_en	-	adap2_gems_std_en	adap2_vps_std_en	adap2_wss_cgms_std_en	-	adap2_ccap_std_en
0x9C	0x20	vdp_status_config	rw	-	-	gs_vps_pdc_utc_cb_change	wss_cgms_cb_change	raw_status_enable	gs_vps_pdc_utc_cgms[2]	gs_vps_pdc_utc_cgms[1]	gs_vps_pdc_utc_cgms[0]
0x9D	0x02	vdp_misc_config	rw	-	-	-	-	-	-	slice_corrector_en	-
0x9E	0x00	vdp_adap2_fast_learn_en	rw	-	-	-	-	adap2_vps_ctb_fast_learn_en	-	-	-
0xA5	0x90	vdp_new_ttx_config1	rw	-	vdp_use_predef_req	vdp_cri_tolerance	vdp_frm_code_tolerance	vdp_cri_8bit	-	-	-
0xA6	0x00	vdp_new_ttx_config2	rw	-	-	-	vdp_invert_even_field	-	-	-	-
0xA8	0x08	vdp_parity_max	rw	-	vdp_manual_ttxc	-	-	-	-	-	-
0xAC	0xC8	vdp_cri_mag_thresh	rw	vdp_cri_mag_thresh[7]	vdp_cri_mag_thresh[6]	vdp_cri_mag_thresh[5]	vdp_cri_mag_thresh[4]	vdp_cri_mag_thresh[3]	vdp_cri_mag_thresh[2]	vdp_cri_mag_thresh[1]	vdp_cri_mag_thresh[0]
0xC0	0x00	fast_i2c_reg_conf1	rw	vdp_fast_reg_conf_cus2	vdp_fast_reg_conf_cust	vdp_fast_reg_conf_ccap	vdp_fast_reg_conf_gem1x_2x	vdp_fast_reg_conf_cgms_wss	vdp_fast_reg_conf_vitc	vdp_fast_reg_conf_vps_cgms	vdp_fast_reg_conf_ttxt
0xC2	0x00	fast_i2c_vbi_std	r	-	-	-	-	vdp_fast_vbi_std[3]	vdp_fast_vbi_std[2]	vdp_fast_vbi_std[1]	vdp_fast_vbi_std[0]

Addr 48 (VDP)

ADV7850 Register Map

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xC3	0x00	fast_i2c_packet_size	r	vdp_fast_packet_size[7]	vdp_fast_packet_size[6]	vdp_fast_packet_size[5]	vdp_fast_packet_size[4]	vdp_fast_packet_size[3]	vdp_fast_packet_size[2]	vdp_fast_packet_size[1]	vdp_fast_packet_size[0]

1.6 ADDR A0 (VFE)

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x08	video standard	rw	-	-	vid_std[5]	vid_std[4]	vid_std[3]	vid_std[2]	vid_std[1]	vid_std[0]
0x01	0x06	primary mode	rw	-	v_freq[2]	v_freq[1]	v_freq[0]	prim_mode[3]	prim_mode[2]	prim_mode[1]	prim_mode[0]
0x02	0xF0	io_reg_02	rw	inp_color_space[3]]	inp_color_space[2]]	inp_color_space[1]]	inp_color_space[0]]	alt_gamma	op_656_range	rgb_out	alt_data_sat
0x05	0x2C	io_reg_05	rw	-	-	-	-	-	-	-	op_swap_cb_cr
0x0C	0x02		rw	-	-	-	-	-	cp_pwrdsn	vdp_pdn	-
0x16	0x43	io_reg_16	rw	pll_div_man_en	-	-	pll_div_ratio[12]	pll_div_ratio[11]	pll_div_ratio[10]	pll_div_ratio[9]	pll_div_ratio[8]
0x17	0x5A		rw	pll_div_ratio[7]	pll_div_ratio[6]	pll_div_ratio[5]	pll_div_ratio[4]	pll_div_ratio[3]	pll_div_ratio[2]	pll_div_ratio[1]	pll_div_ratio[0]
0x19	0x00		sc	-	-	-	-	-	-	-	coeff_part_wr
0x21	0x00	dcm_config	rw	dcm_config_en	dcm_ch_sel[2]	dcm_ch_sel[1]	dcm_ch_sel[0]	dcm_filt_en	dcm_filt_sel[2]	dcm_filt_sel[1]	dcm_filt_sel[0]
0x22	0x00	dc_ch_en_1	rw	dcm_mode[2]	dcm_mode[1]	dcm_mode[0]	dcm_filt_size[1]	dcm_filt_size[0]	dcm_bandwidth[2]]	dcm_bandwidth[1]]	dcm_bandwidth[0]]
0x23	0x00	dc_ch_en_2	rw	dcm_ch_en	-	-	-	dcm_ch3_en	dcm_ch2_en	dcm_ch1_en	dcm_ch0_en
0x24	0x00	dcm_filt_gain	rw	-	-	-	-	dcm_filt_gain[3]	dcm_filt_gain[2]	dcm_filt_gain[1]	dcm_filt_gain[0]
0x25	0x00	dcm_filt_sel	rw	filt_sel[3]	filt_sel[2]	filt_sel[1]	filt_sel[0]	-	-	-	-
0x27	0x00	coeff_part_1	rw	coeff_part_sel[111]]	coeff_part_sel[110]]	coeff_part_sel[109]]	coeff_part_sel[108]]	coeff_part_sel[107]]	coeff_part_sel[106]]	coeff_part_sel[105]]	coeff_part_sel[104]]
0x28	0x00	coeff_part_2	rw	coeff_part_sel[103]]	coeff_part_sel[102]]	coeff_part_sel[101]]	coeff_part_sel[100]]	coeff_part_sel[99]	coeff_part_sel[98]	coeff_part_sel[97]	coeff_part_sel[96]
0x29	0x00	coeff_part_3	rw	coeff_part_sel[95]	coeff_part_sel[94]	coeff_part_sel[93]	coeff_part_sel[92]	coeff_part_sel[91]	coeff_part_sel[90]	coeff_part_sel[89]	coeff_part_sel[88]
0x2A	0x00	coeff_part_4	rw	coeff_part_sel[87]	coeff_part_sel[86]	coeff_part_sel[85]	coeff_part_sel[84]	coeff_part_sel[83]	coeff_part_sel[82]	coeff_part_sel[81]	coeff_part_sel[80]
0x2B	0x00	coeff_part_5	rw	coeff_part_sel[79]	coeff_part_sel[78]	coeff_part_sel[77]	coeff_part_sel[76]	coeff_part_sel[75]	coeff_part_sel[74]	coeff_part_sel[73]	coeff_part_sel[72]
0x2C	0x00	coeff_part_6	rw	coeff_part_sel[71]	coeff_part_sel[70]	coeff_part_sel[69]	coeff_part_sel[68]	coeff_part_sel[67]	coeff_part_sel[66]	coeff_part_sel[65]	coeff_part_sel[64]
0x2D	0x00	coeff_part_7	rw	coeff_part_sel[63]	coeff_part_sel[62]	coeff_part_sel[61]	coeff_part_sel[60]	coeff_part_sel[59]	coeff_part_sel[58]	coeff_part_sel[57]	coeff_part_sel[56]
0x2E	0x00	coeff_part_8	rw	coeff_part_sel[55]	coeff_part_sel[54]	coeff_part_sel[53]	coeff_part_sel[52]	coeff_part_sel[51]	coeff_part_sel[50]	coeff_part_sel[49]	coeff_part_sel[48]
0x2F	0x00	coeff_part_9	rw	coeff_part_sel[47]	coeff_part_sel[46]	coeff_part_sel[45]	coeff_part_sel[44]	coeff_part_sel[43]	coeff_part_sel[42]	coeff_part_sel[41]	coeff_part_sel[40]
0x30	0x00	coeff_part_10	rw	coeff_part_sel[39]	coeff_part_sel[38]	coeff_part_sel[37]	coeff_part_sel[36]	coeff_part_sel[35]	coeff_part_sel[34]	coeff_part_sel[33]	coeff_part_sel[32]
0x31	0x00	coeff_part_11	rw	coeff_part_sel[31]	coeff_part_sel[30]	coeff_part_sel[29]	coeff_part_sel[28]	coeff_part_sel[27]	coeff_part_sel[26]	coeff_part_sel[25]	coeff_part_sel[24]
0x32	0x00	coeff_part_12	rw	coeff_part_sel[23]	coeff_part_sel[22]	coeff_part_sel[21]	coeff_part_sel[20]	coeff_part_sel[19]	coeff_part_sel[18]	coeff_part_sel[17]	coeff_part_sel[16]
0x33	0x00	coeff_part_13	rw	coeff_part_sel[15]	coeff_part_sel[14]	coeff_part_sel[13]	coeff_part_sel[12]	coeff_part_sel[11]	coeff_part_sel[10]	coeff_part_sel[9]	coeff_part_sel[8]
0x34	0x00	coeff_part_14	rw	coeff_part_sel[7]	coeff_part_sel[6]	coeff_part_sel[5]	coeff_part_sel[4]	coeff_part_sel[3]	coeff_part_sel[2]	coeff_part_sel[1]	coeff_part_sel[0]
0xBF	0x00		rw	-	-	-	-	-	-	-	coeff_part

1.7 ADDR 90 (SDP)

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x02	autodetect_enables	rw	-	sdp_ad_secam_en	sdp_ad_n443_en	sdp_ad_pal60_en	sdp_ad_palcn_en	sdp_ad_palm_en	sdp_ad_ntsc_en	sdp_ad_pal_en
0x01	0x36	pedestal_selection	rw	-	sdp_secam_ped_en	sdp_n443_ped_en	sdp_pal60_ped_en	sdp_palcn_ped_en	sdp_palm_ped_en	sdp_ntsc_ped_en	sdp_pal_ped_en
0x02	0x27	colour_kill_control	rw	-	sdp_cr_mode_en	-	-	-	-	-	-
0x03	0xC4	luma_gain_1	rw	sdp_y_agc_en	sdp_pw_en	sdp_man_gain_vc_r	sdp_y_gain_man[12]	sdp_y_gain_man[11]	sdp_y_gain_man[10]	sdp_y_gain_man[9]	sdp_y_gain_man[8]
0x04	0x0B	luma_gain_2	rw	sdp_y_gain_man[7]	sdp_y_gain_man[6]	sdp_y_gain_man[5]	sdp_y_gain_man[4]	sdp_y_gain_man[3]	sdp_y_gain_man[2]	sdp_y_gain_man[1]	sdp_y_gain_man[0]
0x05	0xC3	chroma_gain_1	rw	sdp_c_agc_en	sdp_pc_en	-	sdp_c_gain_act_man[12]	sdp_c_gain_act_man[11]	sdp_c_gain_act_man[10]	sdp_c_gain_act_man[9]	sdp_c_gain_act_man[8]
0x06	0xC0	chroma_gain_2	rw	sdp_c_gain_act_man[7]	sdp_c_gain_act_man[6]	sdp_c_gain_act_man[5]	sdp_c_gain_act_man[4]	sdp_c_gain_act_man[3]	sdp_c_gain_act_man[2]	sdp_c_gain_act_man[1]	sdp_c_gain_act_man[0]
0x07	0x8B	colour_kill_on_level	rw	sdp_ckill_en	sdp_ck_low_thr[6]	sdp_ck_low_thr[5]	sdp_ck_low_thr[4]	sdp_ck_low_thr[3]	sdp_ck_low_thr[2]	sdp_ck_low_thr[1]	sdp_ck_low_thr[0]
0x08	0x1A	colour_kill_off_level	rw	sdp_ck_high_thr[7]	sdp_ck_high_thr[6]	sdp_ck_high_thr[5]	sdp_ck_high_thr[4]	sdp_ck_high_thr[3]	sdp_ck_high_thr[2]	sdp_ck_high_thr[1]	sdp_ck_high_thr[0]
0x0A	0xE5	luma_gain_speed	rw	-	-	-	sdp_dgain_speed[4]	sdp_dgain_speed[3]	sdp_dgain_speed[2]	sdp_dgain_speed[1]	sdp_dgain_speed[0]
0x0B	0xE5	chroma_gain_speed	rw	-	-	-	sdp_c_dgain_speed[4]	sdp_c_dgain_speed[3]	sdp_c_dgain_speed[2]	sdp_c_dgain_speed[1]	sdp_c_dgain_speed[0]
0x0C	0xE5	digital_clamp_speed	rw	-	-	-	sdp_dclp_speed[4]	sdp_dclp_speed[3]	sdp_dclp_speed[2]	sdp_dclp_speed[1]	sdp_dclp_speed[0]
0x0D	0xE4	analogue_clamp_speed	rw	-	-	-	sdp_aclp_speed[4]	sdp_aclp_speed[3]	sdp_aclp_speed[2]	sdp_aclp_speed[1]	sdp_aclp_speed[0]
0x0E	0x31	video_enhancements	rw	-	-	sdp_scm_cti_en	sdp_y_2d_pk_en	sdp_v_pk_en	sdp_h_pk_en	sdp_lti_en	sdp_cti_en
0x0F	0x00	gain_recovery_speed_1	rw	sdp_pc_rec_rate[11]	sdp_pc_rec_rate[10]	sdp_pc_rec_rate[9]	sdp_pc_rec_rate[8]	sdp_pw_rec_rate[11]	sdp_pw_rec_rate[10]	sdp_pw_rec_rate[9]	sdp_pw_rec_rate[8]
0x10	0x01	gain_recovery_speed_2	rw	sdp_pw_rec_rate[7]	sdp_pw_rec_rate[6]	sdp_pw_rec_rate[5]	sdp_pw_rec_rate[4]	sdp_pw_rec_rate[3]	sdp_pw_rec_rate[2]	sdp_pw_rec_rate[1]	sdp_pw_rec_rate[0]
0x11	0x10	gain_recovery_speed_3	rw	sdp_pc_rec_rate[7]	sdp_pc_rec_rate[6]	sdp_pc_rec_rate[5]	sdp_pc_rec_rate[4]	sdp_pc_rec_rate[3]	sdp_pc_rec_rate[2]	sdp_pc_rec_rate[1]	sdp_pc_rec_rate[0]
0x12	0x01	3d_enables	rw	-	-	-	-	-	sdp_fr_tbc_en	-	sdp_3d_comb_en
0x13	0x80	contrast	rw	sdp_contrast[9]	sdp_contrast[8]	sdp_contrast[7]	sdp_contrast[6]	sdp_contrast[5]	sdp_contrast[4]	sdp_contrast[3]	sdp_contrast[2]
0x14	0x00	brightness	rw	sdp_brightness[9]	sdp_brightness[8]	sdp_brightness[7]	sdp_brightness[6]	sdp_brightness[5]	sdp_brightness[4]	sdp_brightness[3]	sdp_brightness[2]
0x15	0x80	saturation	rw	sdp_saturation[9]	sdp_saturation[8]	sdp_saturation[7]	sdp_saturation[6]	sdp_saturation[5]	sdp_saturation[4]	sdp_saturation[3]	sdp_saturation[2]
0x16	0x00	hue_tint_1	rw	sdp_hue[9]	sdp_hue[8]	sdp_hue[7]	sdp_hue[6]	sdp_hue[5]	sdp_hue[4]	sdp_hue[3]	sdp_hue[2]
0x17	0x00	hue_tint_2	rw	sdp_hue[1]	sdp_hue[0]	sdp_saturation[1]	sdp_saturation[0]	sdp_brightness[1]	sdp_brightness[0]	sdp_contrast[1]	sdp_contrast[0]
0x18	0xFF	y_shaping_filter_1	rw	sdp_blank_c_vbi	sdp_force_kill_hqi	sdp_y_shape_sel_vbi[5]	sdp_y_shape_sel_vbi[4]	sdp_y_shape_sel_vbi[3]	sdp_y_shape_sel_vbi[2]	sdp_y_shape_sel_vbi[1]	sdp_y_shape_sel_vbi[0]
0x19	0xCD	y_shaping_filter_2	rw	sdp_y_shape_auto_en	sdp_force_comp_hqi	sdp_y_shape_sel_hqi[5]	sdp_y_shape_sel_hqi[4]	sdp_y_shape_sel_hqi[3]	sdp_y_shape_sel_hqi[2]	sdp_y_shape_sel_hqi[1]	sdp_y_shape_sel_hqi[0]
0x1A	0x95	y_shaping_filter_3	rw	sdp_hqi_req_std	-	sdp_y_shape_sel_lqi[5]	sdp_y_shape_sel_lqi[4]	sdp_y_shape_sel_lqi[3]	sdp_y_shape_sel_lqi[2]	sdp_y_shape_sel_lqi[1]	sdp_y_shape_sel_lqi[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x1B	0x1E	y_shaping_filter_4	rw	-	-	sdp_y_shape_sel_scm[5]	sdp_y_shape_sel_scm[4]	sdp_y_shape_sel_scm[3]	sdp_y_shape_sel_scm[2]	sdp_y_shape_sel_scm[1]	sdp_y_shape_sel_scm[0]
0x1C	0xC4	c_shaping_filter_1	rw	sdp_c_shape_aut_o_en	sdp_csh_wbw_au_to	-	sdp_c_shape_sel_hqi[4]	sdp_c_shape_sel_hqi[3]	sdp_c_shape_sel_hqi[2]	sdp_c_shape_sel_hqi[1]	sdp_c_shape_sel_hqi[0]
0x1D	0x02	c_shaping_filter_2	rw	sdp_c_shape_sel_hqi_adj[2]	sdp_c_shape_sel_hqi_adj[1]	sdp_c_shape_sel_hqi_adj[0]	sdp_c_shape_sel_lqi[4]	sdp_c_shape_sel_lqi[3]	sdp_c_shape_sel_lqi[2]	sdp_c_shape_sel_lqi[1]	sdp_c_shape_sel_lqi[0]
0x1E	0x04	c_shaping_filter_3	rw	-	-	-	sdp_c_shape_sel_scm[4]	sdp_c_shape_sel_scm[3]	sdp_c_shape_sel_scm[2]	sdp_c_shape_sel_scm[1]	sdp_c_shape_sel_scm[0]
0x20	0x00	c_if_filter	rw	-	-	-	sdp_if_filt_sel[4]	sdp_if_filt_sel[3]	sdp_if_filt_sel[2]	sdp_if_filt_sel[1]	sdp_if_filt_sel[0]
0x21	0xFF	delay_line	rw	sdp_u_del_line_en	sdp_v_del_line_en	-	-	-	-	-	-
0x22	0x20	horizontal_peaking	rw	sdp_h_pk_inv	sdp_h_pk_gain[3]	sdp_h_pk_gain[2]	sdp_h_pk_gain[1]	sdp_h_pk_gain[0]	sdp_h_pk_core[2]	sdp_h_pk_core[1]	sdp_h_pk_core[0]
0x23	0x10	vertical_peaking	rw	sdp_v_pk_inv	sdp_v_pk_gain[3]	sdp_v_pk_gain[2]	sdp_v_pk_gain[1]	sdp_v_pk_gain[0]	sdp_v_pk_core[2]	sdp_v_pk_core[1]	sdp_v_pk_core[0]
0x24	0x4C	h_v_peaking	rw	-	sdp_v_pk_flip[2]	sdp_v_pk_flip[1]	sdp_v_pk_flip[0]	sdp_v_pk_clip[1]	sdp_v_pk_clip[0]	sdp_h_pk_band[1]	sdp_h_pk_band[0]
0x25	0x00	lti	rw	sdp_lti_filt_sel	sdp_lti_level[6]	sdp_lti_level[5]	sdp_lti_level[4]	sdp_lti_level[3]	sdp_lti_level[2]	sdp_lti_level[1]	sdp_lti_level[0]
0x26	0x8F	cti	rw	sdp_cti_filt_sel	sdp_cti_filt_sel_4_22	sdp_cti_level[5]	sdp_cti_level[4]	sdp_cti_level[3]	sdp_cti_level[2]	sdp_cti_level[1]	sdp_cti_level[0]
0x27	0xAA	lti_cti	rw	sdp_cti_flip[1]	sdp_cti_flip[0]	-	-	sdp_lti_flip[1]	sdp_lti_flip[0]	-	-
0x28	0x02	secam cti	rw	-	-	-	-	-	sdp_scm_cti_gain[1]	sdp_scm_cti_gain[0]	-
0x2A	0x00	rgb_fb_delay_adjust	rw	sdp_man_fb	sdp_rgb_delay_adj[2]	sdp_rgb_delay_adj[1]	sdp_rgb_delay_adj[0]	sdp_man_fb_en	sdp_fb_delay_adj[2]	sdp_fb_delay_adj[1]	sdp_fb_delay_adj[0]
0x34	0xA0	line_tbc	rw	sdp_tbc_en	-	-	-	-	-	-	-
0x4C	0x00	status_letterbox_top	r	sdp_lbox_blk_top[7]	sdp_lbox_blk_top[6]	sdp_lbox_blk_top[5]	sdp_lbox_blk_top[4]	sdp_lbox_blk_top[3]	sdp_lbox_blk_top[2]	sdp_lbox_blk_top[1]	sdp_lbox_blk_top[0]
0x4D	0x00	status_letterbox_bottom	r	sdp_lbox_blk_bot[7]	sdp_lbox_blk_bot[6]	sdp_lbox_blk_bot[5]	sdp_lbox_blk_bot[4]	sdp_lbox_blk_bot[3]	sdp_lbox_blk_bot[2]	sdp_lbox_blk_bot[1]	sdp_lbox_blk_bot[0]
0x4E	0x00	status_letterbox_subtitles_bottom	r	sdp_lbox_blk_sub_bot[7]	sdp_lbox_blk_sub_bot[6]	sdp_lbox_blk_sub_bot[5]	sdp_lbox_blk_sub_bot[4]	sdp_lbox_blk_sub_bot[3]	sdp_lbox_blk_sub_bot[2]	sdp_lbox_blk_sub_bot[1]	sdp_lbox_blk_sub_bot[0]
0x4F	0x00	status_noise_level_lsbs	r	sdp_synctip_noise[7]	sdp_synctip_noise[6]	sdp_synctip_noise[5]	sdp_synctip_noise[4]	sdp_synctip_noise[3]	sdp_synctip_noise[2]	sdp_synctip_noise[1]	sdp_synctip_noise[0]
0x50	0x00	status_macrovision_detection_1	r	-	-	-	-	sdp_mv_agc_detected	sdp_mv_ps_detected	sdp_mvcs_type3	sdp_mvcs_detect
0x51	0x00	status_macrovision_detection_2	r	sdp_bp_total_pulse_beg[3]	sdp_bp_total_pulse_beg[2]	sdp_bp_total_pulse_beg[1]	sdp_bp_total_pulse_beg[0]	sdp_bp_total_pulse_end[3]	sdp_bp_total_pulse_end[2]	sdp_bp_total_pulse_end[1]	sdp_bp_total_pulse_end[0]
0x52	0x00	status_active_standard	r	-	-	-	-	sdp_std[3]	sdp_std[2]	sdp_std[1]	sdp_std[0]
0x53	0x00	status_noise_level_msbs	r	sdp_synctip_noise[11]	sdp_synctip_noise[10]	sdp_synctip_noise[9]	sdp_synctip_noise[8]	-	-	-	-
0x54	0x00	status_luma_gain_1	r	sdp_noisy_ip	sdp_very_noisy_ip	sdp_c_chan_active	sdp_y_gain_man_rb[12]	sdp_y_gain_man_rb[11]	sdp_y_gain_man_rb[10]	sdp_y_gain_man_rb[9]	sdp_y_gain_man_rb[8]
0x55	0x00	status_luma_gain_2	r	sdp_y_gain_man_rb[7]	sdp_y_gain_man_rb[6]	sdp_y_gain_man_rb[5]	sdp_y_gain_man_rb[4]	sdp_y_gain_man_rb[3]	sdp_y_gain_man_rb[2]	sdp_y_gain_man_rb[1]	sdp_y_gain_man_rb[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x56	0x00	sdp_status_input_type_1	r	sdp_hswitch_present	sdp_blk_nstd	sdp fld_nstd	sdp_frm_nstd	sdp_lc_nstd	sdp_allow_med_pll	sdp_allow_slow_pll	sdp_free_run
0x57	0x00	sdp_status_input_type_2	r	sdp_ckill_act	sdp_vs_std_mode	-	sdp_allow_3d_comb	sdp_interlaced	sdp_trick_mode	-	-
0x58	0x00	status_pr_sd_detection	r	-	sdp_pr_detected_in_sd	-	-	-	-	-	-
0x59	0x00	status_burst_locking	r	sdp_burst_locked_rb	-	-	-	sdp_ad_50_60_hz	sdp_pal_sw_lockd	sdp_fsc_freq_ok	sdp_scm_locked
0x5A	0x00	status_input_type_3	r	-	-	-	-	-	-	-	sdp_video_detected
0x7B	0x69	sync_detection_parameters_4	rw	-	-	-	-	-	sdp_extend_vs_max_freq	sdp_extend_vs_min_freq	-
0x89	0x03	luma_agc_target_1	rw	sdp_limit_y_gain	sdp_limit_c_gain	sdp_limit_uv_gain	sdp_limit_g_gain	-	-	-	-
0x96	0x98	y_shaping_filter_5	rw	shape_1d_auto	shape_1d_force	y_shape_sel_1d[5]	y_shape_sel_1d[4]	y_shape_sel_1d[3]	y_shape_sel_1d[2]	y_shape_sel_1d[1]	y_shape_sel_1d[0]
0x97	0x02	c_shaping_filter_5	rw	-	-	-	c_shape_sel_1d[4]	c_shape_sel_1d[3]	c_shape_sel_1d[2]	c_shape_sel_1d[1]	c_shape_sel_1d[0]
0x98	0xBF	hqi_shaping_filter_disable	rw	sdp_nsy_dis_sfs_std	sdp_hsw2_dis_sfs_std	sdp_hsw1_dis_sfs_std	sdp_lc_dis_sfs_std	sdp_blk_dis_sfs_std	sdp fld_sfs_std	sdp_frm_dis_sfs_std	sdp_vnsy_dis_sfs_std
0x99	0x10	detection_filtering_1	rw	-	sdp_shape_std_filt_sel[2]	sdp_shape_std_filt_sel[1]	sdp_shape_std_filt_sel[0]	-	-	-	-
0x9A	0x01	detection_filtering_2	rw	-	-	-	-	-	sdp_allow_3d_filt_sel[2]	sdp_allow_3d_filt_sel[1]	sdp_allow_3d_filt_sel[0]
0xA1	0x50	noisy_threshold	rw	sdp_noisy_thr[7]	sdp_noisy_thr[6]	sdp_noisy_thr[5]	sdp_noisy_thr[4]	sdp_noisy_thr[3]	sdp_noisy_thr[2]	sdp_noisy_thr[1]	sdp_noisy_thr[0]
0xA2	0xA0	very_noisy_threshold	rw	sdp_very_noisy_thr[7]	sdp_very_noisy_thr[6]	sdp_very_noisy_thr[5]	sdp_very_noisy_thr[4]	sdp_very_noisy_thr[3]	sdp_very_noisy_thr[2]	sdp_very_noisy_thr[1]	sdp_very_noisy_thr[0]
0xA3	0xBE	3d_comb_disable_clean	rw	sdp_ckill_dis_3d	-	-	-	-	-	-	-
0xA4	0xBF	3d_comb_disable_noisy	rw	sdp_ckill_dis_2d	sdp_noisy_hsw2_dis_3d	sdp_noisy_hsw1_dis_3d	sdp_noisy_lc_dis_3d	sdp_noisy_blk_dis_3d	sdp_noisy fld_dis_3d	sdp_noisy_frm_dis_3d	sdp_noisy_dis_3d
0xA5	0xBF	3d_comb_disable_very_noisy	rw	sdp_p60_n443_dis_3d	sdp_vnoisy_hsw2_dis_3d	sdp_vnoisy_hsw1_dis_3d	sdp_vnoisy_lc_dis_3d	sdp_vnoisy_blk_dis_3d	sdp_vnoisy fld_dis_3d	sdp_vnoisy_frm_dis_3d	sdp_vnoisy_dis_3d
0xA8	0x40	3d_comb_noise_sensitivity	rw	-	sdp_3d_comb_noise_sns[6]	sdp_3d_comb_noise_sns[5]	sdp_3d_comb_noise_sns[4]	sdp_3d_comb_noise_sns[3]	sdp_3d_comb_noise_sns[2]	sdp_3d_comb_noise_sns[1]	sdp_3d_comb_noise_sns[0]
0xA9	0x88	3d_comb_chroma_sensitivity	rw	sdp_3d_comb_chroma_core[3]	sdp_3d_comb_chroma_core[2]	sdp_3d_comb_chroma_core[1]	sdp_3d_comb_chroma_core[0]	sdp_3d_comb_chroma_sns[3]	sdp_3d_comb_chroma_sns[2]	sdp_3d_comb_chroma_sns[1]	sdp_3d_comb_chroma_sns[0]
0xAA	0x88	3d_comb_luma_sensitivity	rw	sdp_3d_comb_luma_core[3]	sdp_3d_comb_luma_core[2]	sdp_3d_comb_luma_core[1]	sdp_3d_comb_luma_core[0]	sdp_3d_comb_luma_sns[3]	sdp_3d_comb_luma_sns[2]	sdp_3d_comb_luma_sns[1]	sdp_3d_comb_luma_sns[0]
0xDB	0x88	letterbox_detect_1	rw	sdp_lbox_end_del[3]	sdp_lbox_end_del[2]	sdp_lbox_end_del[1]	sdp_lbox_end_del[0]	sdp_lbox_beg_del[3]	sdp_lbox_beg_del[2]	sdp_lbox_beg_del[1]	sdp_lbox_beg_del[0]
0xDC	0x02	letterbox_detect_2	rw	sdp_lbox_blk_lv[2]	sdp_lbox_blk_lv[1]	sdp_lbox_blk_lv[0]	sdp_lbox_thr[4]	sdp_lbox_thr[3]	sdp_lbox_thr[2]	sdp_lbox_thr[1]	sdp_lbox_thr[0]
0xDD	0xBC	sdp_free_run	rw	-	-	-	-	sdp_free_run_auto	sdp_free_run_man_col_en	sdp_free_run_cbar_en	sdp_force_free_run
0xDE	0x23	sdp_free_run_y	rw	sdp_free_run_y[7]	sdp_free_run_y[6]	sdp_free_run_y[5]	sdp_free_run_y[4]	sdp_free_run_y[3]	sdp_free_run_y[2]	sdp_free_run_y[1]	sdp_free_run_y[0]
0xDF	0x7D	sdp_free_run_c	rw	sdp_free_run_v[3]	sdp_free_run_v[2]	sdp_free_run_v[1]	sdp_free_run_v[0]	sdp_free_run_u[3]	sdp_free_run_u[2]	sdp_free_run_u[1]	sdp_free_run_u[0]

1.8 ADDR 94 (SDP_IO)

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x38	0x00	v_field_1_length_1	r	field_2_flag	-	-	-	-	-	field_1_length[9]	field_1_length[8]
0x39	0x00	v_field_1_length_2	r	field_1_length[7]	field_1_length[6]	field_1_length[5]	field_1_length[4]	field_1_length[3]	field_1_length[2]	field_1_length[1]	field_1_length[0]
0x3A	0x00	v_field_2_length_1	r	-	-	-	-	-	-	field_2_length[9]	field_2_length[8]
0x3B	0x00	v_field_2_length_2	r	field_2_length[7]	field_2_length[6]	field_2_length[5]	field_2_length[4]	field_2_length[3]	field_2_length[2]	field_2_length[1]	field_2_length[0]
0x3C	0x10	h_period_measurement_1	rw	h_err_1d_on[7]	h_err_1d_on[6]	h_err_1d_on[5]	h_err_1d_on[4]	h_err_1d_on[3]	h_err_1d_on[2]	h_err_1d_on[1]	h_err_1d_on[0]
0x3D	0x08	h_period_measurement_2	rw	h_err_1d_off[7]	h_err_1d_off[6]	h_err_1d_off[5]	h_err_1d_off[4]	h_err_1d_off[3]	h_err_1d_off[2]	h_err_1d_off[1]	h_err_1d_off[0]
0x3E	0x0C	h_period_measurement_3	rw	h_err_cgain_ovr_on[7]	h_err_cgain_ovr_on[6]	h_err_cgain_ovr_on[5]	h_err_cgain_ovr_on[4]	h_err_cgain_ovr_on[3]	h_err_cgain_ovr_on[2]	h_err_cgain_ovr_on[1]	h_err_cgain_ovr_on[0]
0x3F	0x0B	h_period_measurement_4	rw	h_err_cgain_ovr_off[7]	h_err_cgain_ovr_off[6]	h_err_cgain_ovr_off[5]	h_err_cgain_ovr_off[4]	h_err_cgain_ovr_off[3]	h_err_cgain_ovr_off[2]	h_err_cgain_ovr_off[1]	h_err_cgain_ovr_off[0]
0x40	0x00	status_chroma_gain_act_1	r	-	-	-	c_gain_act[12]	c_gain_act[11]	c_gain_act[10]	c_gain_act[9]	c_gain_act[8]
0x41	0x00	status_chroma_gain_act_2	r	c_gain_act[7]	c_gain_act[6]	c_gain_act[5]	c_gain_act[4]	c_gain_act[3]	c_gain_act[2]	c_gain_act[1]	c_gain_act[0]
0x42	0x00	status_chroma_gain_ad_1	r	-	-	-	c_gain_ad[12]	c_gain_ad[11]	c_gain_ad[10]	c_gain_ad[9]	c_gain_ad[8]
0x43	0x00	status_chroma_gain_ad_2	r	c_gain_ad[7]	c_gain_ad[6]	c_gain_ad[5]	c_gain_ad[4]	c_gain_ad[3]	c_gain_ad[2]	c_gain_ad[1]	c_gain_ad[0]
0x44	0x00	status_burst_power_act_1	r	-	-	-	-	burst_power_act[11]	burst_power_act[10]	burst_power_act[9]	burst_power_act[8]
0x45	0x00	status_burst_power_act_2	r	burst_power_act[7]	burst_power_act[6]	burst_power_act[5]	burst_power_act[4]	burst_power_act[3]	burst_power_act[2]	burst_power_act[1]	burst_power_act[0]
0x46	0x00	status_burst_power_ad_1	r	-	-	-	-	burst_power_ad[11]	burst_power_ad[10]	burst_power_ad[9]	burst_power_ad[8]
0x47	0x00	status_burst_power_ad_2	r	burst_power_ad[7]	burst_power_ad[6]	burst_power_ad[5]	burst_power_ad[4]	burst_power_ad[3]	burst_power_ad[2]	burst_power_ad[1]	burst_power_ad[0]
0x49	0xB8	h_period_measurement_6	rw	auto_cgain_ovr_en	force_cgain_ovr_en	auto_c_comb_1d	auto_y_comb_1d	auto_1d_yc_sep_en	force_y_1d	-	force_c_1d
0x4A	0x00	status_h_period_err_raw_1	r	-	-	-	-	hs_period_err_raw[11]	hs_period_err_raw[10]	hs_period_err_raw[9]	hs_period_err_raw[8]
0x4B	0x00	status_h_period_err_raw_2	r	hs_period_err_raw[7]	hs_period_err_raw[6]	hs_period_err_raw[5]	hs_period_err_raw[4]	hs_period_err_raw[3]	hs_period_err_raw[2]	hs_period_err_raw[1]	hs_period_err_raw[0]
0x4C	0x00	status_h_period_err_1	r	-	-	-	-	hs_period_err_filt[11]	hs_period_err_filt[10]	hs_period_err_filt[9]	hs_period_err_filt[8]
0x4D	0x00	status_h_period_err_2	r	hs_period_err_filt[7]	hs_period_err_filt[6]	hs_period_err_filt[5]	hs_period_err_filt[4]	hs_period_err_filt[3]	hs_period_err_filt[2]	hs_period_err_filt[1]	hs_period_err_filt[0]
0x4E	0x00	sdp_status_input_type_4	r	-	burst_detected	burst_4_43_det	burst_4_43_valid	-	-	-	hs_period_valid

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x4F	0x00	sdp_readback_control	sc	-	-	-	-	-	-	-	upd_sdp_rb
0x51	0x00	ringing_reduction_control_1	rw	sdp_ring_red_en	sdp_ring_red_level[6]	sdp_ring_red_level[5]	sdp_ring_red_level[4]	sdp_ring_red_level[3]	sdp_ring_red_level[2]	sdp_ring_red_level[1]	sdp_ring_red_level[0]
0xE0	0x47	sdp_csc_a1_1	rw	sdp_csc_scale	sdp_csc_auto	-	sdp_a1[12]	sdp_a1[11]	sdp_a1[10]	sdp_a1[9]	sdp_a1[8]
0xE1	0xD2	sdp_csc_a1_2	rw	sdp_a1[7]	sdp_a1[6]	sdp_a1[5]	sdp_a1[4]	sdp_a1[3]	sdp_a1[2]	sdp_a1[1]	sdp_a1[0]
0xE2	0x00	sdp_csc_a2_1	rw	-	-	-	sdp_a2[12]	sdp_a2[11]	sdp_a2[10]	sdp_a2[9]	sdp_a2[8]
0xE3	0x00	sdp_csc_a2_2	rw	sdp_a2[7]	sdp_a2[6]	sdp_a2[5]	sdp_a2[4]	sdp_a2[3]	sdp_a2[2]	sdp_a2[1]	sdp_a2[0]
0xE4	0x00	sdp_csc_a3_1	rw	-	-	-	sdp_a3[12]	sdp_a3[11]	sdp_a3[10]	sdp_a3[9]	sdp_a3[8]
0xE5	0x40	sdp_csc_a3_2	rw	sdp_a3[7]	sdp_a3[6]	sdp_a3[5]	sdp_a3[4]	sdp_a3[3]	sdp_a3[2]	sdp_a3[1]	sdp_a3[0]
0xE6	0x7F	sdp_csc_a4_1	rw	-	sdp_a4[14]	sdp_a4[13]	sdp_a4[12]	sdp_a4[11]	sdp_a4[10]	sdp_a4[9]	sdp_a4[8]
0xE7	0x00	sdp_csc_a4_2	rw	sdp_a4[7]	sdp_a4[6]	sdp_a4[5]	sdp_a4[4]	sdp_a4[3]	sdp_a4[2]	sdp_a4[1]	sdp_a4[0]
0xE8	0x00	sdp_csc_b1_1	rw	-	-	-	sdp_b1[12]	sdp_b1[11]	sdp_b1[10]	sdp_b1[9]	sdp_b1[8]
0xE9	0x00	sdp_csc_b1_2	rw	sdp_b1[7]	sdp_b1[6]	sdp_b1[5]	sdp_b1[4]	sdp_b1[3]	sdp_b1[2]	sdp_b1[1]	sdp_b1[0]
0xEA	0x09	sdp_csc_b2_1	rw	-	-	-	sdp_b2[12]	sdp_b2[11]	sdp_b2[10]	sdp_b2[9]	sdp_b2[8]
0xEB	0x26	sdp_csc_b2_2	rw	sdp_b2[7]	sdp_b2[6]	sdp_b2[5]	sdp_b2[4]	sdp_b2[3]	sdp_b2[2]	sdp_b2[1]	sdp_b2[0]
0xEC	0x00	sdp_csc_b3_1	rw	-	-	-	sdp_b3[12]	sdp_b3[11]	sdp_b3[10]	sdp_b3[9]	sdp_b3[8]
0xED	0x00	sdp_csc_b3_2	rw	sdp_b3[7]	sdp_b3[6]	sdp_b3[5]	sdp_b3[4]	sdp_b3[3]	sdp_b3[2]	sdp_b3[1]	sdp_b3[0]
0xEE	0x00	sdp_csc_b4_1	rw	-	sdp_b4[14]	sdp_b4[13]	sdp_b4[12]	sdp_b4[11]	sdp_b4[10]	sdp_b4[9]	sdp_b4[8]
0xEF	0x00	sdp_csc_b4_2	rw	sdp_b4[7]	sdp_b4[6]	sdp_b4[5]	sdp_b4[4]	sdp_b4[3]	sdp_b4[2]	sdp_b4[1]	sdp_b4[0]
0xF0	0x00	sdp_csc_c1_1	rw	-	-	-	sdp_c1[12]	sdp_c1[11]	sdp_c1[10]	sdp_c1[9]	sdp_c1[8]
0xF1	0x00	sdp_csc_c1_2	rw	sdp_c1[7]	sdp_c1[6]	sdp_c1[5]	sdp_c1[4]	sdp_c1[3]	sdp_c1[2]	sdp_c1[1]	sdp_c1[0]
0xF2	0x00	sdp_csc_c2_1	rw	-	-	-	sdp_c2[12]	sdp_c2[11]	sdp_c2[10]	sdp_c2[9]	sdp_c2[8]
0xF3	0x00	sdp_csc_c2_2	rw	sdp_c2[7]	sdp_c2[6]	sdp_c2[5]	sdp_c2[4]	sdp_c2[3]	sdp_c2[2]	sdp_c2[1]	sdp_c2[0]
0xF4	0x06	sdp_csc_c3_1	rw	-	-	-	sdp_c3[12]	sdp_c3[11]	sdp_c3[10]	sdp_c3[9]	sdp_c3[8]
0xF5	0x81	sdp_csc_c3_2	rw	sdp_c3[7]	sdp_c3[6]	sdp_c3[5]	sdp_c3[4]	sdp_c3[3]	sdp_c3[2]	sdp_c3[1]	sdp_c3[0]
0xF6	0x00	sdp_csc_c4_1	rw	-	sdp_c4[14]	sdp_c4[13]	sdp_c4[12]	sdp_c4[11]	sdp_c4[10]	sdp_c4[9]	sdp_c4[8]
0xF7	0x00	sdp_csc_c4_2	rw	sdp_c4[7]	sdp_c4[6]	sdp_c4[5]	sdp_c4[4]	sdp_c4[3]	sdp_c4[2]	sdp_c4[1]	sdp_c4[0]

1.9 ADDR 68 (HDMI)

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00	hdmi_register_00h	rw	hdcp_a0	hdcp_only_mode	bg_meas_port_sel[2]	bg_meas_port_sel[1]	bg_meas_port_sel[0]	hdmi_port_select[2]	hdmi_port_select[1]	hdmi_port_select[0]
0x01	0x00	hdmi_register_01h	rw	-	-	-	mux_dsd_out	ovr_auto_mux_dsd_out	ovr_mux_hbr	mux_hbr_out	term_auto
0x02	0x00	hdmi_register_bg_port_enable	rw	-	-	-	-	en_bg_port_d	en_bg_port_c	en_bg_port_b	en_bg_port_a
0x03	0x18	hdmi_register_03h	rw	-	i2soutmode[1]	i2soutmode[0]	i2sbitwidth[4]	i2sbitwidth[3]	i2sbitwidth[2]	i2sbitwidth[1]	i2sbitwidth[0]
0x04	0x00	hdmi_register_04h	r	-	av_mute	hdcp_keys_read	hdcp_key_error	hdcp_ri_expired	-	tmds_pll_locked	audio_pll_locked
0x05	0x00	hdmi_register_05h	r	hdmi_mode	hdmi_content_encrypted	dvi_hsync_polarity	dvi_vsync_polarity	hdmi_pixel_repetition[3]	hdmi_pixel_repetition[2]	hdmi_pixel_repetition[1]	hdmi_pixel_repetition[0]
0x07	0x00	line_width_1	r	vert_filter_locked	audio_channel_mode	de_regen_filter_locked	line_width[12]	line_width[11]	line_width[10]	line_width[9]	line_width[8]
0x08	0x00	line_width_2	r	line_width[7]	line_width[6]	line_width[5]	line_width[4]	line_width[3]	line_width[2]	line_width[1]	line_width[0]
0x09	0x00	field0_height_1	r	-	-	-	field0_height[12]	field0_height[11]	field0_height[10]	field0_height[9]	field0_height[8]
0x0A	0x00	field0_height_2	r	field0_height[7]	field0_height[6]	field0_height[5]	field0_height[4]	field0_height[3]	field0_height[2]	field0_height[1]	field0_height[0]
0x0B	0x00	field1_height_1	r	deep_color_mode[1]	deep_color_mode[0]	hdmi_interlaced	field1_height[12]	field1_height[11]	field1_height[10]	field1_height[9]	field1_height[8]
0x0C	0x00	field1_height_2	r	field1_height[7]	field1_height[6]	field1_height[5]	field1_height[4]	field1_height[3]	field1_height[2]	field1_height[1]	field1_height[0]
0x0D	0x04	hdmi_register_0dh	rw	-	hdmi_port_select_tx_b[2]	hdmi_port_select_tx_b[1]	hdmi_port_select_tx_b[0]	freqtolerance[3]	freqtolerance[2]	freqtolerance[1]	freqtolerance[0]
0x10	0x25	hdmi_register_10h	rw	-	-	cts_change_threshold[5]	cts_change_threshold[4]	cts_change_threshold[3]	cts_change_threshold[2]	cts_change_threshold[1]	cts_change_threshold[0]
0x11	0x7D	audio_fifo_almost_full_threshold	rw	-	audio_fifo_almost_full_threshold[6]	audio_fifo_almost_full_threshold[5]	audio_fifo_almost_full_threshold[4]	audio_fifo_almost_full_threshold[3]	audio_fifo_almost_full_threshold[2]	audio_fifo_almost_full_threshold[1]	audio_fifo_almost_full_threshold[0]
0x12	0x02	audio_fifo_almost_empty_threshold	rw	-	audio_fifo_almost_empty_threshold[6]	audio_fifo_almost_empty_threshold[5]	audio_fifo_almost_empty_threshold[4]	audio_fifo_almost_empty_threshold[3]	audio_fifo_almost_empty_threshold[2]	audio_fifo_almost_empty_threshold[1]	audio_fifo_almost_empty_threshold[0]
0x13	0x7F	audio_coast_mask	rw	-	ac_msk_vclk_chng	ac_msk_vpll_unlock	-	ac_msk_new_cts	ac_msk_new_n	ac_msk_chng_port	ac_msk_vclk_det
0x14	0x3F	mute_mask_21_16	rw	-	-	mt_msk_compr_saud	mt_msk_aud_mode_chng	-	-	mt_msk_parity_err	mt_msk_vclk_chng
0x15	0xFF	mute_mask_15_8	rw	mt_msk_apll_unlock	mt_msk_vpll_unlock	mt_msk_acr_not_det	-	mt_msk_flatline_det	-	mt_msk_fifo_underrfow	mt_msk_fifo_overflow
0x16	0xFF	mute_mask_7_0	rw	mt_msk_avmute	mt_msk_not_hdmimode	mt_msk_new_cts	mt_msk_new_n	mt_msk_chmode_chng	mt_msk_apckt_err	mt_msk_chng_port	mt_msk_vclk_det
0x18	0x00	packets_detected_2	r	-	-	-	-	hbr_audio_pckt_det	dst_audio_pckt_det	dsd_packet_det	audio_sample_pckt_det
0x19	0x00	packets_detected_3	r	-	-	-	-	-	dst_double	-	-
0x1A	0x80	mute_ctrl	rw	-	ignore_parity_err	-	mute_audio	wait_unmute[2]	wait_unmute[1]	wait_unmute[0]	not_auto_unmute
0x1B	0x18	deepcolor_fifo_debug_1	rw	-	-	-	dcfifo_reset_on_lock	dcfifo_kill_not_locked	dcfifo_kill_dis	-	-
0x1C	0x00	deepcolor_fifo_debug_2	r	-	-	-	-	dcfifo_locked	dcfifo_level[2]	dcfifo_level[1]	dcfifo_level[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x1D	0x00	register_1dh	rw	-	pdn_pkt_processor	up_conversion_mode	-	-	-	-	-
0x1E	0x00	total_line_width_1	r	-	-	total_line_width[13]	total_line_width[12]	total_line_width[11]	total_line_width[10]	total_line_width[9]	total_line_width[8]
0x1F	0x00	total_line_width_2	r	total_line_width[7]	total_line_width[6]	total_line_width[5]	total_line_width[4]	total_line_width[3]	total_line_width[2]	total_line_width[1]	total_line_width[0]
0x20	0x00	hsync_front_porch_1	r	-	-	-	hsync_front_porch[12]	hsync_front_porch[11]	hsync_front_porch[10]	hsync_front_porch[9]	hsync_front_porch[8]
0x21	0x00	hsync_front_porch_2	r	hsync_front_porch[7]	hsync_front_porch[6]	hsync_front_porch[5]	hsync_front_porch[4]	hsync_front_porch[3]	hsync_front_porch[2]	hsync_front_porch[1]	hsync_front_porch[0]
0x22	0x00	hsync_pulse_width_1	r	-	-	-	hsync_pulse_width[12]	hsync_pulse_width[11]	hsync_pulse_width[10]	hsync_pulse_width[9]	hsync_pulse_width[8]
0x23	0x00	hsync_pulse_width_2	r	hsync_pulse_width[7]	hsync_pulse_width[6]	hsync_pulse_width[5]	hsync_pulse_width[4]	hsync_pulse_width[3]	hsync_pulse_width[2]	hsync_pulse_width[1]	hsync_pulse_width[0]
0x24	0x00	hsync_back_porch_1	r	-	-	-	hsync_back_porch[12]	hsync_back_porch[11]	hsync_back_porch[10]	hsync_back_porch[9]	hsync_back_porch[8]
0x25	0x00	hsync_back_porch_2	r	hsync_back_porch[7]	hsync_back_porch[6]	hsync_back_porch[5]	hsync_back_porch[4]	hsync_back_porch[3]	hsync_back_porch[2]	hsync_back_porch[1]	hsync_back_porch[0]
0x26	0x00	field0_total_height_1	r	-	-	field0_total_height[13]	field0_total_height[12]	field0_total_height[11]	field0_total_height[10]	field0_total_height[9]	field0_total_height[8]
0x27	0x00	field0_total_height_2	r	field0_total_height[7]	field0_total_height[6]	field0_total_height[5]	field0_total_height[4]	field0_total_height[3]	field0_total_height[2]	field0_total_height[1]	field0_total_height[0]
0x28	0x00	field1_total_height_1	r	-	-	field1_total_height[13]	field1_total_height[12]	field1_total_height[11]	field1_total_height[10]	field1_total_height[9]	field1_total_height[8]
0x29	0x00	field1_total_height_2	r	field1_total_height[7]	field1_total_height[6]	field1_total_height[5]	field1_total_height[4]	field1_total_height[3]	field1_total_height[2]	field1_total_height[1]	field1_total_height[0]
0x2A	0x00	field0_vs_front_porch_1	r	-	-	field0_vs_front_porch[13]	field0_vs_front_porch[12]	field0_vs_front_porch[11]	field0_vs_front_porch[10]	field0_vs_front_porch[9]	field0_vs_front_porch[8]
0x2B	0x00	field0_vs_front_porch_2	r	field0_vs_front_porch[7]	field0_vs_front_porch[6]	field0_vs_front_porch[5]	field0_vs_front_porch[4]	field0_vs_front_porch[3]	field0_vs_front_porch[2]	field0_vs_front_porch[1]	field0_vs_front_porch[0]
0x2C	0x00	field1_vs_front_porch_1	r	-	-	field1_vs_front_porch[13]	field1_vs_front_porch[12]	field1_vs_front_porch[11]	field1_vs_front_porch[10]	field1_vs_front_porch[9]	field1_vs_front_porch[8]
0x2D	0x00	field1_vs_front_porch_2	r	field1_vs_front_porch[7]	field1_vs_front_porch[6]	field1_vs_front_porch[5]	field1_vs_front_porch[4]	field1_vs_front_porch[3]	field1_vs_front_porch[2]	field1_vs_front_porch[1]	field1_vs_front_porch[0]
0x2E	0x00	field0_vs_pulse_width_1	r	-	-	field0_vs_pulse_width[13]	field0_vs_pulse_width[12]	field0_vs_pulse_width[11]	field0_vs_pulse_width[10]	field0_vs_pulse_width[9]	field0_vs_pulse_width[8]
0x2F	0x00	field0_vs_pulse_width_2	r	field0_vs_pulse_width[7]	field0_vs_pulse_width[6]	field0_vs_pulse_width[5]	field0_vs_pulse_width[4]	field0_vs_pulse_width[3]	field0_vs_pulse_width[2]	field0_vs_pulse_width[1]	field0_vs_pulse_width[0]
0x30	0x00	field1_vs_pulse_width_1	r	-	-	field1_vs_pulse_width[13]	field1_vs_pulse_width[12]	field1_vs_pulse_width[11]	field1_vs_pulse_width[10]	field1_vs_pulse_width[9]	field1_vs_pulse_width[8]
0x31	0x00	field1_vs_pulse_width_2	r	field1_vs_pulse_width[7]	field1_vs_pulse_width[6]	field1_vs_pulse_width[5]	field1_vs_pulse_width[4]	field1_vs_pulse_width[3]	field1_vs_pulse_width[2]	field1_vs_pulse_width[1]	field1_vs_pulse_width[0]
0x32	0x00	field0_vs_back_porch_1	r	-	-	field0_vs_back_porch[13]	field0_vs_back_porch[12]	field0_vs_back_porch[11]	field0_vs_back_porch[10]	field0_vs_back_porch[9]	field0_vs_back_porch[8]
0x33	0x00	field0_vs_back_porch_2	r	field0_vs_back_porch[7]	field0_vs_back_porch[6]	field0_vs_back_porch[5]	field0_vs_back_porch[4]	field0_vs_back_porch[3]	field0_vs_back_porch[2]	field0_vs_back_porch[1]	field0_vs_back_porch[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x34	0x00	field1_vs_back_porch_1	r	-	-	field1_vs_back_porch[13]	field1_vs_back_porch[12]	field1_vs_back_porch[11]	field1_vs_back_porch[10]	field1_vs_back_porch[9]	field1_vs_back_porch[8]
0x35	0x00	field1_vs_back_porch_2	r	field1_vs_back_porch[7]	field1_vs_back_porch[6]	field1_vs_back_porch[5]	field1_vs_back_porch[4]	field1_vs_back_porch[3]	field1_vs_back_porch[2]	field1_vs_back_porch[1]	field1_vs_back_porch[0]
0x36	0x00	channel status data_1	r	cs_data[7]	cs_data[6]	cs_data[5]	cs_data[4]	cs_data[3]	cs_data[2]	cs_data[1]	cs_data[0]
0x37	0x00	channel status data_2	r	cs_data[15]	cs_data[14]	cs_data[13]	cs_data[12]	cs_data[11]	cs_data[10]	cs_data[9]	cs_data[8]
0x38	0x00	channel status data_3	r	cs_data[23]	cs_data[22]	cs_data[21]	cs_data[20]	cs_data[19]	cs_data[18]	cs_data[17]	cs_data[16]
0x39	0x00	channel status data_4	r	cs_data[31]	cs_data[30]	cs_data[29]	cs_data[28]	cs_data[27]	cs_data[26]	cs_data[25]	cs_data[24]
0x3A	0x00	channel status data_5	r	cs_data[39]	cs_data[38]	cs_data[37]	cs_data[36]	cs_data[35]	cs_data[34]	cs_data[33]	cs_data[32]
0x40	0x00	register_40h	rw	-	override_deep_color_mode	deep_color_mode_user[1]	deep_color_mode_user[0]	-	-	-	-
0x41	0x40	register_41h	rw	-	-	-	derep_n_override	derep_n[3]	derep_n[2]	derep_n[1]	derep_n[0]
0x47	0x00	register_47h	rw	-	-	-	-	-	qzero_itc_dis	qzero_rgb_full	always_store_inf
0x48	0x00	register_48h	rw	dis_pwrndb	dis_cable_det_rst	-	-	-	-	-	-
0x50	0x00	hdmi_register_50	rw	-	-	-	gamut_irq_next_field	-	-	cs_copyright_manual	cs_copyright_value
0x51	0x00		r	tmdsfreq[8]	tmdsfreq[7]	tmdsfreq[6]	tmdsfreq[5]	tmdsfreq[4]	tmdsfreq[3]	tmdsfreq[2]	tmdsfreq[1]
0x52	0x00		r	tmdsfreq[0]	tmdsfreq_frac[6]	tmdsfreq_frac[5]	tmdsfreq_frac[4]	tmdsfreq_frac[3]	tmdsfreq_frac[2]	tmdsfreq_frac[1]	tmdsfreq_frac[0]
0x53	0x00	hdmi_colorspace	r	-	-	-	-	hdmi_colorspace[3]	hdmi_colorspace[2]	hdmi_colorspace[1]	hdmi_colorspace[0]
0x56	0x58	filt_5v_det_reg	rw	filt_5v_det_dis	filt_5v_det_timer[6]	filt_5v_det_timer[5]	filt_5v_det_timer[4]	filt_5v_det_timer[3]	filt_5v_det_timer[2]	filt_5v_det_timer[1]	filt_5v_det_timer[0]
0x5A	0x00	register_5a	sc	load_eq_stat	hdcp_i2c_reset_tx	bg_meas_req	-	hdcp_rept_edid_reset	dcfifo_recenter	-	force_n_update
0x5B	0x00	cts_n_1	r	cts[19]	cts[18]	cts[17]	cts[16]	cts[15]	cts[14]	cts[13]	cts[12]
0x5C	0x00	cts_n_2	r	cts[11]	cts[10]	cts[9]	cts[8]	cts[7]	cts[6]	cts[5]	cts[4]
0x5D	0x00	cts_n_3	r	cts[3]	cts[2]	cts[1]	cts[0]	n[19]	n[18]	n[17]	n[16]
0x5E	0x00	cts_n_4	r	n[15]	n[14]	n[13]	n[12]	n[11]	n[10]	n[9]	n[8]
0x5F	0x00	cts_n_5	r	n[7]	n[6]	n[5]	n[4]	n[3]	n[2]	n[1]	n[0]
0x6C	0xA3		rw	hpa_delay_sel[3]	hpa_delay_sel[2]	hpa_delay_sel[1]	hpa_delay_sel[0]	hpa_ovr_term	-	-	hpa_manual
0x6D	0x00		rw	-	i2s_spdif_map_inv	i2s_spdif_map_rot[1]	i2s_spdif_map_rot[0]	dsd_map_inv	dsd_map_rot[2]	dsd_map_rot[1]	dsd_map_rot[0]
0x6E	0x04		rw	-	-	-	-	-	dst_map_rot[2]	dst_map_rot[1]	dst_map_rot[0]
0x71	0x00		rw	-	-	-	-	edid_pwrsw3p3[1]	edid_pwrsw3p3[0]	edid_pwrsw1p8[1]	edid_pwrsw1p8[0]
0x72	0x04		rw	-	-	-	-	vga_pwrnd	-	-	-
0x73	0x00	ddc pad	rw	ddc_pwrnd[7]	ddc_pwrnd[6]	ddc_pwrnd[5]	ddc_pwrnd[4]	ddc_pwrnd[3]	ddc_pwrnd[2]	ddc_pwrnd[1]	ddc_pwrnd[0]
0x83	0xFF	hdmi_register_02h	rw	-	-	-	-	clock_termd_disable	clock_termc_disable	clock_termb_disable	clock_termina_disable
0x85	0x16		rw	eq_bypass_mode	-	-	-	eq_agc_mode[3]	eq_agc_mode[2]	eq_agc_mode[1]	eq_agc_mode[0]
0x87	0x00		rw	-	eq_agc_readback_sel[1]	eq_agc_readback_sel[0]	-	-	-	-	-

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x88	0x00	eq_readback	r	eq_agc_readback[7]	eq_agc_readback[6]	eq_agc_readback[5]	eq_agc_readback[4]	eq_agc_readback[3]	eq_agc_readback[2]	eq_agc_readback[1]	eq_agc_readback[0]
0x91	0x00	eq_stat	rw	-	eq_stat_port_sel[2]	eq_stat_port_sel[1]	eq_stat_port_sel[0]	-	-	-	-
0x92	0x08	eq_stat_gctrl	rw	-	-	-	eq_stat_gctrl[4]	eq_stat_gctrl[3]	eq_stat_gctrl[2]	eq_stat_gctrl[1]	eq_stat_gctrl[0]
0x93	0x00	eq_stat_zctrl	rw	eq_stat_zctrl[7]	eq_stat_zctrl[6]	eq_stat_zctrl[5]	eq_stat_zctrl[4]	eq_stat_zctrl[3]	eq_stat_zctrl[2]	eq_stat_zctrl[1]	eq_stat_zctrl[0]
0xE0	0x00		r	bg_tmbsfreq[8]	bg_tmbsfreq[7]	bg_tmbsfreq[6]	bg_tmbsfreq[5]	bg_tmbsfreq[4]	bg_tmbsfreq[3]	bg_tmbsfreq[2]	bg_tmbsfreq[1]
0xE1	0x00		r	bg_tmbsfreq[0]	bg_tmbsfreq_frac[6]	bg_tmbsfreq_frac[5]	bg_tmbsfreq_frac[4]	bg_tmbsfreq_frac[3]	bg_tmbsfreq_frac[2]	bg_tmbsfreq_frac[1]	bg_tmbsfreq_frac[0]
0xE2	0x00		r	-	-	-	bg_line_width[12]	bg_line_width[11]	bg_line_width[10]	bg_line_width[9]	bg_line_width[8]
0xE3	0x00		r	bg_line_width[7]	bg_line_width[6]	bg_line_width[5]	bg_line_width[4]	bg_line_width[3]	bg_line_width[2]	bg_line_width[1]	bg_line_width[0]
0xE4	0x00		r	-	-	bg_total_line_width[13]	bg_total_line_width[12]	bg_total_line_width[11]	bg_total_line_width[10]	bg_total_line_width[9]	bg_total_line_width[8]
0xE5	0x00		r	bg_total_line_width[7]	bg_total_line_width[6]	bg_total_line_width[5]	bg_total_line_width[4]	bg_total_line_width[3]	bg_total_line_width[2]	bg_total_line_width[1]	bg_total_line_width[0]
0xE6	0x00		r	-	-	-	bg_field_height[12]	bg_field_height[11]	bg_field_height[10]	bg_field_height[9]	bg_field_height[8]
0xE7	0x00		r	bg_field_height[7]	bg_field_height[6]	bg_field_height[5]	bg_field_height[4]	bg_field_height[3]	bg_field_height[2]	bg_field_height[1]	bg_field_height[0]
0xE8	0x00		r	-	-	-	bg_total_field_height[12]	bg_total_field_height[11]	bg_total_field_height[10]	bg_total_field_height[9]	bg_total_field_height[8]
0xE9	0x00		r	bg_total_field_height[7]	bg_total_field_height[6]	bg_total_field_height[5]	bg_total_field_height[4]	bg_total_field_height[3]	bg_total_field_height[2]	bg_total_field_height[1]	bg_total_field_height[0]
0xEA	0x00		r	bg_pix_rep[3]	bg_pix_rep[2]	bg_pix_rep[1]	bg_pix_rep[0]	bg_deep_color_mode[1]	bg_deep_color_mode[0]	bg_param_lock	bg_hdmi_interlaced
0xEB	0x00		r	-	-	-	-	-	-	-	bg_hdmi_mode
0xEE	0x00		r	-	-	-	bg_dst_double	bg_audio_detected[3]	bg_audio_detected[2]	bg_audio_detected[1]	bg_audio_detected[0]
0xEF	0x82		rw	bg_header_requested[7]	bg_header_requested[6]	bg_header_requested[5]	bg_header_requested[4]	bg_header_requested[3]	bg_header_requested[2]	bg_header_requested[1]	bg_header_requested[0]
0xF0	0x00		r	bg_header_byte1[7]	bg_header_byte1[6]	bg_header_byte1[5]	bg_header_byte1[4]	bg_header_byte1[3]	bg_header_byte1[2]	bg_header_byte1[1]	bg_header_byte1[0]
0xF1	0x00		r	bg_packet_byte1[7]	bg_packet_byte1[6]	bg_packet_byte1[5]	bg_packet_byte1[4]	bg_packet_byte1[3]	bg_packet_byte1[2]	bg_packet_byte1[1]	bg_packet_byte1[0]
0xF2	0x00		r	bg_packet_byte2[7]	bg_packet_byte2[6]	bg_packet_byte2[5]	bg_packet_byte2[4]	bg_packet_byte2[3]	bg_packet_byte2[2]	bg_packet_byte2[1]	bg_packet_byte2[0]
0xF3	0x00		r	bg_packet_byte3[7]	bg_packet_byte3[6]	bg_packet_byte3[5]	bg_packet_byte3[4]	bg_packet_byte3[3]	bg_packet_byte3[2]	bg_packet_byte3[1]	bg_packet_byte3[0]
0xF4	0x00		r	bg_packet_byte4[7]	bg_packet_byte4[6]	bg_packet_byte4[5]	bg_packet_byte4[4]	bg_packet_byte4[3]	bg_packet_byte4[2]	bg_packet_byte4[1]	bg_packet_byte4[0]
0xF5	0x00		r	bg_packet_byte5[7]	bg_packet_byte5[6]	bg_packet_byte5[5]	bg_packet_byte5[4]	bg_packet_byte5[3]	bg_packet_byte5[2]	bg_packet_byte5[1]	bg_packet_byte5[0]
0xF6	0x00		r	-	-	-	-	-	-	-	bg_valid_packet

1.10 ADDR 64 (REPEATER)

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00	bksv_1	r	bksv[7]	bksv[6]	bksv[5]	bksv[4]	bksv[3]	bksv[2]	bksv[1]	bksv[0]
0x01	0x00	bksv_2	r	bksv[15]	bksv[14]	bksv[13]	bksv[12]	bksv[11]	bksv[10]	bksv[9]	bksv[8]
0x02	0x00	bksv_3	r	bksv[23]	bksv[22]	bksv[21]	bksv[20]	bksv[19]	bksv[18]	bksv[17]	bksv[16]
0x03	0x00	bksv_4	r	bksv[31]	bksv[30]	bksv[29]	bksv[28]	bksv[27]	bksv[26]	bksv[25]	bksv[24]
0x04	0x00	bksv_5	r	bksv[39]	bksv[38]	bksv[37]	bksv[36]	bksv[35]	bksv[34]	bksv[33]	bksv[32]
0x08	0x00	ri_1	r	ri[7]	ri[6]	ri[5]	ri[4]	ri[3]	ri[2]	ri[1]	ri[0]
0x09	0x00	ri_2	r	ri[15]	ri[14]	ri[13]	ri[12]	ri[11]	ri[10]	ri[9]	ri[8]
0x0A	0x00	pj	r	pj[7]	pj[6]	pj[5]	pj[4]	pj[3]	pj[2]	pj[1]	pj[0]
0x10	0x00	aksv_1	rw	aksv[7]	aksv[6]	aksv[5]	aksv[4]	aksv[3]	aksv[2]	aksv[1]	aksv[0]
0x11	0x00	aksv_2	rw	aksv[15]	aksv[14]	aksv[13]	aksv[12]	aksv[11]	aksv[10]	aksv[9]	aksv[8]
0x12	0x00	aksv_3	rw	aksv[23]	aksv[22]	aksv[21]	aksv[20]	aksv[19]	aksv[18]	aksv[17]	aksv[16]
0x13	0x00	aksv_4	rw	aksv[31]	aksv[30]	aksv[29]	aksv[28]	aksv[27]	aksv[26]	aksv[25]	aksv[24]
0x14	0x00	aksv_5	rw	aksv[39]	aksv[38]	aksv[37]	aksv[36]	aksv[35]	aksv[34]	aksv[33]	aksv[32]
0x15	0x00	ainfo	rw	ainfo[7]	ainfo[6]	ainfo[5]	ainfo[4]	ainfo[3]	ainfo[2]	ainfo[1]	ainfo[0]
0x16	0x00	ainfo_rb	r	ainfo_rb[7]	ainfo_rb[6]	ainfo_rb[5]	ainfo_rb[4]	ainfo_rb[3]	ainfo_rb[2]	ainfo_rb[1]	ainfo_rb[0]
0x18	0x00	an_1	rw	an[7]	an[6]	an[5]	an[4]	an[3]	an[2]	an[1]	an[0]
0x19	0x00	an_2	rw	an[15]	an[14]	an[13]	an[12]	an[11]	an[10]	an[9]	an[8]
0x1A	0x00	an_3	rw	an[23]	an[22]	an[21]	an[20]	an[19]	an[18]	an[17]	an[16]
0x1B	0x00	an_4	rw	an[31]	an[30]	an[29]	an[28]	an[27]	an[26]	an[25]	an[24]
0x1C	0x00	an_5	rw	an[39]	an[38]	an[37]	an[36]	an[35]	an[34]	an[33]	an[32]
0x1D	0x00	an_6	rw	an[47]	an[46]	an[45]	an[44]	an[43]	an[42]	an[41]	an[40]
0x1E	0x00	an_7	rw	an[55]	an[54]	an[53]	an[52]	an[51]	an[50]	an[49]	an[48]
0x1F	0x00	an_8	rw	an[63]	an[62]	an[61]	an[60]	an[59]	an[58]	an[57]	an[56]
0x20	0x00	sha_a_1	rw	sha_a[7]	sha_a[6]	sha_a[5]	sha_a[4]	sha_a[3]	sha_a[2]	sha_a[1]	sha_a[0]
0x21	0x00	sha_a_2	rw	sha_a[15]	sha_a[14]	sha_a[13]	sha_a[12]	sha_a[11]	sha_a[10]	sha_a[9]	sha_a[8]
0x22	0x00	sha_a_3	rw	sha_a[23]	sha_a[22]	sha_a[21]	sha_a[20]	sha_a[19]	sha_a[18]	sha_a[17]	sha_a[16]
0x23	0x00	sha_a_4	rw	sha_a[31]	sha_a[30]	sha_a[29]	sha_a[28]	sha_a[27]	sha_a[26]	sha_a[25]	sha_a[24]
0x24	0x00	sha_b_1	rw	sha_b[7]	sha_b[6]	sha_b[5]	sha_b[4]	sha_b[3]	sha_b[2]	sha_b[1]	sha_b[0]
0x25	0x00	sha_b_2	rw	sha_b[15]	sha_b[14]	sha_b[13]	sha_b[12]	sha_b[11]	sha_b[10]	sha_b[9]	sha_b[8]
0x26	0x00	sha_b_3	rw	sha_b[23]	sha_b[22]	sha_b[21]	sha_b[20]	sha_b[19]	sha_b[18]	sha_b[17]	sha_b[16]
0x27	0x00	sha_b_4	rw	sha_b[31]	sha_b[30]	sha_b[29]	sha_b[28]	sha_b[27]	sha_b[26]	sha_b[25]	sha_b[24]
0x28	0x00	sha_c_1	rw	sha_c[7]	sha_c[6]	sha_c[5]	sha_c[4]	sha_c[3]	sha_c[2]	sha_c[1]	sha_c[0]
0x29	0x00	sha_c_2	rw	sha_c[15]	sha_c[14]	sha_c[13]	sha_c[12]	sha_c[11]	sha_c[10]	sha_c[9]	sha_c[8]
0x2A	0x00	sha_c_3	rw	sha_c[23]	sha_c[22]	sha_c[21]	sha_c[20]	sha_c[19]	sha_c[18]	sha_c[17]	sha_c[16]
0x2B	0x00	sha_c_4	rw	sha_c[31]	sha_c[30]	sha_c[29]	sha_c[28]	sha_c[27]	sha_c[26]	sha_c[25]	sha_c[24]
0x2C	0x00	sha_d_1	rw	sha_d[7]	sha_d[6]	sha_d[5]	sha_d[4]	sha_d[3]	sha_d[2]	sha_d[1]	sha_d[0]
0x2D	0x00	sha_d_2	rw	sha_d[15]	sha_d[14]	sha_d[13]	sha_d[12]	sha_d[11]	sha_d[10]	sha_d[9]	sha_d[8]
0x2E	0x00	sha_d_3	rw	sha_d[23]	sha_d[22]	sha_d[21]	sha_d[20]	sha_d[19]	sha_d[18]	sha_d[17]	sha_d[16]
0x2F	0x00	sha_d_4	rw	sha_d[31]	sha_d[30]	sha_d[29]	sha_d[28]	sha_d[27]	sha_d[26]	sha_d[25]	sha_d[24]
0x30	0x00	sha_e_1	rw	sha_e[7]	sha_e[6]	sha_e[5]	sha_e[4]	sha_e[3]	sha_e[2]	sha_e[1]	sha_e[0]
0x31	0x00	sha_e_2	rw	sha_e[15]	sha_e[14]	sha_e[13]	sha_e[12]	sha_e[11]	sha_e[10]	sha_e[9]	sha_e[8]
0x32	0x00	sha_e_3	rw	sha_e[23]	sha_e[22]	sha_e[21]	sha_e[20]	sha_e[19]	sha_e[18]	sha_e[17]	sha_e[16]
0x33	0x00	sha_e_4	rw	sha_e[31]	sha_e[30]	sha_e[29]	sha_e[28]	sha_e[27]	sha_e[26]	sha_e[25]	sha_e[24]
0x40	0x83	bcaps	rw	bcaps[7]	bcaps[6]	bcaps[5]	bcaps[4]	bcaps[3]	bcaps[2]	bcaps[1]	bcaps[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x41	0x00	bstatus_1	rw	bstatus[7]	bstatus[6]	bstatus[5]	bstatus[4]	bstatus[3]	bstatus[2]	bstatus[1]	bstatus[0]
0x42	0x00	bstatus_2	rw	bstatus[15]	bstatus[14]	bstatus[13]	bstatus[12]	bstatus[11]	bstatus[10]	bstatus[9]	bstatus[8]
0x52	0x00	spa port b_1	rw	spa_port_b[15]	spa_port_b[14]	spa_port_b[13]	spa_port_b[12]	spa_port_b[11]	spa_port_b[10]	spa_port_b[9]	spa_port_b[8]
0x53	0x00	spa port b_2	rw	spa_port_b[7]	spa_port_b[6]	spa_port_b[5]	spa_port_b[4]	spa_port_b[3]	spa_port_b[2]	spa_port_b[1]	spa_port_b[0]
0x54	0x00	spa port c_1	rw	spa_port_c[15]	spa_port_c[14]	spa_port_c[13]	spa_port_c[12]	spa_port_c[11]	spa_port_c[10]	spa_port_c[9]	spa_port_c[8]
0x55	0x00	spa port c_2	rw	spa_port_c[7]	spa_port_c[6]	spa_port_c[5]	spa_port_c[4]	spa_port_c[3]	spa_port_c[2]	spa_port_c[1]	spa_port_c[0]
0x56	0x00	spa port d_1	rw	spa_port_d[15]	spa_port_d[14]	spa_port_d[13]	spa_port_d[12]	spa_port_d[11]	spa_port_d[10]	spa_port_d[9]	spa_port_d[8]
0x57	0x00	spa port d_2	rw	spa_port_d[7]	spa_port_d[6]	spa_port_d[5]	spa_port_d[4]	spa_port_d[3]	spa_port_d[2]	spa_port_d[1]	spa_port_d[0]
0x61	0x00	port b checksum	rw	port_b_checksum[7]	port_b_checksum[6]	port_b_checksum[5]	port_b_checksum[4]	port_b_checksum[3]	port_b_checksum[2]	port_b_checksum[1]	port_b_checksum[0]
0x62	0x00	port c checksum_1	rw	port_c_checksum[7]	port_c_checksum[6]	port_c_checksum[5]	port_c_checksum[4]	port_c_checksum[3]	port_c_checksum[2]	port_c_checksum[1]	port_c_checksum[0]
0x63	0x00	port d checksum_1	rw	port_d_checksum[7]	port_d_checksum[6]	port_d_checksum[5]	port_d_checksum[4]	port_d_checksum[3]	port_d_checksum[2]	port_d_checksum[1]	port_d_checksum[0]
0x70	0xC0	spa location	rw	spa_location[7]	spa_location[6]	spa_location[5]	spa_location[4]	spa_location[3]	spa_location[2]	spa_location[1]	spa_location[0]
0x71	0x00		rw	ksv_list_ready	-	-	-	-	-	-	spa_location_msb
0x72	0x00	irom bist	rw	-	ext_eeprom_tri	ext_eeprom_man_select	ext_eeprom_man_value	-	-	-	-
0x73	0x00		r	-	-	vga_edid_enabled	-	-	-	-	-
0x74	0x00	hdcp edid controls	rw	-	-	-	-	man_edid_d_enable	man_edid_c_enable	man_edid_b_enable	man_edid_a_enable
0x76	0x00	edid debug_2	r	-	-	-	-	edid_d_enabled	edid_c_enabled	edid_b_enabled	edid_a_enabled
0x77	0x00		sc	-	-	-	-	clear_ksv_list	cksum_calc	load_edid	store_edid
0x78	0x00	edid debug_3	sc	-	-	-	-	ksv_list_ready_clr_d	ksv_list_ready_clr_c	ksv_list_ready_clr_b	ksv_list_ready_clr_a
0x79	0x88		rw	man_vga_edid_enable	-	-	-	auto_hdcp_map_enable	hdcp_map_select[2]	hdcp_map_select[1]	hdcp_map_select[0]
0x7A	0x04		rw	-	-	-	-	disable_auto_edid	-	vga_edid_space_sel	hdmi_edid_segment_sel
0x7C	0x00		rw	-	-	spi_cfg[5]	spi_cfg[4]	spi_cfg[3]	spi_cfg[2]	spi_cfg[1]	spi_cfg[0]
0x80	0x00	ksv_0_1	rw	ksv_byte_0[7]	ksv_byte_0[6]	ksv_byte_0[5]	ksv_byte_0[4]	ksv_byte_0[3]	ksv_byte_0[2]	ksv_byte_0[1]	ksv_byte_0[0]
0x81	0x00	ksv_0_2	rw	ksv_byte_1[7]	ksv_byte_1[6]	ksv_byte_1[5]	ksv_byte_1[4]	ksv_byte_1[3]	ksv_byte_1[2]	ksv_byte_1[1]	ksv_byte_1[0]
0x82	0x00	ksv_0_3	rw	ksv_byte_2[7]	ksv_byte_2[6]	ksv_byte_2[5]	ksv_byte_2[4]	ksv_byte_2[3]	ksv_byte_2[2]	ksv_byte_2[1]	ksv_byte_2[0]
0x83	0x00	ksv_0_4	rw	ksv_byte_3[7]	ksv_byte_3[6]	ksv_byte_3[5]	ksv_byte_3[4]	ksv_byte_3[3]	ksv_byte_3[2]	ksv_byte_3[1]	ksv_byte_3[0]
0x84	0x00	ksv_0_5	rw	ksv_byte_4[7]	ksv_byte_4[6]	ksv_byte_4[5]	ksv_byte_4[4]	ksv_byte_4[3]	ksv_byte_4[2]	ksv_byte_4[1]	ksv_byte_4[0]
0x85	0x00	ksv_0_6	rw	ksv_byte_5[7]	ksv_byte_5[6]	ksv_byte_5[5]	ksv_byte_5[4]	ksv_byte_5[3]	ksv_byte_5[2]	ksv_byte_5[1]	ksv_byte_5[0]
0x86	0x00	ksv_0_7	rw	ksv_byte_6[7]	ksv_byte_6[6]	ksv_byte_6[5]	ksv_byte_6[4]	ksv_byte_6[3]	ksv_byte_6[2]	ksv_byte_6[1]	ksv_byte_6[0]
0x87	0x00	ksv_0_8	rw	ksv_byte_7[7]	ksv_byte_7[6]	ksv_byte_7[5]	ksv_byte_7[4]	ksv_byte_7[3]	ksv_byte_7[2]	ksv_byte_7[1]	ksv_byte_7[0]
0x88	0x00	ksv_0_9	rw	ksv_byte_8[7]	ksv_byte_8[6]	ksv_byte_8[5]	ksv_byte_8[4]	ksv_byte_8[3]	ksv_byte_8[2]	ksv_byte_8[1]	ksv_byte_8[0]
0x89	0x00	ksv_0_10	rw	ksv_byte_9[7]	ksv_byte_9[6]	ksv_byte_9[5]	ksv_byte_9[4]	ksv_byte_9[3]	ksv_byte_9[2]	ksv_byte_9[1]	ksv_byte_9[0]
0x8A	0x00	ksv_0_11	rw	ksv_byte_10[7]	ksv_byte_10[6]	ksv_byte_10[5]	ksv_byte_10[4]	ksv_byte_10[3]	ksv_byte_10[2]	ksv_byte_10[1]	ksv_byte_10[0]
0x8B	0x00	ksv_0_12	rw	ksv_byte_11[7]	ksv_byte_11[6]	ksv_byte_11[5]	ksv_byte_11[4]	ksv_byte_11[3]	ksv_byte_11[2]	ksv_byte_11[1]	ksv_byte_11[0]
0x8C	0x00	ksv_0_13	rw	ksv_byte_12[7]	ksv_byte_12[6]	ksv_byte_12[5]	ksv_byte_12[4]	ksv_byte_12[3]	ksv_byte_12[2]	ksv_byte_12[1]	ksv_byte_12[0]
0x8D	0x00	ksv_0_14	rw	ksv_byte_13[7]	ksv_byte_13[6]	ksv_byte_13[5]	ksv_byte_13[4]	ksv_byte_13[3]	ksv_byte_13[2]	ksv_byte_13[1]	ksv_byte_13[0]
0x8E	0x00	ksv_0_15	rw	ksv_byte_14[7]	ksv_byte_14[6]	ksv_byte_14[5]	ksv_byte_14[4]	ksv_byte_14[3]	ksv_byte_14[2]	ksv_byte_14[1]	ksv_byte_14[0]
0x8F	0x00	ksv_0_16	rw	ksv_byte_15[7]	ksv_byte_15[6]	ksv_byte_15[5]	ksv_byte_15[4]	ksv_byte_15[3]	ksv_byte_15[2]	ksv_byte_15[1]	ksv_byte_15[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xEA	0x00	ksv_0_107	rw	ksv_byte_106[7]	ksv_byte_106[6]	ksv_byte_106[5]	ksv_byte_106[4]	ksv_byte_106[3]	ksv_byte_106[2]	ksv_byte_106[1]	ksv_byte_106[0]
0xEB	0x00	ksv_0_108	rw	ksv_byte_107[7]	ksv_byte_107[6]	ksv_byte_107[5]	ksv_byte_107[4]	ksv_byte_107[3]	ksv_byte_107[2]	ksv_byte_107[1]	ksv_byte_107[0]
0xEC	0x00	ksv_0_109	rw	ksv_byte_108[7]	ksv_byte_108[6]	ksv_byte_108[5]	ksv_byte_108[4]	ksv_byte_108[3]	ksv_byte_108[2]	ksv_byte_108[1]	ksv_byte_108[0]
0xED	0x00	ksv_0_110	rw	ksv_byte_109[7]	ksv_byte_109[6]	ksv_byte_109[5]	ksv_byte_109[4]	ksv_byte_109[3]	ksv_byte_109[2]	ksv_byte_109[1]	ksv_byte_109[0]
0xEE	0x00	ksv_0_111	rw	ksv_byte_110[7]	ksv_byte_110[6]	ksv_byte_110[5]	ksv_byte_110[4]	ksv_byte_110[3]	ksv_byte_110[2]	ksv_byte_110[1]	ksv_byte_110[0]
0xEF	0x00	ksv_0_112	rw	ksv_byte_111[7]	ksv_byte_111[6]	ksv_byte_111[5]	ksv_byte_111[4]	ksv_byte_111[3]	ksv_byte_111[2]	ksv_byte_111[1]	ksv_byte_111[0]
0xF0	0x00	ksv_0_113	rw	ksv_byte_112[7]	ksv_byte_112[6]	ksv_byte_112[5]	ksv_byte_112[4]	ksv_byte_112[3]	ksv_byte_112[2]	ksv_byte_112[1]	ksv_byte_112[0]
0xF1	0x00	ksv_0_114	rw	ksv_byte_113[7]	ksv_byte_113[6]	ksv_byte_113[5]	ksv_byte_113[4]	ksv_byte_113[3]	ksv_byte_113[2]	ksv_byte_113[1]	ksv_byte_113[0]
0xF2	0x00	ksv_0_115	rw	ksv_byte_114[7]	ksv_byte_114[6]	ksv_byte_114[5]	ksv_byte_114[4]	ksv_byte_114[3]	ksv_byte_114[2]	ksv_byte_114[1]	ksv_byte_114[0]
0xF3	0x00	ksv_0_116	rw	ksv_byte_115[7]	ksv_byte_115[6]	ksv_byte_115[5]	ksv_byte_115[4]	ksv_byte_115[3]	ksv_byte_115[2]	ksv_byte_115[1]	ksv_byte_115[0]
0xF4	0x00	ksv_0_117	rw	ksv_byte_116[7]	ksv_byte_116[6]	ksv_byte_116[5]	ksv_byte_116[4]	ksv_byte_116[3]	ksv_byte_116[2]	ksv_byte_116[1]	ksv_byte_116[0]
0xF5	0x00	ksv_0_118	rw	ksv_byte_117[7]	ksv_byte_117[6]	ksv_byte_117[5]	ksv_byte_117[4]	ksv_byte_117[3]	ksv_byte_117[2]	ksv_byte_117[1]	ksv_byte_117[0]
0xF6	0x00	ksv_0_119	rw	ksv_byte_118[7]	ksv_byte_118[6]	ksv_byte_118[5]	ksv_byte_118[4]	ksv_byte_118[3]	ksv_byte_118[2]	ksv_byte_118[1]	ksv_byte_118[0]
0xF7	0x00	ksv_0_120	rw	ksv_byte_119[7]	ksv_byte_119[6]	ksv_byte_119[5]	ksv_byte_119[4]	ksv_byte_119[3]	ksv_byte_119[2]	ksv_byte_119[1]	ksv_byte_119[0]
0xF8	0x00	ksv_0_121	rw	ksv_byte_120[7]	ksv_byte_120[6]	ksv_byte_120[5]	ksv_byte_120[4]	ksv_byte_120[3]	ksv_byte_120[2]	ksv_byte_120[1]	ksv_byte_120[0]
0xF9	0x00	ksv_0_122	rw	ksv_byte_121[7]	ksv_byte_121[6]	ksv_byte_121[5]	ksv_byte_121[4]	ksv_byte_121[3]	ksv_byte_121[2]	ksv_byte_121[1]	ksv_byte_121[0]
0xFA	0x00	ksv_0_123	rw	ksv_byte_122[7]	ksv_byte_122[6]	ksv_byte_122[5]	ksv_byte_122[4]	ksv_byte_122[3]	ksv_byte_122[2]	ksv_byte_122[1]	ksv_byte_122[0]
0xFB	0x00	ksv_0_124	rw	ksv_byte_123[7]	ksv_byte_123[6]	ksv_byte_123[5]	ksv_byte_123[4]	ksv_byte_123[3]	ksv_byte_123[2]	ksv_byte_123[1]	ksv_byte_123[0]
0xFC	0x00	ksv_0_125	rw	ksv_byte_124[7]	ksv_byte_124[6]	ksv_byte_124[5]	ksv_byte_124[4]	ksv_byte_124[3]	ksv_byte_124[2]	ksv_byte_124[1]	ksv_byte_124[0]
0xFD	0x00	ksv_0_126	rw	ksv_byte_125[7]	ksv_byte_125[6]	ksv_byte_125[5]	ksv_byte_125[4]	ksv_byte_125[3]	ksv_byte_125[2]	ksv_byte_125[1]	ksv_byte_125[0]
0xFE	0x00	ksv_0_127	rw	ksv_byte_126[7]	ksv_byte_126[6]	ksv_byte_126[5]	ksv_byte_126[4]	ksv_byte_126[3]	ksv_byte_126[2]	ksv_byte_126[1]	ksv_byte_126[0]
0xFF	0x00	ksv_0_128	rw	ksv_byte_127[7]	ksv_byte_127[6]	ksv_byte_127[5]	ksv_byte_127[4]	ksv_byte_127[3]	ksv_byte_127[2]	ksv_byte_127[1]	ksv_byte_127[0]

1.11 ADDR 7C (INFOFRAME)

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00	avi_inf_pb_0_1	r	avi_inf_pb[7]	avi_inf_pb[6]	avi_inf_pb[5]	avi_inf_pb[4]	avi_inf_pb[3]	avi_inf_pb[2]	avi_inf_pb[1]	avi_inf_pb[0]
0x01	0x00	avi_inf_pb_0_2	r	avi_inf_pb[15]	avi_inf_pb[14]	avi_inf_pb[13]	avi_inf_pb[12]	avi_inf_pb[11]	avi_inf_pb[10]	avi_inf_pb[9]	avi_inf_pb[8]
0x02	0x00	avi_inf_pb_0_3	r	avi_inf_pb[23]	avi_inf_pb[22]	avi_inf_pb[21]	avi_inf_pb[20]	avi_inf_pb[19]	avi_inf_pb[18]	avi_inf_pb[17]	avi_inf_pb[16]
0x03	0x00	avi_inf_pb_0_4	r	avi_inf_pb[31]	avi_inf_pb[30]	avi_inf_pb[29]	avi_inf_pb[28]	avi_inf_pb[27]	avi_inf_pb[26]	avi_inf_pb[25]	avi_inf_pb[24]
0x04	0x00	avi_inf_pb_0_5	r	avi_inf_pb[39]	avi_inf_pb[38]	avi_inf_pb[37]	avi_inf_pb[36]	avi_inf_pb[35]	avi_inf_pb[34]	avi_inf_pb[33]	avi_inf_pb[32]
0x05	0x00	avi_inf_pb_0_6	r	avi_inf_pb[47]	avi_inf_pb[46]	avi_inf_pb[45]	avi_inf_pb[44]	avi_inf_pb[43]	avi_inf_pb[42]	avi_inf_pb[41]	avi_inf_pb[40]
0x06	0x00	avi_inf_pb_0_7	r	avi_inf_pb[55]	avi_inf_pb[54]	avi_inf_pb[53]	avi_inf_pb[52]	avi_inf_pb[51]	avi_inf_pb[50]	avi_inf_pb[49]	avi_inf_pb[48]
0x07	0x00	avi_inf_pb_0_8	r	avi_inf_pb[63]	avi_inf_pb[62]	avi_inf_pb[61]	avi_inf_pb[60]	avi_inf_pb[59]	avi_inf_pb[58]	avi_inf_pb[57]	avi_inf_pb[56]
0x08	0x00	avi_inf_pb_0_9	r	avi_inf_pb[71]	avi_inf_pb[70]	avi_inf_pb[69]	avi_inf_pb[68]	avi_inf_pb[67]	avi_inf_pb[66]	avi_inf_pb[65]	avi_inf_pb[64]
0x09	0x00	avi_inf_pb_0_10	r	avi_inf_pb[79]	avi_inf_pb[78]	avi_inf_pb[77]	avi_inf_pb[76]	avi_inf_pb[75]	avi_inf_pb[74]	avi_inf_pb[73]	avi_inf_pb[72]
0x0A	0x00	avi_inf_pb_0_11	r	avi_inf_pb[87]	avi_inf_pb[86]	avi_inf_pb[85]	avi_inf_pb[84]	avi_inf_pb[83]	avi_inf_pb[82]	avi_inf_pb[81]	avi_inf_pb[80]
0x0B	0x00	avi_inf_pb_0_12	r	avi_inf_pb[95]	avi_inf_pb[94]	avi_inf_pb[93]	avi_inf_pb[92]	avi_inf_pb[91]	avi_inf_pb[90]	avi_inf_pb[89]	avi_inf_pb[88]
0x0C	0x00	avi_inf_pb_0_13	r	avi_inf_pb[103]	avi_inf_pb[102]	avi_inf_pb[101]	avi_inf_pb[100]	avi_inf_pb[99]	avi_inf_pb[98]	avi_inf_pb[97]	avi_inf_pb[96]
0x0D	0x00	avi_inf_pb_0_14	r	avi_inf_pb[111]	avi_inf_pb[110]	avi_inf_pb[109]	avi_inf_pb[108]	avi_inf_pb[107]	avi_inf_pb[106]	avi_inf_pb[105]	avi_inf_pb[104]
0x0E	0x00	avi_inf_pb_0_15	r	avi_inf_pb[119]	avi_inf_pb[118]	avi_inf_pb[117]	avi_inf_pb[116]	avi_inf_pb[115]	avi_inf_pb[114]	avi_inf_pb[113]	avi_inf_pb[112]
0x0F	0x00	avi_inf_pb_0_16	r	avi_inf_pb[127]	avi_inf_pb[126]	avi_inf_pb[125]	avi_inf_pb[124]	avi_inf_pb[123]	avi_inf_pb[122]	avi_inf_pb[121]	avi_inf_pb[120]
0x10	0x00	avi_inf_pb_0_17	r	avi_inf_pb[135]	avi_inf_pb[134]	avi_inf_pb[133]	avi_inf_pb[132]	avi_inf_pb[131]	avi_inf_pb[130]	avi_inf_pb[129]	avi_inf_pb[128]
0x11	0x00	avi_inf_pb_0_18	r	avi_inf_pb[143]	avi_inf_pb[142]	avi_inf_pb[141]	avi_inf_pb[140]	avi_inf_pb[139]	avi_inf_pb[138]	avi_inf_pb[137]	avi_inf_pb[136]
0x12	0x00	avi_inf_pb_0_19	r	avi_inf_pb[151]	avi_inf_pb[150]	avi_inf_pb[149]	avi_inf_pb[148]	avi_inf_pb[147]	avi_inf_pb[146]	avi_inf_pb[145]	avi_inf_pb[144]
0x13	0x00	avi_inf_pb_0_20	r	avi_inf_pb[159]	avi_inf_pb[158]	avi_inf_pb[157]	avi_inf_pb[156]	avi_inf_pb[155]	avi_inf_pb[154]	avi_inf_pb[153]	avi_inf_pb[152]
0x14	0x00	avi_inf_pb_0_21	r	avi_inf_pb[167]	avi_inf_pb[166]	avi_inf_pb[165]	avi_inf_pb[164]	avi_inf_pb[163]	avi_inf_pb[162]	avi_inf_pb[161]	avi_inf_pb[160]
0x15	0x00	avi_inf_pb_0_22	r	avi_inf_pb[175]	avi_inf_pb[174]	avi_inf_pb[173]	avi_inf_pb[172]	avi_inf_pb[171]	avi_inf_pb[170]	avi_inf_pb[169]	avi_inf_pb[168]
0x16	0x00	avi_inf_pb_0_23	r	avi_inf_pb[183]	avi_inf_pb[182]	avi_inf_pb[181]	avi_inf_pb[180]	avi_inf_pb[179]	avi_inf_pb[178]	avi_inf_pb[177]	avi_inf_pb[176]
0x17	0x00	avi_inf_pb_0_24	r	avi_inf_pb[191]	avi_inf_pb[190]	avi_inf_pb[189]	avi_inf_pb[188]	avi_inf_pb[187]	avi_inf_pb[186]	avi_inf_pb[185]	avi_inf_pb[184]
0x18	0x00	avi_inf_pb_0_25	r	avi_inf_pb[199]	avi_inf_pb[198]	avi_inf_pb[197]	avi_inf_pb[196]	avi_inf_pb[195]	avi_inf_pb[194]	avi_inf_pb[193]	avi_inf_pb[192]
0x19	0x00	avi_inf_pb_0_26	r	avi_inf_pb[207]	avi_inf_pb[206]	avi_inf_pb[205]	avi_inf_pb[204]	avi_inf_pb[203]	avi_inf_pb[202]	avi_inf_pb[201]	avi_inf_pb[200]
0x1A	0x00	avi_inf_pb_0_27	r	avi_inf_pb[215]	avi_inf_pb[214]	avi_inf_pb[213]	avi_inf_pb[212]	avi_inf_pb[211]	avi_inf_pb[210]	avi_inf_pb[209]	avi_inf_pb[208]
0x1B	0x00	avi_inf_pb_0_28	r	avi_inf_pb[223]	avi_inf_pb[222]	avi_inf_pb[221]	avi_inf_pb[220]	avi_inf_pb[219]	avi_inf_pb[218]	avi_inf_pb[217]	avi_inf_pb[216]
0x1C	0x00	aud_inf_pb_0_1	r	aud_inf_pb[7]	aud_inf_pb[6]	aud_inf_pb[5]	aud_inf_pb[4]	aud_inf_pb[3]	aud_inf_pb[2]	aud_inf_pb[1]	aud_inf_pb[0]
0x1D	0x00	aud_inf_pb_0_2	r	aud_inf_pb[15]	aud_inf_pb[14]	aud_inf_pb[13]	aud_inf_pb[12]	aud_inf_pb[11]	aud_inf_pb[10]	aud_inf_pb[9]	aud_inf_pb[8]
0x1E	0x00	aud_inf_pb_0_3	r	aud_inf_pb[23]	aud_inf_pb[22]	aud_inf_pb[21]	aud_inf_pb[20]	aud_inf_pb[19]	aud_inf_pb[18]	aud_inf_pb[17]	aud_inf_pb[16]
0x1F	0x00	aud_inf_pb_0_4	r	aud_inf_pb[31]	aud_inf_pb[30]	aud_inf_pb[29]	aud_inf_pb[28]	aud_inf_pb[27]	aud_inf_pb[26]	aud_inf_pb[25]	aud_inf_pb[24]
0x20	0x00	aud_inf_pb_0_5	r	aud_inf_pb[39]	aud_inf_pb[38]	aud_inf_pb[37]	aud_inf_pb[36]	aud_inf_pb[35]	aud_inf_pb[34]	aud_inf_pb[33]	aud_inf_pb[32]
0x21	0x00	aud_inf_pb_0_6	r	aud_inf_pb[47]	aud_inf_pb[46]	aud_inf_pb[45]	aud_inf_pb[44]	aud_inf_pb[43]	aud_inf_pb[42]	aud_inf_pb[41]	aud_inf_pb[40]
0x22	0x00	aud_inf_pb_0_7	r	aud_inf_pb[55]	aud_inf_pb[54]	aud_inf_pb[53]	aud_inf_pb[52]	aud_inf_pb[51]	aud_inf_pb[50]	aud_inf_pb[49]	aud_inf_pb[48]
0x23	0x00	aud_inf_pb_0_8	r	aud_inf_pb[63]	aud_inf_pb[62]	aud_inf_pb[61]	aud_inf_pb[60]	aud_inf_pb[59]	aud_inf_pb[58]	aud_inf_pb[57]	aud_inf_pb[56]
0x24	0x00	aud_inf_pb_0_9	r	aud_inf_pb[71]	aud_inf_pb[70]	aud_inf_pb[69]	aud_inf_pb[68]	aud_inf_pb[67]	aud_inf_pb[66]	aud_inf_pb[65]	aud_inf_pb[64]
0x25	0x00	aud_inf_pb_0_10	r	aud_inf_pb[79]	aud_inf_pb[78]	aud_inf_pb[77]	aud_inf_pb[76]	aud_inf_pb[75]	aud_inf_pb[74]	aud_inf_pb[73]	aud_inf_pb[72]
0x26	0x00	aud_inf_pb_0_11	r	aud_inf_pb[87]	aud_inf_pb[86]	aud_inf_pb[85]	aud_inf_pb[84]	aud_inf_pb[83]	aud_inf_pb[82]	aud_inf_pb[81]	aud_inf_pb[80]
0x27	0x00	aud_inf_pb_0_12	r	aud_inf_pb[95]	aud_inf_pb[94]	aud_inf_pb[93]	aud_inf_pb[92]	aud_inf_pb[91]	aud_inf_pb[90]	aud_inf_pb[89]	aud_inf_pb[88]
0x28	0x00	aud_inf_pb_0_13	r	aud_inf_pb[103]	aud_inf_pb[102]	aud_inf_pb[101]	aud_inf_pb[100]	aud_inf_pb[99]	aud_inf_pb[98]	aud_inf_pb[97]	aud_inf_pb[96]
0x29	0x00	aud_inf_pb_0_14	r	aud_inf_pb[111]	aud_inf_pb[110]	aud_inf_pb[109]	aud_inf_pb[108]	aud_inf_pb[107]	aud_inf_pb[106]	aud_inf_pb[105]	aud_inf_pb[104]
0x2A	0x00	spd_inf_pb_0_1	r	spd_inf_pb[7]	spd_inf_pb[6]	spd_inf_pb[5]	spd_inf_pb[4]	spd_inf_pb[3]	spd_inf_pb[2]	spd_inf_pb[1]	spd_inf_pb[0]
0x2B	0x00	spd_inf_pb_0_2	r	spd_inf_pb[15]	spd_inf_pb[14]	spd_inf_pb[13]	spd_inf_pb[12]	spd_inf_pb[11]	spd_inf_pb[10]	spd_inf_pb[9]	spd_inf_pb[8]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x2C	0x00	spd_inf_pb_0_3	r	spd_inf_pb[23]	spd_inf_pb[22]	spd_inf_pb[21]	spd_inf_pb[20]	spd_inf_pb[19]	spd_inf_pb[18]	spd_inf_pb[17]	spd_inf_pb[16]
0x2D	0x00	spd_inf_pb_0_4	r	spd_inf_pb[31]	spd_inf_pb[30]	spd_inf_pb[29]	spd_inf_pb[28]	spd_inf_pb[27]	spd_inf_pb[26]	spd_inf_pb[25]	spd_inf_pb[24]
0x2E	0x00	spd_inf_pb_0_5	r	spd_inf_pb[39]	spd_inf_pb[38]	spd_inf_pb[37]	spd_inf_pb[36]	spd_inf_pb[35]	spd_inf_pb[34]	spd_inf_pb[33]	spd_inf_pb[32]
0x2F	0x00	spd_inf_pb_0_6	r	spd_inf_pb[47]	spd_inf_pb[46]	spd_inf_pb[45]	spd_inf_pb[44]	spd_inf_pb[43]	spd_inf_pb[42]	spd_inf_pb[41]	spd_inf_pb[40]
0x30	0x00	spd_inf_pb_0_7	r	spd_inf_pb[55]	spd_inf_pb[54]	spd_inf_pb[53]	spd_inf_pb[52]	spd_inf_pb[51]	spd_inf_pb[50]	spd_inf_pb[49]	spd_inf_pb[48]
0x31	0x00	spd_inf_pb_0_8	r	spd_inf_pb[63]	spd_inf_pb[62]	spd_inf_pb[61]	spd_inf_pb[60]	spd_inf_pb[59]	spd_inf_pb[58]	spd_inf_pb[57]	spd_inf_pb[56]
0x32	0x00	spd_inf_pb_0_9	r	spd_inf_pb[71]	spd_inf_pb[70]	spd_inf_pb[69]	spd_inf_pb[68]	spd_inf_pb[67]	spd_inf_pb[66]	spd_inf_pb[65]	spd_inf_pb[64]
0x33	0x00	spd_inf_pb_0_10	r	spd_inf_pb[79]	spd_inf_pb[78]	spd_inf_pb[77]	spd_inf_pb[76]	spd_inf_pb[75]	spd_inf_pb[74]	spd_inf_pb[73]	spd_inf_pb[72]
0x34	0x00	spd_inf_pb_0_11	r	spd_inf_pb[87]	spd_inf_pb[86]	spd_inf_pb[85]	spd_inf_pb[84]	spd_inf_pb[83]	spd_inf_pb[82]	spd_inf_pb[81]	spd_inf_pb[80]
0x35	0x00	spd_inf_pb_0_12	r	spd_inf_pb[95]	spd_inf_pb[94]	spd_inf_pb[93]	spd_inf_pb[92]	spd_inf_pb[91]	spd_inf_pb[90]	spd_inf_pb[89]	spd_inf_pb[88]
0x36	0x00	spd_inf_pb_0_13	r	spd_inf_pb[103]	spd_inf_pb[102]	spd_inf_pb[101]	spd_inf_pb[100]	spd_inf_pb[99]	spd_inf_pb[98]	spd_inf_pb[97]	spd_inf_pb[96]
0x37	0x00	spd_inf_pb_0_14	r	spd_inf_pb[111]	spd_inf_pb[110]	spd_inf_pb[109]	spd_inf_pb[108]	spd_inf_pb[107]	spd_inf_pb[106]	spd_inf_pb[105]	spd_inf_pb[104]
0x38	0x00	spd_inf_pb_0_15	r	spd_inf_pb[119]	spd_inf_pb[118]	spd_inf_pb[117]	spd_inf_pb[116]	spd_inf_pb[115]	spd_inf_pb[114]	spd_inf_pb[113]	spd_inf_pb[112]
0x39	0x00	spd_inf_pb_0_16	r	spd_inf_pb[127]	spd_inf_pb[126]	spd_inf_pb[125]	spd_inf_pb[124]	spd_inf_pb[123]	spd_inf_pb[122]	spd_inf_pb[121]	spd_inf_pb[120]
0x3A	0x00	spd_inf_pb_0_17	r	spd_inf_pb[135]	spd_inf_pb[134]	spd_inf_pb[133]	spd_inf_pb[132]	spd_inf_pb[131]	spd_inf_pb[130]	spd_inf_pb[129]	spd_inf_pb[128]
0x3B	0x00	spd_inf_pb_0_18	r	spd_inf_pb[143]	spd_inf_pb[142]	spd_inf_pb[141]	spd_inf_pb[140]	spd_inf_pb[139]	spd_inf_pb[138]	spd_inf_pb[137]	spd_inf_pb[136]
0x3C	0x00	spd_inf_pb_0_19	r	spd_inf_pb[151]	spd_inf_pb[150]	spd_inf_pb[149]	spd_inf_pb[148]	spd_inf_pb[147]	spd_inf_pb[146]	spd_inf_pb[145]	spd_inf_pb[144]
0x3D	0x00	spd_inf_pb_0_20	r	spd_inf_pb[159]	spd_inf_pb[158]	spd_inf_pb[157]	spd_inf_pb[156]	spd_inf_pb[155]	spd_inf_pb[154]	spd_inf_pb[153]	spd_inf_pb[152]
0x3E	0x00	spd_inf_pb_0_21	r	spd_inf_pb[167]	spd_inf_pb[166]	spd_inf_pb[165]	spd_inf_pb[164]	spd_inf_pb[163]	spd_inf_pb[162]	spd_inf_pb[161]	spd_inf_pb[160]
0x3F	0x00	spd_inf_pb_0_22	r	spd_inf_pb[175]	spd_inf_pb[174]	spd_inf_pb[173]	spd_inf_pb[172]	spd_inf_pb[171]	spd_inf_pb[170]	spd_inf_pb[169]	spd_inf_pb[168]
0x40	0x00	spd_inf_pb_0_23	r	spd_inf_pb[183]	spd_inf_pb[182]	spd_inf_pb[181]	spd_inf_pb[180]	spd_inf_pb[179]	spd_inf_pb[178]	spd_inf_pb[177]	spd_inf_pb[176]
0x41	0x00	spd_inf_pb_0_24	r	spd_inf_pb[191]	spd_inf_pb[190]	spd_inf_pb[189]	spd_inf_pb[188]	spd_inf_pb[187]	spd_inf_pb[186]	spd_inf_pb[185]	spd_inf_pb[184]
0x42	0x00	spd_inf_pb_0_25	r	spd_inf_pb[199]	spd_inf_pb[198]	spd_inf_pb[197]	spd_inf_pb[196]	spd_inf_pb[195]	spd_inf_pb[194]	spd_inf_pb[193]	spd_inf_pb[192]
0x43	0x00	spd_inf_pb_0_26	r	spd_inf_pb[207]	spd_inf_pb[206]	spd_inf_pb[205]	spd_inf_pb[204]	spd_inf_pb[203]	spd_inf_pb[202]	spd_inf_pb[201]	spd_inf_pb[200]
0x44	0x00	spd_inf_pb_0_27	r	spd_inf_pb[215]	spd_inf_pb[214]	spd_inf_pb[213]	spd_inf_pb[212]	spd_inf_pb[211]	spd_inf_pb[210]	spd_inf_pb[209]	spd_inf_pb[208]
0x45	0x00	spd_inf_pb_0_28	r	spd_inf_pb[223]	spd_inf_pb[222]	spd_inf_pb[221]	spd_inf_pb[220]	spd_inf_pb[219]	spd_inf_pb[218]	spd_inf_pb[217]	spd_inf_pb[216]
0x46	0x00	ms_inf_pb_0_1	r	ms_inf_pb[7]	ms_inf_pb[6]	ms_inf_pb[5]	ms_inf_pb[4]	ms_inf_pb[3]	ms_inf_pb[2]	ms_inf_pb[1]	ms_inf_pb[0]
0x47	0x00	ms_inf_pb_0_2	r	ms_inf_pb[15]	ms_inf_pb[14]	ms_inf_pb[13]	ms_inf_pb[12]	ms_inf_pb[11]	ms_inf_pb[10]	ms_inf_pb[9]	ms_inf_pb[8]
0x48	0x00	ms_inf_pb_0_3	r	ms_inf_pb[23]	ms_inf_pb[22]	ms_inf_pb[21]	ms_inf_pb[20]	ms_inf_pb[19]	ms_inf_pb[18]	ms_inf_pb[17]	ms_inf_pb[16]
0x49	0x00	ms_inf_pb_0_4	r	ms_inf_pb[31]	ms_inf_pb[30]	ms_inf_pb[29]	ms_inf_pb[28]	ms_inf_pb[27]	ms_inf_pb[26]	ms_inf_pb[25]	ms_inf_pb[24]
0x4A	0x00	ms_inf_pb_0_5	r	ms_inf_pb[39]	ms_inf_pb[38]	ms_inf_pb[37]	ms_inf_pb[36]	ms_inf_pb[35]	ms_inf_pb[34]	ms_inf_pb[33]	ms_inf_pb[32]
0x4B	0x00	ms_inf_pb_0_6	r	ms_inf_pb[47]	ms_inf_pb[46]	ms_inf_pb[45]	ms_inf_pb[44]	ms_inf_pb[43]	ms_inf_pb[42]	ms_inf_pb[41]	ms_inf_pb[40]
0x4C	0x00	ms_inf_pb_0_7	r	ms_inf_pb[55]	ms_inf_pb[54]	ms_inf_pb[53]	ms_inf_pb[52]	ms_inf_pb[51]	ms_inf_pb[50]	ms_inf_pb[49]	ms_inf_pb[48]
0x4D	0x00	ms_inf_pb_0_8	r	ms_inf_pb[63]	ms_inf_pb[62]	ms_inf_pb[61]	ms_inf_pb[60]	ms_inf_pb[59]	ms_inf_pb[58]	ms_inf_pb[57]	ms_inf_pb[56]
0x4E	0x00	ms_inf_pb_0_9	r	ms_inf_pb[71]	ms_inf_pb[70]	ms_inf_pb[69]	ms_inf_pb[68]	ms_inf_pb[67]	ms_inf_pb[66]	ms_inf_pb[65]	ms_inf_pb[64]
0x4F	0x00	ms_inf_pb_0_10	r	ms_inf_pb[79]	ms_inf_pb[78]	ms_inf_pb[77]	ms_inf_pb[76]	ms_inf_pb[75]	ms_inf_pb[74]	ms_inf_pb[73]	ms_inf_pb[72]
0x50	0x00	ms_inf_pb_0_11	r	ms_inf_pb[87]	ms_inf_pb[86]	ms_inf_pb[85]	ms_inf_pb[84]	ms_inf_pb[83]	ms_inf_pb[82]	ms_inf_pb[81]	ms_inf_pb[80]
0x51	0x00	ms_inf_pb_0_12	r	ms_inf_pb[95]	ms_inf_pb[94]	ms_inf_pb[93]	ms_inf_pb[92]	ms_inf_pb[91]	ms_inf_pb[90]	ms_inf_pb[89]	ms_inf_pb[88]
0x52	0x00	ms_inf_pb_0_13	r	ms_inf_pb[103]	ms_inf_pb[102]	ms_inf_pb[101]	ms_inf_pb[100]	ms_inf_pb[99]	ms_inf_pb[98]	ms_inf_pb[97]	ms_inf_pb[96]
0x53	0x00	ms_inf_pb_0_14	r	ms_inf_pb[111]	ms_inf_pb[110]	ms_inf_pb[109]	ms_inf_pb[108]	ms_inf_pb[107]	ms_inf_pb[106]	ms_inf_pb[105]	ms_inf_pb[104]
0x54	0x00	vs_inf_pb_0_1	r	vs_inf_pb[7]	vs_inf_pb[6]	vs_inf_pb[5]	vs_inf_pb[4]	vs_inf_pb[3]	vs_inf_pb[2]	vs_inf_pb[1]	vs_inf_pb[0]
0x55	0x00	vs_inf_pb_0_2	r	vs_inf_pb[15]	vs_inf_pb[14]	vs_inf_pb[13]	vs_inf_pb[12]	vs_inf_pb[11]	vs_inf_pb[10]	vs_inf_pb[9]	vs_inf_pb[8]
0x56	0x00	vs_inf_pb_0_3	r	vs_inf_pb[23]	vs_inf_pb[22]	vs_inf_pb[21]	vs_inf_pb[20]	vs_inf_pb[19]	vs_inf_pb[18]	vs_inf_pb[17]	vs_inf_pb[16]
0x57	0x00	vs_inf_pb_0_4	r	vs_inf_pb[31]	vs_inf_pb[30]	vs_inf_pb[29]	vs_inf_pb[28]	vs_inf_pb[27]	vs_inf_pb[26]	vs_inf_pb[25]	vs_inf_pb[24]
0x58	0x00	vs_inf_pb_0_5	r	vs_inf_pb[39]	vs_inf_pb[38]	vs_inf_pb[37]	vs_inf_pb[36]	vs_inf_pb[35]	vs_inf_pb[34]	vs_inf_pb[33]	vs_inf_pb[32]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x59	0x00	vs_inf_pb_0_6	r	vs_inf_pb[47]	vs_inf_pb[46]	vs_inf_pb[45]	vs_inf_pb[44]	vs_inf_pb[43]	vs_inf_pb[42]	vs_inf_pb[41]	vs_inf_pb[40]
0x5A	0x00	vs_inf_pb_0_7	r	vs_inf_pb[55]	vs_inf_pb[54]	vs_inf_pb[53]	vs_inf_pb[52]	vs_inf_pb[51]	vs_inf_pb[50]	vs_inf_pb[49]	vs_inf_pb[48]
0x5B	0x00	vs_inf_pb_0_8	r	vs_inf_pb[63]	vs_inf_pb[62]	vs_inf_pb[61]	vs_inf_pb[60]	vs_inf_pb[59]	vs_inf_pb[58]	vs_inf_pb[57]	vs_inf_pb[56]
0x5C	0x00	vs_inf_pb_0_9	r	vs_inf_pb[71]	vs_inf_pb[70]	vs_inf_pb[69]	vs_inf_pb[68]	vs_inf_pb[67]	vs_inf_pb[66]	vs_inf_pb[65]	vs_inf_pb[64]
0x5D	0x00	vs_inf_pb_0_10	r	vs_inf_pb[79]	vs_inf_pb[78]	vs_inf_pb[77]	vs_inf_pb[76]	vs_inf_pb[75]	vs_inf_pb[74]	vs_inf_pb[73]	vs_inf_pb[72]
0x5E	0x00	vs_inf_pb_0_11	r	vs_inf_pb[87]	vs_inf_pb[86]	vs_inf_pb[85]	vs_inf_pb[84]	vs_inf_pb[83]	vs_inf_pb[82]	vs_inf_pb[81]	vs_inf_pb[80]
0x5F	0x00	vs_inf_pb_0_12	r	vs_inf_pb[95]	vs_inf_pb[94]	vs_inf_pb[93]	vs_inf_pb[92]	vs_inf_pb[91]	vs_inf_pb[90]	vs_inf_pb[89]	vs_inf_pb[88]
0x60	0x00	vs_inf_pb_0_13	r	vs_inf_pb[103]	vs_inf_pb[102]	vs_inf_pb[101]	vs_inf_pb[100]	vs_inf_pb[99]	vs_inf_pb[98]	vs_inf_pb[97]	vs_inf_pb[96]
0x61	0x00	vs_inf_pb_0_14	r	vs_inf_pb[111]	vs_inf_pb[110]	vs_inf_pb[109]	vs_inf_pb[108]	vs_inf_pb[107]	vs_inf_pb[106]	vs_inf_pb[105]	vs_inf_pb[104]
0x62	0x00	vs_inf_pb_0_15	r	vs_inf_pb[119]	vs_inf_pb[118]	vs_inf_pb[117]	vs_inf_pb[116]	vs_inf_pb[115]	vs_inf_pb[114]	vs_inf_pb[113]	vs_inf_pb[112]
0x63	0x00	vs_inf_pb_0_16	r	vs_inf_pb[127]	vs_inf_pb[126]	vs_inf_pb[125]	vs_inf_pb[124]	vs_inf_pb[123]	vs_inf_pb[122]	vs_inf_pb[121]	vs_inf_pb[120]
0x64	0x00	vs_inf_pb_0_17	r	vs_inf_pb[135]	vs_inf_pb[134]	vs_inf_pb[133]	vs_inf_pb[132]	vs_inf_pb[131]	vs_inf_pb[130]	vs_inf_pb[129]	vs_inf_pb[128]
0x65	0x00	vs_inf_pb_0_18	r	vs_inf_pb[143]	vs_inf_pb[142]	vs_inf_pb[141]	vs_inf_pb[140]	vs_inf_pb[139]	vs_inf_pb[138]	vs_inf_pb[137]	vs_inf_pb[136]
0x66	0x00	vs_inf_pb_0_19	r	vs_inf_pb[151]	vs_inf_pb[150]	vs_inf_pb[149]	vs_inf_pb[148]	vs_inf_pb[147]	vs_inf_pb[146]	vs_inf_pb[145]	vs_inf_pb[144]
0x67	0x00	vs_inf_pb_0_20	r	vs_inf_pb[159]	vs_inf_pb[158]	vs_inf_pb[157]	vs_inf_pb[156]	vs_inf_pb[155]	vs_inf_pb[154]	vs_inf_pb[153]	vs_inf_pb[152]
0x68	0x00	vs_inf_pb_0_21	r	vs_inf_pb[167]	vs_inf_pb[166]	vs_inf_pb[165]	vs_inf_pb[164]	vs_inf_pb[163]	vs_inf_pb[162]	vs_inf_pb[161]	vs_inf_pb[160]
0x69	0x00	vs_inf_pb_0_22	r	vs_inf_pb[175]	vs_inf_pb[174]	vs_inf_pb[173]	vs_inf_pb[172]	vs_inf_pb[171]	vs_inf_pb[170]	vs_inf_pb[169]	vs_inf_pb[168]
0x6A	0x00	vs_inf_pb_0_23	r	vs_inf_pb[183]	vs_inf_pb[182]	vs_inf_pb[181]	vs_inf_pb[180]	vs_inf_pb[179]	vs_inf_pb[178]	vs_inf_pb[177]	vs_inf_pb[176]
0x6B	0x00	vs_inf_pb_0_24	r	vs_inf_pb[191]	vs_inf_pb[190]	vs_inf_pb[189]	vs_inf_pb[188]	vs_inf_pb[187]	vs_inf_pb[186]	vs_inf_pb[185]	vs_inf_pb[184]
0x6C	0x00	vs_inf_pb_0_25	r	vs_inf_pb[199]	vs_inf_pb[198]	vs_inf_pb[197]	vs_inf_pb[196]	vs_inf_pb[195]	vs_inf_pb[194]	vs_inf_pb[193]	vs_inf_pb[192]
0x6D	0x00	vs_inf_pb_0_26	r	vs_inf_pb[207]	vs_inf_pb[206]	vs_inf_pb[205]	vs_inf_pb[204]	vs_inf_pb[203]	vs_inf_pb[202]	vs_inf_pb[201]	vs_inf_pb[200]
0x6E	0x00	vs_inf_pb_0_27	r	vs_inf_pb[215]	vs_inf_pb[214]	vs_inf_pb[213]	vs_inf_pb[212]	vs_inf_pb[211]	vs_inf_pb[210]	vs_inf_pb[209]	vs_inf_pb[208]
0x6F	0x00	vs_inf_pb_0_28	r	vs_inf_pb[223]	vs_inf_pb[222]	vs_inf_pb[221]	vs_inf_pb[220]	vs_inf_pb[219]	vs_inf_pb[218]	vs_inf_pb[217]	vs_inf_pb[216]
0x70	0x00	acp_pb_0_1	r	acp_pb[7]	acp_pb[6]	acp_pb[5]	acp_pb[4]	acp_pb[3]	acp_pb[2]	acp_pb[1]	acp_pb[0]
0x71	0x00	acp_pb_0_2	r	acp_pb[15]	acp_pb[14]	acp_pb[13]	acp_pb[12]	acp_pb[11]	acp_pb[10]	acp_pb[9]	acp_pb[8]
0x72	0x00	acp_pb_0_3	r	acp_pb[23]	acp_pb[22]	acp_pb[21]	acp_pb[20]	acp_pb[19]	acp_pb[18]	acp_pb[17]	acp_pb[16]
0x73	0x00	acp_pb_0_4	r	acp_pb[31]	acp_pb[30]	acp_pb[29]	acp_pb[28]	acp_pb[27]	acp_pb[26]	acp_pb[25]	acp_pb[24]
0x74	0x00	acp_pb_0_5	r	acp_pb[39]	acp_pb[38]	acp_pb[37]	acp_pb[36]	acp_pb[35]	acp_pb[34]	acp_pb[33]	acp_pb[32]
0x75	0x00	acp_pb_0_6	r	acp_pb[47]	acp_pb[46]	acp_pb[45]	acp_pb[44]	acp_pb[43]	acp_pb[42]	acp_pb[41]	acp_pb[40]
0x76	0x00	acp_pb_0_7	r	acp_pb[55]	acp_pb[54]	acp_pb[53]	acp_pb[52]	acp_pb[51]	acp_pb[50]	acp_pb[49]	acp_pb[48]
0x77	0x00	acp_pb_0_8	r	acp_pb[63]	acp_pb[62]	acp_pb[61]	acp_pb[60]	acp_pb[59]	acp_pb[58]	acp_pb[57]	acp_pb[56]
0x78	0x00	acp_pb_0_9	r	acp_pb[71]	acp_pb[70]	acp_pb[69]	acp_pb[68]	acp_pb[67]	acp_pb[66]	acp_pb[65]	acp_pb[64]
0x79	0x00	acp_pb_0_10	r	acp_pb[79]	acp_pb[78]	acp_pb[77]	acp_pb[76]	acp_pb[75]	acp_pb[74]	acp_pb[73]	acp_pb[72]
0x7A	0x00	acp_pb_0_11	r	acp_pb[87]	acp_pb[86]	acp_pb[85]	acp_pb[84]	acp_pb[83]	acp_pb[82]	acp_pb[81]	acp_pb[80]
0x7B	0x00	acp_pb_0_12	r	acp_pb[95]	acp_pb[94]	acp_pb[93]	acp_pb[92]	acp_pb[91]	acp_pb[90]	acp_pb[89]	acp_pb[88]
0x7C	0x00	acp_pb_0_13	r	acp_pb[103]	acp_pb[102]	acp_pb[101]	acp_pb[100]	acp_pb[99]	acp_pb[98]	acp_pb[97]	acp_pb[96]
0x7D	0x00	acp_pb_0_14	r	acp_pb[111]	acp_pb[110]	acp_pb[109]	acp_pb[108]	acp_pb[107]	acp_pb[106]	acp_pb[105]	acp_pb[104]
0x7E	0x00	acp_pb_0_15	r	acp_pb[119]	acp_pb[118]	acp_pb[117]	acp_pb[116]	acp_pb[115]	acp_pb[114]	acp_pb[113]	acp_pb[112]
0x7F	0x00	acp_pb_0_16	r	acp_pb[127]	acp_pb[126]	acp_pb[125]	acp_pb[124]	acp_pb[123]	acp_pb[122]	acp_pb[121]	acp_pb[120]
0x80	0x00	acp_pb_0_17	r	acp_pb[135]	acp_pb[134]	acp_pb[133]	acp_pb[132]	acp_pb[131]	acp_pb[130]	acp_pb[129]	acp_pb[128]
0x81	0x00	acp_pb_0_18	r	acp_pb[143]	acp_pb[142]	acp_pb[141]	acp_pb[140]	acp_pb[139]	acp_pb[138]	acp_pb[137]	acp_pb[136]
0x82	0x00	acp_pb_0_19	r	acp_pb[151]	acp_pb[150]	acp_pb[149]	acp_pb[148]	acp_pb[147]	acp_pb[146]	acp_pb[145]	acp_pb[144]
0x83	0x00	acp_pb_0_20	r	acp_pb[159]	acp_pb[158]	acp_pb[157]	acp_pb[156]	acp_pb[155]	acp_pb[154]	acp_pb[153]	acp_pb[152]
0x84	0x00	acp_pb_0_21	r	acp_pb[167]	acp_pb[166]	acp_pb[165]	acp_pb[164]	acp_pb[163]	acp_pb[162]	acp_pb[161]	acp_pb[160]
0x85	0x00	acp_pb_0_22	r	acp_pb[175]	acp_pb[174]	acp_pb[173]	acp_pb[172]	acp_pb[171]	acp_pb[170]	acp_pb[169]	acp_pb[168]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x86	0x00	acp_pb_0_23	r	acp_pb[183]	acp_pb[182]	acp_pb[181]	acp_pb[180]	acp_pb[179]	acp_pb[178]	acp_pb[177]	acp_pb[176]
0x87	0x00	acp_pb_0_24	r	acp_pb[191]	acp_pb[190]	acp_pb[189]	acp_pb[188]	acp_pb[187]	acp_pb[186]	acp_pb[185]	acp_pb[184]
0x88	0x00	acp_pb_0_25	r	acp_pb[199]	acp_pb[198]	acp_pb[197]	acp_pb[196]	acp_pb[195]	acp_pb[194]	acp_pb[193]	acp_pb[192]
0x89	0x00	acp_pb_0_26	r	acp_pb[207]	acp_pb[206]	acp_pb[205]	acp_pb[204]	acp_pb[203]	acp_pb[202]	acp_pb[201]	acp_pb[200]
0x8A	0x00	acp_pb_0_27	r	acp_pb[215]	acp_pb[214]	acp_pb[213]	acp_pb[212]	acp_pb[211]	acp_pb[210]	acp_pb[209]	acp_pb[208]
0x8B	0x00	acp_pb_0_28	r	acp_pb[223]	acp_pb[222]	acp_pb[221]	acp_pb[220]	acp_pb[219]	acp_pb[218]	acp_pb[217]	acp_pb[216]
0x8C	0x00	isrc1_pb_0_1	r	isrc1_pb[7]	isrc1_pb[6]	isrc1_pb[5]	isrc1_pb[4]	isrc1_pb[3]	isrc1_pb[2]	isrc1_pb[1]	isrc1_pb[0]
0x8D	0x00	isrc1_pb_0_2	r	isrc1_pb[15]	isrc1_pb[14]	isrc1_pb[13]	isrc1_pb[12]	isrc1_pb[11]	isrc1_pb[10]	isrc1_pb[9]	isrc1_pb[8]
0x8E	0x00	isrc1_pb_0_3	r	isrc1_pb[23]	isrc1_pb[22]	isrc1_pb[21]	isrc1_pb[20]	isrc1_pb[19]	isrc1_pb[18]	isrc1_pb[17]	isrc1_pb[16]
0x8F	0x00	isrc1_pb_0_4	r	isrc1_pb[31]	isrc1_pb[30]	isrc1_pb[29]	isrc1_pb[28]	isrc1_pb[27]	isrc1_pb[26]	isrc1_pb[25]	isrc1_pb[24]
0x90	0x00	isrc1_pb_0_5	r	isrc1_pb[39]	isrc1_pb[38]	isrc1_pb[37]	isrc1_pb[36]	isrc1_pb[35]	isrc1_pb[34]	isrc1_pb[33]	isrc1_pb[32]
0x91	0x00	isrc1_pb_0_6	r	isrc1_pb[47]	isrc1_pb[46]	isrc1_pb[45]	isrc1_pb[44]	isrc1_pb[43]	isrc1_pb[42]	isrc1_pb[41]	isrc1_pb[40]
0x92	0x00	isrc1_pb_0_7	r	isrc1_pb[55]	isrc1_pb[54]	isrc1_pb[53]	isrc1_pb[52]	isrc1_pb[51]	isrc1_pb[50]	isrc1_pb[49]	isrc1_pb[48]
0x93	0x00	isrc1_pb_0_8	r	isrc1_pb[63]	isrc1_pb[62]	isrc1_pb[61]	isrc1_pb[60]	isrc1_pb[59]	isrc1_pb[58]	isrc1_pb[57]	isrc1_pb[56]
0x94	0x00	isrc1_pb_0_9	r	isrc1_pb[71]	isrc1_pb[70]	isrc1_pb[69]	isrc1_pb[68]	isrc1_pb[67]	isrc1_pb[66]	isrc1_pb[65]	isrc1_pb[64]
0x95	0x00	isrc1_pb_0_10	r	isrc1_pb[79]	isrc1_pb[78]	isrc1_pb[77]	isrc1_pb[76]	isrc1_pb[75]	isrc1_pb[74]	isrc1_pb[73]	isrc1_pb[72]
0x96	0x00	isrc1_pb_0_11	r	isrc1_pb[87]	isrc1_pb[86]	isrc1_pb[85]	isrc1_pb[84]	isrc1_pb[83]	isrc1_pb[82]	isrc1_pb[81]	isrc1_pb[80]
0x97	0x00	isrc1_pb_0_12	r	isrc1_pb[95]	isrc1_pb[94]	isrc1_pb[93]	isrc1_pb[92]	isrc1_pb[91]	isrc1_pb[90]	isrc1_pb[89]	isrc1_pb[88]
0x98	0x00	isrc1_pb_0_13	r	isrc1_pb[103]	isrc1_pb[102]	isrc1_pb[101]	isrc1_pb[100]	isrc1_pb[99]	isrc1_pb[98]	isrc1_pb[97]	isrc1_pb[96]
0x99	0x00	isrc1_pb_0_14	r	isrc1_pb[111]	isrc1_pb[110]	isrc1_pb[109]	isrc1_pb[108]	isrc1_pb[107]	isrc1_pb[106]	isrc1_pb[105]	isrc1_pb[104]
0x9A	0x00	isrc1_pb_0_15	r	isrc1_pb[119]	isrc1_pb[118]	isrc1_pb[117]	isrc1_pb[116]	isrc1_pb[115]	isrc1_pb[114]	isrc1_pb[113]	isrc1_pb[112]
0x9B	0x00	isrc1_pb_0_16	r	isrc1_pb[127]	isrc1_pb[126]	isrc1_pb[125]	isrc1_pb[124]	isrc1_pb[123]	isrc1_pb[122]	isrc1_pb[121]	isrc1_pb[120]
0x9C	0x00	isrc1_pb_0_17	r	isrc1_pb[135]	isrc1_pb[134]	isrc1_pb[133]	isrc1_pb[132]	isrc1_pb[131]	isrc1_pb[130]	isrc1_pb[129]	isrc1_pb[128]
0x9D	0x00	isrc1_pb_0_18	r	isrc1_pb[143]	isrc1_pb[142]	isrc1_pb[141]	isrc1_pb[140]	isrc1_pb[139]	isrc1_pb[138]	isrc1_pb[137]	isrc1_pb[136]
0x9E	0x00	isrc1_pb_0_19	r	isrc1_pb[151]	isrc1_pb[150]	isrc1_pb[149]	isrc1_pb[148]	isrc1_pb[147]	isrc1_pb[146]	isrc1_pb[145]	isrc1_pb[144]
0x9F	0x00	isrc1_pb_0_20	r	isrc1_pb[159]	isrc1_pb[158]	isrc1_pb[157]	isrc1_pb[156]	isrc1_pb[155]	isrc1_pb[154]	isrc1_pb[153]	isrc1_pb[152]
0xA0	0x00	isrc1_pb_0_21	r	isrc1_pb[167]	isrc1_pb[166]	isrc1_pb[165]	isrc1_pb[164]	isrc1_pb[163]	isrc1_pb[162]	isrc1_pb[161]	isrc1_pb[160]
0xA1	0x00	isrc1_pb_0_22	r	isrc1_pb[175]	isrc1_pb[174]	isrc1_pb[173]	isrc1_pb[172]	isrc1_pb[171]	isrc1_pb[170]	isrc1_pb[169]	isrc1_pb[168]
0xA2	0x00	isrc1_pb_0_23	r	isrc1_pb[183]	isrc1_pb[182]	isrc1_pb[181]	isrc1_pb[180]	isrc1_pb[179]	isrc1_pb[178]	isrc1_pb[177]	isrc1_pb[176]
0xA3	0x00	isrc1_pb_0_24	r	isrc1_pb[191]	isrc1_pb[190]	isrc1_pb[189]	isrc1_pb[188]	isrc1_pb[187]	isrc1_pb[186]	isrc1_pb[185]	isrc1_pb[184]
0xA4	0x00	isrc1_pb_0_25	r	isrc1_pb[199]	isrc1_pb[198]	isrc1_pb[197]	isrc1_pb[196]	isrc1_pb[195]	isrc1_pb[194]	isrc1_pb[193]	isrc1_pb[192]
0xA5	0x00	isrc1_pb_0_26	r	isrc1_pb[207]	isrc1_pb[206]	isrc1_pb[205]	isrc1_pb[204]	isrc1_pb[203]	isrc1_pb[202]	isrc1_pb[201]	isrc1_pb[200]
0xA6	0x00	isrc1_pb_0_27	r	isrc1_pb[215]	isrc1_pb[214]	isrc1_pb[213]	isrc1_pb[212]	isrc1_pb[211]	isrc1_pb[210]	isrc1_pb[209]	isrc1_pb[208]
0xA7	0x00	isrc1_pb_0_28	r	isrc1_pb[223]	isrc1_pb[222]	isrc1_pb[221]	isrc1_pb[220]	isrc1_pb[219]	isrc1_pb[218]	isrc1_pb[217]	isrc1_pb[216]
0xA8	0x00	isrc2_pb_0_1	r	isrc2_pb[7]	isrc2_pb[6]	isrc2_pb[5]	isrc2_pb[4]	isrc2_pb[3]	isrc2_pb[2]	isrc2_pb[1]	isrc2_pb[0]
0xA9	0x00	isrc2_pb_0_2	r	isrc2_pb[15]	isrc2_pb[14]	isrc2_pb[13]	isrc2_pb[12]	isrc2_pb[11]	isrc2_pb[10]	isrc2_pb[9]	isrc2_pb[8]
0xAA	0x00	isrc2_pb_0_3	r	isrc2_pb[23]	isrc2_pb[22]	isrc2_pb[21]	isrc2_pb[20]	isrc2_pb[19]	isrc2_pb[18]	isrc2_pb[17]	isrc2_pb[16]
0xAB	0x00	isrc2_pb_0_4	r	isrc2_pb[31]	isrc2_pb[30]	isrc2_pb[29]	isrc2_pb[28]	isrc2_pb[27]	isrc2_pb[26]	isrc2_pb[25]	isrc2_pb[24]
0xAC	0x00	isrc2_pb_0_5	r	isrc2_pb[39]	isrc2_pb[38]	isrc2_pb[37]	isrc2_pb[36]	isrc2_pb[35]	isrc2_pb[34]	isrc2_pb[33]	isrc2_pb[32]
0xAD	0x00	isrc2_pb_0_6	r	isrc2_pb[47]	isrc2_pb[46]	isrc2_pb[45]	isrc2_pb[44]	isrc2_pb[43]	isrc2_pb[42]	isrc2_pb[41]	isrc2_pb[40]
0xAE	0x00	isrc2_pb_0_7	r	isrc2_pb[55]	isrc2_pb[54]	isrc2_pb[53]	isrc2_pb[52]	isrc2_pb[51]	isrc2_pb[50]	isrc2_pb[49]	isrc2_pb[48]
0xAF	0x00	isrc2_pb_0_8	r	isrc2_pb[63]	isrc2_pb[62]	isrc2_pb[61]	isrc2_pb[60]	isrc2_pb[59]	isrc2_pb[58]	isrc2_pb[57]	isrc2_pb[56]
0xB0	0x00	isrc2_pb_0_9	r	isrc2_pb[71]	isrc2_pb[70]	isrc2_pb[69]	isrc2_pb[68]	isrc2_pb[67]	isrc2_pb[66]	isrc2_pb[65]	isrc2_pb[64]
0xB1	0x00	isrc2_pb_0_10	r	isrc2_pb[79]	isrc2_pb[78]	isrc2_pb[77]	isrc2_pb[76]	isrc2_pb[75]	isrc2_pb[74]	isrc2_pb[73]	isrc2_pb[72]
0xB2	0x00	isrc2_pb_0_11	r	isrc2_pb[87]	isrc2_pb[86]	isrc2_pb[85]	isrc2_pb[84]	isrc2_pb[83]	isrc2_pb[82]	isrc2_pb[81]	isrc2_pb[80]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xB3	0x00	isrc2_pb_0_12	r	isrc2_pb[95]	isrc2_pb[94]	isrc2_pb[93]	isrc2_pb[92]	isrc2_pb[91]	isrc2_pb[90]	isrc2_pb[89]	isrc2_pb[88]
0xB4	0x00	isrc2_pb_0_13	r	isrc2_pb[103]	isrc2_pb[102]	isrc2_pb[101]	isrc2_pb[100]	isrc2_pb[99]	isrc2_pb[98]	isrc2_pb[97]	isrc2_pb[96]
0xB5	0x00	isrc2_pb_0_14	r	isrc2_pb[111]	isrc2_pb[110]	isrc2_pb[109]	isrc2_pb[108]	isrc2_pb[107]	isrc2_pb[106]	isrc2_pb[105]	isrc2_pb[104]
0xB6	0x00	isrc2_pb_0_15	r	isrc2_pb[119]	isrc2_pb[118]	isrc2_pb[117]	isrc2_pb[116]	isrc2_pb[115]	isrc2_pb[114]	isrc2_pb[113]	isrc2_pb[112]
0xB7	0x00	isrc2_pb_0_16	r	isrc2_pb[127]	isrc2_pb[126]	isrc2_pb[125]	isrc2_pb[124]	isrc2_pb[123]	isrc2_pb[122]	isrc2_pb[121]	isrc2_pb[120]
0xB8	0x00	isrc2_pb_0_17	r	isrc2_pb[135]	isrc2_pb[134]	isrc2_pb[133]	isrc2_pb[132]	isrc2_pb[131]	isrc2_pb[130]	isrc2_pb[129]	isrc2_pb[128]
0xB9	0x00	isrc2_pb_0_18	r	isrc2_pb[143]	isrc2_pb[142]	isrc2_pb[141]	isrc2_pb[140]	isrc2_pb[139]	isrc2_pb[138]	isrc2_pb[137]	isrc2_pb[136]
0xBA	0x00	isrc2_pb_0_19	r	isrc2_pb[151]	isrc2_pb[150]	isrc2_pb[149]	isrc2_pb[148]	isrc2_pb[147]	isrc2_pb[146]	isrc2_pb[145]	isrc2_pb[144]
0xBB	0x00	isrc2_pb_0_20	r	isrc2_pb[159]	isrc2_pb[158]	isrc2_pb[157]	isrc2_pb[156]	isrc2_pb[155]	isrc2_pb[154]	isrc2_pb[153]	isrc2_pb[152]
0xBC	0x00	isrc2_pb_0_21	r	isrc2_pb[167]	isrc2_pb[166]	isrc2_pb[165]	isrc2_pb[164]	isrc2_pb[163]	isrc2_pb[162]	isrc2_pb[161]	isrc2_pb[160]
0xBD	0x00	isrc2_pb_0_22	r	isrc2_pb[175]	isrc2_pb[174]	isrc2_pb[173]	isrc2_pb[172]	isrc2_pb[171]	isrc2_pb[170]	isrc2_pb[169]	isrc2_pb[168]
0xBE	0x00	isrc2_pb_0_23	r	isrc2_pb[183]	isrc2_pb[182]	isrc2_pb[181]	isrc2_pb[180]	isrc2_pb[179]	isrc2_pb[178]	isrc2_pb[177]	isrc2_pb[176]
0xBF	0x00	isrc2_pb_0_24	r	isrc2_pb[191]	isrc2_pb[190]	isrc2_pb[189]	isrc2_pb[188]	isrc2_pb[187]	isrc2_pb[186]	isrc2_pb[185]	isrc2_pb[184]
0xC0	0x00	isrc2_pb_0_25	r	isrc2_pb[199]	isrc2_pb[198]	isrc2_pb[197]	isrc2_pb[196]	isrc2_pb[195]	isrc2_pb[194]	isrc2_pb[193]	isrc2_pb[192]
0xC1	0x00	isrc2_pb_0_26	r	isrc2_pb[207]	isrc2_pb[206]	isrc2_pb[205]	isrc2_pb[204]	isrc2_pb[203]	isrc2_pb[202]	isrc2_pb[201]	isrc2_pb[200]
0xC2	0x00	isrc2_pb_0_27	r	isrc2_pb[215]	isrc2_pb[214]	isrc2_pb[213]	isrc2_pb[212]	isrc2_pb[211]	isrc2_pb[210]	isrc2_pb[209]	isrc2_pb[208]
0xC3	0x00	isrc2_pb_0_28	r	isrc2_pb[223]	isrc2_pb[222]	isrc2_pb[221]	isrc2_pb[220]	isrc2_pb[219]	isrc2_pb[218]	isrc2_pb[217]	isrc2_pb[216]
0xC4	0x00	gamut_mdata_pb_0_1	r	gbd[7]	gbd[6]	gbd[5]	gbd[4]	gbd[3]	gbd[2]	gbd[1]	gbd[0]
0xC5	0x00	gamut_mdata_pb_0_2	r	gbd[15]	gbd[14]	gbd[13]	gbd[12]	gbd[11]	gbd[10]	gbd[9]	gbd[8]
0xC6	0x00	gamut_mdata_pb_0_3	r	gbd[23]	gbd[22]	gbd[21]	gbd[20]	gbd[19]	gbd[18]	gbd[17]	gbd[16]
0xC7	0x00	gamut_mdata_pb_0_4	r	gbd[31]	gbd[30]	gbd[29]	gbd[28]	gbd[27]	gbd[26]	gbd[25]	gbd[24]
0xC8	0x00	gamut_mdata_pb_0_5	r	gbd[39]	gbd[38]	gbd[37]	gbd[36]	gbd[35]	gbd[34]	gbd[33]	gbd[32]
0xC9	0x00	gamut_mdata_pb_0_6	r	gbd[47]	gbd[46]	gbd[45]	gbd[44]	gbd[43]	gbd[42]	gbd[41]	gbd[40]
0xCA	0x00	gamut_mdata_pb_0_7	r	gbd[55]	gbd[54]	gbd[53]	gbd[52]	gbd[51]	gbd[50]	gbd[49]	gbd[48]
0xCB	0x00	gamut_mdata_pb_0_8	r	gbd[63]	gbd[62]	gbd[61]	gbd[60]	gbd[59]	gbd[58]	gbd[57]	gbd[56]
0xCC	0x00	gamut_mdata_pb_0_9	r	gbd[71]	gbd[70]	gbd[69]	gbd[68]	gbd[67]	gbd[66]	gbd[65]	gbd[64]
0xCD	0x00	gamut_mdata_pb_0_10	r	gbd[79]	gbd[78]	gbd[77]	gbd[76]	gbd[75]	gbd[74]	gbd[73]	gbd[72]
0xCE	0x00	gamut_mdata_pb_0_11	r	gbd[87]	gbd[86]	gbd[85]	gbd[84]	gbd[83]	gbd[82]	gbd[81]	gbd[80]
0xCF	0x00	gamut_mdata_pb_0_12	r	gbd[95]	gbd[94]	gbd[93]	gbd[92]	gbd[91]	gbd[90]	gbd[89]	gbd[88]
0xD0	0x00	gamut_mdata_pb_0_13	r	gbd[103]	gbd[102]	gbd[101]	gbd[100]	gbd[99]	gbd[98]	gbd[97]	gbd[96]
0xD1	0x00	gamut_mdata_pb_0_14	r	gbd[111]	gbd[110]	gbd[109]	gbd[108]	gbd[107]	gbd[106]	gbd[105]	gbd[104]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xD2	0x00	gamut_mdata_pb_0_15	r	gbd[119]	gbd[118]	gbd[117]	gbd[116]	gbd[115]	gbd[114]	gbd[113]	gbd[112]
0xD3	0x00	gamut_mdata_pb_0_16	r	gbd[127]	gbd[126]	gbd[125]	gbd[124]	gbd[123]	gbd[122]	gbd[121]	gbd[120]
0xD4	0x00	gamut_mdata_pb_0_17	r	gbd[135]	gbd[134]	gbd[133]	gbd[132]	gbd[131]	gbd[130]	gbd[129]	gbd[128]
0xD5	0x00	gamut_mdata_pb_0_18	r	gbd[143]	gbd[142]	gbd[141]	gbd[140]	gbd[139]	gbd[138]	gbd[137]	gbd[136]
0xD6	0x00	gamut_mdata_pb_0_19	r	gbd[151]	gbd[150]	gbd[149]	gbd[148]	gbd[147]	gbd[146]	gbd[145]	gbd[144]
0xD7	0x00	gamut_mdata_pb_0_20	r	gbd[159]	gbd[158]	gbd[157]	gbd[156]	gbd[155]	gbd[154]	gbd[153]	gbd[152]
0xD8	0x00	gamut_mdata_pb_0_21	r	gbd[167]	gbd[166]	gbd[165]	gbd[164]	gbd[163]	gbd[162]	gbd[161]	gbd[160]
0xD9	0x00	gamut_mdata_pb_0_22	r	gbd[175]	gbd[174]	gbd[173]	gbd[172]	gbd[171]	gbd[170]	gbd[169]	gbd[168]
0xDA	0x00	gamut_mdata_pb_0_23	r	gbd[183]	gbd[182]	gbd[181]	gbd[180]	gbd[179]	gbd[178]	gbd[177]	gbd[176]
0xDB	0x00	gamut_mdata_pb_0_24	r	gbd[191]	gbd[190]	gbd[189]	gbd[188]	gbd[187]	gbd[186]	gbd[185]	gbd[184]
0xDC	0x00	gamut_mdata_pb_0_25	r	gbd[199]	gbd[198]	gbd[197]	gbd[196]	gbd[195]	gbd[194]	gbd[193]	gbd[192]
0xDD	0x00	gamut_mdata_pb_0_26	r	gbd[207]	gbd[206]	gbd[205]	gbd[204]	gbd[203]	gbd[202]	gbd[201]	gbd[200]
0xDE	0x00	gamut_mdata_pb_0_27	r	gbd[215]	gbd[214]	gbd[213]	gbd[212]	gbd[211]	gbd[210]	gbd[209]	gbd[208]
0xDF	0x00	gamut_mdata_pb_0_28	r	gbd[223]	gbd[222]	gbd[221]	gbd[220]	gbd[219]	gbd[218]	gbd[217]	gbd[216]
0xE0	0x82	avi_packet_id	rw	avi_packet_id[7]	avi_packet_id[6]	avi_packet_id[5]	avi_packet_id[4]	avi_packet_id[3]	avi_packet_id[2]	avi_packet_id[1]	avi_packet_id[0]
0xE1	0x00	avi_inf_vers	r	avi_inf_vers[7]	avi_inf_vers[6]	avi_inf_vers[5]	avi_inf_vers[4]	avi_inf_vers[3]	avi_inf_vers[2]	avi_inf_vers[1]	avi_inf_vers[0]
0xE2	0x00	avi_inf_len	r	avi_inf_len[7]	avi_inf_len[6]	avi_inf_len[5]	avi_inf_len[4]	avi_inf_len[3]	avi_inf_len[2]	avi_inf_len[1]	avi_inf_len[0]
0xE3	0x84	aud_packet_id	rw	aud_packet_id[7]	aud_packet_id[6]	aud_packet_id[5]	aud_packet_id[4]	aud_packet_id[3]	aud_packet_id[2]	aud_packet_id[1]	aud_packet_id[0]
0xE4	0x00	aud_inf_vers	r	aud_inf_vers[7]	aud_inf_vers[6]	aud_inf_vers[5]	aud_inf_vers[4]	aud_inf_vers[3]	aud_inf_vers[2]	aud_inf_vers[1]	aud_inf_vers[0]
0xE5	0x00	aud_inf_len	r	aud_inf_len[7]	aud_inf_len[6]	aud_inf_len[5]	aud_inf_len[4]	aud_inf_len[3]	aud_inf_len[2]	aud_inf_len[1]	aud_inf_len[0]
0xE6	0x83	spd_packet_id	rw	spd_packet_id[7]	spd_packet_id[6]	spd_packet_id[5]	spd_packet_id[4]	spd_packet_id[3]	spd_packet_id[2]	spd_packet_id[1]	spd_packet_id[0]
0xE7	0x00	spd_inf_vers	r	spd_inf_vers[7]	spd_inf_vers[6]	spd_inf_vers[5]	spd_inf_vers[4]	spd_inf_vers[3]	spd_inf_vers[2]	spd_inf_vers[1]	spd_inf_vers[0]
0xE8	0x00	spd_inf_len	r	spd_inf_len[7]	spd_inf_len[6]	spd_inf_len[5]	spd_inf_len[4]	spd_inf_len[3]	spd_inf_len[2]	spd_inf_len[1]	spd_inf_len[0]
0xE9	0x85	ms_packet_id	rw	ms_packet_id[7]	ms_packet_id[6]	ms_packet_id[5]	ms_packet_id[4]	ms_packet_id[3]	ms_packet_id[2]	ms_packet_id[1]	ms_packet_id[0]
0xEA	0x00	ms_inf_vers	r	ms_inf_vers[7]	ms_inf_vers[6]	ms_inf_vers[5]	ms_inf_vers[4]	ms_inf_vers[3]	ms_inf_vers[2]	ms_inf_vers[1]	ms_inf_vers[0]
0xEB	0x00	ms_inf_len	r	ms_inf_len[7]	ms_inf_len[6]	ms_inf_len[5]	ms_inf_len[4]	ms_inf_len[3]	ms_inf_len[2]	ms_inf_len[1]	ms_inf_len[0]
0xEC	0x81	vs_packet_id	rw	vs_packet_id[7]	vs_packet_id[6]	vs_packet_id[5]	vs_packet_id[4]	vs_packet_id[3]	vs_packet_id[2]	vs_packet_id[1]	vs_packet_id[0]
0xED	0x00	vs_inf_vers	r	vs_inf_vers[7]	vs_inf_vers[6]	vs_inf_vers[5]	vs_inf_vers[4]	vs_inf_vers[3]	vs_inf_vers[2]	vs_inf_vers[1]	vs_inf_vers[0]
0xEE	0x00	vs_inf_len	r	vs_inf_len[7]	vs_inf_len[6]	vs_inf_len[5]	vs_inf_len[4]	vs_inf_len[3]	vs_inf_len[2]	vs_inf_len[1]	vs_inf_len[0]
0xEF	0x04	acp_packet_id	rw	acp_packet_id[7]	acp_packet_id[6]	acp_packet_id[5]	acp_packet_id[4]	acp_packet_id[3]	acp_packet_id[2]	acp_packet_id[1]	acp_packet_id[0]
0xF0	0x00	acp_type	r	acp_type[7]	acp_type[6]	acp_type[5]	acp_type[4]	acp_type[3]	acp_type[2]	acp_type[1]	acp_type[0]
0xF1	0x00	acp_header2	r	acp_header2[7]	acp_header2[6]	acp_header2[5]	acp_header2[4]	acp_header2[3]	acp_header2[2]	acp_header2[1]	acp_header2[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xF2	0x05	isrc1_packet_id	rw	isrc1_packet_id[7]	isrc1_packet_id[6]	isrc1_packet_id[5]	isrc1_packet_id[4]	isrc1_packet_id[3]	isrc1_packet_id[2]	isrc1_packet_id[1]	isrc1_packet_id[0]
0xF3	0x00	isrc1_header1	r	isrc1_header1[7]	isrc1_header1[6]	isrc1_header1[5]	isrc1_header1[4]	isrc1_header1[3]	isrc1_header1[2]	isrc1_header1[1]	isrc1_header1[0]
0xF4	0x00	isrc1_header2	r	isrc1_header2[7]	isrc1_header2[6]	isrc1_header2[5]	isrc1_header2[4]	isrc1_header2[3]	isrc1_header2[2]	isrc1_header2[1]	isrc1_header2[0]
0xF5	0x06	isrc2_packet_id	rw	isrc2_packet_id[7]	isrc2_packet_id[6]	isrc2_packet_id[5]	isrc2_packet_id[4]	isrc2_packet_id[3]	isrc2_packet_id[2]	isrc2_packet_id[1]	isrc2_packet_id[0]
0xF6	0x00	isrc2_header1	r	isrc2_header1[7]	isrc2_header1[6]	isrc2_header1[5]	isrc2_header1[4]	isrc2_header1[3]	isrc2_header1[2]	isrc2_header1[1]	isrc2_header1[0]
0xF7	0x00	isrc2_header2	r	isrc2_header2[7]	isrc2_header2[6]	isrc2_header2[5]	isrc2_header2[4]	isrc2_header2[3]	isrc2_header2[2]	isrc2_header2[1]	isrc2_header2[0]
0xF8	0x0A	gamut_packet_id	rw	gamut_packet_id[7]	gamut_packet_id[6]	gamut_packet_id[5]	gamut_packet_id[4]	gamut_packet_id[3]	gamut_packet_id[2]	gamut_packet_id[1]	gamut_packet_id[0]
0xF9	0x00	gamut_header1	r	gamut_header1[7]	gamut_header1[6]	gamut_header1[5]	gamut_header1[4]	gamut_header1[3]	gamut_header1[2]	gamut_header1[1]	gamut_header1[0]
0xFA	0x00	gamut_header2	r	gamut_header2[7]	gamut_header2[6]	gamut_header2[5]	gamut_header2[4]	gamut_header2[3]	gamut_header2[2]	gamut_header2[1]	gamut_header2[0]
0xFD	0x81		rw	pkt_cnt_id[7]	pkt_cnt_id[6]	pkt_cnt_id[5]	pkt_cnt_id[4]	pkt_cnt_id[3]	pkt_cnt_id[2]	pkt_cnt_id[1]	pkt_cnt_id[0]
0xFE	0x00		rw	-	-	-	en_pkt_cnt_sel	pkt_cnt_sel[3]	pkt_cnt_sel[2]	pkt_cnt_sel[1]	pkt_cnt_sel[0]
0xFF	0x00		r	-	-	-	-	rb_pkt_cnt[3]	rb_pkt_cnt[2]	rb_pkt_cnt[1]	rb_pkt_cnt[0]

1.12 ADDR 4C (DPLL)

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xB5	0x01	mclk fs	rw	-	-	-	-	-	mclk_fs_n[2]	mclk_fs_n[1]	mclk_fs_n[0]
0xC8	0x00	dll control_2	rw	-	-	dll_phase[5]	dll_phase[4]	dll_phase[3]	dll_phase[2]	dll_phase[1]	dll_phase[0]
0xC9	0x00	fb control	rw	-	-	-	-	fb_phase_adjust[3]]	fb_phase_adjust[2]]	fb_phase_adjust[1]]	fb_phase_adjust[0]]

1.13 ADDR 5C (AUDIO_CODEC)

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x01	initialization_register	rw	pll_ref_freq[1]	pll_ref_freq[0]	-	-	-	adc_input_mux[2]	adc_input_mux[1]	adc_input_mux[0]
0x01	0x01	powerup_register_1	rw	-	-	-	-	eng_dig_pu	pll_pu	ref_buf_pu	dac_ana_stdbys
0x02	0x00	dac_powerup	rw	-	-	-	-	-	-	right_dac_1_pu	left_dac_1_pu
0x03	0x00	adc_powerup	rw	-	-	-	-	-	-	right_adc_1_pu	left_adc_1_pu
0x05	0x00	hp_setup	rw	-	-	hp_right_amp_pu	hp_left_amp_pu	hp_scp	hp_mute	hp_left_right_tri_enb	hp_right_right_tri_enb
0x06	0x00	hp_attenuation	rw	-	-	-	hp1_atten[4]	hp1_atten[3]	hp1_atten[2]	hp1_atten[1]	hp1_atten[0]
0x07	0x44	general_0	rw	-	pu_dac_cur_gen	dac_clamp_op	idac_buf_pu	idac_en	pu_dac_ibias_dist	hp_clamp_op	-
0x08	0x00	general_1	rw	-	-	-	-	pu_pdn_dwhmpr_i	pu_pup_dwhmpr_i	-	vref_enb
0x09	0x00	dac_stdbymode_reg	rw	-	-	-	-	-	-	right_dac_1_ana_stdbymode	left_dac_1_ana_stdbymode
0x0A	0x00	dac_mute_in_pd	rw	-	-	-	-	-	-	right_dac_vol_ramp_pd_pu	left_dac_vol_ramp_pd_pu
0x0B	0x00	adc_mute_in_pd	rw	-	-	-	-	-	-	right_adc_vol_ramp_pd_pu	left_adc_vol_ramp_pd_pu
0x0C	0x02	serial_ports	rw	-	-	-	-	-	-	dac_slave_serial_port	adc_slave_serial_port
0x0D	0x00	pll_status	r	-	-	-	-	-	-	-	audio_pll_locked
0x0E	0x43	mux_select	rw	mux_out_l_sel[3]	mux_out_l_sel[2]	mux_out_l_sel[1]	mux_out_l_sel[0]	mux_out_r_sel[3]	mux_out_r_sel[2]	mux_out_r_sel[1]	mux_out_r_sel[0]
0x10	0x00	volume_register_1	rw	vol_dac_left[7]	vol_dac_left[6]	vol_dac_left[5]	vol_dac_left[4]	vol_dac_left[3]	vol_dac_left[2]	vol_dac_left[1]	vol_dac_left[0]
0x11	0x00	volume_register_2	rw	vol_dac_right[7]	vol_dac_right[6]	vol_dac_right[5]	vol_dac_right[4]	vol_dac_right[3]	vol_dac_right[2]	vol_dac_right[1]	vol_dac_right[0]
0x18	0x00	volume_register_9	rw	vol_adc_left[7]	vol_adc_left[6]	vol_adc_left[5]	vol_adc_left[4]	vol_adc_left[3]	vol_adc_left[2]	vol_adc_left[1]	vol_adc_left[0]
0x19	0x00	volume_register_10	rw	vol_adc_right[7]	vol_adc_right[6]	vol_adc_right[5]	vol_adc_right[4]	vol_adc_right[3]	vol_adc_right[2]	vol_adc_right[1]	vol_adc_right[0]
0x2C	0x01	mux_out	rw	-	-	-	-	-	-	-	muxout_pdb
0x33	0x00	general_2	rw	-	ref_core_pd	-	-	-	-	-	-
0x38	0x00	dac_debug_reg1	rw	-	-	-	-	-	-	dac_ana_stndby_adj[1]	dac_ana_stndby_adj[0]

1.14 ADDR B8 (TX MAIN)

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x01	0x00	main_reg_01	rw	-	-	-	-	n_high_byte[3]	n_high_byte[2]	n_high_byte[1]	n_high_byte[0]
0x02	0x00	main_reg_02	rw	n_mid_byte[7]	n_mid_byte[6]	n_mid_byte[5]	n_mid_byte[4]	n_mid_byte[3]	n_mid_byte[2]	n_mid_byte[1]	n_mid_byte[0]
0x03	0x00	main_reg_03	rw	n_low_byte[7]	n_low_byte[6]	n_low_byte[5]	n_low_byte[4]	n_low_byte[3]	n_low_byte[2]	n_low_byte[1]	n_low_byte[0]
0x04	0x00	main_reg_04	r	spdif_sf[3]	spdif_sf[2]	spdif_sf[1]	spdif_sf[0]	int_cts_high_byte[3]	int_cts_high_byte[2]	int_cts_high_byte[1]	int_cts_high_byte[0]
0x05	0x00	main_reg_05	r	int_cts_mid_byte[7]	int_cts_mid_byte[6]	int_cts_mid_byte[5]	int_cts_mid_byte[4]	int_cts_mid_byte[3]	int_cts_mid_byte[2]	int_cts_mid_byte[1]	int_cts_mid_byte[0]
0x06	0x00	main_reg_06	r	int_cts_low_byte[7]	int_cts_low_byte[6]	int_cts_low_byte[5]	int_cts_low_byte[4]	int_cts_low_byte[3]	int_cts_low_byte[2]	int_cts_low_byte[1]	int_cts_low_byte[0]
0x07	0x00	main_reg_07	rw	-	-	-	-	external_cts_high_byte[3]	external_cts_high_byte[2]	external_cts_high_byte[1]	external_cts_high_byte[0]
0x08	0x00	main_reg_08	rw	external_cts_mid_byte[7]	external_cts_mid_byte[6]	external_cts_mid_byte[5]	external_cts_mid_byte[4]	external_cts_mid_byte[3]	external_cts_mid_byte[2]	external_cts_mid_byte[1]	external_cts_mid_byte[0]
0x09	0x00	main_reg_09	rw	external_cts_low_byte[7]	external_cts_low_byte[6]	external_cts_low_byte[5]	external_cts_low_byte[4]	external_cts_low_byte[3]	external_cts_low_byte[2]	external_cts_low_byte[1]	external_cts_low_byte[0]
0x0A	0x01	main_reg_0a	rw	cts_sel	audio_sel[2]	audio_sel[1]	audio_sel[0]	audio_mode[1]	audio_mode[0]	mclk_ratio[1]	mclk_ratio[0]
0x0B	0x0E	main_reg_0b	rw	spdif_en	mclk_pol	mclk_en	-	-	-	-	-
0x0C	0xBC	main_reg_0c	rw	ext_audiosf_sel	cs_bit_override	i2senable[3]	i2senable[2]	i2senable[1]	i2senable[0]	i2sformat[1]	i2sformat[0]
0x0D	0x18	main_reg_0d	rw	-	-	-	i2s_bit_width[4]	i2s_bit_width[3]	i2s_bit_width[2]	i2s_bit_width[1]	i2s_bit_width[0]
0x0E	0x01	main_reg_0e	rw	-	-	subpkt0_l_src[2]	subpkt0_l_src[1]	subpkt0_l_src[0]	subpkt0_r_src[2]	subpkt0_r_src[1]	subpkt0_r_src[0]
0x0F	0x13	main_reg_0f	rw	-	-	subpkt1_l_src[2]	subpkt1_l_src[1]	subpkt1_l_src[0]	subpkt1_r_src[2]	subpkt1_r_src[1]	subpkt1_r_src[0]
0x10	0x25	main_reg_10	rw	-	-	subpkt2_l_src[2]	subpkt2_l_src[1]	subpkt2_l_src[0]	subpkt2_r_src[2]	subpkt2_r_src[1]	subpkt2_r_src[0]
0x11	0x37	main_reg_11	rw	-	-	subpkt3_l_src[2]	subpkt3_l_src[1]	subpkt3_l_src[0]	subpkt3_r_src[2]	subpkt3_r_src[1]	subpkt3_r_src[0]
0x12	0x00	main_reg_12	rw	cs_bit_1_0[1]	cs_bit_1_0[0]	cr_bit	a_info[2]	a_info[1]	a_info[0]	clk_acc[1]	clk_acc[0]
0x13	0x00	main_reg_13	rw	category_code[7]	category_code[6]	category_code[5]	category_code[4]	category_code[3]	category_code[2]	category_code[1]	category_code[0]
0x14	0x00	main_reg_14	rw	source_number[3]	source_number[2]	source_number[1]	source_number[0]	word_length[3]	word_length[2]	word_length[1]	word_length[0]
0x15	0x00	main_reg_15	rw	i2s_sf[3]	i2s_sf[2]	i2s_sf[1]	i2s_sf[0]	vfe_input_id[3]	vfe_input_id[2]	vfe_input_id[1]	vfe_input_id[0]
0x16	0x00	main_reg_16	rw	vfe_out_fmt[1]	vfe_out_fmt[0]	vfe_422_width[1]	vfe_422_width[0]	-	-	-	-
0x17	0x00	main_reg_17	rw	-	-	-	-	-	gen_444_en	asp_ratio	-
0x18	0x46	main_reg_18	rw	csc_en	csc_mode[1]	csc_mode[0]	csc_a1[12]	csc_a1[11]	csc_a1[10]	csc_a1[9]	csc_a1[8]
0x19	0x62	main_reg_19	rw	csc_a1[7]	csc_a1[6]	csc_a1[5]	csc_a1[4]	csc_a1[3]	csc_a1[2]	csc_a1[1]	csc_a1[0]
0x1A	0x04	main_reg_1a	rw	-	-	-	csc_a2[12]	csc_a2[11]	csc_a2[10]	csc_a2[9]	csc_a2[8]
0x1B	0xA8	main_reg_1b	rw	csc_a2[7]	csc_a2[6]	csc_a2[5]	csc_a2[4]	csc_a2[3]	csc_a2[2]	csc_a2[1]	csc_a2[0]
0x1C	0x00	main_reg_1c	rw	-	-	-	csc_a3[12]	csc_a3[11]	csc_a3[10]	csc_a3[9]	csc_a3[8]
0x1D	0x00	main_reg_1d	rw	csc_a3[7]	csc_a3[6]	csc_a3[5]	csc_a3[4]	csc_a3[3]	csc_a3[2]	csc_a3[1]	csc_a3[0]
0x1E	0x1C	main_reg_1e	rw	-	-	-	csc_a4[12]	csc_a4[11]	csc_a4[10]	csc_a4[9]	csc_a4[8]
0x1F	0x84	main_reg_1f	rw	csc_a4[7]	csc_a4[6]	csc_a4[5]	csc_a4[4]	csc_a4[3]	csc_a4[2]	csc_a4[1]	csc_a4[0]
0x20	0x1C	main_reg_20	rw	-	-	-	csc_b1[12]	csc_b1[11]	csc_b1[10]	csc_b1[9]	csc_b1[8]
0x21	0xBF	main_reg_21	rw	csc_b1[7]	csc_b1[6]	csc_b1[5]	csc_b1[4]	csc_b1[3]	csc_b1[2]	csc_b1[1]	csc_b1[0]
0x22	0x04	main_reg_22	rw	-	-	-	csc_b2[12]	csc_b2[11]	csc_b2[10]	csc_b2[9]	csc_b2[8]
0x23	0xAB	main_reg_23	rw	csc_b2[7]	csc_b2[6]	csc_b2[5]	csc_b2[4]	csc_b2[3]	csc_b2[2]	csc_b2[1]	csc_b2[0]
0x24	0x1E	main_reg_24	rw	-	-	-	csc_b3[12]	csc_b3[11]	csc_b3[10]	csc_b3[9]	csc_b3[8]
0x25	0x70	main_reg_25	rw	csc_b3[7]	csc_b3[6]	csc_b3[5]	csc_b3[4]	csc_b3[3]	csc_b3[2]	csc_b3[1]	csc_b3[0]
0x26	0x02	main_reg_26	rw	-	-	-	csc_b4[12]	csc_b4[11]	csc_b4[10]	csc_b4[9]	csc_b4[8]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x27	0x1E	main_reg_27	rw	csc_b4[7]	csc_b4[6]	csc_b4[5]	csc_b4[4]	csc_b4[3]	csc_b4[2]	csc_b4[1]	csc_b4[0]
0x28	0x00	main_reg_28	rw	-	-	-	csc_c1[12]	csc_c1[11]	csc_c1[10]	csc_c1[9]	csc_c1[8]
0x29	0x00	main_reg_29	rw	csc_c1[7]	csc_c1[6]	csc_c1[5]	csc_c1[4]	csc_c1[3]	csc_c1[2]	csc_c1[1]	csc_c1[0]
0x2A	0x04	main_reg_2a	rw	-	-	-	csc_c2[12]	csc_c2[11]	csc_c2[10]	csc_c2[9]	csc_c2[8]
0x2B	0xA8	main_reg_2b	rw	csc_c2[7]	csc_c2[6]	csc_c2[5]	csc_c2[4]	csc_c2[3]	csc_c2[2]	csc_c2[1]	csc_c2[0]
0x2C	0x08	main_reg_2c	rw	-	-	-	csc_c3[12]	csc_c3[11]	csc_c3[10]	csc_c3[9]	csc_c3[8]
0x2D	0x12	main_reg_2d	rw	csc_c3[7]	csc_c3[6]	csc_c3[5]	csc_c3[4]	csc_c3[3]	csc_c3[2]	csc_c3[1]	csc_c3[0]
0x2E	0x1B	main_reg_2e	rw	-	-	-	csc_c4[12]	csc_c4[11]	csc_c4[10]	csc_c4[9]	csc_c4[8]
0x2F	0xAC	main_reg_2f	rw	csc_c4[7]	csc_c4[6]	csc_c4[5]	csc_c4[4]	csc_c4[3]	csc_c4[2]	csc_c4[1]	csc_c4[0]
0x3B	0x80	main_reg_3b	rw	-	pr_mode[1]	pr_mode[0]	ext_pll_pr[1]	ext_pll_pr[0]	ext_target_pr[1]	ext_target_pr[0]	-
0x3C	0x00	main_reg_3c	rw	-	-	ext_vid_to_rx[5]	ext_vid_to_rx[4]	ext_vid_to_rx[3]	ext_vid_to_rx[2]	ext_vid_to_rx[1]	ext_vid_to_rx[0]
0x3D	0x00	main_reg_3d	r	pr_to_rx[1]	pr_to_rx[0]	vid_to_rx[5]	vid_to_rx[4]	vid_to_rx[3]	vid_to_rx[2]	vid_to_rx[1]	vid_to_rx[0]
0x3E	0x00	main_reg_3e	r	vfe_fmt_vid[5]	vfe_fmt_vid[4]	vfe_fmt_vid[3]	vfe_fmt_vid[2]	vfe_fmt_vid[1]	vfe_fmt_vid[0]	-	-
0x3F	0x00	main_reg_3f	r	vfe_aux_vid[2]	vfe_aux_vid[1]	vfe_aux_vid[0]	vfe_prog_mode[1]	vfe_prog_mode[0]	-	-	-
0x40	0x00	main_reg_40	rw	gc_pkt_en	spd_pkt_en	mpeg_pkt_en	acp_pkt_en	isrc_pkt_en	gm_pkt_en	spare_pkt1_en	spare_pkt0_en
0x41	0x50	main_reg_41	rw	-	system_pd	-	-	-	-	-	-
0x42	0x90	main_reg_42	r	-	hpd_state	msen_state	-	i2s_32bit_mode	-	-	-
0x43	0x7E	main_reg_43	rw	edid_id[7]	edid_id[6]	edid_id[5]	edid_id[4]	edid_id[3]	edid_id[2]	edid_id[1]	edid_id[0]
0x44	0x79	main_reg_44	rw	-	n_cts_pkt_en	audio_sample_pkt_en	aviif_pkt_en	audioif_pkt_en	-	-	dcm_mode
0x46	0x00	main_reg_46	rw	dsd_en[7]	dsd_en[6]	dsd_en[5]	dsd_en[4]	dsd_en[3]	dsd_en[2]	dsd_en[1]	dsd_en[0]
0x4A	0x80	main_reg_4a	rw	auto_checksum_en	avi_update	audio_update	gcp_update	-	-	-	-
0x4B	0x00	main_reg_4b	rw	clear_avmute	set_avmute	-	-	-	-	-	-
0x4C	0x00	main_reg_4c	rw	-	-	-	-	gc_cd[3]	gc_cd[2]	gc_cd[1]	gc_cd[0]
0x4D	0x00	main_reg_4d	rw	gc_byte2[7]	gc_byte2[6]	gc_byte2[5]	gc_byte2[4]	gc_byte2[3]	gc_byte2[2]	gc_byte2[1]	gc_byte2[0]
0x4E	0x00	main_reg_4e	rw	gc_byte3[7]	gc_byte3[6]	gc_byte3[5]	gc_byte3[4]	gc_byte3[3]	gc_byte3[2]	gc_byte3[1]	gc_byte3[0]
0x4F	0x00	main_reg_4f	rw	gc_byte4[7]	gc_byte4[6]	gc_byte4[5]	gc_byte4[4]	gc_byte4[3]	gc_byte4[2]	gc_byte4[1]	gc_byte4[0]
0x50	0x00	main_reg_50	rw	gc_byte5[7]	gc_byte5[6]	gc_byte5[5]	gc_byte5[4]	gc_byte5[3]	gc_byte5[2]	gc_byte5[1]	gc_byte5[0]
0x51	0x00	main_reg_51	rw	gc_byte6[7]	gc_byte6[6]	gc_byte6[5]	gc_byte6[4]	gc_byte6[3]	gc_byte6[2]	gc_byte6[1]	gc_byte6[0]
0x52	0x02	main_reg_52	rw	-	-	-	-	-	avi_version[2]	avi_version[1]	avi_version[0]
0x53	0x0D	main_reg_53	rw	-	-	-	avi_length[4]	avi_length[3]	avi_length[2]	avi_length[1]	avi_length[0]
0x54	0x00	main_reg_54	rw	avi_checksum[7]	avi_checksum[6]	avi_checksum[5]	avi_checksum[4]	avi_checksum[3]	avi_checksum[2]	avi_checksum[1]	avi_checksum[0]
0x55	0x00	main_reg_55	rw	avi_byte1_7	y1y0[1]	y1y0[0]	a0	b1b0[1]	b1b0[0]	s1s0[1]	s1s0[0]
0x56	0x00	main_reg_56	rw	c1c0[1]	c1c0[0]	m1m0[1]	m1m0[0]	r3210[3]	r3210[2]	r3210[1]	r3210[0]
0x57	0x00	main_reg_57	rw	itc	ec210[2]	ec210[1]	ec210[0]	q1q0[1]	q1q0[0]	sc[1]	sc[0]
0x58	0x00	main_reg_58	rw	avi_byte4_7	-	-	-	-	-	-	-
0x59	0x00	main_reg_59	rw	avi_byte5_7_4[3]	avi_byte5_7_4[2]	avi_byte5_7_4[1]	avi_byte5_7_4[0]	-	-	-	-
0x5A	0x00	main_reg_5a	rw	avi_byte6[7]	avi_byte6[6]	avi_byte6[5]	avi_byte6[4]	avi_byte6[3]	avi_byte6[2]	avi_byte6[1]	avi_byte6[0]
0x5B	0x00	main_reg_5b	rw	avi_byte7[7]	avi_byte7[6]	avi_byte7[5]	avi_byte7[4]	avi_byte7[3]	avi_byte7[2]	avi_byte7[1]	avi_byte7[0]
0x5C	0x00	main_reg_5c	rw	avi_byte8[7]	avi_byte8[6]	avi_byte8[5]	avi_byte8[4]	avi_byte8[3]	avi_byte8[2]	avi_byte8[1]	avi_byte8[0]
0x5D	0x00	main_reg_5d	rw	avi_byte9[7]	avi_byte9[6]	avi_byte9[5]	avi_byte9[4]	avi_byte9[3]	avi_byte9[2]	avi_byte9[1]	avi_byte9[0]
0x5E	0x00	main_reg_5e	rw	avi_byte10[7]	avi_byte10[6]	avi_byte10[5]	avi_byte10[4]	avi_byte10[3]	avi_byte10[2]	avi_byte10[1]	avi_byte10[0]
0x5F	0x00	main_reg_5f	rw	avi_byte11[7]	avi_byte11[6]	avi_byte11[5]	avi_byte11[4]	avi_byte11[3]	avi_byte11[2]	avi_byte11[1]	avi_byte11[0]
0x60	0x00	main_reg_60	rw	avi_byte12[7]	avi_byte12[6]	avi_byte12[5]	avi_byte12[4]	avi_byte12[3]	avi_byte12[2]	avi_byte12[1]	avi_byte12[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x61	0x00	main_reg_61	rw	avi_byte13[7]	avi_byte13[6]	avi_byte13[5]	avi_byte13[4]	avi_byte13[3]	avi_byte13[2]	avi_byte13[1]	avi_byte13[0]
0x62	0x00	main_reg_62	rw	avi_byte14[7]	avi_byte14[6]	avi_byte14[5]	avi_byte14[4]	avi_byte14[3]	avi_byte14[2]	avi_byte14[1]	avi_byte14[0]
0x63	0x00	main_reg_63	rw	avi_byte15[7]	avi_byte15[6]	avi_byte15[5]	avi_byte15[4]	avi_byte15[3]	avi_byte15[2]	avi_byte15[1]	avi_byte15[0]
0x64	0x00	main_reg_64	rw	avi_byte16[7]	avi_byte16[6]	avi_byte16[5]	avi_byte16[4]	avi_byte16[3]	avi_byte16[2]	avi_byte16[1]	avi_byte16[0]
0x65	0x00	main_reg_65	rw	avi_byte17[7]	avi_byte17[6]	avi_byte17[5]	avi_byte17[4]	avi_byte17[3]	avi_byte17[2]	avi_byte17[1]	avi_byte17[0]
0x66	0x00	main_reg_66	rw	avi_byte18[7]	avi_byte18[6]	avi_byte18[5]	avi_byte18[4]	avi_byte18[3]	avi_byte18[2]	avi_byte18[1]	avi_byte18[0]
0x67	0x00	main_reg_67	rw	avi_byte19[7]	avi_byte19[6]	avi_byte19[5]	avi_byte19[4]	avi_byte19[3]	avi_byte19[2]	avi_byte19[1]	avi_byte19[0]
0x68	0x00	main_reg_68	rw	avi_byte20[7]	avi_byte20[6]	avi_byte20[5]	avi_byte20[4]	avi_byte20[3]	avi_byte20[2]	avi_byte20[1]	avi_byte20[0]
0x69	0x00	main_reg_69	rw	avi_byte21[7]	avi_byte21[6]	avi_byte21[5]	avi_byte21[4]	avi_byte21[3]	avi_byte21[2]	avi_byte21[1]	avi_byte21[0]
0x6A	0x00	main_reg_6a	rw	avi_byte22[7]	avi_byte22[6]	avi_byte22[5]	avi_byte22[4]	avi_byte22[3]	avi_byte22[2]	avi_byte22[1]	avi_byte22[0]
0x6B	0x00	main_reg_6b	rw	avi_byte23[7]	avi_byte23[6]	avi_byte23[5]	avi_byte23[4]	avi_byte23[3]	avi_byte23[2]	avi_byte23[1]	avi_byte23[0]
0x6C	0x00	main_reg_6c	rw	avi_byte24[7]	avi_byte24[6]	avi_byte24[5]	avi_byte24[4]	avi_byte24[3]	avi_byte24[2]	avi_byte24[1]	avi_byte24[0]
0x6E	0x00	main_reg_6e	rw	avi_byte26[7]	avi_byte26[6]	avi_byte26[5]	avi_byte26[4]	avi_byte26[3]	avi_byte26[2]	avi_byte26[1]	avi_byte26[0]
0x6F	0x00	main_reg_6f	rw	avi_byte27[7]	avi_byte27[6]	avi_byte27[5]	avi_byte27[4]	avi_byte27[3]	avi_byte27[2]	avi_byte27[1]	avi_byte27[0]
0x70	0x01	main_reg_70	rw	-	-	-	-	-	audioif_version[2]	audioif_version[1]	audioif_version[0]
0x71	0x0A	main_reg_71	rw	-	-	-	audioif_length[4]	audioif_length[3]	audioif_length[2]	audioif_length[1]	audioif_length[0]
0x72	0x00	main_reg_72	rw	audioif_checksum [7]	audioif_checksum [6]	audioif_checksum [5]	audioif_checksum [4]	audioif_checksum [3]	audioif_checksum [2]	audioif_checksum [1]	audioif_checksum [0]
0x73	0x00	main_reg_73	rw	-	-	-	-	audioif_byte1_3	audioif_cc[2]	audioif_cc[1]	audioif_cc[0]
0x74	0x00	main_reg_74	rw	audioif_byte2_7_ 5[2]	audioif_byte2_7_ 5[1]	audioif_byte2_7_ 5[0]	audioif_sf[2]	audioif_sf[1]	audioif_sf[0]	audioif_ss[1]	audioif_ss[0]
0x75	0x00	main_reg_75	rw	audioif_byte3[7]	audioif_byte3[6]	audioif_byte3[5]	audioif_byte3[4]	audioif_byte3[3]	audioif_byte3[2]	audioif_byte3[1]	audioif_byte3[0]
0x76	0x00	main_reg_76	rw	audioif_ca[7]	audioif_ca[6]	audioif_ca[5]	audioif_ca[4]	audioif_ca[3]	audioif_ca[2]	audioif_ca[1]	audioif_ca[0]
0x77	0x00	main_reg_77	rw	-	-	-	-	-	audioif_byte5_2_ 0[2]	audioif_byte5_2_ 0[1]	audioif_byte5_2_ 0[0]
0x78	0x00	main_reg_78	rw	audioif_byte6[7]	audioif_byte6[6]	audioif_byte6[5]	audioif_byte6[4]	audioif_byte6[3]	audioif_byte6[2]	audioif_byte6[1]	audioif_byte6[0]
0x79	0x00	main_reg_79	rw	audioif_byte7[7]	audioif_byte7[6]	audioif_byte7[5]	audioif_byte7[4]	audioif_byte7[3]	audioif_byte7[2]	audioif_byte7[1]	audioif_byte7[0]
0x7A	0x00	main_reg_7a	rw	audioif_byte8[7]	audioif_byte8[6]	audioif_byte8[5]	audioif_byte8[4]	audioif_byte8[3]	audioif_byte8[2]	audioif_byte8[1]	audioif_byte8[0]
0x7B	0x00	main_reg_7b	rw	audioif_byte9[7]	audioif_byte9[6]	audioif_byte9[5]	audioif_byte9[4]	audioif_byte9[3]	audioif_byte9[2]	audioif_byte9[1]	audioif_byte9[0]
0x7C	0x00	main_reg_7c	rw	audioif_byte10[7]	audioif_byte10[6]	audioif_byte10[5]	audioif_byte10[4]	audioif_byte10[3]	audioif_byte10[2]	audioif_byte10[1]	audioif_byte10[0]
0x94	0xC0	main_reg_94	rw	hpd_intr_mask	msen_intr_mask	vs_intr_mask	-	-	edid_rdy_intr_ma sk	-	ri_rdy_intr_mask
0x95	0x00	main_reg_95	rw	hdcp_error_intr_ mask	bksv_flag_intr_ma sk	-	-	-	-	-	-
0x96	0x00	main_reg_96	rw	hpd_intr	msen_intr	vs_intr	-	-	edid_rdy_intr	-	ri_rdy_intr
0x97	0x00	main_reg_97	rw	hdcp_error_intr	-	tx_ready_intr	tx_arbitration_lost _intr	tx_retry_timeout_ _intr	-	-	-
0x9E	0x00	main_reg_9e	rw	high_vsync[1]	high_vsync[0]	video_offset_ctl[1]	video_offset_ctl[0]	-	-	-	-
0x9F	0x00	main_reg_9f	rw	lower_vsync[1]	lower_vsync[0]	-	-	-	-	-	-
0xAB	0x00	main_reg_ab	rw	-	-	hdcp_start_delay[2]	hdcp_start_delay[1]	hdcp_start_delay[0]	-	-	-
0xAD	0x00	main_reg_ad	rw	an_delay[2]	an_delay[1]	an_delay[0]	aksv_delay[2]	aksv_delay[1]	aksv_delay[0]	-	-
0xAF	0x14	main_reg_af	rw	hdcp_desired	-	-	frame_enc	-	hdmi_mode_sel	ext_hdmi_mode	-
0xB8	0x00	main_reg_b8	r	-	enc_on	-	keys_read_error	-	-	-	-
0xBE	0x00	main_reg_be	r	bcaps[7]	bcaps[6]	bcaps[5]	bcaps[4]	bcaps[3]	bcaps[2]	bcaps[1]	bcaps[0]
0xBF	0x00	main_reg_bf	r	bksv0[7]	bksv0[6]	bksv0[5]	bksv0[4]	bksv0[3]	bksv0[2]	bksv0[1]	bksv0[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xC0	0x00	main_reg_c0	r	bksv1[7]	bksv1[6]	bksv1[5]	bksv1[4]	bksv1[3]	bksv1[2]	bksv1[1]	bksv1[0]
0xC1	0x00	main_reg_c1	r	bksv2[7]	bksv2[6]	bksv2[5]	bksv2[4]	bksv2[3]	bksv2[2]	bksv2[1]	bksv2[0]
0xC2	0x00	main_reg_c2	r	bksv3[7]	bksv3[6]	bksv3[5]	bksv3[4]	bksv3[3]	bksv3[2]	bksv3[1]	bksv3[0]
0xC3	0x00	main_reg_c3	r	bksv4[7]	bksv4[6]	bksv4[5]	bksv4[4]	bksv4[3]	bksv4[2]	bksv4[1]	bksv4[0]
0xC4	0x00	main_reg_c4	rw	edid_segment[7]	edid_segment[6]	edid_segment[5]	edid_segment[4]	edid_segment[3]	edid_segment[2]	edid_segment[1]	edid_segment[0]
0xC5	0x00	main_reg_c5	rw	error_flag	an_stop	hdcp_enabled	edid_ready_flag	i2c_interrupt	ri_flag	-	pj_flag
0xC6	0x00	main_reg_c6	r	-	-	-	hdmi_mode	hdcp_requested	rx_sense	eeeprom_read_ok	-
0xC7	0x00	main_reg_c7	rw	bksv_flag	bksv_count[6]	bksv_count[5]	bksv_count[4]	bksv_count[3]	bksv_count[2]	bksv_count[1]	bksv_count[0]
0xC8	0x00	main_reg_c8	r	hdcp_controller_error[3]	hdcp_controller_error[2]	hdcp_controller_error[1]	hdcp_controller_error[0]	hdcp_controller_state[3]	hdcp_controller_state[2]	hdcp_controller_state[1]	hdcp_controller_state[0]
0xC9	0x03	main_reg_c9	rw	-	-	-	-	edid_trys[3]	edid_trys[2]	edid_trys[1]	edid_trys[0]
0xE4	0x00	main_reg_e4	r	pll_lock_status	-	-	-	-	-	-	-
0xE6	0x00	main_reg_e6	rw	-	-	-	-	-	termpwrdwn_i2c	-	-
0xE8	0x10	main_reg_e8	rw	-	-	-	clkdrvenable_i2c	-	-	-	-
0xEA	0x84	main_reg_ea	rw	-	-	-	-	-	-	tmds_clk_inv_i2c	-
0xEF	0x82	main_reg_ef	rw	-	-	-	-	-	video_clock_detect	-	-
0xFE	0x00	main_reg_fe	rw	-	-	-	-	-	-	hs_active_det_en	-

1.15 ADDR 70 (PACKETMEMORY)

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00	packetmemory_re g_00	rw	spd_header_byte _0[7]	spd_header_byte _0[6]	spd_header_byte _0[5]	spd_header_byte _0[4]	spd_header_byte _0[3]	spd_header_byte _0[2]	spd_header_byte _0[1]	spd_header_byte _0[0]
0x01	0x00	packetmemory_re g_01	rw	spd_header_byte _1[7]	spd_header_byte _1[6]	spd_header_byte _1[5]	spd_header_byte _1[4]	spd_header_byte _1[3]	spd_header_byte _1[2]	spd_header_byte _1[1]	spd_header_byte _1[0]
0x02	0x00	packetmemory_re g_02	rw	spd_header_byte _2[7]	spd_header_byte _2[6]	spd_header_byte _2[5]	spd_header_byte _2[4]	spd_header_byte _2[3]	spd_header_byte _2[2]	spd_header_byte _2[1]	spd_header_byte _2[0]
0x03	0x00	packetmemory_re g_03	rw	spd_packet_byte_ 0[7]	spd_packet_byte_ 0[6]	spd_packet_byte_ 0[5]	spd_packet_byte_ 0[4]	spd_packet_byte_ 0[3]	spd_packet_byte_ 0[2]	spd_packet_byte_ 0[1]	spd_packet_byte_ 0[0]
0x04	0x00	packetmemory_re g_04	rw	spd_packet_byte_ 1[7]	spd_packet_byte_ 1[6]	spd_packet_byte_ 1[5]	spd_packet_byte_ 1[4]	spd_packet_byte_ 1[3]	spd_packet_byte_ 1[2]	spd_packet_byte_ 1[1]	spd_packet_byte_ 1[0]
0x05	0x00	packetmemory_re g_05	rw	spd_packet_byte_ 2[7]	spd_packet_byte_ 2[6]	spd_packet_byte_ 2[5]	spd_packet_byte_ 2[4]	spd_packet_byte_ 2[3]	spd_packet_byte_ 2[2]	spd_packet_byte_ 2[1]	spd_packet_byte_ 2[0]
0x06	0x00	packetmemory_re g_06	rw	spd_packet_byte_ 3[7]	spd_packet_byte_ 3[6]	spd_packet_byte_ 3[5]	spd_packet_byte_ 3[4]	spd_packet_byte_ 3[3]	spd_packet_byte_ 3[2]	spd_packet_byte_ 3[1]	spd_packet_byte_ 3[0]
0x07	0x00	packetmemory_re g_07	rw	spd_packet_byte_ 4[7]	spd_packet_byte_ 4[6]	spd_packet_byte_ 4[5]	spd_packet_byte_ 4[4]	spd_packet_byte_ 4[3]	spd_packet_byte_ 4[2]	spd_packet_byte_ 4[1]	spd_packet_byte_ 4[0]
0x08	0x00	packetmemory_re g_08	rw	spd_packet_byte_ 5[7]	spd_packet_byte_ 5[6]	spd_packet_byte_ 5[5]	spd_packet_byte_ 5[4]	spd_packet_byte_ 5[3]	spd_packet_byte_ 5[2]	spd_packet_byte_ 5[1]	spd_packet_byte_ 5[0]
0x09	0x00	packetmemory_re g_09	rw	spd_packet_byte_ 6[7]	spd_packet_byte_ 6[6]	spd_packet_byte_ 6[5]	spd_packet_byte_ 6[4]	spd_packet_byte_ 6[3]	spd_packet_byte_ 6[2]	spd_packet_byte_ 6[1]	spd_packet_byte_ 6[0]
0x0A	0x00	packetmemory_re g_0a	rw	spd_packet_byte_ 7[7]	spd_packet_byte_ 7[6]	spd_packet_byte_ 7[5]	spd_packet_byte_ 7[4]	spd_packet_byte_ 7[3]	spd_packet_byte_ 7[2]	spd_packet_byte_ 7[1]	spd_packet_byte_ 7[0]
0x0B	0x00	packetmemory_re g_0b	rw	spd_packet_byte_ 8[7]	spd_packet_byte_ 8[6]	spd_packet_byte_ 8[5]	spd_packet_byte_ 8[4]	spd_packet_byte_ 8[3]	spd_packet_byte_ 8[2]	spd_packet_byte_ 8[1]	spd_packet_byte_ 8[0]
0x0C	0x00	packetmemory_re g_0c	rw	spd_packet_byte_ 9[7]	spd_packet_byte_ 9[6]	spd_packet_byte_ 9[5]	spd_packet_byte_ 9[4]	spd_packet_byte_ 9[3]	spd_packet_byte_ 9[2]	spd_packet_byte_ 9[1]	spd_packet_byte_ 9[0]
0x0D	0x00	packetmemory_re g_0d	rw	spd_packet_byte_ 10[7]	spd_packet_byte_ 10[6]	spd_packet_byte_ 10[5]	spd_packet_byte_ 10[4]	spd_packet_byte_ 10[3]	spd_packet_byte_ 10[2]	spd_packet_byte_ 10[1]	spd_packet_byte_ 10[0]
0x0E	0x00	packetmemory_re g_0e	rw	spd_packet_byte_ 11[7]	spd_packet_byte_ 11[6]	spd_packet_byte_ 11[5]	spd_packet_byte_ 11[4]	spd_packet_byte_ 11[3]	spd_packet_byte_ 11[2]	spd_packet_byte_ 11[1]	spd_packet_byte_ 11[0]
0x0F	0x00	packetmemory_re g_0f	rw	spd_packet_byte_ 12[7]	spd_packet_byte_ 12[6]	spd_packet_byte_ 12[5]	spd_packet_byte_ 12[4]	spd_packet_byte_ 12[3]	spd_packet_byte_ 12[2]	spd_packet_byte_ 12[1]	spd_packet_byte_ 12[0]
0x10	0x00	packetmemory_re g_10	rw	spd_packet_byte_ 13[7]	spd_packet_byte_ 13[6]	spd_packet_byte_ 13[5]	spd_packet_byte_ 13[4]	spd_packet_byte_ 13[3]	spd_packet_byte_ 13[2]	spd_packet_byte_ 13[1]	spd_packet_byte_ 13[0]
0x11	0x00	packetmemory_re g_11	rw	spd_packet_byte_ 14[7]	spd_packet_byte_ 14[6]	spd_packet_byte_ 14[5]	spd_packet_byte_ 14[4]	spd_packet_byte_ 14[3]	spd_packet_byte_ 14[2]	spd_packet_byte_ 14[1]	spd_packet_byte_ 14[0]
0x12	0x00	packetmemory_re g_12	rw	spd_packet_byte_ 15[7]	spd_packet_byte_ 15[6]	spd_packet_byte_ 15[5]	spd_packet_byte_ 15[4]	spd_packet_byte_ 15[3]	spd_packet_byte_ 15[2]	spd_packet_byte_ 15[1]	spd_packet_byte_ 15[0]
0x13	0x00	packetmemory_re g_13	rw	spd_packet_byte_ 16[7]	spd_packet_byte_ 16[6]	spd_packet_byte_ 16[5]	spd_packet_byte_ 16[4]	spd_packet_byte_ 16[3]	spd_packet_byte_ 16[2]	spd_packet_byte_ 16[1]	spd_packet_byte_ 16[0]
0x14	0x00	packetmemory_re g_14	rw	spd_packet_byte_ 17[7]	spd_packet_byte_ 17[6]	spd_packet_byte_ 17[5]	spd_packet_byte_ 17[4]	spd_packet_byte_ 17[3]	spd_packet_byte_ 17[2]	spd_packet_byte_ 17[1]	spd_packet_byte_ 17[0]
0x15	0x00	packetmemory_re g_15	rw	spd_packet_byte_ 18[7]	spd_packet_byte_ 18[6]	spd_packet_byte_ 18[5]	spd_packet_byte_ 18[4]	spd_packet_byte_ 18[3]	spd_packet_byte_ 18[2]	spd_packet_byte_ 18[1]	spd_packet_byte_ 18[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x16	0x00	packetmemory_re g_16	rw	spd_packet_byte_ 19[7]	spd_packet_byte_ 19[6]	spd_packet_byte_ 19[5]	spd_packet_byte_ 19[4]	spd_packet_byte_ 19[3]	spd_packet_byte_ 19[2]	spd_packet_byte_ 19[1]	spd_packet_byte_ 19[0]
0x17	0x00	packetmemory_re g_17	rw	spd_packet_byte_ 20[7]	spd_packet_byte_ 20[6]	spd_packet_byte_ 20[5]	spd_packet_byte_ 20[4]	spd_packet_byte_ 20[3]	spd_packet_byte_ 20[2]	spd_packet_byte_ 20[1]	spd_packet_byte_ 20[0]
0x18	0x00	packetmemory_re g_18	rw	spd_packet_byte_ 21[7]	spd_packet_byte_ 21[6]	spd_packet_byte_ 21[5]	spd_packet_byte_ 21[4]	spd_packet_byte_ 21[3]	spd_packet_byte_ 21[2]	spd_packet_byte_ 21[1]	spd_packet_byte_ 21[0]
0x19	0x00	packetmemory_re g_19	rw	spd_packet_byte_ 22[7]	spd_packet_byte_ 22[6]	spd_packet_byte_ 22[5]	spd_packet_byte_ 22[4]	spd_packet_byte_ 22[3]	spd_packet_byte_ 22[2]	spd_packet_byte_ 22[1]	spd_packet_byte_ 22[0]
0x1A	0x00	packetmemory_re g_1a	rw	spd_packet_byte_ 23[7]	spd_packet_byte_ 23[6]	spd_packet_byte_ 23[5]	spd_packet_byte_ 23[4]	spd_packet_byte_ 23[3]	spd_packet_byte_ 23[2]	spd_packet_byte_ 23[1]	spd_packet_byte_ 23[0]
0x1B	0x00	packetmemory_re g_1b	rw	spd_packet_byte_ 24[7]	spd_packet_byte_ 24[6]	spd_packet_byte_ 24[5]	spd_packet_byte_ 24[4]	spd_packet_byte_ 24[3]	spd_packet_byte_ 24[2]	spd_packet_byte_ 24[1]	spd_packet_byte_ 24[0]
0x1C	0x00	packetmemory_re g_1c	rw	spd_packet_byte_ 25[7]	spd_packet_byte_ 25[6]	spd_packet_byte_ 25[5]	spd_packet_byte_ 25[4]	spd_packet_byte_ 25[3]	spd_packet_byte_ 25[2]	spd_packet_byte_ 25[1]	spd_packet_byte_ 25[0]
0x1D	0x00	packetmemory_re g_1d	rw	spd_packet_byte_ 26[7]	spd_packet_byte_ 26[6]	spd_packet_byte_ 26[5]	spd_packet_byte_ 26[4]	spd_packet_byte_ 26[3]	spd_packet_byte_ 26[2]	spd_packet_byte_ 26[1]	spd_packet_byte_ 26[0]
0x1E	0x00	packetmemory_re g_1e	rw	spd_packet_byte_ 27[7]	spd_packet_byte_ 27[6]	spd_packet_byte_ 27[5]	spd_packet_byte_ 27[4]	spd_packet_byte_ 27[3]	spd_packet_byte_ 27[2]	spd_packet_byte_ 27[1]	spd_packet_byte_ 27[0]
0x1F	0x00	packetmemory_re g_1f	rw	spd_update	-	-	-	-	-	-	-
0x20	0x00	packetmemory_re g_20	rw	mpeg_header_byt e_0[7]	mpeg_header_byt e_0[6]	mpeg_header_byt e_0[5]	mpeg_header_byt e_0[4]	mpeg_header_byt e_0[3]	mpeg_header_byt e_0[2]	mpeg_header_byt e_0[1]	mpeg_header_byt e_0[0]
0x21	0x00	packetmemory_re g_21	rw	mpeg_header_byt e_1[7]	mpeg_header_byt e_1[6]	mpeg_header_byt e_1[5]	mpeg_header_byt e_1[4]	mpeg_header_byt e_1[3]	mpeg_header_byt e_1[2]	mpeg_header_byt e_1[1]	mpeg_header_byt e_1[0]
0x22	0x00	packetmemory_re g_22	rw	mpeg_header_byt e_2[7]	mpeg_header_byt e_2[6]	mpeg_header_byt e_2[5]	mpeg_header_byt e_2[4]	mpeg_header_byt e_2[3]	mpeg_header_byt e_2[2]	mpeg_header_byt e_2[1]	mpeg_header_byt e_2[0]
0x23	0x00	packetmemory_re g_23	rw	mpeg_packet_byt e_0[7]	mpeg_packet_byt e_0[6]	mpeg_packet_byt e_0[5]	mpeg_packet_byt e_0[4]	mpeg_packet_byt e_0[3]	mpeg_packet_byt e_0[2]	mpeg_packet_byt e_0[1]	mpeg_packet_byt e_0[0]
0x24	0x00	packetmemory_re g_24	rw	mpeg_packet_byt e_1[7]	mpeg_packet_byt e_1[6]	mpeg_packet_byt e_1[5]	mpeg_packet_byt e_1[4]	mpeg_packet_byt e_1[3]	mpeg_packet_byt e_1[2]	mpeg_packet_byt e_1[1]	mpeg_packet_byt e_1[0]
0x25	0x00	packetmemory_re g_25	rw	mpeg_packet_byt e_2[7]	mpeg_packet_byt e_2[6]	mpeg_packet_byt e_2[5]	mpeg_packet_byt e_2[4]	mpeg_packet_byt e_2[3]	mpeg_packet_byt e_2[2]	mpeg_packet_byt e_2[1]	mpeg_packet_byt e_2[0]
0x26	0x00	packetmemory_re g_26	rw	mpeg_packet_byt e_3[7]	mpeg_packet_byt e_3[6]	mpeg_packet_byt e_3[5]	mpeg_packet_byt e_3[4]	mpeg_packet_byt e_3[3]	mpeg_packet_byt e_3[2]	mpeg_packet_byt e_3[1]	mpeg_packet_byt e_3[0]
0x27	0x00	packetmemory_re g_27	rw	mpeg_packet_byt e_4[7]	mpeg_packet_byt e_4[6]	mpeg_packet_byt e_4[5]	mpeg_packet_byt e_4[4]	mpeg_packet_byt e_4[3]	mpeg_packet_byt e_4[2]	mpeg_packet_byt e_4[1]	mpeg_packet_byt e_4[0]
0x28	0x00	packetmemory_re g_28	rw	mpeg_packet_byt e_5[7]	mpeg_packet_byt e_5[6]	mpeg_packet_byt e_5[5]	mpeg_packet_byt e_5[4]	mpeg_packet_byt e_5[3]	mpeg_packet_byt e_5[2]	mpeg_packet_byt e_5[1]	mpeg_packet_byt e_5[0]
0x29	0x00	packetmemory_re g_29	rw	mpeg_packet_byt e_6[7]	mpeg_packet_byt e_6[6]	mpeg_packet_byt e_6[5]	mpeg_packet_byt e_6[4]	mpeg_packet_byt e_6[3]	mpeg_packet_byt e_6[2]	mpeg_packet_byt e_6[1]	mpeg_packet_byt e_6[0]
0x2A	0x00	packetmemory_re g_2a	rw	mpeg_packet_byt e_7[7]	mpeg_packet_byt e_7[6]	mpeg_packet_byt e_7[5]	mpeg_packet_byt e_7[4]	mpeg_packet_byt e_7[3]	mpeg_packet_byt e_7[2]	mpeg_packet_byt e_7[1]	mpeg_packet_byt e_7[0]
0x2B	0x00	packetmemory_re g_2b	rw	mpeg_packet_byt e_8[7]	mpeg_packet_byt e_8[6]	mpeg_packet_byt e_8[5]	mpeg_packet_byt e_8[4]	mpeg_packet_byt e_8[3]	mpeg_packet_byt e_8[2]	mpeg_packet_byt e_8[1]	mpeg_packet_byt e_8[0]
0x2C	0x00	packetmemory_re g_2c	rw	mpeg_packet_byt e_9[7]	mpeg_packet_byt e_9[6]	mpeg_packet_byt e_9[5]	mpeg_packet_byt e_9[4]	mpeg_packet_byt e_9[3]	mpeg_packet_byt e_9[2]	mpeg_packet_byt e_9[1]	mpeg_packet_byt e_9[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x2D	0x00	packetmemory_re g_2d	rw	mpeg_packet_byt e_10[7]	mpeg_packet_byt e_10[6]	mpeg_packet_byt e_10[5]	mpeg_packet_byt e_10[4]	mpeg_packet_byt e_10[3]	mpeg_packet_byt e_10[2]	mpeg_packet_byt e_10[1]	mpeg_packet_byt e_10[0]
0x2E	0x00	packetmemory_re g_2e	rw	mpeg_packet_byt e_11[7]	mpeg_packet_byt e_11[6]	mpeg_packet_byt e_11[5]	mpeg_packet_byt e_11[4]	mpeg_packet_byt e_11[3]	mpeg_packet_byt e_11[2]	mpeg_packet_byt e_11[1]	mpeg_packet_byt e_11[0]
0x2F	0x00	packetmemory_re g_2f	rw	mpeg_packet_byt e_12[7]	mpeg_packet_byt e_12[6]	mpeg_packet_byt e_12[5]	mpeg_packet_byt e_12[4]	mpeg_packet_byt e_12[3]	mpeg_packet_byt e_12[2]	mpeg_packet_byt e_12[1]	mpeg_packet_byt e_12[0]
0x30	0x00	packetmemory_re g_30	rw	mpeg_packet_byt e_13[7]	mpeg_packet_byt e_13[6]	mpeg_packet_byt e_13[5]	mpeg_packet_byt e_13[4]	mpeg_packet_byt e_13[3]	mpeg_packet_byt e_13[2]	mpeg_packet_byt e_13[1]	mpeg_packet_byt e_13[0]
0x31	0x00	packetmemory_re g_31	rw	mpeg_packet_byt e_14[7]	mpeg_packet_byt e_14[6]	mpeg_packet_byt e_14[5]	mpeg_packet_byt e_14[4]	mpeg_packet_byt e_14[3]	mpeg_packet_byt e_14[2]	mpeg_packet_byt e_14[1]	mpeg_packet_byt e_14[0]
0x32	0x00	packetmemory_re g_32	rw	mpeg_packet_byt e_15[7]	mpeg_packet_byt e_15[6]	mpeg_packet_byt e_15[5]	mpeg_packet_byt e_15[4]	mpeg_packet_byt e_15[3]	mpeg_packet_byt e_15[2]	mpeg_packet_byt e_15[1]	mpeg_packet_byt e_15[0]
0x33	0x00	packetmemory_re g_33	rw	mpeg_packet_byt e_16[7]	mpeg_packet_byt e_16[6]	mpeg_packet_byt e_16[5]	mpeg_packet_byt e_16[4]	mpeg_packet_byt e_16[3]	mpeg_packet_byt e_16[2]	mpeg_packet_byt e_16[1]	mpeg_packet_byt e_16[0]
0x34	0x00	packetmemory_re g_34	rw	mpeg_packet_byt e_17[7]	mpeg_packet_byt e_17[6]	mpeg_packet_byt e_17[5]	mpeg_packet_byt e_17[4]	mpeg_packet_byt e_17[3]	mpeg_packet_byt e_17[2]	mpeg_packet_byt e_17[1]	mpeg_packet_byt e_17[0]
0x35	0x00	packetmemory_re g_35	rw	mpeg_packet_byt e_18[7]	mpeg_packet_byt e_18[6]	mpeg_packet_byt e_18[5]	mpeg_packet_byt e_18[4]	mpeg_packet_byt e_18[3]	mpeg_packet_byt e_18[2]	mpeg_packet_byt e_18[1]	mpeg_packet_byt e_18[0]
0x36	0x00	packetmemory_re g_36	rw	mpeg_packet_byt e_19[7]	mpeg_packet_byt e_19[6]	mpeg_packet_byt e_19[5]	mpeg_packet_byt e_19[4]	mpeg_packet_byt e_19[3]	mpeg_packet_byt e_19[2]	mpeg_packet_byt e_19[1]	mpeg_packet_byt e_19[0]
0x37	0x00	packetmemory_re g_37	rw	mpeg_packet_byt e_20[7]	mpeg_packet_byt e_20[6]	mpeg_packet_byt e_20[5]	mpeg_packet_byt e_20[4]	mpeg_packet_byt e_20[3]	mpeg_packet_byt e_20[2]	mpeg_packet_byt e_20[1]	mpeg_packet_byt e_20[0]
0x38	0x00	packetmemory_re g_38	rw	mpeg_packet_byt e_21[7]	mpeg_packet_byt e_21[6]	mpeg_packet_byt e_21[5]	mpeg_packet_byt e_21[4]	mpeg_packet_byt e_21[3]	mpeg_packet_byt e_21[2]	mpeg_packet_byt e_21[1]	mpeg_packet_byt e_21[0]
0x39	0x00	packetmemory_re g_39	rw	mpeg_packet_byt e_22[7]	mpeg_packet_byt e_22[6]	mpeg_packet_byt e_22[5]	mpeg_packet_byt e_22[4]	mpeg_packet_byt e_22[3]	mpeg_packet_byt e_22[2]	mpeg_packet_byt e_22[1]	mpeg_packet_byt e_22[0]
0x3A	0x00	packetmemory_re g_3a	rw	mpeg_packet_byt e_23[7]	mpeg_packet_byt e_23[6]	mpeg_packet_byt e_23[5]	mpeg_packet_byt e_23[4]	mpeg_packet_byt e_23[3]	mpeg_packet_byt e_23[2]	mpeg_packet_byt e_23[1]	mpeg_packet_byt e_23[0]
0x3B	0x00	packetmemory_re g_3b	rw	mpeg_packet_byt e_24[7]	mpeg_packet_byt e_24[6]	mpeg_packet_byt e_24[5]	mpeg_packet_byt e_24[4]	mpeg_packet_byt e_24[3]	mpeg_packet_byt e_24[2]	mpeg_packet_byt e_24[1]	mpeg_packet_byt e_24[0]
0x3C	0x00	packetmemory_re g_3c	rw	mpeg_packet_byt e_25[7]	mpeg_packet_byt e_25[6]	mpeg_packet_byt e_25[5]	mpeg_packet_byt e_25[4]	mpeg_packet_byt e_25[3]	mpeg_packet_byt e_25[2]	mpeg_packet_byt e_25[1]	mpeg_packet_byt e_25[0]
0x3D	0x00	packetmemory_re g_3d	rw	mpeg_packet_byt e_26[7]	mpeg_packet_byt e_26[6]	mpeg_packet_byt e_26[5]	mpeg_packet_byt e_26[4]	mpeg_packet_byt e_26[3]	mpeg_packet_byt e_26[2]	mpeg_packet_byt e_26[1]	mpeg_packet_byt e_26[0]
0x3E	0x00	packetmemory_re g_3e	rw	mpeg_packet_byt e_27[7]	mpeg_packet_byt e_27[6]	mpeg_packet_byt e_27[5]	mpeg_packet_byt e_27[4]	mpeg_packet_byt e_27[3]	mpeg_packet_byt e_27[2]	mpeg_packet_byt e_27[1]	mpeg_packet_byt e_27[0]
0x3F	0x00	packetmemory_re g_3f	rw	mpeg_update	-	-	-	-	-	-	-
0x40	0x00	packetmemory_re g_40	rw	acp_header_byte_ 0[7]	acp_header_byte_ 0[6]	acp_header_byte_ 0[5]	acp_header_byte_ 0[4]	acp_header_byte_ 0[3]	acp_header_byte_ 0[2]	acp_header_byte_ 0[1]	acp_header_byte_ 0[0]
0x41	0x00	packetmemory_re g_41	rw	acp_header_byte_ 1[7]	acp_header_byte_ 1[6]	acp_header_byte_ 1[5]	acp_header_byte_ 1[4]	acp_header_byte_ 1[3]	acp_header_byte_ 1[2]	acp_header_byte_ 1[1]	acp_header_byte_ 1[0]
0x42	0x00	packetmemory_re g_42	rw	acp_header_byte_ 2[7]	acp_header_byte_ 2[6]	acp_header_byte_ 2[5]	acp_header_byte_ 2[4]	acp_header_byte_ 2[3]	acp_header_byte_ 2[2]	acp_header_byte_ 2[1]	acp_header_byte_ 2[0]
0x43	0x00	packetmemory_re g_43	rw	acp_packet_byte_ 0[7]	acp_packet_byte_ 0[6]	acp_packet_byte_ 0[5]	acp_packet_byte_ 0[4]	acp_packet_byte_ 0[3]	acp_packet_byte_ 0[2]	acp_packet_byte_ 0[1]	acp_packet_byte_ 0[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x44	0x00	packetmemory_re g_44	rw	acp_packet_byte_ 1[7]	acp_packet_byte_ 1[6]	acp_packet_byte_ 1[5]	acp_packet_byte_ 1[4]	acp_packet_byte_ 1[3]	acp_packet_byte_ 1[2]	acp_packet_byte_ 1[1]	acp_packet_byte_ 1[0]
0x45	0x00	packetmemory_re g_45	rw	acp_packet_byte_ 2[7]	acp_packet_byte_ 2[6]	acp_packet_byte_ 2[5]	acp_packet_byte_ 2[4]	acp_packet_byte_ 2[3]	acp_packet_byte_ 2[2]	acp_packet_byte_ 2[1]	acp_packet_byte_ 2[0]
0x46	0x00	packetmemory_re g_46	rw	acp_packet_byte_ 3[7]	acp_packet_byte_ 3[6]	acp_packet_byte_ 3[5]	acp_packet_byte_ 3[4]	acp_packet_byte_ 3[3]	acp_packet_byte_ 3[2]	acp_packet_byte_ 3[1]	acp_packet_byte_ 3[0]
0x47	0x00	packetmemory_re g_47	rw	acp_packet_byte_ 4[7]	acp_packet_byte_ 4[6]	acp_packet_byte_ 4[5]	acp_packet_byte_ 4[4]	acp_packet_byte_ 4[3]	acp_packet_byte_ 4[2]	acp_packet_byte_ 4[1]	acp_packet_byte_ 4[0]
0x48	0x00	packetmemory_re g_48	rw	acp_packet_byte_ 5[7]	acp_packet_byte_ 5[6]	acp_packet_byte_ 5[5]	acp_packet_byte_ 5[4]	acp_packet_byte_ 5[3]	acp_packet_byte_ 5[2]	acp_packet_byte_ 5[1]	acp_packet_byte_ 5[0]
0x49	0x00	packetmemory_re g_49	rw	acp_packet_byte_ 6[7]	acp_packet_byte_ 6[6]	acp_packet_byte_ 6[5]	acp_packet_byte_ 6[4]	acp_packet_byte_ 6[3]	acp_packet_byte_ 6[2]	acp_packet_byte_ 6[1]	acp_packet_byte_ 6[0]
0x4A	0x00	packetmemory_re g_4a	rw	acp_packet_byte_ 7[7]	acp_packet_byte_ 7[6]	acp_packet_byte_ 7[5]	acp_packet_byte_ 7[4]	acp_packet_byte_ 7[3]	acp_packet_byte_ 7[2]	acp_packet_byte_ 7[1]	acp_packet_byte_ 7[0]
0x4B	0x00	packetmemory_re g_4b	rw	acp_packet_byte_ 8[7]	acp_packet_byte_ 8[6]	acp_packet_byte_ 8[5]	acp_packet_byte_ 8[4]	acp_packet_byte_ 8[3]	acp_packet_byte_ 8[2]	acp_packet_byte_ 8[1]	acp_packet_byte_ 8[0]
0x4C	0x00	packetmemory_re g_4c	rw	acp_packet_byte_ 9[7]	acp_packet_byte_ 9[6]	acp_packet_byte_ 9[5]	acp_packet_byte_ 9[4]	acp_packet_byte_ 9[3]	acp_packet_byte_ 9[2]	acp_packet_byte_ 9[1]	acp_packet_byte_ 9[0]
0x4D	0x00	packetmemory_re g_4d	rw	acp_packet_byte_ 10[7]	acp_packet_byte_ 10[6]	acp_packet_byte_ 10[5]	acp_packet_byte_ 10[4]	acp_packet_byte_ 10[3]	acp_packet_byte_ 10[2]	acp_packet_byte_ 10[1]	acp_packet_byte_ 10[0]
0x4E	0x00	packetmemory_re g_4e	rw	acp_packet_byte_ 11[7]	acp_packet_byte_ 11[6]	acp_packet_byte_ 11[5]	acp_packet_byte_ 11[4]	acp_packet_byte_ 11[3]	acp_packet_byte_ 11[2]	acp_packet_byte_ 11[1]	acp_packet_byte_ 11[0]
0x4F	0x00	packetmemory_re g_4f	rw	acp_packet_byte_ 12[7]	acp_packet_byte_ 12[6]	acp_packet_byte_ 12[5]	acp_packet_byte_ 12[4]	acp_packet_byte_ 12[3]	acp_packet_byte_ 12[2]	acp_packet_byte_ 12[1]	acp_packet_byte_ 12[0]
0x50	0x00	packetmemory_re g_50	rw	acp_packet_byte_ 13[7]	acp_packet_byte_ 13[6]	acp_packet_byte_ 13[5]	acp_packet_byte_ 13[4]	acp_packet_byte_ 13[3]	acp_packet_byte_ 13[2]	acp_packet_byte_ 13[1]	acp_packet_byte_ 13[0]
0x51	0x00	packetmemory_re g_51	rw	acp_packet_byte_ 14[7]	acp_packet_byte_ 14[6]	acp_packet_byte_ 14[5]	acp_packet_byte_ 14[4]	acp_packet_byte_ 14[3]	acp_packet_byte_ 14[2]	acp_packet_byte_ 14[1]	acp_packet_byte_ 14[0]
0x52	0x00	packetmemory_re g_52	rw	acp_packet_byte_ 15[7]	acp_packet_byte_ 15[6]	acp_packet_byte_ 15[5]	acp_packet_byte_ 15[4]	acp_packet_byte_ 15[3]	acp_packet_byte_ 15[2]	acp_packet_byte_ 15[1]	acp_packet_byte_ 15[0]
0x53	0x00	packetmemory_re g_53	rw	acp_packet_byte_ 16[7]	acp_packet_byte_ 16[6]	acp_packet_byte_ 16[5]	acp_packet_byte_ 16[4]	acp_packet_byte_ 16[3]	acp_packet_byte_ 16[2]	acp_packet_byte_ 16[1]	acp_packet_byte_ 16[0]
0x54	0x00	packetmemory_re g_54	rw	acp_packet_byte_ 17[7]	acp_packet_byte_ 17[6]	acp_packet_byte_ 17[5]	acp_packet_byte_ 17[4]	acp_packet_byte_ 17[3]	acp_packet_byte_ 17[2]	acp_packet_byte_ 17[1]	acp_packet_byte_ 17[0]
0x55	0x00	packetmemory_re g_55	rw	acp_packet_byte_ 18[7]	acp_packet_byte_ 18[6]	acp_packet_byte_ 18[5]	acp_packet_byte_ 18[4]	acp_packet_byte_ 18[3]	acp_packet_byte_ 18[2]	acp_packet_byte_ 18[1]	acp_packet_byte_ 18[0]
0x56	0x00	packetmemory_re g_56	rw	acp_packet_byte_ 19[7]	acp_packet_byte_ 19[6]	acp_packet_byte_ 19[5]	acp_packet_byte_ 19[4]	acp_packet_byte_ 19[3]	acp_packet_byte_ 19[2]	acp_packet_byte_ 19[1]	acp_packet_byte_ 19[0]
0x57	0x00	packetmemory_re g_57	rw	acp_packet_byte_ 20[7]	acp_packet_byte_ 20[6]	acp_packet_byte_ 20[5]	acp_packet_byte_ 20[4]	acp_packet_byte_ 20[3]	acp_packet_byte_ 20[2]	acp_packet_byte_ 20[1]	acp_packet_byte_ 20[0]
0x58	0x00	packetmemory_re g_58	rw	acp_packet_byte_ 21[7]	acp_packet_byte_ 21[6]	acp_packet_byte_ 21[5]	acp_packet_byte_ 21[4]	acp_packet_byte_ 21[3]	acp_packet_byte_ 21[2]	acp_packet_byte_ 21[1]	acp_packet_byte_ 21[0]
0x59	0x00	packetmemory_re g_59	rw	acp_packet_byte_ 22[7]	acp_packet_byte_ 22[6]	acp_packet_byte_ 22[5]	acp_packet_byte_ 22[4]	acp_packet_byte_ 22[3]	acp_packet_byte_ 22[2]	acp_packet_byte_ 22[1]	acp_packet_byte_ 22[0]
0x5A	0x00	packetmemory_re g_5a	rw	acp_packet_byte_ 23[7]	acp_packet_byte_ 23[6]	acp_packet_byte_ 23[5]	acp_packet_byte_ 23[4]	acp_packet_byte_ 23[3]	acp_packet_byte_ 23[2]	acp_packet_byte_ 23[1]	acp_packet_byte_ 23[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x5B	0x00	packetmemory_re g_5b	rw	acp_packet_byte_ 24[7]	acp_packet_byte_ 24[6]	acp_packet_byte_ 24[5]	acp_packet_byte_ 24[4]	acp_packet_byte_ 24[3]	acp_packet_byte_ 24[2]	acp_packet_byte_ 24[1]	acp_packet_byte_ 24[0]
0x5C	0x00	packetmemory_re g_5c	rw	acp_packet_byte_ 25[7]	acp_packet_byte_ 25[6]	acp_packet_byte_ 25[5]	acp_packet_byte_ 25[4]	acp_packet_byte_ 25[3]	acp_packet_byte_ 25[2]	acp_packet_byte_ 25[1]	acp_packet_byte_ 25[0]
0x5D	0x00	packetmemory_re g_5d	rw	acp_packet_byte_ 26[7]	acp_packet_byte_ 26[6]	acp_packet_byte_ 26[5]	acp_packet_byte_ 26[4]	acp_packet_byte_ 26[3]	acp_packet_byte_ 26[2]	acp_packet_byte_ 26[1]	acp_packet_byte_ 26[0]
0x5E	0x00	packetmemory_re g_5e	rw	acp_packet_byte_ 27[7]	acp_packet_byte_ 27[6]	acp_packet_byte_ 27[5]	acp_packet_byte_ 27[4]	acp_packet_byte_ 27[3]	acp_packet_byte_ 27[2]	acp_packet_byte_ 27[1]	acp_packet_byte_ 27[0]
0x5F	0x00	packetmemory_re g_5f	rw	acp_update	-	-	-	-	-	-	-
0x60	0x00	packetmemory_re g_60	rw	isrc1_header_byte_ _0[7]	isrc1_header_byte_ _0[6]	isrc1_header_byte_ _0[5]	isrc1_header_byte_ _0[4]	isrc1_header_byte_ _0[3]	isrc1_header_byte_ _0[2]	isrc1_header_byte_ _0[1]	isrc1_header_byte_ _0[0]
0x61	0x00	packetmemory_re g_61	rw	isrc1_header_byte_ _1[7]	isrc1_header_byte_ _1[6]	isrc1_header_byte_ _1[5]	isrc1_header_byte_ _1[4]	isrc1_header_byte_ _1[3]	isrc1_header_byte_ _1[2]	isrc1_header_byte_ _1[1]	isrc1_header_byte_ _1[0]
0x62	0x00	packetmemory_re g_62	rw	isrc1_header_byte_ _2[7]	isrc1_header_byte_ _2[6]	isrc1_header_byte_ _2[5]	isrc1_header_byte_ _2[4]	isrc1_header_byte_ _2[3]	isrc1_header_byte_ _2[2]	isrc1_header_byte_ _2[1]	isrc1_header_byte_ _2[0]
0x63	0x00	packetmemory_re g_63	rw	isrc1_packet_byte_ _0[7]	isrc1_packet_byte_ _0[6]	isrc1_packet_byte_ _0[5]	isrc1_packet_byte_ _0[4]	isrc1_packet_byte_ _0[3]	isrc1_packet_byte_ _0[2]	isrc1_packet_byte_ _0[1]	isrc1_packet_byte_ _0[0]
0x64	0x00	packetmemory_re g_64	rw	isrc1_packet_byte_ _1[7]	isrc1_packet_byte_ _1[6]	isrc1_packet_byte_ _1[5]	isrc1_packet_byte_ _1[4]	isrc1_packet_byte_ _1[3]	isrc1_packet_byte_ _1[2]	isrc1_packet_byte_ _1[1]	isrc1_packet_byte_ _1[0]
0x65	0x00	packetmemory_re g_65	rw	isrc1_packet_byte_ _2[7]	isrc1_packet_byte_ _2[6]	isrc1_packet_byte_ _2[5]	isrc1_packet_byte_ _2[4]	isrc1_packet_byte_ _2[3]	isrc1_packet_byte_ _2[2]	isrc1_packet_byte_ _2[1]	isrc1_packet_byte_ _2[0]
0x66	0x00	packetmemory_re g_66	rw	isrc1_packet_byte_ _3[7]	isrc1_packet_byte_ _3[6]	isrc1_packet_byte_ _3[5]	isrc1_packet_byte_ _3[4]	isrc1_packet_byte_ _3[3]	isrc1_packet_byte_ _3[2]	isrc1_packet_byte_ _3[1]	isrc1_packet_byte_ _3[0]
0x67	0x00	packetmemory_re g_67	rw	isrc1_packet_byte_ _4[7]	isrc1_packet_byte_ _4[6]	isrc1_packet_byte_ _4[5]	isrc1_packet_byte_ _4[4]	isrc1_packet_byte_ _4[3]	isrc1_packet_byte_ _4[2]	isrc1_packet_byte_ _4[1]	isrc1_packet_byte_ _4[0]
0x68	0x00	packetmemory_re g_68	rw	isrc1_packet_byte_ _5[7]	isrc1_packet_byte_ _5[6]	isrc1_packet_byte_ _5[5]	isrc1_packet_byte_ _5[4]	isrc1_packet_byte_ _5[3]	isrc1_packet_byte_ _5[2]	isrc1_packet_byte_ _5[1]	isrc1_packet_byte_ _5[0]
0x69	0x00	packetmemory_re g_69	rw	isrc1_packet_byte_ _6[7]	isrc1_packet_byte_ _6[6]	isrc1_packet_byte_ _6[5]	isrc1_packet_byte_ _6[4]	isrc1_packet_byte_ _6[3]	isrc1_packet_byte_ _6[2]	isrc1_packet_byte_ _6[1]	isrc1_packet_byte_ _6[0]
0x6A	0x00	packetmemory_re g_6a	rw	isrc1_packet_byte_ _7[7]	isrc1_packet_byte_ _7[6]	isrc1_packet_byte_ _7[5]	isrc1_packet_byte_ _7[4]	isrc1_packet_byte_ _7[3]	isrc1_packet_byte_ _7[2]	isrc1_packet_byte_ _7[1]	isrc1_packet_byte_ _7[0]
0x6B	0x00	packetmemory_re g_6b	rw	isrc1_packet_byte_ _8[7]	isrc1_packet_byte_ _8[6]	isrc1_packet_byte_ _8[5]	isrc1_packet_byte_ _8[4]	isrc1_packet_byte_ _8[3]	isrc1_packet_byte_ _8[2]	isrc1_packet_byte_ _8[1]	isrc1_packet_byte_ _8[0]
0x6C	0x00	packetmemory_re g_6c	rw	isrc1_packet_byte_ _9[7]	isrc1_packet_byte_ _9[6]	isrc1_packet_byte_ _9[5]	isrc1_packet_byte_ _9[4]	isrc1_packet_byte_ _9[3]	isrc1_packet_byte_ _9[2]	isrc1_packet_byte_ _9[1]	isrc1_packet_byte_ _9[0]
0x6D	0x00	packetmemory_re g_6d	rw	isrc1_packet_byte_ _10[7]	isrc1_packet_byte_ _10[6]	isrc1_packet_byte_ _10[5]	isrc1_packet_byte_ _10[4]	isrc1_packet_byte_ _10[3]	isrc1_packet_byte_ _10[2]	isrc1_packet_byte_ _10[1]	isrc1_packet_byte_ _10[0]
0x6E	0x00	packetmemory_re g_6e	rw	isrc1_packet_byte_ _11[7]	isrc1_packet_byte_ _11[6]	isrc1_packet_byte_ _11[5]	isrc1_packet_byte_ _11[4]	isrc1_packet_byte_ _11[3]	isrc1_packet_byte_ _11[2]	isrc1_packet_byte_ _11[1]	isrc1_packet_byte_ _11[0]
0x6F	0x00	packetmemory_re g_6f	rw	isrc1_packet_byte_ _12[7]	isrc1_packet_byte_ _12[6]	isrc1_packet_byte_ _12[5]	isrc1_packet_byte_ _12[4]	isrc1_packet_byte_ _12[3]	isrc1_packet_byte_ _12[2]	isrc1_packet_byte_ _12[1]	isrc1_packet_byte_ _12[0]
0x70	0x00	packetmemory_re g_70	r	isrc1_packet_byte_ _13[7]	isrc1_packet_byte_ _13[6]	isrc1_packet_byte_ _13[5]	isrc1_packet_byte_ _13[4]	isrc1_packet_byte_ _13[3]	isrc1_packet_byte_ _13[2]	isrc1_packet_byte_ _13[1]	isrc1_packet_byte_ _13[0]
0x71	0x00	packetmemory_re g_71	r	isrc1_packet_byte_ _14[7]	isrc1_packet_byte_ _14[6]	isrc1_packet_byte_ _14[5]	isrc1_packet_byte_ _14[4]	isrc1_packet_byte_ _14[3]	isrc1_packet_byte_ _14[2]	isrc1_packet_byte_ _14[1]	isrc1_packet_byte_ _14[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x72	0x00	packetmemory_re g_72	r	isrc1_packet_byte _15[7]	isrc1_packet_byte _15[6]	isrc1_packet_byte _15[5]	isrc1_packet_byte _15[4]	isrc1_packet_byte _15[3]	isrc1_packet_byte _15[2]	isrc1_packet_byte _15[1]	isrc1_packet_byte _15[0]
0x73	0x00	packetmemory_re g_73	r	isrc1_packet_byte _16[7]	isrc1_packet_byte _16[6]	isrc1_packet_byte _16[5]	isrc1_packet_byte _16[4]	isrc1_packet_byte _16[3]	isrc1_packet_byte _16[2]	isrc1_packet_byte _16[1]	isrc1_packet_byte _16[0]
0x74	0x00	packetmemory_re g_74	r	isrc1_packet_byte _17[7]	isrc1_packet_byte _17[6]	isrc1_packet_byte _17[5]	isrc1_packet_byte _17[4]	isrc1_packet_byte _17[3]	isrc1_packet_byte _17[2]	isrc1_packet_byte _17[1]	isrc1_packet_byte _17[0]
0x75	0x00	packetmemory_re g_75	rw	isrc1_packet_byte _18[7]	isrc1_packet_byte _18[6]	isrc1_packet_byte _18[5]	isrc1_packet_byte _18[4]	isrc1_packet_byte _18[3]	isrc1_packet_byte _18[2]	isrc1_packet_byte _18[1]	isrc1_packet_byte _18[0]
0x76	0x00	packetmemory_re g_76	rw	isrc1_packet_byte _19[7]	isrc1_packet_byte _19[6]	isrc1_packet_byte _19[5]	isrc1_packet_byte _19[4]	isrc1_packet_byte _19[3]	isrc1_packet_byte _19[2]	isrc1_packet_byte _19[1]	isrc1_packet_byte _19[0]
0x77	0x00	packetmemory_re g_77	rw	isrc1_packet_byte _20[7]	isrc1_packet_byte _20[6]	isrc1_packet_byte _20[5]	isrc1_packet_byte _20[4]	isrc1_packet_byte _20[3]	isrc1_packet_byte _20[2]	isrc1_packet_byte _20[1]	isrc1_packet_byte _20[0]
0x78	0x00	packetmemory_re g_78	rw	isrc1_packet_byte _21[7]	isrc1_packet_byte _21[6]	isrc1_packet_byte _21[5]	isrc1_packet_byte _21[4]	isrc1_packet_byte _21[3]	isrc1_packet_byte _21[2]	isrc1_packet_byte _21[1]	isrc1_packet_byte _21[0]
0x79	0x00	packetmemory_re g_79	rw	isrc1_packet_byte _22[7]	isrc1_packet_byte _22[6]	isrc1_packet_byte _22[5]	isrc1_packet_byte _22[4]	isrc1_packet_byte _22[3]	isrc1_packet_byte _22[2]	isrc1_packet_byte _22[1]	isrc1_packet_byte _22[0]
0x7A	0x00	packetmemory_re g_7a	rw	isrc1_packet_byte _23[7]	isrc1_packet_byte _23[6]	isrc1_packet_byte _23[5]	isrc1_packet_byte _23[4]	isrc1_packet_byte _23[3]	isrc1_packet_byte _23[2]	isrc1_packet_byte _23[1]	isrc1_packet_byte _23[0]
0x7B	0x00	packetmemory_re g_7b	rw	isrc1_packet_byte _24[7]	isrc1_packet_byte _24[6]	isrc1_packet_byte _24[5]	isrc1_packet_byte _24[4]	isrc1_packet_byte _24[3]	isrc1_packet_byte _24[2]	isrc1_packet_byte _24[1]	isrc1_packet_byte _24[0]
0x7C	0x00	packetmemory_re g_7c	rw	isrc1_packet_byte _25[7]	isrc1_packet_byte _25[6]	isrc1_packet_byte _25[5]	isrc1_packet_byte _25[4]	isrc1_packet_byte _25[3]	isrc1_packet_byte _25[2]	isrc1_packet_byte _25[1]	isrc1_packet_byte _25[0]
0x7D	0x00	packetmemory_re g_7d	rw	isrc1_packet_byte _26[7]	isrc1_packet_byte _26[6]	isrc1_packet_byte _26[5]	isrc1_packet_byte _26[4]	isrc1_packet_byte _26[3]	isrc1_packet_byte _26[2]	isrc1_packet_byte _26[1]	isrc1_packet_byte _26[0]
0x7E	0x00	packetmemory_re g_7e	rw	isrc1_packet_byte _27[7]	isrc1_packet_byte _27[6]	isrc1_packet_byte _27[5]	isrc1_packet_byte _27[4]	isrc1_packet_byte _27[3]	isrc1_packet_byte _27[2]	isrc1_packet_byte _27[1]	isrc1_packet_byte _27[0]
0x7F	0x00	packetmemory_re g_7f	rw	isrc1_update	-	-	-	-	-	-	-
0x80	0x00	packetmemory_re g_80	rw	isrc2_header_byte _0[7]	isrc2_header_byte _0[6]	isrc2_header_byte _0[5]	isrc2_header_byte _0[4]	isrc2_header_byte _0[3]	isrc2_header_byte _0[2]	isrc2_header_byte _0[1]	isrc2_header_byte _0[0]
0x81	0x00	packetmemory_re g_81	rw	isrc2_header_byte _1[7]	isrc2_header_byte _1[6]	isrc2_header_byte _1[5]	isrc2_header_byte _1[4]	isrc2_header_byte _1[3]	isrc2_header_byte _1[2]	isrc2_header_byte _1[1]	isrc2_header_byte _1[0]
0x82	0x00	packetmemory_re g_82	rw	isrc2_header_byte _2[7]	isrc2_header_byte _2[6]	isrc2_header_byte _2[5]	isrc2_header_byte _2[4]	isrc2_header_byte _2[3]	isrc2_header_byte _2[2]	isrc2_header_byte _2[1]	isrc2_header_byte _2[0]
0x83	0x00	packetmemory_re g_83	rw	isrc2_packet_byte _0[7]	isrc2_packet_byte _0[6]	isrc2_packet_byte _0[5]	isrc2_packet_byte _0[4]	isrc2_packet_byte _0[3]	isrc2_packet_byte _0[2]	isrc2_packet_byte _0[1]	isrc2_packet_byte _0[0]
0x84	0x00	packetmemory_re g_84	rw	isrc2_packet_byte _1[7]	isrc2_packet_byte _1[6]	isrc2_packet_byte _1[5]	isrc2_packet_byte _1[4]	isrc2_packet_byte _1[3]	isrc2_packet_byte _1[2]	isrc2_packet_byte _1[1]	isrc2_packet_byte _1[0]
0x85	0x00	packetmemory_re g_85	rw	isrc2_packet_byte _2[7]	isrc2_packet_byte _2[6]	isrc2_packet_byte _2[5]	isrc2_packet_byte _2[4]	isrc2_packet_byte _2[3]	isrc2_packet_byte _2[2]	isrc2_packet_byte _2[1]	isrc2_packet_byte _2[0]
0x86	0x00	packetmemory_re g_86	rw	isrc2_packet_byte _3[7]	isrc2_packet_byte _3[6]	isrc2_packet_byte _3[5]	isrc2_packet_byte _3[4]	isrc2_packet_byte _3[3]	isrc2_packet_byte _3[2]	isrc2_packet_byte _3[1]	isrc2_packet_byte _3[0]
0x87	0x00	packetmemory_re g_87	rw	isrc2_packet_byte _4[7]	isrc2_packet_byte _4[6]	isrc2_packet_byte _4[5]	isrc2_packet_byte _4[4]	isrc2_packet_byte _4[3]	isrc2_packet_byte _4[2]	isrc2_packet_byte _4[1]	isrc2_packet_byte _4[0]
0x88	0x00	packetmemory_re g_88	rw	isrc2_packet_byte _5[7]	isrc2_packet_byte _5[6]	isrc2_packet_byte _5[5]	isrc2_packet_byte _5[4]	isrc2_packet_byte _5[3]	isrc2_packet_byte _5[2]	isrc2_packet_byte _5[1]	isrc2_packet_byte _5[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xA0	0x00	packetmemory_re g_a0	rw	gm_header_byte_ 0[7]	gm_header_byte_ 0[6]	gm_header_byte_ 0[5]	gm_header_byte_ 0[4]	gm_header_byte_ 0[3]	gm_header_byte_ 0[2]	gm_header_byte_ 0[1]	gm_header_byte_ 0[0]
0xA1	0x00	packetmemory_re g_a1	rw	gm_header_byte_ 1[7]	gm_header_byte_ 1[6]	gm_header_byte_ 1[5]	gm_header_byte_ 1[4]	gm_header_byte_ 1[3]	gm_header_byte_ 1[2]	gm_header_byte_ 1[1]	gm_header_byte_ 1[0]
0xA2	0x00	packetmemory_re g_a2	rw	gm_header_byte_ 2[7]	gm_header_byte_ 2[6]	gm_header_byte_ 2[5]	gm_header_byte_ 2[4]	gm_header_byte_ 2[3]	gm_header_byte_ 2[2]	gm_header_byte_ 2[1]	gm_header_byte_ 2[0]
0xA3	0x00	packetmemory_re g_a3	rw	gm_packet_byte_ 0[7]	gm_packet_byte_ 0[6]	gm_packet_byte_ 0[5]	gm_packet_byte_ 0[4]	gm_packet_byte_ 0[3]	gm_packet_byte_ 0[2]	gm_packet_byte_ 0[1]	gm_packet_byte_ 0[0]
0xA4	0x00	packetmemory_re g_a4	rw	gm_packet_byte_ 1[7]	gm_packet_byte_ 1[6]	gm_packet_byte_ 1[5]	gm_packet_byte_ 1[4]	gm_packet_byte_ 1[3]	gm_packet_byte_ 1[2]	gm_packet_byte_ 1[1]	gm_packet_byte_ 1[0]
0xA5	0x00	packetmemory_re g_a5	rw	gm_packet_byte_ 2[7]	gm_packet_byte_ 2[6]	gm_packet_byte_ 2[5]	gm_packet_byte_ 2[4]	gm_packet_byte_ 2[3]	gm_packet_byte_ 2[2]	gm_packet_byte_ 2[1]	gm_packet_byte_ 2[0]
0xA6	0x00	packetmemory_re g_a6	rw	gm_packet_byte_ 3[7]	gm_packet_byte_ 3[6]	gm_packet_byte_ 3[5]	gm_packet_byte_ 3[4]	gm_packet_byte_ 3[3]	gm_packet_byte_ 3[2]	gm_packet_byte_ 3[1]	gm_packet_byte_ 3[0]
0xA7	0x00	packetmemory_re g_a7	rw	gm_packet_byte_ 4[7]	gm_packet_byte_ 4[6]	gm_packet_byte_ 4[5]	gm_packet_byte_ 4[4]	gm_packet_byte_ 4[3]	gm_packet_byte_ 4[2]	gm_packet_byte_ 4[1]	gm_packet_byte_ 4[0]
0xA8	0x00	packetmemory_re g_a8	rw	gm_packet_byte_ 5[7]	gm_packet_byte_ 5[6]	gm_packet_byte_ 5[5]	gm_packet_byte_ 5[4]	gm_packet_byte_ 5[3]	gm_packet_byte_ 5[2]	gm_packet_byte_ 5[1]	gm_packet_byte_ 5[0]
0xA9	0x00	packetmemory_re g_a9	rw	gm_packet_byte_ 6[7]	gm_packet_byte_ 6[6]	gm_packet_byte_ 6[5]	gm_packet_byte_ 6[4]	gm_packet_byte_ 6[3]	gm_packet_byte_ 6[2]	gm_packet_byte_ 6[1]	gm_packet_byte_ 6[0]
0xAA	0x00	packetmemory_re g_aa	rw	gm_packet_byte_ 7[7]	gm_packet_byte_ 7[6]	gm_packet_byte_ 7[5]	gm_packet_byte_ 7[4]	gm_packet_byte_ 7[3]	gm_packet_byte_ 7[2]	gm_packet_byte_ 7[1]	gm_packet_byte_ 7[0]
0xAB	0x00	packetmemory_re g_ab	rw	gm_packet_byte_ 8[7]	gm_packet_byte_ 8[6]	gm_packet_byte_ 8[5]	gm_packet_byte_ 8[4]	gm_packet_byte_ 8[3]	gm_packet_byte_ 8[2]	gm_packet_byte_ 8[1]	gm_packet_byte_ 8[0]
0xAC	0x00	packetmemory_re g_ac	rw	gm_packet_byte_ 9[7]	gm_packet_byte_ 9[6]	gm_packet_byte_ 9[5]	gm_packet_byte_ 9[4]	gm_packet_byte_ 9[3]	gm_packet_byte_ 9[2]	gm_packet_byte_ 9[1]	gm_packet_byte_ 9[0]
0xAD	0x00	packetmemory_re g_ad	rw	gm_packet_byte_ 10[7]	gm_packet_byte_ 10[6]	gm_packet_byte_ 10[5]	gm_packet_byte_ 10[4]	gm_packet_byte_ 10[3]	gm_packet_byte_ 10[2]	gm_packet_byte_ 10[1]	gm_packet_byte_ 10[0]
0xAE	0x00	packetmemory_re g_ae	rw	gm_packet_byte_ 11[7]	gm_packet_byte_ 11[6]	gm_packet_byte_ 11[5]	gm_packet_byte_ 11[4]	gm_packet_byte_ 11[3]	gm_packet_byte_ 11[2]	gm_packet_byte_ 11[1]	gm_packet_byte_ 11[0]
0xAF	0x00	packetmemory_re g_af	rw	gm_packet_byte_ 12[7]	gm_packet_byte_ 12[6]	gm_packet_byte_ 12[5]	gm_packet_byte_ 12[4]	gm_packet_byte_ 12[3]	gm_packet_byte_ 12[2]	gm_packet_byte_ 12[1]	gm_packet_byte_ 12[0]
0xB0	0x00	packetmemory_re g_b0	rw	gm_packet_byte_ 13[7]	gm_packet_byte_ 13[6]	gm_packet_byte_ 13[5]	gm_packet_byte_ 13[4]	gm_packet_byte_ 13[3]	gm_packet_byte_ 13[2]	gm_packet_byte_ 13[1]	gm_packet_byte_ 13[0]
0xB1	0x00	packetmemory_re g_b1	rw	gm_packet_byte_ 14[7]	gm_packet_byte_ 14[6]	gm_packet_byte_ 14[5]	gm_packet_byte_ 14[4]	gm_packet_byte_ 14[3]	gm_packet_byte_ 14[2]	gm_packet_byte_ 14[1]	gm_packet_byte_ 14[0]
0xB2	0x00	packetmemory_re g_b2	rw	gm_packet_byte_ 15[7]	gm_packet_byte_ 15[6]	gm_packet_byte_ 15[5]	gm_packet_byte_ 15[4]	gm_packet_byte_ 15[3]	gm_packet_byte_ 15[2]	gm_packet_byte_ 15[1]	gm_packet_byte_ 15[0]
0xB3	0x00	packetmemory_re g_b3	rw	gm_packet_byte_ 16[7]	gm_packet_byte_ 16[6]	gm_packet_byte_ 16[5]	gm_packet_byte_ 16[4]	gm_packet_byte_ 16[3]	gm_packet_byte_ 16[2]	gm_packet_byte_ 16[1]	gm_packet_byte_ 16[0]
0xB4	0x00	packetmemory_re g_b4	rw	gm_packet_byte_ 17[7]	gm_packet_byte_ 17[6]	gm_packet_byte_ 17[5]	gm_packet_byte_ 17[4]	gm_packet_byte_ 17[3]	gm_packet_byte_ 17[2]	gm_packet_byte_ 17[1]	gm_packet_byte_ 17[0]
0xB5	0x00	packetmemory_re g_b5	rw	gm_packet_byte_ 18[7]	gm_packet_byte_ 18[6]	gm_packet_byte_ 18[5]	gm_packet_byte_ 18[4]	gm_packet_byte_ 18[3]	gm_packet_byte_ 18[2]	gm_packet_byte_ 18[1]	gm_packet_byte_ 18[0]
0xB6	0x00	packetmemory_re g_b6	rw	gm_packet_byte_ 19[7]	gm_packet_byte_ 19[6]	gm_packet_byte_ 19[5]	gm_packet_byte_ 19[4]	gm_packet_byte_ 19[3]	gm_packet_byte_ 19[2]	gm_packet_byte_ 19[1]	gm_packet_byte_ 19[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xFC	0x00	packetmemory_reg_fc	rw	spare_packet_2_packet_byte_25[7]	spare_packet_2_packet_byte_25[6]	spare_packet_2_packet_byte_25[5]	spare_packet_2_packet_byte_25[4]	spare_packet_2_packet_byte_25[3]	spare_packet_2_packet_byte_25[2]	spare_packet_2_packet_byte_25[1]	spare_packet_2_packet_byte_25[0]
0xFD	0x00	packetmemory_reg_fd	rw	spare_packet_2_packet_byte_26[7]	spare_packet_2_packet_byte_26[6]	spare_packet_2_packet_byte_26[5]	spare_packet_2_packet_byte_26[4]	spare_packet_2_packet_byte_26[3]	spare_packet_2_packet_byte_26[2]	spare_packet_2_packet_byte_26[1]	spare_packet_2_packet_byte_26[0]
0xFE	0x00	packetmemory_reg_fe	rw	spare_packet_2_packet_byte_27[7]	spare_packet_2_packet_byte_27[6]	spare_packet_2_packet_byte_27[5]	spare_packet_2_packet_byte_27[4]	spare_packet_2_packet_byte_27[3]	spare_packet_2_packet_byte_27[2]	spare_packet_2_packet_byte_27[1]	spare_packet_2_packet_byte_27[0]
0xFF	0x00	packetmemory_reg_ff	rw	spare2_update	-	-	-	-	-	-	-

2 SIGNAL DOCUMENTATION

2.1 ADDR 40 (IO)

Reg	Bits	Description	
ADC_HDMI_SIMULT_MODE			R/W
0x01	00000000	This control is used to enable ADC and HDMI simultaneous mode. In this mode, certain HDMI functionality is available when processing analog inputs. 0 - Disable simultaneous mode 1 - Enable simultaneous mode	
SYNC_CH_AUTO_MODE			R/W
0x07	01000000	This control is used to set automatic synchronization channel selection to the CP core. Auto mode selects which synchronization channel drives the CP based on the free run status of each channel. The priority of selection is determined by SYNC_CH1_PRIORITY when both channels are in free run mode. 0 - Disable auto mode 1 - Enable auto mode	
SYNC_CH1_PRIORITY			R/W
0x07	01000000	This control is used to select which sync channel has priority to the CP core. 0 - Sync channel 2 processing result takes priority 1 - Sync channel 1 sync processing result takes priority	
SYNC_CH1_HS_SEL[1:0]			R/W
0x07	01000000	This control is used to select the HSync input to sync channel 1. 00 - Auto-select mode; hs_in1 or HSync from HDMI (HDMI-HS) set to channel 1 based on primary mode set in prim_mode[3:0]. HDMI-HS selected in HDMI mode. HS1 input selected in component or graphics mode. 01 - Select hs_in1 10 - Select hs_in2 11 - HDMI-HS	
SYNC_CH1_VS_SEL[1:0]			R/W
0x07	01000000	This control is used to select the VSync input to sync channel 1. 00 - Auto-select mode; vs_in1 or VSync from HDMI (HDMI-VS) set to channel 1 based on primary mode set in prim_mode[3:0]. HDMI-VS selected in HDMI mode. VS1 input selected in component or graphics mode. 01 - Select vs_in1 input 10 - Select vs_in2 input 11 - Reserved	
SYNC_CH1_EMB_SYNC_SEL[1:0]			R/W
0x07	01000000	This control is used to select from the outputs of the two synchronization sources as input to sync channel 1. 00 - Auto-select mode; emb_sync_sel1 in component or graphics mode or tied low in HDMI mode. The selection is based on primary mode. 01 - emb_sync_sel1 10 - emb_sync_sel2 11 - Tie to GND	
SYNC_CH2_HS_SEL[1:0]			R/W
0x08	00010100	This control is used to select the HSync input to sync channel 2. 00 - Select HS2 input 01 - Select HS1 input 10 - Select HS2 input 11 - Select HDMI HS	
SYNC_CH2_VS_SEL[1:0]			R/W
0x08	00010100	This control is used to select the VSync input to sync channel 2. 00 - Select VS2 input 01 - Select VS1 input 10 - Select VS2 input 11 - Select HDMI VS	
SYNC_CH2_EMB_SYNC_SEL[1:0]			R/W
0x08	00010100	This control is used to select from the outputs of the two sync slicers as input to sync channel 2. 00 - emb_sync_sel2 01 - emb_sync_sel1 10 - emb_sync_sel2 11 - Tie to GND	

Reg	Bits	Description	
CORE_PDN			R/W
0x0B	000000 <u>00</u>	This control is used to power down the DPP, CP core and digital sections of the HDMI core. 0 - Power up DPP, CP, SDP and digital sections of HDMI block. 1 - Power down DPP, CP, SDP and digital sections of HDMI block. STDI and SSPD still active when core_pdn set.	
XTAL_PDN			R/W
0x0B	000000 <u>00</u>	This control is used to power down the xtal in the digital blocks. 0 - Power up xtal buffer to digital core 1 - Power down xtal buffer to digital core	
POWER_DOWN			R/W
0x0C	01 <u>100000</u>	This control is used to enable power-down mode. This is the main I2C power-down control. 0 - Chip operational 1 - Enable chip power down	
CH1 DLY SEL[1:0]			R/W
0x11	00 <u>000000</u>	This control is used to select the delay in terms of pixels for channel 1 (i.e. Y/G). 00 - No delay 01 - 1 pixel delay 10 - 2 pixel delay 11 - 3 pixel delay	
CH2 DLY SEL[1:0]			R/W
0x11	000000 <u>00</u>	This control is used to select the delay in terms of pixels for channel 2 (i.e. V/R). 00 - No delay 01 - 1 pixel delay 10 - 2 pixel delay 11 - 3 pixel delay	
CH3 DLY SEL[1:0]			R/W
0x11	000000 <u>00</u>	This control is used to select the delay in terms of pixels for channel 3 (i.e. U/B). 00 - No delay 01 - 1 pixel delay 10 - 2 pixel delay 11 - 3 pixel delay	
SEL_SYNC_CHANNEL			R
0x12	0 <u>0000000</u>	This readback indicates the currently selected sync processing channel applied to the CP core. 0 - Sync channel 2 processed by CP core 1 - Sync channel 1 processed by CP core	
CP_STDI_INTERLACED			R
0x12	000 <u>00000</u>	This readback indicates the interlaced status of the currently selected STDI block applied to the CP core. 0 - Selected STDI detected progressive input 1 - Selected STDI detected interlaced input	
CP_INTERLACED			R
0x12	00000 <u>000</u>	This readback indicates the interlaced status of the CP core based on the configuration of the video standard and Interlaced bit in the CP Map. 0 - CP core processing input as progressive input 1 - CP core processing input as interlaced input	
CP_PROG_PARM_FOR_INT			R
0x12	00000 <u>000</u>	This readback indicates if the CP core is processing for progressive standard while the video standard and the Interlaced bit in the CP Map are configured for an interlaced standard. 0 - CP core processing for progressive standard when video standard and Interlaced bits configured for interlaced standard 1 - CP core processing for progressive standard when video standard and Interlaced bits configured for progressive standard	
CP_FORCE_INTERLACED			R
0x12	000000 <u>00</u>	This readback indicates the forced-interlaced status of the CP core based on the configuration of the video standard and the Interlaced bit in the CP Map. 0 - Input detected as interlaced and CP programmed in interlaced mode via vid_std[5:0] 1 - Input detected as progressive and CP programmed in interlaced mode	

Reg	Bits	Description	
CP_NON_STD_VIDEO			R
0x12	00000000	This control is used to indicate that the CP core has detected a non standard number of lines on the incoming video compared to the standard specified by vid_std[5:0]. 0 - Input has same number of lines as that of format programmed 1 - Input has different number of lines to that of format programmed	
CP_CURRENT_SYNC_SRC[1:0]			R
0x13	00000000	This readback indicates the synchronization source currently being used by CP core 00 - Invalid 01 - Separate HSync and VSync on HS_IN and VS_IN pins 10 - External CSync on HS_IN pin 11 - Embedded synchronization (SOG/SOY)	
TRI_AUDIO			R/W
0x15	10111110	This control is used to tristate the HDMI audio output interface pins, HA_AP[5:0]. 0 - HDMI audio output pins active 1 - Tristate audio output pins	
TX_SOFT_RESET			SC
0x1B	00000000	This control is used for software reset of the HDMI Tx. This is a self clearing bit. 1 - Software reset to Tx block	
VDP DATA PACKET SIZE[5:0]			R/W
0x1C	10111111	This control is used to tell the SPI master how many bits to transmit.	
VDP SPI MASTER BUSY			R
0x1D	00000000	This readback indicates the status of the SPI interface. 0 - Master idle 1 - Master busy	
VDP SPI SLAVE BUSY			R
0x1D	00000000	This readback indicates the status of the SPI interface. 0 - Slave idle 1 - Slave busy	
SPI CONFIG[1:0]			R/W
0x1E	00101110	This control is used to configure the SPI interface for transmitting VDP data. 00 - Tristate 01 - Master 10 - Slave configuration	
VDP_DEDICATED_INTR_EN			R/W
0x1E	00101110	This control is used to route the VDP interrupt to a dedicated pin I2S2. 0 - Dedicated VDP interrupt disabled 1 - Dedicated VDP interrupt	
SPI MASTER CLOCK SEL[1:0]			R/W
0x1E	00101110	This control is used to select the SPI clock frequency when the ADV7850 is configured as SPI master. 0 - xtal clock 1 - xtal divide by 2 2 - xtal divide by 4 3 - xtal divide by 8	
VDP_INTR_ACTIVE_LOW			R/W
0x1E	00101110	This control is used to configure the VDP dedicated interrupt pin active output level. 0 - Active high operation 1 - Active low operation	
HPA_MAN_VALUE_A			R/W
0x20	00000000	This control is used to set the value of HPA on Port A. It is only valid if hpa_manual is set to 1. 0 - 0 V applied to HPA_A pin 1 - High level applied to HPA_A pin	
HPA_MAN_VALUE_B			R/W
0x20	00000000	This control is used to set the value of HPA on Port B. It is only valid if hpa_manual is set to 1. 0 - 0 V applied to HPA_B pin 1 - High level applied to HPA_B pin	

Reg	Bits	Description	
HPA_MAN_VALUE_C			R/W
0x20	00000000	This control is used to set the value of HPA on Port C. It is only valid if hpa_manual is set to 1. 0 - 0 V applied to HPA_C pin 1 - High level applied to HPA_C pin	
HPA_MAN_VALUE_D			R/W
0x20	00000000	This control is used to set the value of HPA on Port D. It is only valid if hpa_manual is set to 1. 0 - 0 V applied to HPA_D pin 1 - High level applied to HPA_D pin	
HPA_TRISTATE_A			R/W
0x20	00000000	This control is used to tristate the HPA output pin for Port A. 0 - HPA_A pin active 1 - Tristate HPA_A pin	
HPA_TRISTATE_B			R/W
0x20	00000000	This control is used to tristate the HPA output pin for Port B. 0 - HPA_B pin active 1 - Tristate HPA_B pin	
HPA_TRISTATE_C			R/W
0x20	00000000	This control is used to tristate the HPA output pin for Port C. 0 - HPA_C pin active 1 - Tristate HPA_C pin	
HPA_TRISTATE_D			R/W
0x20	00000000	This control is used to tristate the HPA output pin for Port D. 0 - HPA_D pin active 1 - Tristate HPA_D pin	
HPA_STATUS_PORT_A			R
0x21	00000000	This readback displays the HPA status for Port A. 0 - +5 V not applied to HPA_A pin by chip 1 - +5 V applied to HPA_A pin by chip	
HPA_STATUS_PORT_B			R
0x21	00000000	This readback displays the HPA status for Port B. 0 - +5 V not applied to HPA_B pin by chip 1 - +5 V applied to HPA_B pin by chip	
HPA_STATUS_PORT_C			R
0x21	00000000	This readback displays the HPA status for Port C. 0 - +5 V not applied to HPA_C pin by chip 1 - +5 V applied to HPA_C pin by chip	
HPA_STATUS_PORT_D			R
0x21	00000000	This readback displays the HPA status for Port D. 0 - +5 V not applied to HPA_D pin by chip 1 - +5 V applied to HPA_D pin by chip	
LINE_CNT_FOR_VDP_INTR[5:0]			R/W
0x22	00010110	This control is used to delay a VDP interrupt to a particular line. 010110 - Default	
TX_HPD_OVERRIDE			R/W
0x2C	00000000	This control is used to allow the HDMI Tx to power on when HPD is low. 0 - Normal operation 1 - HPD override	
TX_INTRQ_RAW			R
0x3F	00000000	Status of the interrupt signal on INT1 interrupt pin. If an interrupt event that has been enabled for the INT1 pin has occurred this bit will be set to 1. Interrupts for INT1 are set via the interrupt 1 mask bits. This bit will remain set to 1 until all status for interrupts enabled on INT1 are cleared. 0 - No interrupt on HDMI TX 1 - Interrupt event for HDMI TX occurred	

Reg	Bits	Description	
INTRQ_RAW			R
0x3F	000000 <u>00</u>	This readback indicates the status of the interrupt signal on the INT1 interrupt pin. If an interrupt event enabled for the INT1 pin has occurred, this bit is set to 1. Interrupts for INT1 are set via the interrupt 1 mask bits. This bit will remain set to 1 until all status for interrupts enabled on INT1 are cleared. 0 - No interrupt on INT1 1 - Interrupt event for INT1 occurred	
INTRQ2_RAW			R
0x3F	000000 <u>00</u>	This readback indicates the status of the interrupt signal on the INT2 interrupt pin. If an interrupt event enabled for the INT2 pin has occurred, this bit is set to 1. Interrupts for INT2 are set via the interrupt 1 mask bits. This bit will remain set to 1 until all status for interrupts enabled on INT2 are cleared. 0 - No interrupt on INT2 1 - Interrupt event for INT2 occurred	
INTRQ_DUR_SEL[1:0]			R/W
0x40	<u>00</u> 000000	This control is used to select the interrupt signal duration for the interrupt signal on INT1. 00 - 4 Xtal periods 01 - 16 Xtal periods 10 - 64 Xtal periods 11 - Active until cleared	
STORE_UNMASKED_IRQS			R/W
0x40	000 <u>0</u> 0000	This control is used to allow the HDMI status flags for any HDMI interrupt to be triggered regardless of whether or not the mask bits are set. This bit allows an HDMI interrupt to trigger and allows this interrupt to be read back through the corresponding status bit without triggering an interrupt on the interrupt pin. The status is stored until the clear bit is used to clear the status register and allows another interrupt to occur. 0 - Do not allow x_ST flag of any HDMI interrupt to be set independently of mask bits 1 - Allow x_ST flag of any HDMI interrupt to be set independently of mask bits	
MPU_STIM_INTRQ			R/W
0x40	00000 <u>0</u> 00	This control is used to set a manual interrupt. This feature should be used for test purposes only. Note that the appropriate mask bit must be set to generate an interrupt at the pin. 0 - Disable manual interrupt mode 1 - Enable manual interrupt mode	
INTRQ_OP_SEL[1:0]			R/W
0x40	000000 <u>00</u>	This control is used to configure an interrupt signal for INT1. 00 - Open drain 01 - Drive low when active 10 - Drive high when active 11 - Disabled	
INTRQ2_DUR_SEL[1:0]			R/W
0x41	<u>00</u> 10000	This control is used to select the interrupt signal duration for the interrupt signal on INT2. 00 - 4 Xtal periods 01 - 16 Xtal periods 10 - 64 Xtal periods 11 - Active until cleared	
CP_LOCK_UNLOCK_EDGE_SEL			R/W
0x41	00 <u>1</u> 0000	This control is used to configure the functionality of the cp_lock and unlock interrupts. 0 - Generate interrupt for a low to high change in cp_lock and unlock status for channel 1 and channel 2 1 - Generate interrupt for a low to high or a high to low change in cp_lock and unlock status for channel 1 and channel 2	
STDI_DATA_VALID_EDGE_SEL			R/W
0x41	00 <u>1</u> 0000	This control is used to configure the functionality of the stdi_data_valid interrupt. The interrupt can be generated when STDI changes to an STDI valid state. Alternatively, it can be generated to indicate a change in stdi_valid status. 0 - Generate interrupt for a low to high change in stdi_valid status 1 - Generate interrupt for a low to high or a high to low change in stdi_valid status	
EN_UMASK_RAW_INTRQ2			R/W
0x41	00 <u>1</u> 0000	This control is used to apply the internal raw interrupts signal 2 on the INT2 interrupt pin. 0 - Do not output raw interrupt 2 on INT2 1 - Output audio raw interrupt 2 on INT2	

Reg	Bits	Description	
INT2_EN			R/W
0x41	00110000	This control is used to enable INT2. 0 - Disable INT2 1 - Enable INT2	
INTRQ2_OP_SEL[1:0]			R/W
0x41	00110000	This control is used to configure an interrupt signal for INT2. 00 - Open drain 01 - Drive low when active 10 - Drive high when active 11 - Disabled	
SSPD_RSLT_CHNGD_RAW			R
0x42	00000000	This readback indicates the status of the SSPD result changed interrupt signal. When set to 1, it indicates a change in the SSPD result of the currently selected sync channel. A change in SSPD result can be either due to a polarity or source change. The currently selected channel refers to sync channel currently applied to the CP core. Once set, this bit will remain high until it is cleared via SSPD_RSLT_CHNGD_CLR. 0 - No change in SSPD result. 1 - Change in SSPD result	
MV_PS_DET_RAW			R
0x42	00000000	This readback indicates the raw signal status of the Macrovision pseudo sync detected signal. 0 - No Macrovision pseudo syncs detected 1 - Macrovision pseudo sync detected	
STDI_DATA_VALID_RAW			R
0x42	00000000	This readback indicates the status of the STDI data. The stdi_data_valid interrupt can be either an edge sensitive or level sensitive interrupt, depending on the configuration of the stdi_data_valid_edge_sel register. When STDI_DATA_VALID_EDGE_SEL set to 1 it is a level sensitive interrupt and STDI_DATA_VALID_RAW is the raw signal status of the STDI Data Valid signal. When STDI_DATA_VALID_EDGE_SEL set to 0 it is an edge sensitive interrupt and STDI_DATA_VALID_RAW is a sampled -status of the STDI Data Valid signal following a change in the signal. Once set, this bit will remain high until it is cleared via STDI_DATA_VALID_CLR. 0 - STDI data not valid 1 - STDI data valid	
CP_UNLOCK_RAW			R
0x42	00000000	This readback indicates the status of the cp_unlock interrupt signal. When set to 1, it indicates a change in unlock status of the CP core. Once set, this bit remains high until it is cleared via cp_unlock_clr. 0 - CP locked 1 - CP unlocked	
CP_LOCK_RAW			R
0x42	00000000	This readback indicates the status of the cp_lock interrupt signal. When set to 1, it indicates a change in lock status of the CP core. Once set, this bit remains high until it is cleared via cp_lock_clr. 0 - CP unlocked 1 - CP locked	
AFE_INTERRUPT_RAW			R
0x42	00000000	This readback indicates the raw signal status of the Analog Front end interrupt signal. 0 - No AFE interrupt pending 1 - AFE interrupt present	
SSPD_RSLT_CHNGD_ST			R
0x43	00000000	This readback indicates the latched signal status of the SSPD result changed interrupt signal. Once set, this bit remains high until the interrupt is cleared via sspd_rslt_chngd_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No SSPD result changed interrupt event occurred 1 - SSPD result changed interrupt event occurred	
MV_PS_DET_ST			R
0x43	00000000	This readback indicates the latched signal status of the Macrovision pseudo sync detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via mv_ps_det_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 Interrupt mask bit. 0 - No Macrovision pseudo sync detection interrupt event occurred 1 - Macrovision pseudo sync detected interrupt event occurred	

Reg	Bits	Description	
STDI_DATA_VALID_ST			R
0x43	000 <u>0</u> 0000	This readback indicates the latched signal status of the STDI valid interrupt signal. Once set, this bit remains high until the interrupt is cleared via stdi_data_valid_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No STDI valid interrupt occurred 1 - STDI valid interrupt occurred	
CP_UNLOCK_ST			R
0x43	0000 <u>0</u> 000	This readback indicates the latched signal status of the CP unlock interrupt signal. Once set, this bit remains high until the interrupt is cleared via cp_unlock_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No CP unlock interrupt event occurred 1 - CP unlock interrupt event occurred	
CP_LOCK_ST			R
0x43	00000 <u>0</u> 00	This readback indicates the latched signal status of the CP lock interrupt signal. Once set, this bit remains high until the interrupt is cleared via cp_lock_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No CP LOCK interrupt event occurred 1 - CP LOCK interrupt event occurred	
AFE_INTERRUPT_ST			R
0x43	000000 <u>0</u> 0	This readback indicates the latched signal status of the AFE interrupt signal. Once set, this bit remains high until the interrupt is cleared via afe_interrupt_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No AFE interrupt event occurred 1 - AFE interrupt event occurred	
SSPD_RSLT_CHNGD_CLR			SC
0x44	<u>0</u> 0000000	This control is used to clear the SSPD result changed interrupt signal. This is a self clearing bit. 0 - Do not clear sspd_result_st 1 - Clear sspd_result_st	
MV_PS_DET_CLR			SC
0x44	<u>0</u> 0000000	This control is used to clear the Macrovision pseudo sync detected interrupt signal. This is a self clearing bit. 0 - Do not clear mv_ps_det_st 1 - Clear mv_ps_det_st	
STDI_DATA_VALID_CLR			SC
0x44	000 <u>0</u> 0000	This control is used to clear the STDI data valid interrupt signal. This is a self clearing bit. 0 - Do not clear stdi_dvalid_st 1 - Clear stdi_dvalid_st	
CP_UNLOCK_CLR			SC
0x44	0000 <u>0</u> 000	This control is used to clear the CP unlock interrupt signal. This is a self clearing bit. 0 - Do not clear cp_unlock_st 1 - Clear cp_unlock_st	
CP_LOCK_CLR			SC
0x44	00000 <u>0</u> 00	This control is used to clear the CP lock interrupt signal. This is a self clearing bit. 0 - Do not clear cp_unlock_st 1 - Clear cp_unlock_st	
AFE_INTERRUPT_CLR			SC
0x44	000000 <u>0</u> 0	This control is used to clear the Analog Front end interrupt signal. This is a self clearing bit. 0 - Do not clear afe_interrupt_st 1 - Clear afe_interrupt_st	
SSPD_RSLT_CHNGD_MB2			R/W
0x45	<u>0</u> 0000000	This control is used to set the INT2 interrupt mask for the SSPD result changed interrupt. When set, the SSPD result changed interrupt triggers the INT2 interrupt and sspd_rslt_chngd_st indicates the interrupt status. 0 - Disable SSPD changed interrupt for INT2 1 - Enable SSPD changed interrupt for INT2	
MV_PS_DET_MB2			R/W
0x45	<u>0</u> 0000000	This control is used to set the INT2 interrupt mask for the Macrovision pseudo sync detected interrupt. When set, the Macrovision pseudo sync detected interrupt triggers the INT2 interrupt and mv_ps_det_st indicates the interrupt status. 0 - Disable Macrovision pseudo sync detected interrupt for INT2 1 - Enable Macrovision pseudo sync detected interrupt for INT2	

Reg	Bits	Description	
STDI_DATA_VALID_MB2			R/W
0x45	00000000	This control is used to set the INT2 interrupt mask for the STDI the data valid interrupt. When set, the STDI data valid interrupt triggers the INT2 interrupt and stdi_data_valid_st indicates the interrupt status. 0 - Disable STDI data valid interrupt for INT2 1 - Enable STDI data valid interrupt for INT2	
CP_UNLOCK_MB2			R/W
0x45	00000000	This control is used to set the INT2 interrupt mask for the CP unlock interrupt. When set, the CP unlock interrupt triggers the INT2 interrupt and cp_unlock_st indicates the interrupt status. 0 - Disable CP unlock interrupt for INT2 1 - Enable CP unlock interrupt for INT2	
CP_LOCK_MB2			R/W
0x45	00000000	This control is used to set the INT2 interrupt mask for the CP lock interrupt. When set, the CP lock interrupt triggers the INT2 interrupt and cp_lock_st indicates the interrupt status. 0 - Disable CP lock interrupt for INT2 1 - Enable CP lock interrupt for INT2	
AFE_INTERRUPT_MB2			R/W
0x45	00000000	This control is used to set the INT2 interrupt mask for the Analog Front end interrupt. When set, the Analog Front end interrupt triggers the INT2 interrupt and afe_interrupt_st indicates the interrupt status. 0 - Disable Analog Front end interrupt for INT2 1 - Enable Analog Front end interrupt for INT2	
SSPD_RSLT_CHNGD_MB1			R/W
0x46	00000000	This control is used to set the INT1 interrupt mask for the SSPD result changed interrupt. When set, the SSPD result changed interrupt triggers the INT1 interrupt and sspd_rslt_chngd_st indicates the interrupt status. 0 - Disable SSPD changed interrupt for INT1 1 - Enable SSPD changed interrupt for INT1	
MV_PS_DET_MB1			R/W
0x46	00000000	This control is used to set the INT1 interrupt mask for the Macrovision pseudo sync detected interrupt. When set, the Macrovision pseudo sync detected interrupt triggers the INT1 interrupt and mv_ps_det_st indicates the interrupt status. 0 - Disable Macrovision pseudo sync detected interrupt for INT1 1 - Enable Macrovision pseudo sync detected interrupt for INT1	
STDI_DATA_VALID_MB1			R/W
0x46	00000000	This control is used to set the INT1 interrupt mask for the STDI data valid interrupt. When set, the STDI data valid interrupt triggers the INT1 interrupt and stdi_data_valid_st indicates the interrupt status. 0 - Disable STDI data valid interrupt for INT1 1 - Enable STDI data valid interrupt for INT1	
CP_UNLOCK_MB1			R/W
0x46	00000000	This control is used to set the INT1 interrupt mask for the CP unlock interrupt. When set, the CP unlock interrupt triggers the INT1 interrupt and cp_unlock_st indicates the interrupt status. 0 - Disable CP unlock interrupt for INT1 1 - Enable CP unlock interrupt for INT1	
CP_LOCK_MB1			R/W
0x46	00000000	This control is used to set the INT1 interrupt mask for the CP lock interrupt. When set, the CP lock interrupt triggers the INT1 interrupt and cp_lock_st indicates the interrupt status. 0 - Disable CP lock interrupt for INT1 1 - Enable CP lock interrupt for INT1	
AFE_INTERRUPT_MB1			R/W
0x46	00000000	This control is used to set the INT1 interrupt mask for Analog Front End interrupt. When set, the Analog Front end interrupt triggers the INT1 interrupt and afe_interrupt_st indicates the interrupt status. 0 - Disable Analog Front End interrupt for INT1 1 - Enable Analog Front end interrupt for INT1	
MPU_STIM_INTRQ_RAW			R
0x47	00000000	This readback indicates the raw status of the manual forced interrupt signal. 0 - Manual forced interrupt not applied 1 - Manual forced interrupt applied	

Reg	Bits	Description	
MV_AGC_DET_RAW			R
0x47	00000000	This readback indicates the raw status of the Macrovision AGC detection signal. 0 - Macrovision AGC not detected 1 - Macrovision AGC detected	
MV_CS_DET_RAW			R
0x47	00000000	This readback indicates the raw status of the Macrovision color stripe detection signal. 0 - Macrovision color stripe not detected 1 - Macrovision color stripe detected	
CP_CGMS_CHNGD_RAW			R
0x47	00000000	This readback indicates the status of the CP CGMS data changed interrupt signal. When set to 1, it indicates a change in CGMS data or a change in CGMS data availability. Once set, this bit remains high until the interrupt is cleared via cp_cgms_chngd_clr. 0 - No change in CGMS data or CGMS availability occurred 1 - Change in CGMS data or CGMS availability occurred	
MPU_STIM_INTRQ_ST			R
0x48	00000000	This readback indicates the latched signal status of the forced manual interrupt signal. Once set, this bit remains high until the interrupt is cleared via mpu_stim_intrq_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - Forced manual interrupt event not occurred 1 - Forced manual interrupt event occurred	
MV_AGC_DET_ST			R
0x48	00000000	This readback indicates the latched signal status of the Macrovision AGC detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via mv_agc_det_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - Macrovision AGC detected interrupt event not occurred 1 - Macrovision AGC detected interrupt event occurred	
MV_CS_DET_ST			R
0x48	00000000	This readback indicates the latched signal status of the Macrovision color stripe detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via mv_cs_det_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 mask bit. 0 - Macrovision color stripe detected interrupt event not occurred 1 - Macrovision color stripe detected interrupt event occurred	
CP_CGMS_CHNGD_ST			R
0x48	00000000	This readback indicates the latched signal status of the CP CGMS changed interrupt signal. Once set, this bit remains high until the interrupt is cleared via cp_cgms_chngd_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - CGMS data changed, interrupt event occurred 1 - CGMS data changed, interrupt event occurred	
MPU_STIM_INTRQ_CLR			SC
0x49	00000000	This control is used to clear the manual forced interrupt signal. This is a self clearing bit. 0 - Do not clear mpu_stim_int_st 1 - Clear mpu_stim_int_st	
MV_AGC_DET_CLR			SC
0x49	00000000	This control is used to clear the Macrovision AGC detected interrupt signal. This is a self clearing bit. 0 - Do not clear mv_agc_det_st 1 - Clear mv_agc_det_st	
MV_CS_DET_CLR			SC
0x49	00000000	This control is used to clear the Macrovision color stripe detected interrupt signal. This is a self clearing bit. 0 - Do not clear mv_cs_det_st 1 - Clear mv_cs_det_st	
CP_CGMS_CHNGD_CLR			SC
0x49	00000000	This control is used to clear the CP CGMS changed interrupt signal. This is a self clearing bit. 0 - Do not clear cp_cgms_chngd 1 - Clear cp_cgms_chngd	

Reg	Bits	Description	
MPU_STIM_INTRQ_MB2			R/W
0x4A	00000000	This control is used to set the INT2 interrupt mask for the manual forced interrupt signal. When set, the manual forced interrupt triggers the INT2 interrupt and mpu_stim_intrq_st indicates the interrupt status. 0 - Disable manual forced interrupt for INT2 1 - Enable manual forced interrupt for INT2	
MV_AGC_DET_MB2			R/W
0x4A	00000000	This control is used to set the INT2 interrupt mask for the Macrovision AGC detected interrupt signal. When set, the Macrovision AGC detected interrupt triggers the INT2 interrupt and mv_agc_det_st indicates the interrupt status. 0 - Disable Macrovision AGC detected interrupt for INT2 1 - Enable Macrovision AGC detected interrupt for INT2	
MV_CS_DET_MB2			R/W
0x4A	00000000	This control is used to set the INT2 interrupt mask for the Macrovision color stripe detected interrupt signal. When set, the Macrovision color stripe detected interrupt triggers the INT2 interrupt and mv_cs_det_st indicates the interrupt status. 0 - Disable Macrovision color stripe detected interrupt for INT2 1 - Enable Macrovision color stripe detected interrupt for INT2	
CP_CGMS_CHNGD_MB2			R/W
0x4A	00000000	This control is used to set the INT2 interrupt mask for the CP CGMS changed interrupt signal. When set, the CP CGMS changed interrupt triggers the INT2 interrupt and cp_cgms_chngd_st indicates the interrupt status. 0 - Disable CP CGMS changed interrupt for INT2 1 - Enable CP CGMS changed interrupt for INT2	
MPU_STIM_INTRQ_MB1			R/W
0x4B	00000000	This control is used to set the INT1 interrupt mask for the manual forced interrupt signal. When set, the manual forced interrupt triggers the INT1 interrupt and mpu_stim_intrq_st indicates the interrupt status. 0 - Disable manual forced interrupt for INT1 1 - Enable manual forced interrupt for INT1	
MV_AGC_DET_MB1			R/W
0x4B	00000000	This control is used to set the INT1 interrupt mask for the Macrovision AGC detected interrupt signal. When set, the Macrovision AGC detected interrupt triggers the INT1 interrupt and mv_agc_det_st indicates the interrupt status. 0 - Disable Macrovision AGC detected interrupt for INT1 1 - Enable Macrovision AGC detected interrupt for INT1	
MV_CS_DET_MB1			R/W
0x4B	00000000	This control is used to set the INT1 interrupt mask for the Macrovision color stripe detected interrupt signal. When set, the Macrovision color stripe detected interrupt triggers the INT1 interrupt and mv_cs_det_st indicates the interrupt status. 0 - Disable Macrovision color stripe detected interrupt for INT1 1 - Enable Macrovision color stripe detected interrupt for INT1	
CP_CGMS_CHNGD_MB1			R/W
0x4B	00000000	This control is used to set the INT1 interrupt mask for the CP CGMS changed interrupt signal. When set, the CP CGMS changed interrupt triggers the INT1 interrupt and cp_cgms_chngd_st indicates the interrupt status. 0 - Disable CP CGMS changed interrupt for INT1 1 - Enable CP CGMS changed interrupt for INT1	
TTXT_AVL_RAW			R
0x51	00000000	This readback indicates the raw status of the Teletext data available signal. 0 - Teletext not detected/available 1 - Teletext detected/available	
VITC_AVL_RAW			R
0x51	00000000	This readback indicates the raw status of the VITC data available signal. 0 - VITC data not detected/available 1 - VITC data detected/available	
GS_DATA_TYPE_RAW			R
0x51	00000000	This readback indicates the raw status of the Gemstar type available signal. 0 - Gemstar data type not detected/available 1 - Gemstar data type detected/available	
GS_PDC_VPS_UTC_AVL_RAW			R
0x51	00000000	This readback indicates the raw status of the Gemstar/PDC/VPS/UTC data available signal. 0 - Gemstar/PDC/VPS/UTC data not detected/available 1 - Gemstar/PDC/VPS/UTC data detected/available	

Reg	Bits	Description	
CGMS_WSS_AVL_RAW			R
0x51	00000 <u>0</u> 00	This readback indicates the raw status of the CGMS/WSS data available signal. 0 - CGMS/WSS data not detected/available 1 - CGMS/WSS data detected/available	
CCAP_EVEN_FIELD_RAW			R
0x51	00000 <u>0</u> 0	This readback indicates the raw status of the closed captioning detected on even field signal. 0 - CCAP even field data not detected/available 1 - CCAP even field data detected/available	
CCAP_AVL_RAW			R
0x51	000000 <u>0</u>	This readback indicates the raw status of the closed captioning data available signal. 0 - Closed captioning data not available 1 - Closed captioning data available	
TTXT_AVL_ST			R
0x52	<u>0</u> 0000000	This readback indicates the latched status of the Teletext data available interrupt signal. Once set, this bit remains high until the interrupt is cleared via ttxt_avl_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No Teletext data available, no interrupt 1 - Teletext data available, interrupt event occurred	
VITC_AVL_ST			R
0x52	<u>0</u> 0000000	This readback indicates the latched status of the VITC data available interrupt signal. Once set, this bit remains high until the interrupt is cleared via vitc_avl_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No VITC data available interrupt event occurred 1 - VITC data available interrupt event occurred	
GS_DATA_TYPE_ST			R
0x52	<u>0</u> 0000000	This readback indicates the latched status of the Gemstar type available interrupt signal. Once set, this bit remains high until the interrupt is cleared via gs_data_type_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt bit. 0 - No Gemstar data type interrupt event occurred 1 - Gemstar data type interrupt event occurred	
GS_PDC_VPS_UTC_AVL_ST			R
0x52	<u>0</u> 0000000	This readback indicates the latched status of the Gemstar/PDC/VPS/UTC data available interrupt signal. Once set, this bit remains high until the interrupt is cleared via gs_pdc_vps_utc_avl_clr. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit. 0 - No Gemstar/PDC/VPS/UTC data available interrupt event occurred 1 - Gemstar/PDC/VPS/UTC data available interrupt event occurred	
CGMS_WSS_AVL_ST			R
0x52	00000 <u>0</u> 00	This readback indicates the latched status of the CGMS/WSS data available interrupt signal. Once set, this bit remains high until the interrupt is cleared via cgms_wss_avl_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt bit. 0 - No CGMS/WSS data available interrupt event occurred 1 - CGMS/WSS data available interrupt event occurred	
CCAP_EVEN_FIELD_ST			R
0x52	00000 <u>0</u> 0	This readback indicates the latched status of the closed captioning detected on even field interrupt signal. Once set, this bit remains high until the interrupt is cleared via ccap_even_field_clr. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit. 0 - No closed captioning detected on even field interrupt event occurred 1 - Closed captioning detected on even field interrupt event occurred	
CCAP_AVL_ST			R
0x52	000000 <u>0</u>	This readback indicates the latched status of the closed captioning data available interrupt signal. Once set, this bit remains high until the interrupt is cleared via ccap_avl_clr. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit. 0 - No closed captioning data available interrupt event occurred 1 - Closed captioning data available interrupt event occurred	
TTXT_AVL_CLR			SC
0x53	<u>0</u> 0000000	This control is used to clear the Teletext data available interrupt signal. This is a self clearing bit. 0 - Do not clear ttx_avl_st 1 - Clear ttx_avl_st	

Reg	Bits	Description	
VITC_AVL_CLR			SC
0x53	00000000	This control is used to clear the VITC data available interrupt signal. This is a self clearing bit. 0 - Do not clear vitc_avl_st 1 - Clear vitc_avl_st	
GS_DATA_TYPE_CLR			SC
0x53	00000000	This control is used to clear the Gemstar data type interrupt signal. This is a self clearing bit. 0 - Do not clear gs_data_type_st 1 - Clear gs_data_type_st	
GS_PDC_VPS_UTC_AVL_CLR			SC
0x53	00000000	This control is used to clear the Gemstar/PDC/VPS/UTC data available interrupt signal. This is a self clearing bit. 0 - Do not clear gs_vps_pdc_utc_avl_st 1 - Clear gs_vps_pdc_utc_avl_st	
CGMS_WSS_AVL_CLR			SC
0x53	00000000	This control is used to clear the CGMS/WSS data available interrupt signal. This is a self clearing bit. 0 - Do not clear cgms_wss_avl_st 1 - Clear cgms_wss_avl_st	
CCAP_EVEN_FIELD_CLR			SC
0x53	00000000	This control is used to clear the closed captioning detected on interrupt signal. This is a self clearing bit. 0 - Do not clear ccap_even_field_st 1 - Clear ccap_even_field_st	
CCAP_AVL_CLR			SC
0x53	00000000	This control is used to clear the closed captioning data available interrupt signal. This is a self clearing bit. 0 - Do not clear ccap_avl_st 1 - Clear ccap_avl_st	
TTXT_AVL_MB2			R/W
0x54	00000000	This control is used to set the INT2 interrupt mask for the Teletext data available interrupt signal. When set, the Teletext data available interrupt triggers the INT2 interrupt and ttxt_avl_st indicates the interrupt status. 0 - Disable Teletext data available interrupt on INT2 1 - Enable Teletext data available interrupt on INT2	
VITC_AVL_MB2			R/W
0x54	00000000	This control is used to set the INT2 interrupt mask for the VITC data available interrupt signal. When set, the VITC data available interrupt triggers the INT2 interrupt and vitc_avl_st indicates the interrupt status. 0 - Disable VITC data available interrupt on INT2 1 - Enable VITC data available interrupt on INT2	
GS_DATA_TYPE_MB2			R/W
0x54	00000000	This control is used to set the INT2 interrupt mask for the Gemstar data type interrupt signal. When set, the Gemstar data type available interrupt triggers the INT2 interrupt and gs_type_st indicates the interrupt status. 0 - Disable Gemstar data type interrupt on INT2 1 - Enable Gemstar data type available interrupt on INT2	
GS_PDC_VPS_UTC_AVL_MB2			R/W
0x54	00000000	This control is used to set the INT2 interrupt mask for the Gemstar/PDC/VPS/UTC data available interrupt signal. When set, the Gemstar/PDC/VPS/UTC data available interrupt triggers the INT2 interrupt and gs_pdc_vps_utc_avl_st indicates the interrupt status. 0 - Disable Gemstar/PDC/VPS/UTC data available interrupt on INT2 1 - Enable Gemstar/PDC/VPS/UTC data available interrupt on INT2	
CGMS_WSS_AVL_MB2			R/W
0x54	00000000	This control is used to set the INT2 interrupt mask for the CGMS/WSS data available interrupt signal. When set, the CGMS/WSS data available interrupt triggers the INT2 interrupt and gs_type_st indicates the interrupt status. 0 - Disable CGMS/WSS data available interrupt on INT2 1 - Enable CGMS/WSS data available interrupt on INT2	
CCAP_EVEN_FIELD_MB2			R/W
0x54	00000000	This control is used to set the INT2 interrupt mask for the CCAP even field detected interrupt signal. When set, the CCAP even field detected interrupt triggers the INT2 interrupt and ccap_even_field_st indicates the interrupt status. 0 - Disable closed caption on even field detected interrupt on INT2 1 - Enable closed caption on even field detected interrupt on INT2	

Reg	Bits	Description	
CCAP_AVL_MB2			R/W
0x54	0000000 <u>0</u>	This control is used to set the INT2 interrupt mask for the CCAP data available interrupt signal. When set, the CCAP data available interrupt triggers the INT2 interrupt and ccap_avl_st indicates the interrupt status. 0 - Disable closed caption data available interrupt on INT2 1 - Enable closed caption data available interrupt on INT2	
TTXT_AVL_MB1			R/W
0x55	<u>0</u> 0000000	This control is used to set the INT1 interrupt mask for the Teletext data available interrupt signal. When set, the Teletext data available interrupt triggers the INT1 interrupt and ttxt_avl_st indicates the interrupt status. 0 - Disable Teletext data available interrupt on INT1 1 - Enable Teletext data available interrupt on INT1	
VITC_AVL_MB1			R/W
0x55	<u>0</u> 0000000	This control is used to set the INT2 interrupt mask for the VITC data available interrupt signal. When set, the VITC data available interrupt triggers the INT2 interrupt and vitc_avl_st indicates the interrupt status. 0 - Disable VITC data available interrupt on INT1 1 - Enable VITC data available interrupt on INT1	
GS_DATA_TYPE_MB1			R/W
0x55	<u>0</u> 0000000	This control is used to set the INT1 interrupt mask for Gemstar data type interrupt signal. When set, the Gemstar data type available interrupt triggers the INT1 interrupt and gs_type_st indicates the interrupt status. 0 - Disable Gemstar data type interrupt on INT1 1 - Enable Gemstar data type available interrupt on INT1	
GS_PDC_VPS_UTC_AVL_MB1			R/W
0x55	000 <u>0</u> 00000	This control is used to set the INT1 interrupt mask for the Gemstar/PDC/VPS/UTC data available interrupt signal. When set, the Gemstar/PDC/VPS/UTC data available interrupt triggers the INT1 interrupt and gs_pdc_vps_utc_avl_st indicates the interrupt status. 0 - Disable Gemstar/PDC/VPS/UTC data available interrupt on INT1 1 - Enable Gemstar/PDC/VPS/UTC data available interrupt on INT1	
CGMS_WSS_AVL_MB1			R/W
0x55	00000 <u>0</u> 00	This control is used to set the INT1 interrupt mask for the CGMS/WSS data available interrupt signal. When set, the CGMS/WSS data available interrupt triggers the INT1 interrupt and gs_type_st indicates the interrupt status. 0 - Disable CGMS/WSS data available interrupt on INT1 1 - Enable CGMS/WSS data available interrupt on INT1	
CCAP_EVEN_FIELD_MB1			R/W
0x55	00000 <u>0</u> 0	This control is used to set the INT1 interrupt mask for the CCAP even field detected interrupt signal. When set, the CCAP even field detected interrupt triggers the INT1 interrupt and ccap_even_field_st indicates the interrupt status. 0 - Disable closed caption on even field detected interrupt on INT1 1 - Enable closed caption on even field detected interrupt on INT1	
CCAP_AVL_MB1			R/W
0x55	000000 <u>0</u>	This control is used to set the INT1 interrupt mask for the CCAP data available interrupt signal. When set, the CCAP data available interrupt triggers the INT1 interrupt and ccap_avl_st indicates the interrupt status. 0 - Disable closed caption data available interrupt on INT1 1 - Enable closed caption data available interrupt on INT1	
CP_LOCK_CH2_RAW			R
0x5B	<u>0</u> 0000000	This readback indicates that STDI channel 2 has changed from an unlocked state to a locked state. 0 - No change 1 - Channel 2 CP input has changed from unlocked to locked state	
CP_UNLOCK_CH2_RAW			R
0x5B	<u>0</u> 0000000	This readback indicates that STDI channel 2 has changed from a locked state to an unlocked state. 0 - No change 1 - Channel 2 CP input has changed from locked to unlocked state	
STDI_DVALID_CH2_RAW			R
0x5B	<u>0</u> 0000000	This readback indicates the raw status of the STDI data valid for sync channel 2 signal. 0 - STDI data not valid on sync channel 2 1 - STDI data valid on sync channel 2	

Reg	Bits	Description	
SSPD_RSLT_CHNGD_CH2_RAW			R
0x5B	00000000	This readback indicates the status of the SSPD result changed on sync channel 2 interrupt signal. When set to 1, it indicates a change in SSPD result of the currently selected sync channel. A change in SSPD result can be either due to a polarity or source change. Once set, this bit will remain high until it is cleared via SSPD_RSLT_CHNGD_CH1_CLR. 0 - No change in SSPD result for sync channel 2 1 - Change occurred in SSPD result for sync channel 2	
CP_LOCK_CH1_RAW			R
0x5B	00000000	This readback indicates that STDI channel 1 has changed from a unlocked state to an locked state 0 - No change 1 - Channel 1 input changed from unlocked to locked state	
CP_UNLOCK_CH1_RAW			R
0x5B	00000000	This readback indicates that STDI channel 1 has changed from a locked state to an unlocked state 0 - No change 1 - Channel 1 CP input changed from locked to unlocked state	
STDI_DVALID_CH1_RAW			R
0x5B	00000000	This readback indicates the raw status of the STDI data valid for sync channel 1 signal. 0 - STDI data not valid for sync channel 1 1 - STDI data valid for sync channel 1	
SSPD_RSLT_CHNGD_CH1_RAW			R
0x5B	00000000	Status of the SSPD Result Changed on sync channel 1 interrupt signal. When set to 1 it indicates a change in SSPD result of the currently selected sync channel. A change in SSPD result can be either due to a polarity or source change. Once set, this bit will remain high until it is cleared via SSPD_RSLT_CHNGD_CH1_CLR. 0 - No change in SSPD result for sync channel 1 1 - Change occurred in SSPD result for sync channel 1	
CP_LOCK_CH2_ST			R
0x5C	00000000	This readback indicates that STDI channel 2 has changed from an unlocked state to a locked state. 0 - No change, no interrupt generated 1 - Channel 2 CP input caused the decoder to go from unlocked to locked state	
CP_UNLOCK_CH2_ST			R
0x5C	00000000	This readback indicates that STDI channel 2 has changed from a locked state to an unlocked state. 0 - No change, no interrupt generated 1 - CP input caused the decoder to go from locked to unlocked state	
STDI_DVALID_CH2_ST			R
0x5C	00000000	This readback indicates the latched signal status of the STDI valid for sync channel 2 interrupt signal. Once set, this bit remains high until the interrupt is cleared via stdi_data_valid_ch2_clr. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit. 0 - No STDI valid for sync channel 2 interrupt occurred 1 - STDI valid for sync channel 2 interrupt occurred	
SSPD_RSLT_CHNGD_CH2_ST			R
0x5C	00000000	This readback indicates the latched signal status of the SSPD result changed for sync channel 2 interrupt signal. Once set, this bit remains high until the interrupt is cleared via sspd_rslt_chngd_ch2_clr. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit. 0 - No SSPD result changed for sync channel 2 interrupt event occurred 1 - SSPD result changed for sync channel 2 interrupt event occurred	
CP_LOCK_CH1_ST			R
0x5C	00000000	This readback indicates that STDI channel 1 has changed from an unlocked state to a locked state. 0 - No change. No interrupt generated . 1 - Channel 1 CP input caused decoder to go from unlocked to locked state.	
CP_UNLOCK_CH1_ST			R
0x5C	00000000	This readback indicates that STDI channel 1 has changed from a locked state to an unlocked state. 0 - No change. No interrupt generated . 1 - Channel 1 CP input changed from locked to unlocked state and triggered an interrupt	

Reg	Bits	Description	
STDI_DVALID_CH1_ST			R
0x5C	000000 <u>00</u>	This readback indicates the latched signal status of the STDI valid for sync channel 1 interrupt signal. Once set, this bit remains high until the interrupt is cleared via stdi_data_valid_ch1_clr. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit. 0 - No STDI valid for sync channel 1 interrupt occurred 1 - STDI valid for sync channel 1 interrupt occurred	
SSPD_RSLT_CHNGD_CH1_ST			R
0x5C	000000 <u>00</u>	This readback indicates the latched signal status of the SSPD result changed for sync channel 1 interrupt signal. Once set, this bit remains high until the interrupt is cleared via sspd_rslt_chngd_ch1_clr. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit. 0 - No SSPD result changed for sync channel 1 interrupt event occurred 1 - SSPD result changed for sync channel 1 interrupt event occurred	
CP_LOCK_CH2_CLR			SC
0x5D	<u>00000000</u>	This control is used to clear the CP lock status bit on STDI channel 2. This is a self clearing bit. 0 - Do not clear cp_lock_ch2_st 1 - Clear cp_lock_ch2_st	
CP_UNLOCK_CH2_CLR			SC
0x5D	<u>00000000</u>	This control is used to clear the CP unlock status bit on STDI channel 2. This is a self clearing bit. 0 - Do not clear cp_unlock_ch2_st 1 - Clear cp_unlock_ch2_st	
STDI_DVALID_CH2_CLR			SC
0x5D	<u>00000000</u>	This control is used to clear the STDI data valid on sync channel 2 interrupt signal. This is a self clearing bit. 0 - Do not clear stdi_data_valid_ch2_st 1 - Clear stdi_data_valid_ch2_st	
SSPD_RSLT_CHNGD_CH2_CLR			SC
0x5D	<u>00000000</u>	This control is used to clear the SSPD result changed on sync channel 2 interrupt signal. This is a self clearing bit. 0 - Do not clear sspd_rslt_chngd_ch2_st 1 - Clear sspd_rslt_chngd_ch2_st	
CP_LOCK_CH1_CLR			SC
0x5D	<u>00000000</u>	This control is used to clear the CP lock status bit on STDI channel 1. This is a self clearing bit. 0 - Do not clear cp_lock_ch1_st 1 - Clear cp_lock_ch1_st	
CP_UNLOCK_CH1_CLR			SC
0x5D	<u>00000000</u>	This control is used to clear the CP unlock status bit on STDI channel 1. This is a self clearing bit. 0 - Do not clear cp_unlock_ch1_st 1 - Clear cp_unlock_ch1_st	
STDI_DVALID_CH1_CLR			SC
0x5D	<u>00000000</u>	This control is used to clear the STDI data valid on sync channel 1 interrupt signal. This is a self clearing bit. 0 - Do not clear stdi_data_valid_ch1_st 1 - Clear stdi_data_valid_ch1_st	
SSPD_RSLT_CHNGD_CH1_CLR			SC
0x5D	<u>00000000</u>	This control is used to clear the SSPD result changed on sync channel 1 interrupt signal. This is a self clearing bit. 0 - Do not clear sspd_rslt_chngd_ch1_st 1 - Clear sspd_rslt_chngd_ch1_st	
CP_LOCK_CH2_MB2			R/W
0x5E	<u>00000000</u>	This control is used to set the CP lock channel 2 interrupt mask on the interrupt 2 pin. 0 - Masks cp_lock_ch2_st 1 - Unmasks cp_lock_ch2_st	
CP_UNLOCK_CH2_MB2			R/W
0x5E	<u>00000000</u>	This control is used to set the CP unlock channel 2 interrupt mask on the interrupt 2 pin. 0 - Masks cp_unlock_ch2_st 1 - Unmasks cp_unlock_ch2_st	

Reg	Bits	Description	
STDI_DVALID_CH2_MB2			R/W
0x5E	00000000	This control is used to set the INT2 interrupt mask for the STDI data valid for sync channel 2 interrupt. When set, the STDI data valid for sync channel 2 interrupt triggers the INT2 interrupt and <code>stdi_data_valid_ch2_st</code> indicates the interrupt status. 0 - Disable STDI data valid for sync channel 2 interrupt for INT2 1 - Enable STDI data valid for sync channel 2 interrupt for INT2	
SSPD_RSLT_CHNGD_CH2_MB2			R/W
0x5E	00000000	This control is used to set the INT2 interrupt mask for the SSPD result changed on sync channel 2 interrupt. When set, the SSPD result changed for sync channel 2 interrupt triggers the INT2 interrupt and <code>sspd_rslt_chngd_ch2_st</code> indicates the interrupt status. 0 - Disable SSPD changed for sync channel 2 interrupt for INT2 1 - Enable SSPD changed for sync channel 2 interrupt for INT2	
CP_LOCK_CH1_MB2			R/W
0x5E	00000000	This control is used to set the CP lock channel 1 interrupt mask on the interrupt 2 pin. 0 - Masks <code>cp_lock_ch1_st</code> 1 - Unmasks <code>cp_lock_ch1_st</code>	
CP_UNLOCK_CH1_MB2			R/W
0x5E	00000000	This control is used to set the CP unlock channel 1 interrupt mask on the interrupt 2 pin. 0 - Masks <code>cp_unlock_ch1_st</code> 1 - Unmasks <code>cp_unlock_ch1_st</code>	
STDI_DVALID_CH1_MB2			R/W
0x5E	00000000	This control is used to set the INT2 interrupt mask for STDI Data valid for sync channel 1 interrupt. When set, the STDI Data valid for sync channel 1 interrupt triggers the INT2 interrupt and <code>stdi_data_valid_ch1_st</code> indicates the interrupt status. 0 - Disable STDI data valid for sync channel 1 interrupt for INT2 1 - Enable STDI data valid for sync channel 1 interrupt for INT2	
SSPD_RSLT_CHNGD_CH1_MB2			R/W
0x5E	00000000	This control is used to set the INT2 interrupt mask for SSPD Result Changed on sync channel 1 interrupt. When set, the SSPD Result changed for sync channel 2 interrupt triggers the INT2 interrupt and <code>sspd_rslt_chngd_ch1_st</code> indicates the interrupt status. 0 - Disable SSPD changed for sync channel 1 interrupt for INT2 1 - Enable SSPD changed for sync channel 1 interrupt for INT2	
CP_LOCK_CH2_MB1			R/W
0x5F	00000000	This control is used to set the CP lock channel 2 interrupt mask on the interrupt 1 pin. 0 - Masks <code>cp_lock_ch2_st</code> 1 - Unmasks <code>cp_lock_ch2_st</code>	
CP_UNLOCK_CH2_MB1			R/W
0x5F	00000000	This control is used to set the CP unlock channel 2 interrupt mask on the interrupt 1 pin. 0 - Masks <code>cp_unlock_ch2_st</code> 1 - Unmasks <code>cp_unlock_ch2_st</code>	
STDI_DVALID_CH2_MB1			R/W
0x5F	00000000	This control is used to set the INT1 interrupt mask for the STDI data valid for sync channel 2 interrupt. When set, the STDI data valid for sync channel 2 interrupt triggers the INT1 interrupt and <code>stdi_data_valid_ch2_st</code> indicates the interrupt status. 0 - Disable STDI data valid for sync channel 2 interrupt for INT1 1 - Enable STDI data valid for sync channel 2 interrupt for INT1	
SSPD_RSLT_CHNGD_CH2_MB1			R/W
0x5F	00000000	This control is used to set the INT1 interrupt mask for the SSPD result changed on sync channel 2 interrupt. When set, the SSPD result changed for sync channel 2 interrupt triggers the INT1 interrupt and <code>sspd_rslt_chngd_ch2_st</code> indicates the interrupt status. 0 - Disable SSPD changed for sync channel 2 interrupt for INT1 1 - Enable SSPD changed for sync channel 2 interrupt for INT1	
CP_LOCK_CH1_MB1			R/W
0x5F	00000000	This control is used to set the CP lock channel 1 interrupt mask on the interrupt 1 pin. 0 - Masks <code>cp_lock_ch1_st</code> 1 - Unmasks <code>cp_lock_ch1_st</code>	

Reg	Bits	Description	
CP_UNLOCK_CH1_MB1			R/W
0x5F	00000 <u>0</u> 0	This control is used to set the CP unlock channel 1 interrupt mask on the interrupt 1 pin. 0 - Masks cp_unlock_ch1_st 1 - Unmasks cp_unlock_ch1_st	
STDI_DVALID_CH1_MB1			R/W
0x5F	00000 <u>0</u> 0	This control is used to set the INT1 interrupt mask for the STDI data valid for sync channel 1 interrupt. When set, the STDI data valid for sync channel 1 interrupt triggers the INT1 interrupt and stdi_data_valid_ch1_st indicates the interrupt status. 0 - Disable STDI data valid for sync channel 1 interrupt for INT1 1 - Enable STDI data valid for sync channel 1 interrupt for INT1	
SSPD_RSLT_CHNGD_CH1_MB1			R/W
0x5F	00000 <u>0</u> 0	This control is used to set the INT1 interrupt mask for the SSPD result changed on sync channel 1 interrupt. When set, the SSPD result changed for sync channel 2 interrupt triggers the INT1 interrupt and sspd_rslt_chngd_ch1_st indicates the interrupt status. 0 - Disable SSPD changed for sync channel 1 interrupt for INT1 1 - Enable SSPD changed for sync channel 1 interrupt for INT1	
ISRC2_PCKT_RAW			R
0x60	<u>0</u> 0000000	This readback indicates the raw status signal of the International Standard Recording Code 2 (ISRC2) Packet detection signal. This bit resets to 0 after an HDMI packet detection reset or upon writing to isrc2_packet_id. 0 - No ISRC2 packets received since last HDMI packet detection reset 1 - ISRC2 packets received	
ISRC1_PCKT_RAW			R
0x60	<u>0</u> 0000000	This readback indicates the raw status signal of the International Standard Recording Code 1 (ISRC1) packet detection signal. This bit resets to 0 after an HDMI packet detection reset or upon writing to isrc1_packet_id. 0 - No ISRC1 packets received since last HDMI packet detection reset. 1 - ISRC1 packets received.	
ACP_PCKT_RAW			R
0x60	<u>0</u> 0000000	This readback indicates the raw status signal of the audio content protection packet detection signal. This bit resets to 0 after an HDMI packet detection reset or upon writing to acp_packet_id. 0 - No ACP packet received within last 600 ms or since last HDMI packet detection reset 1 - ACP packets received within last 600 ms	
VS_INFO_RAW			R
0x60	<u>0</u> 0000000	This readback indicates the raw status signal of the vendor specific InfoFrame detection signal. This bit resets to 0 after HDMI packet detection reset or upon writing to vs_packet_id. 0 - No new vendor specific InfoFrame received since last HDMI packet detection reset 1 - New vendor specific InfoFrame received	
MS_INFO_RAW			R
0x60	<u>0</u> 0000000	This readback indicates the raw status signal of the MPEG source InfoFrame detection signal. This bit resets to 0 after an HDMI packet detection reset or upon writing to ms_packet_id. 0 - No MPEG InfoFrame received within last three VSynCs or since last HDMI packet detection reset 1 - MPEG source InfoFrame received	
SPD_INFO_RAW			R
0x60	<u>0</u> 0000000	This readback indicates the raw status of the SPD InfoFrame detected signal. This bit resets to 0 after an HDMI packet detection reset or upon writing to spd_packet_id. 0 - No source product description InfoFrame received since the last HDMI packet detection reset 1 - Source product description InfoFrame received	
AUDIO_INFO_RAW			R
0x60	<u>0</u> 0000000	This readback indicates the raw status of the audio InfoFrame detected signal. This bit resets to 0 on the fourth VSync leading edge following an audio InfoFrame, after an HDMI packet detection reset or upon writing to aud_packet_id. 0 - No AVI InfoFrame received within last three VSynCs or since last HDMI packet detection reset 1 - Audio InfoFrame received within last three VSync	
AVI_INFO_RAW			R
0x60	<u>0</u> 0000000	This readback indicates the raw status of the AVI InfoFrame detected signal. This bit is set to one when an AVI InfoFrame is received and is reset to 0 if no AVI InfoFrame is received for more than seven VSynCs (on the eighth VSync leading edge following the last received AVI InfoFrame), after an HDMI packet detection reset or upon writing to AVI_PACKET_ID. 0 - No AVI InfoFrame received within last seven VSynCs or since last HDMI packet detection reset 1 - AVI InfoFrame received within last seven VSynCs	

Reg	Bits	Description	
ISRC2_PCKT_ST			R
0x61	00000000	This readback indicates the latched status of the ISRC2 packet detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via isrc2_info_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No interrupt generated 1 - isrc2_pckt_raw changed, interrupt generated	
ISRC1_PCKT_ST			R
0x61	00000000	This readback indicates the latched status of ISRC1 packet detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via isrc1_info_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No interrupt generated 1 - isrc1_packet_raw changed, interrupt generated	
ACP_PCKT_ST			R
0x61	00000000	This readback indicates the latched status of the audio content protection packet detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via acp_info_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 mask bit. 0 - No interrupt generated 1 - acp_pckt_raw changed, interrupt generated	
VS_INFO_ST			R
0x61	00000000	This readback indicates the latched status of the vendor specific InfoFrame detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via vs_info_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No interrupt generated 1 - vs_info_raw changed, interrupt generated	
MS_INFO_ST			R
0x61	00000000	This readback indicates the latched status of the MPEG source InfoFrame detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via ms_info_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No interrupt generated 1 - ms_info_raw changed, interrupt generated	
SPD_INFO_ST			R
0x61	00000000	This readback indicates the latched status of the SPD InfoFrame detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via spd_info_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No interrupt generated 1 - spd_info_raw changed, interrupt generated	
AUDIO_INFO_ST			R
0x61	00000000	This readback indicates the latched status of the audio InfoFrame detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via audio_info_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No interrupt generated 1 - audio_inf_raw changed, interrupt generated	
AVI_INFO_ST			R
0x61	00000000	This readback indicates the latched status of the avi_info_raw signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. Once set, this bit remains high until the interrupt is cleared via avi_info_clr. 0 - avi_info_raw not changed state 1 - avi_info_raw changed state	
ISRC2_PCKT_CLR			SC
0x62	00000000	This control is used to clear the ISRC2 packet detection interrupt signal. This is a self clearing bit. 0 - Do not clear 1 - Clear isrc1_pckt_st	
ISRC1_PCKT_CLR			SC
0x62	00000000	This control is used to clear the ISRC1 packet detection interrupt signal. This is a self clearing bit. 0 - Do not clear isrc1_info_st 1 - Clear isrc1_info_st	

Reg	Bits	Description	
ACP_PCKT_CLR			SC
0x62	00000000	This control is used to clear the audio content protection packet detected interrupt signal. This is a self clearing bit. 0 - Do not clear acp_info_st 1 - Clear acp_info_st	
VS_INFO_CLR			SC
0x62	00000000	This control is used to clear the vendor specific InfoFrame interrupt signal. This is a self clearing bit. 0 - Do not clear vs_info_st 1 - Clear vs_info_st	
MS_INFO_CLR			SC
0x62	00000000	This control is used to clear the MPEG source InfoFrame interrupt signal. This is a self clearing bit. 0 - Do not clear ms_info_st 1 - Clear ms_info_st	
SPD_INFO_CLR			SC
0x62	00000000	This control is used to clear the SPD InfoFrame interrupt signal. This is a self clearing bit. 0 - Do not clear spd_info_st 1 - Clear spd_info_st	
AUDIO_INFO_CLR			SC
0x62	00000000	This control is used to clear the audio InfoFrame interrupt signal. This is a self clearing bit. 0 - Do not clear audio_inf_st 1 - Clear audio_inf_st	
AVI_INFO_CLR			SC
0x62	00000000	This control is used to clear the avi_info_raw and avi_info_st bits. This is a self clearing bit. 0 - No function 1 - Clear avi_info_raw and avi_info_st	
ISRC2_PCKT_MB2			R/W
0x63	00000000	This control is used to set the INT2 interrupt mask for the ISRC2 packet detection interrupt. When set, the ISRC2 packet detection interrupt triggers the INT2 interrupt and isrc2_info_st indicates the interrupt status. 0 - Disable ISRC2 InfoFrame detection interrupt for INT2 1 - Enable ISRC2 InfoFrame detection interrupt for INT2	
ISRC1_PCKT_MB2			R/W
0x63	00000000	This control is used to set the INT2 interrupt mask for the ISRC1 packet detection interrupt. When set, the ISRC1 packet detection interrupt triggers the INT2 interrupt and isrc1_info_st indicates the interrupt status. 0 - Disable ISRC1 InfoFrame detection interrupt for INT2 1 - Enable ISRC1 InfoFrame detection interrupt for INT2	
ACP_PCKT_MB2			R/W
0x63	00000000	This control is used to set the INT2 interrupt mask for the audio content protection packet detection interrupt. When set, the audio content protection InfoFrame detection interrupt triggers the INT2 interrupt and acp_info_st indicates the interrupt status. 0 - Disable audio content protection InfoFrame detection interrupt for INT2 1 - Enable audio content protection InfoFrame detection interrupt for INT2	
VS_INFO_MB2			R/W
0x63	00000000	This control is used to set the INT2 interrupt mask for the vendor specific InfoFrame detection interrupt. When set, the vendor specific InfoFrame detection interrupt triggers the INT2 interrupt and vs_info_st indicates the interrupt status. 0 - Disable vendor specific InfoFrame detection interrupt for INT2 1 - Enable vendor specific InfoFrame detection interrupt for INT2	
MS_INFO_MB2			R/W
0x63	00000000	This control is used to set the INT2 interrupt mask for the MPEG source InfoFrame detection interrupt. When set, the MPEG source InfoFrame detection interrupt triggers the INT2 interrupt and ms_info_st indicates the interrupt status. 0 - Disable MPEG source InfoFrame detection interrupt for INT2 1 - Enable MPEG source InfoFrame detection interrupt for INT2	
SPD_INFO_MB2			R/W
0x63	00000000	This control is used to set the INT2 interrupt mask for the SPD InfoFrame detection interrupt. When set, the SPD InfoFrame detection interrupt triggers the INT2 interrupt and spd_info_st indicates the interrupt status. 0 - Disable SPD InfoFrame detection interrupt for INT2 1 - Enable SPD InfoFrame detection interrupt for INT2	

Reg	Bits	Description	
AUDIO_INFO_MB2			R/W
0x63	000000 <u>00</u>	This control is used to set the INT2 interrupt mask for the audio InfoFrame detection interrupt. When set, the audio InfoFrame detection interrupt triggers the INT2 interrupt and avi_info_st indicates the interrupt status. 0 - Disable audio InfoFrame detection interrupt for INT2 1 - Enable audio InfoFrame detection interrupt for INT2	
AVI_INFO_MB2			R/W
0x63	000000 <u>00</u>	This control is used to set the INT2 interrupt mask for the AVI InfoFrame detection interrupt. When set, an AVI InfoFrame detection event causes avi_info_st to be set and an interrupt generated on INT2. 0 - Disable AVI InfoFrame detection interrupt for INT2 1 - Enable AVI InfoFrame detection interrupt for INT2	
ISRC2_PCKT_MB1			R/W
0x64	<u>0</u> 0000000	This control is used to set the INT1 interrupt mask for the ISRC2 InfoFrame detection interrupt. When set, the ISRC2 InfoFrame detection interrupt triggers the INT1 interrupt and isrc2_info_st indicates the interrupt status. 0 - Disable ISRC2 packet detection interrupt for INT1 1 - Enable ISRC2 packet detection interrupt for INT1	
ISRC1_PCKT_MB1			R/W
0x64	<u>00</u> 000000	This control is used to set the INT1 interrupt mask for the ISRC1 InfoFrame detection interrupt. When set, the ISRC1 InfoFrame detection interrupt triggers the INT1 interrupt and isrc1_info_st indicates the interrupt status. 0 - Disable ISRC1 InfoFrame detection interrupt for INT1 1 - Enable ISRC1 InfoFrame detection interrupt for INT1	
ACP_PCKT_MB1			R/W
0x64	<u>000</u> 00000	This control is used to set the INT1 interrupt mask for the audio content protection packet detection interrupt. When set, the audio content protection packet detection interrupt triggers the INT1 interrupt and acp_info_st indicates the interrupt status. 0 - Disable audio content protection InfoFrame detection interrupt for INT1 1 - Enable audio content protection InfoFrame detection interrupt for INT1	
VS_INFO_MB1			R/W
0x64	<u>0000</u> 0000	This control is used to set the INT1 interrupt mask for the vendor specific InfoFrame detection interrupt. When set, the vendor specific InfoFrame detection interrupt triggers the INT1 interrupt and vs_info_st indicates the interrupt status. 0 - Disable vendor specific InfoFrame detection interrupt for INT1 1 - Enable vendor specific InfoFrame detection interrupt for INT1	
MS_INFO_MB1			R/W
0x64	0000 <u>0</u> 000	This control is used to set the INT1 interrupt mask for the MPEG source InfoFrame detection interrupt. When set, the MPEG source InfoFrame detection interrupt triggers the INT1 interrupt and ms_info_st indicates the interrupt status. 0 - Disable MPEG source InfoFrame detection interrupt for INT1 1 - Enable MPEG source InfoFrame detection interrupt for INT1	
SPD_INFO_MB1			R/W
0x64	0000 <u>00</u> 00	This control is used to set the INT1 interrupt mask for the SPD InfoFrame detection interrupt. When set, the SPD InfoFrame detection interrupt triggers the INT1 interrupt and spd_info_st indicates the interrupt status. 0 - Disable SPD InfoFrame detection interrupt for INT1 1 - Enable SPD InfoFrame detection interrupt for INT1	
AUDIO_INFO_MB1			R/W
0x64	00000 <u>00</u> 00	This control is used to set the INT1 interrupt mask for the audio InfoFrame detection interrupt. When set, the audio InfoFrame detection interrupt triggers the INT1 interrupt and avi_info_st indicates the interrupt status. 0 - Disable audio InfoFrame detection interrupt for INT1 1 - Enable audio InfoFrame detection interrupt for INT1	
AVI_INFO_MB1			R/W
0x64	000000 <u>00</u>	This control is used to set the INT1 interrupt mask for the AVI InfoFrame detection interrupt. When set, an AVI InfoFrame detection event causes avi_info_st to be set and an interrupt generated on INT1. 0 - Disable AVI InfoFrame detection interrupt for INT1 1 - Enable AVI InfoFrame detection interrupt for INT1	
CS_DATA_VALID_RAW			R
0x65	<u>0</u> 0000000	This readback indicates the raw status signal of the channel status data valid signal. 0 - Channel status data not valid 1 - Channel status data valid	

Reg	Bits	Description	
INTERNAL_MUTE_RAW			R
0x65	00000000	This readback indicates the raw status signal of the internal mute signal. 0 - Audio not muted 1 - Audio muted	
AV_MUTE_RAW			R
0x65	00000000	This readback indicates the raw status signal of the AV mute detection signal. 0 - No AV mute raw received since last HDMI reset condition 1 - AV mute received	
AUDIO_CH_MD_RAW			R
0x65	00000000	This readback indicates the raw status signal indicating the layout value of the audio packets that were last received. 0 - Last audio packets received have layout value of 1 (e.g. Layout-1 corresponds to 2-channel audio when audio sample packets are received) 1 - Last audio packets received have layout value of 0 (e.g. Layout-0 corresponds to 8-channel audio when audio sa	
HDMI_MODE_RAW			R
0x65	00000000	This readback indicates the raw status signal of the HDMI mode signal. 0 - DVI being received 1 - HDMI being received	
GEN_CTL_PCKT_RAW			R
0x65	00000000	This readback indicates the raw status signal of the general control packet detection signal. 0 - No general control packets received since last HDMI reset condition 1 - General control packets received	
AUDIO_C_PCKT_RAW			R
0x65	00000000	This readback indicates the raw status signal of the audio clock regeneration packet detection signal. 0 - No audio clock regeneration packets received since last HDMI reset condition 1 - Audio clock regeneration packets received	
GAMUT_MDATA_RAW			R
0x65	00000000	This readback indicates the raw status signal of the gamut metadata packet detection signal. This bit resets to 0 after an HDMI packet detection reset or upon writing to gamut_packet_id. 0 - No gamut metadata packet received in last video frame or since last HDMI packet detection reset 1 - Gamut metadata packet received in last video frame	
CS_DATA_VALID_ST			R
0x66	00000000	This readback indicates the latched status of the channel status data valid interrupt signal. Once set, this bit remains high until the interrupt is cleared via cs_data_valid_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - cs_data_valid_raw not changed, interrupt not generated 1 - cs_data_valid_raw changed, interrupt generated	
INTERNAL_MUTE_ST			R
0x66	00000000	This readback indicates the latched status of Internal Mute interrupt signal. Once set, this bit remains high until the interrupt is cleared via internal_mute_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - internal_mute_raw not changed, interrupt not generated 1 - internal_mute_raw changed, interrupt generated	
AV_MUTE_ST			R
0x66	00000000	This readback indicates the latched status of the AV mute detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via av_mute_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - av_mute_raw not changed, interrupt not generated 1 - av_mute_raw changed, interrupt generated	
AUDIO_CH_MD_ST			R
0x66	00000000	This readback indicates the latched status of the audio channel mode interrupt signal. Once set, this bit remains high until the interrupt is cleared via audio_ch_md_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - audio_ch_md_raw not changed, interrupt not generated 1 - audio_....._raw changed, interrupt generated	

Reg	Bits	Description	
HDMI_MODE_ST			R
0x66	00000 <u>000</u>	This readback indicates the latched status of the HDMI mode interrupt signal. Once set, this bit remains high until the interrupt is cleared via <code>hdmi_mode_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - <code>hdmi_mode_raw</code> unchanged, interrupt not generated 1 - (No Suggestions) changed, interrupt generated	
GEN_CTL_PCKT_ST			R
0x66	00000 <u>000</u>	This readback indicates the latched status of the general control packet interrupt signal. Once set, this bit remains high until the interrupt is cleared via <code>gen_ctl_pckt_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - <code>gen_ctl_pckt_raw</code> unchanged, interrupt not generated 1 - <code>gen_ctl_pckt_raw</code> changed, interrupt generated	
AUDIO_C_PCKT_ST			R
0x66	000000 <u>00</u>	This readback indicates the latched status of the audio clock regeneration packet interrupt signal. Once set, this bit remains high until the interrupt is cleared via <code>audio_pckt_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - <code>audio_c_pckt_raw</code> unchanged, no interrupt generated 1 - <code>audio_c_pckt_raw</code> changed, interrupt generated .	
GAMUT_MDATA_ST			R
0x66	0000000 <u>0</u>	This readback indicates the latched status of the gamut metadata packet detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via <code>gamut_mdata_pckt_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 mask bit. 0 - <code>gamut_mdata_raw</code> unchanged, no interrupt generated 1 - <code>gamut_mdata_raw</code> changed, interrupt generated	
CS_DATA_VALID_CLR			SC
0x67	<u>0</u> 0000000	This control is used to clear the channel status data valid interrupt signal. This is a self clearing bit. 0 - Do not clear 1 - Clear <code>cs_data_valid_st</code>	
INTERNAL_MUTE_CLR			SC
0x67	<u>0</u> 0000000	This control is used to clear the internal mute interrupt signal. This is a self clearing bit. 0 - Do not clear <code>internal_mute_st</code> 1 - Clear <code>internal_mute_st</code>	
AV_MUTE_CLR			SC
0x67	<u>0</u> 0000000	This control is used to clear the AV mute detected interrupt signal. This is a self clearing bit. 0 - Do not clear <code>av_mute_st</code> 1 - Clear <code>av_mute_st</code>	
AUDIO_CH_MD_CLR			SC
0x67	<u>0</u> 0000000	This control is used to clear the audio channel mode interrupt signal. This is a self clearing bit. 0 - Do not clear <code>audio_ch_md_st</code> 1 - Clear <code>audio_ch_md_st</code>	
HDMI_MODE_CLR			SC
0x67	<u>0</u> 0000000	This control is used to clear the HDMI mode interrupt signal. This is a self clearing bit. 0 - Do not clear <code>hdmi_mode_st</code> 1 - Clear <code>hdmi_mode_st</code>	
GEN_CTL_PCKT_CLR			SC
0x67	<u>0</u> 0000000	This control is used to clear the general control packet detection interrupt signal. This is a self clearing bit. 0 - Do not clear <code>gen_ctl_pckt_st</code> 1 - Clear <code>gen_ctl_pckt_st</code>	
AUDIO_C_PCKT_CLR			SC
0x67	<u>0</u> 0000000	This control is used to clear the audio clock regeneration packet detection interrupt signal. This is a self clearing bit. 0 - Do not clear <code>audio_c_pckt_st</code> 1 - Clear <code>audio_c_pckt_st</code>	
GAMUT_MDATA_CLR			SC
0x67	<u>0</u> 0000000	This control is used to clear the gamut metadata packet detection interrupt signal. This is a self clearing bit. 0 - Do not clear <code>gamut_mdata_st</code> 1 - Clear <code>gamut_mdata_st</code>	

Reg	Bits	Description	
CS_DATA_VALID_MB2			R/W
0x68	00000000	This control is used to set the INT2 interrupt mask for the channel status data valid interrupt. When set, the channel status data valid interrupt triggers the INT2 interrupt and cs_data_valid_st indicates the interrupt status. 0 - Disable channel status data valid interrupt for INT2 1 - Enable channel status data valid interrupt for INT2	
INTERNAL_MUTE_MB2			R/W
0x68	00000000	This control is used to set the INT2 interrupt mask for the internal mute interrupt. When set, the internal mute interrupt triggers the INT2 interrupt and internal_mute_st indicates the interrupt status. 0 - Disable internal mute interrupt for INT2 1 - Enable internal mute interrupt for INT2	
AV_MUTE_MB2			R/W
0x68	00000000	This control is used to set the INT2 interrupt mask for the AV mute detected interrupt. When set, the AV mute detected interrupt triggers the INT2 interrupt and av_mute_st indicates the interrupt status. 0 - Disable AV mute detected interrupt for INT2 1 - Enable AV mute detected interrupt for INT2	
AUDIO_CH_MD_MB2			R/W
0x68	00000000	This control is used to set the INT2 interrupt mask for the audio channel mode interrupt. When set, the audio channel mode interrupt triggers the INT2 interrupt and audio_ch_md_st indicates the interrupt status. 0 - Disable audio channel mode interrupt for INT2 1 - Enable audio channel mode interrupt for INT2	
HDMI_MODE_MB2			R/W
0x68	00000000	This control is used to set the INT2 interrupt mask for the HDMI mode interrupt. When set, the HDMI mode interrupt triggers the INT2 interrupt and hdmi_mode_st indicates the interrupt status. 0 - Disable HDMI mode interrupt for INT2 1 - Enable HDMI mode interrupt for INT2	
GEN_CTL_PCKT_MB2			R/W
0x68	00000000	This control is used to set the INT2 interrupt mask for general control packet detection interrupt. When set, the general control packet detection interrupt triggers the INT2 interrupt and audio_c_pckt_st indicates the interrupt status. 0 - Disable general control packet detection interrupt for INT2 1 - Enable general control packet detection interrupt for INT2	
AUDIO_C_PCKT_MB2			R/W
0x68	00000000	This control is used to set the INT2 interrupt mask for the audio clock regeneration packet detection interrupt. When set, the audio clock regeneration packet detection interrupt triggers the INT2 interrupt and audio_c_pckt_st indicates the interrupt status 0 - Disable audio clock regeneration packet detection interrupt for INT2 1 - Enable audio clock regeneration packet detection interrupt for INT2	
GAMUT_MDATA_MB2			R/W
0x68	00000000	This control is used to set the INT2 interrupt mask for the gamut metadata packet detection interrupt. When set, the gamut metadata packet detection interrupt triggers the INT2 interrupt and gamut_mdata_pckt_st indicates the interrupt status. 0 - Disable gamut metadata packet detection interrupt for INT2 1 - Enable gamut metadata packet detection interrupt for INT2	
CS_DATA_VALID_MB1			R/W
0x69	00000000	This control is used to set the INT1 interrupt mask for the channel status data valid interrupt. When set, the channel status data valid interrupt triggers the INT1 interrupt and cs_data_valid_st indicates the interrupt status. 0 - Disable channel status data valid interrupt for INT1 1 - Enable channel status data valid interrupt for INT1	
INTERNAL_MUTE_MB1			R/W
0x69	00000000	This control is used to set the INT1 interrupt mask for the internal mute interrupt. When set, the internal mute interrupt triggers the INT1 interrupt and internal_mute_st indicates the interrupt status. 0 - Disable AV Mute detected interrupt for INT1 1 - Enable AV Mute detected interrupt for INT1	
AV_MUTE_MB1			R/W
0x69	00000000	This control is used to set the INT1 interrupt mask for the AV mute detected interrupt. When set, the AV mute detected interrupt triggers the INT1 interrupt and av_mute_st indicates the interrupt status. 0 - Disable AV mute detected interrupt for INT1 1 - Enable AV mute detected interrupt for INT1	

Reg	Bits	Description	
AUDIO_CH_MD_MB1			R/W
0x69	00000000	This control is used to set the INT1 interrupt mask for the audio channel mode interrupt. When set, the audio channel mode interrupt triggers the INT1 interrupt and audio_ch_md_st indicates the interrupt status. 0 - Disable audio channel mode interrupt for INT1 1 - Enable audio channel mode interrupt for INT1	
HDMI_MODE_MB1			R/W
0x69	00000000	This control is used to set the INT1 interrupt mask for the HDMI mode detection interrupt. When set, the HDMI mode interrupt triggers the INT1 interrupt and hdmi_mode_st indicates the interrupt status. 0 - Disable HDMI mode interrupt for INT1 1 - Enable HDMI mode interrupt for INT1	
GEN_CTL_PKT_MB1			R/W
0x69	00000000	This control is used to set the INT1 interrupt mask for the general control packet detection interrupt. When set, the general control packet detection interrupt triggers the INT1 interrupt and gen_ctl_pkt_st indicates the interrupt status. 0 - Disable general control packet detection interrupt for INT1 1 - Enable general control packet detection interrupt for INT1	
AUDIO_C_PKT_MB1			R/W
0x69	00000000	This control is used to set the INT1 interrupt mask for the audio clock regeneration packet detection interrupt. When set, the audio clock regeneration packet detection interrupt triggers the INT1 interrupt and audio_c_pkt_st indicates the interrupt status. 0 - Disable audio clock regeneration packet detection interrupt for INT1 1 - Enable audio clock regeneration packet detection interrupt for INT1	
GAMUT_METADATA_MB1			R/W
0x69	00000000	This control is used to set the INT1 interrupt mask for the gamut metadata packet detection interrupt. When set, the gamut metadata packet detection interrupt triggers the INT1 interrupt and gamut_metadata_pkt_st indicates the interrupt status. 0 - Disable gamut metadata packet detection interrupt for INT1 1 - Enable gamut metadata packet detection interrupt for INT1	
TMDSPLL_LCK_A_RAW			R
0x6A	00000000	This readback indicates the raw status of the Port A TMDS PLL lock signal. 0 - TMDS PLL on Port A not locked 1 - TMDS PLL on Port A locked to incoming clock	
TMDSPLL_LCK_B_RAW			R
0x6A	00000000	This readback indicates the raw status of the Port B TMDS PLL lock signal. 0 - TMDS PLL on Port B not locked 1 - TMDS PLL on Port B locked to incoming clock	
TMDSPLL_LCK_C_RAW			R
0x6A	00000000	This readback indicates the raw status of the Port C TMDS PLL lock signal. 0 - TMDS PLL on Port C not locked 1 - TMDS PLL on Port C locked to incoming clock	
TMDSPLL_LCK_D_RAW			R
0x6A	00000000	This readback indicates the raw status of the Port D TMDS PLL lock signal. 0 - TMDS PLL on Port D not locked 1 - TMDS PLL on Port D locked to incoming clock	
TMDS_CLK_A_RAW			R
0x6A	00000000	This readback indicates the raw status of the Port A TMDS clock detection signal. 0 - No TMDS clock detected on Port A 1 - TMDS clock detected on Port A	
TMDS_CLK_B_RAW			R
0x6A	00000000	This readback indicates the raw status of the Port B TMDS clock detection signal. 0 - No TMDS clock detected on Port B 1 - TMDS clock detected on Port B	
TMDS_CLK_C_RAW			R
0x6A	00000000	This readback indicates the raw status of the Port C TMDS clock detection signal. 0 - No TMDS clock detected on Port C 1 - TMDS clock detected on Port C	

Reg	Bits	Description	
TMDS_CLK_D_RAW			R
0x6A	00000000	This readback indicates the raw status of the Port D TMDS clock detection signal. 0 - No TMDS clock detected on Port D 1 - TMDS clock detected on Port D	
TMDSPLL_LCK_A_ST			R
0x6B	00000000	This readback indicates the latched status of the Port A TMDS PLL lock interrupt signal. Once set, this bit remains high until the interrupt is cleared via <code>tmdsppll_lck_a_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - <code>tmdsppll_lck_a_raw</code> not changed, interrupt not generated 1 - <code>tmdsppll_lck_a_raw</code> changed, interrupt generated	
TMDSPLL_LCK_B_ST			R
0x6B	00000000	This readback indicates the latched status of the Port B TMDS PLL lock interrupt signal. Once set, this bit remains high until the interrupt is cleared via <code>tmdsppll_lck_b_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - <code>tmdsppll_lck_b_raw</code> not changed, interrupt not generated 1 - <code>tmdsppll_lck_b_raw</code> changed, interrupt generated	
TMDSPLL_LCK_C_ST			R
0x6B	00000000	This readback indicates the latched status of the Port C TMDS PLL lock interrupt signal. Once set, this bit remains high until the interrupt is cleared via <code>tmdsppll_lck_c_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - <code>tmdsppll_lck_c_raw</code> not changed, interrupt not generated 1 - <code>tmdsppll_lck_c_raw</code> changed, interrupt generated	
TMDSPLL_LCK_D_ST			R
0x6B	00000000	This readback indicates the latched status of the Port D TMDS PLL lock interrupt signal. Once set, this bit remains high until the interrupt is cleared via <code>tmdsppll_lck_d_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - <code>tmdsppll_lck_d_raw</code> not changed, interrupt not generated 1 - <code>tmdsppll_lck_d_raw</code> changed, interrupt generated	
TMDS_CLK_A_ST			R
0x6B	00000000	This readback indicates the latched status of the Port A TMDS clock detection interrupt signal. Once set, this bit remains high until the interrupt is cleared via <code>tmds_clk_a_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - <code>tmds_clk_a_raw</code> not changed, interrupt not generated 1 - <code>tmds_clk_a_raw</code> changed, interrupt generated	
TMDS_CLK_B_ST			R
0x6B	00000000	This readback indicates the latched status of the Port B TMDS clock detection interrupt signal. Once set, this bit remains high until the interrupt is cleared via <code>tmds_clk_b_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - <code>tmds_clk_b_raw</code> not changed, interrupt not generated 1 - <code>tmds_clk_b_raw</code> changed, interrupt generated	
TMDS_CLK_C_ST			R
0x6B	00000000	This readback indicates the latched status of the Port C TMDS clock detection interrupt signal. Once set, this bit remains high until the interrupt is cleared via <code>tmds_clk_c_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - <code>tmds_clk_c_raw</code> not changed, interrupt not generated 1 - <code>tmds_clk_c_raw</code> changed, interrupt generated	
TMDS_CLK_D_ST			R
0x6B	00000000	This readback indicates the latched status of the Port D TMDS clock detection interrupt signal. Once set, this bit remains high until the interrupt is cleared via <code>tmds_clk_d_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - <code>tmds_clk_d_raw</code> not changed, interrupt not generated 1 - <code>tmds_clk_d_raw</code> changed, interrupt generated	
TMDSPLL_LCK_A_CLR			SC
0x6C	00000000	This control is used to clear the Port A TMDS PLL lock interrupt signal. This is a self clearing bit. 0 - Do not clear <code>tmdsppll_lck_a_st</code> 1 - Clear <code>tmdsppll_lck_a_st</code>	

Reg	Bits	Description	
TMDSPLL_LCK_B_CLR			SC
0x6C	00000000	This control is used to clear the Port B TMDS PLL lock interrupt signal. This is a self clearing bit. 0 - Do not clear tmdspll_lck_b_st 1 - Clear tmdspll_lck_b_st	
TMDSPLL_LCK_C_CLR			SC
0x6C	00000000	This control is used to clear the Port C TMDS PLL lock interrupt signal. This is a self clearing bit. 0 - Do not clear tmdspll_lck_c_st 1 - Clear tmdspll_lck_c_st	
TMDSPLL_LCK_D_CLR			SC
0x6C	00000000	This control is used to clear the Port D TMDS PLL lock interrupt signal. This is a self clearing bit. 0 - Do not clear tmdspll_lck_d_st 1 - Clear tmdspll_lck_d_st	
TMDS_CLK_A_CLR			SC
0x6C	00000000	This control is used to clear the Port A TMDS clock detection interrupt signal. This is a self clearing bit. 0 - Do not clear tmds_clk_a_st 1 - Clear tmds_clk_a_st	
TMDS_CLK_B_CLR			SC
0x6C	00000000	This control is used to clear the Port B TMDS clock detection interrupt signal. This is a self clearing bit. 0 - Do not clear tmds_clk_b_st 1 - Clear tmds_clk_b_st	
TMDS_CLK_C_CLR			SC
0x6C	00000000	This control is used to clear the Port C TMDS clock detection interrupt signal. This is a self clearing bit. 0 - Do not clear tmds_clk_c_st 1 - Clear tmds_clk_c_st	
TMDS_CLK_D_CLR			SC
0x6C	00000000	This control is used to clear the Port D TMDS clock detection interrupt signal. This is a self clearing bit. 0 - Do not clear tmds_clk_d_st 1 - Clear tmds_clk_d_st	
TMDSPLL_LCK_A_MB2			R/W
0x6D	00000000	This control is used to set the INT2 interrupt mask for the Port A TMDS PLL lock interrupt. When set, the Port A TMDS PLL lock interrupt triggers the INT2 interrupt and tmdspll_lck_a_st indicates the interrupt status. 0 - Disable Port A TMDSPLL lock interrupt for INT2 1 - Enable Port A TMDSPLL lock interrupt for INT2	
TMDSPLL_LCK_B_MB2			R/W
0x6D	00000000	This control is used to set the INT2 interrupt mask for the Port B TMDS PLL lock interrupt. When set, the Port B TMDS PLL lock interrupt triggers the INT2 interrupt and tmdspll_lck_b_st indicates the interrupt status. 0 - Disable Port B TMDSPLL lock interrupt for INT2 1 - Enable Port B TMDSPLL lock interrupt for INT2	
TMDSPLL_LCK_C_MB2			R/W
0x6D	00000000	This control is used to set the INT2 interrupt mask for Port C TMDS PLL lock interrupt. When set, the Port C TMDS PLL lock interrupt triggers the INT2 interrupt and tmdspll_lck_c_st indicates the interrupt status. 0 - Disable Port C TMDSPLL lock interrupt for INT2 1 - Enable Port C TMDSPLL lock interrupt for INT2	
TMDSPLL_LCK_D_MB2			R/W
0x6D	00000000	This control is used to set the INT2 interrupt mask for the Port D TMDS PLL lock interrupt. When set, the Port D TMDS PLL lock interrupt triggers the INT2 interrupt and tmdspll_lck_d_st indicates the interrupt status. 0 - Disable Port D TMDSPLL lock interrupt for INT2 1 - Enable Port D TMDSPLL lock interrupt for INT2	
TMDS_CLK_A_MB2			R/W
0x6D	00000000	This control is used to set the INT2 interrupt mask for the Port B TMDS clock detection interrupt. When set, the Port B TMDS clock detection interrupt triggers the INT2 interrupt and tmds_clk_a_st indicates the interrupt status. 0 - Disable Port A TMDS clock detection interrupt for INT2 1 - Enable Port A TMDS clock detection interrupt for INT2	

Reg	Bits	Description	
TMDS_CLK_B_MB2			R/W
0x6D	00000 <u>0</u> 00	This control is used to set the INT2 interrupt mask for the Port B TMDS clock detection interrupt. When set, the Port B TMDS clock detection interrupt triggers the INT2 interrupt and <code>tmds_clk_b_st</code> indicates the interrupt status. 0 - Disable Port B TMDS clock detection interrupt for INT2 1 - Enable Port B TMDS clock detection interrupt for INT2	
TMDS_CLK_C_MB2			R/W
0x6D	00000 <u>0</u> 00	This control is used to set the INT2 interrupt mask for the Port C TMDS clock detection interrupt. When set, the Port C TMDS clock detection interrupt triggers the INT2 interrupt and <code>tmds_clk_c_st</code> indicates the interrupt status. 0 - Disable Port C TMDS clock detection interrupt for INT2 1 - Enable Port C TMDS clock detection interrupt for INT2	
TMDS_CLK_D_MB2			R/W
0x6D	00000 <u>0</u> 00	This control is used to set the INT2 interrupt mask for the port D TMDS clock detection interrupt. When set, the port D TMDS clock detection interrupt triggers the INT2 interrupt and <code>tmds_clk_d_st</code> indicates the interrupt status. 0 - Disable Port D TMDS clock detection interrupt for INT2 1 - Enable Port D TMDS clock detection interrupt for INT2	
TMDSPLL_LCK_A_MB1			R/W
0x6E	<u>0</u> 0000000	This control is used to set the INT1 interrupt mask for the Port A TMDS PLL lock interrupt. When set, the Port A TMDS PLL lock interrupt triggers the INT1 interrupt and <code>tmdspil_lck_a_st</code> indicates the interrupt status. 0 - Disable Port A TMDSPLL lock interrupt for INT1 1 - Enable Port A TMDSPLL lock interrupt for INT1	
TMDSPLL_LCK_B_MB1			R/W
0x6E	<u>0</u> 0000000	This control is used to set the INT1 interrupt mask for the Port B TMDS PLL lock interrupt. When set, the Port B TMDS PLL lock interrupt triggers the INT1 interrupt and <code>tmdspil_lck_b_st</code> indicates the interrupt status. 0 - Disable Port B TMDSPLL lock interrupt for INT1 1 - Enable Port B TMDSPLL lock interrupt for INT1	
TMDSPLL_LCK_C_MB1			R/W
0x6E	<u>0</u> 0000000	This control is used to set the INT1 interrupt mask for the Port C TMDS PLL lock interrupt. When set, the Port C TMDS PLL lock interrupt triggers the INT1 interrupt and <code>tmdspil_lck_c_st</code> indicates the interrupt status. 0 - Disable Port C TMDSPLL lock interrupt for INT1 1 - Enable Port C TMDSPLL lock interrupt for INT1	
TMDSPLL_LCK_D_MB1			R/W
0x6E	<u>0</u> 0000000	This control is used to set the INT1 interrupt mask for the Port D TMDS PLL lock interrupt. When set, the Port D TMDS PLL lock interrupt triggers the INT1 interrupt and <code>tmdspil_lck_d_st</code> indicates the interrupt status. 0 - Disable Port D TMDSPLL lock interrupt for INT1 1 - Enable Port D TMDSPLL lock interrupt for INT1	
TMDS_CLK_A_MB1			R/W
0x6E	0000 <u>0</u> 000	This control is used to set the INT1 interrupt mask for the Port B TMDS clock detection interrupt. When set, the Port B TMDS clock detection interrupt triggers the INT1 interrupt and <code>tmds_clk_a_st</code> indicates the interrupt status. 0 - Disable Port A TMDS clock detection interrupt for INT1 1 - Enable Port A TMDS clock detection interrupt for INT1	
TMDS_CLK_B_MB1			R/W
0x6E	0000 <u>0</u> 000	This control is used to set the INT1 interrupt mask for the Port B TMDS clock detection interrupt. When set, the Port B TMDS clock detection interrupt triggers the INT1 interrupt and <code>tmds_clk_b_st</code> indicates the interrupt status. 0 - Disable Port B TMDS clock detection interrupt for INT1 1 - Enable Port B TMDS clock detection interrupt for INT1	
TMDS_CLK_C_MB1			R/W
0x6E	0000 <u>0</u> 000	This control is used to set the INT1 interrupt mask for the Port C TMDS clock detection interrupt. When set, the Port C TMDS clock detection interrupt triggers the INT1 interrupt and <code>tmds_clk_c_st</code> indicates the interrupt status. 0 - Disable Port C TMDS clock detection interrupt for INT1 1 - Enable Port C TMDS clock detection interrupt for INT1	
TMDS_CLK_D_MB1			R/W
0x6E	0000 <u>0</u> 000	This control is used to set the INT1 interrupt mask for the Port D TMDS clock detection interrupt. When set, the Port D TMDS clock detection interrupt triggers the INT1 interrupt and <code>tmds_clk_d_st</code> indicates the interrupt status. 0 - Disable Port D TMDS clock detection interrupt for INT1 1 - Enable Port D TMDS clock detection interrupt for INT1	

Reg	Bits	Description	
HDMI_ENCRPT_A_RAW			R
0x6F	00000000	This readback indicates the raw status of the Port A encryption detection signal. 0 - Current frame in Port A not encrypted 1 - Current frame in Port A encrypted	
HDMI_ENCRPT_B_RAW			R
0x6F	00000000	This readback indicates the raw status of the Port B encryption detection signal. 0 - Current frame in Port B not encrypted 1 - Current frame in Port B encrypted	
HDMI_ENCRPT_C_RAW			R
0x6F	00000000	This readback indicates the raw status of the Port C encryption detection signal. 0 - Current frame in Port C not encrypted 1 - Current frame in Port C encrypted	
HDMI_ENCRPT_D_RAW			R
0x6F	00000000	This readback indicates the raw status of the Port D encryption detection signal. 0 - Current frame in Port D not encrypted 1 - Current frame in Port D encrypted	
CABLE_DET_A_RAW			R
0x6F	00000000	This readback indicates the raw status of the Port A +5 V cable detection signal. 0 - No cable detected on Port A 1 - Cable detected on Port A (high level on rxa_5v)	
CABLE_DET_B_RAW			R
0x6F	00000000	This readback indicates the raw status of the Port B +5 V cable detection signal. 0 - No cable detected on Port B 1 - Cable detected on Port B (high level on rxb_5v)	
CABLE_DET_C_RAW			R
0x6F	00000000	This readback indicates the raw status of the Port C +5 V cable detection signal. 0 - No cable detected on Port C 1 - Cable detected on Port C (high level on rxc_5v)	
CABLE_DET_D_RAW			R
0x6F	00000000	This readback indicates the raw status of the Port D +5 V cable detection signal. 0 - No cable detected on Port D 1 - Cable detected on Port D (high level on rxd_5v)	
HDMI_ENCRPT_A_ST			R
0x70	00000000	This readback indicates the latched status of the Port A encryption detection interrupt signal. Once set, this bit remains high until the interrupt is cleared via hdmi_encrpt_a_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - hdmi_encrpt_a_raw not changed, interrupt not generated 1 - hdmi_encrpt_a_raw changed, interrupt generated	
HDMI_ENCRPT_B_ST			R
0x70	00000000	This readback indicates the latched status of the Port B encryption detection interrupt signal. Once set, this bit remains high until the interrupt is cleared via hdmi_encrpt_b_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - hdmi_encrpt_b_raw not changed, interrupt not generated 1 - hdmi_encrpt_b_raw changed, interrupt generated	
HDMI_ENCRPT_C_ST			R
0x70	00000000	This readback indicates the latched status of the Port C encryption detection interrupt signal. Once set, this bit remains high until the interrupt is cleared via hdmi_encrpt_c_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - hdmi_encrpt_c_raw not changed, interrupt not generated 1 - hdmi_encrpt_c_raw changed, interrupt generated	
HDMI_ENCRPT_D_ST			R
0x70	00000000	This readback indicates the latched status of the Port D encryption detection interrupt signal. Once set, this bit remains high until the interrupt is cleared via hdmi_encrpt_d_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - hdmi_encrpt_d_raw not changed, interrupt not generated 1 - hdmi_encrpt_d_raw changed, interrupt generated	

Reg	Bits	Description	
CABLE_DET_A_ST			R
0x70	00000 <u>000</u>	This readback indicates the latched status for the Port A +5 V cable detection interrupt signal. Once set, this bit remains high until the interrupt is cleared via cable_det_a_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - cable_det_a_raw not changed, interrupt not generated 1 - cable_det_a_raw changed, interrupt generated .	
CABLE_DET_B_ST			R
0x70	00000 <u>000</u>	This readback indicates the latched status for the Port B +5 V cable detection interrupt signal. Once set, this bit remains high until the interrupt is cleared via cable_det_b_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - cable_det_b_raw not changed, interrupt not generated 1 - cable_det_b_raw changed, interrupt generated	
CABLE_DET_C_ST			R
0x70	00000 <u>000</u>	This readback indicates the latched status of the Port C +5 V cable detection interrupt signal. Once set, this bit remains high until the interrupt is cleared via cable_det_c_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - cable_det_c_raw not changed, interrupt not generated 1 - cable_det_c_raw changed, interrupt generated	
CABLE_DET_D_ST			R
0x70	00000 <u>000</u>	This readback indicates the latched status of the Port D +5 V cable detection interrupt signal. When set, the Port D +5 V cable detection interrupt triggers the INT2 interrupt and cable_det_d_st indicates the interrupt status. 0 - cable_det_d_raw not changed, interrupt not generated 1 - cable_det_d_raw changed, interrupt generated	
HDMI_ENCRPT_A_CLR			SC
0x71	<u>0</u> 0000000	This control is used to clear the Port A encryption detection interrupt signal. This is a self clearing bit. 0 - Do not clear hdmi_encrpt_a_st 1 - Clear hdmi_encrpt_a_st	
HDMI_ENCRPT_B_CLR			SC
0x71	<u>0</u> 0000000	This control is used to clear the Port B encryption detection interrupt signal. This is a self clearing bit. 0 - Do not clear hdmi_encrpt_b_st 1 - Clear hdmi_encrpt_b_st	
HDMI_ENCRPT_C_CLR			SC
0x71	<u>0</u> 0000000	This control is used to clear the Port C encryption detection interrupt signal. This is a self clearing bit. 0 - Do not clear hdmi_encrpt_c_st 1 - Clear hdmi_encrpt_c_st	
HDMI_ENCRPT_D_CLR			SC
0x71	<u>0</u> 0000000	This control is used to clear the Port D encryption detection interrupt signal. This is a self clearing bit. 0 - Do not clear hdmi_encrpt_d_st 1 - Clear hdmi_encrpt_d_st	
CABLE_DET_A_CLR			SC
0x71	00000 <u>000</u>	This control is used to clear the Port A +5 V cable detection interrupt signal. This is a self clearing bit. 0 - Do not clear cable_det_a_st 1 - Clear cable_det_a_st	
CABLE_DET_B_CLR			SC
0x71	00000 <u>000</u>	This control is used to clear the Port B +5 V cable detection interrupt signal. This is a self clearing bit. 0 - Do not clear cable_det_b_st 1 - Clear cable_det_b_st	
CABLE_DET_C_CLR			SC
0x71	00000 <u>000</u>	This control is used to clear the Port C +5 V cable detection interrupt signal. This is a self clearing bit. 0 - Do not clear cable_det_c_st 1 - Clear cable_det_c_st	
CABLE_DET_D_CLR			SC
0x71	00000 <u>000</u>	This control is used to clear the Port D +5 V cable detection interrupt signal. This is a self clearing bit. 0 - Do not clear cable_det_d_st 1 - Clear cable_det_d_st	

Reg	Bits	Description	
HDMI_ENCRPT_A_MB2			R/W
0x72	00000000	This control is used to set the INT2 interrupt mask for the Port A encryption detection interrupt. When set, the Port A encryption detection interrupt triggers the INT2 interrupt and hdmi_encrpt_a_st indicates the interrupt status. 0 - Disable Port A HDMI encryption detection interrupt for INT2 1 - Enable Port A HDMI encryption detection interrupt for INT2	
HDMI_ENCRPT_B_MB2			R/W
0x72	00000000	This control is used to set the INT2 interrupt mask for the Port B encryption detection interrupt. When set, the Port B encryption detection interrupt triggers the INT2 interrupt and hdmi_encrpt_b_st indicates the interrupt status. 0 - Disable Port B HDMI encryption detection interrupt for INT2 1 - Enable Port B HDMI encryption detection interrupt for INT2	
HDMI_ENCRPT_C_MB2			R/W
0x72	00000000	This control is used to set the INT2 interrupt mask for the Port C encryption detection interrupt. When set, the Port C encryption detection interrupt triggers the INT2 interrupt and hdmi_encrpt_c_st indicates the interrupt status. 0 - Disable Port C HDMI encryption detection interrupt for INT2 1 - Enable Port C HDMI encryption detection interrupt for INT2	
HDMI_ENCRPT_D_MB2			R/W
0x72	00000000	This control is used to set the INT2 interrupt mask for the Port D encryption detection interrupt. When set, the Port D encryption detection interrupt triggers the INT2 interrupt and hdmi_encrpt_d_st indicates the interrupt status. 0 - Disable Port D HDMI encryption detection interrupt for INT2 1 - Enable Port D HDMI encryption detection interrupt for INT2	
CABLE_DET_A_MB2			R/W
0x72	00000000	This control is used to set the INT2 interrupt mask for the Port A +5 V cable detection interrupt. When set, the Port B +5 V cable detection interrupt triggers the INT2 interrupt and cable_det_a_st indicates the interrupt status. 0 - Disable Port A +5 V cable detection interrupt for INT2 1 - Enable Port A +5 V cable detection interrupt for INT2	
CABLE_DET_B_MB2			R/W
0x72	00000000	This control is used to set the INT2 interrupt mask for the Port B +5 V cable detection interrupt. When set, the Port B +5 V cable detection interrupt triggers the INT2 interrupt and cable_det_b_st indicates the interrupt status. 0 - Disable Port B +5 V cable detection interrupt for INT2 1 - Enable Port B +5 V cable detection interrupt for INT2	
CABLE_DET_C_MB2			R/W
0x72	00000000	This control is used to set the INT2 interrupt mask for the Port C +5 V cable detection interrupt. When set, the Port C +5 V cable detection interrupt triggers the INT2 interrupt and cable_det_c_st indicates the interrupt status. 0 - Disable Port C +5 V cable detection interrupt for INT2 1 - Enable Port C +5 V cable detection interrupt for INT2	
CABLE_DET_D_MB2			R/W
0x72	00000000	This control is used to set the INT2 interrupt mask for the Port D +5 V cable detection interrupt. When set, the Port D +5 V cable detection interrupt triggers the INT2 interrupt and cable_det_d_st indicates the interrupt status. 0 - Disable Port D +5 V cable detection interrupt for INT2 1 - Enable Port D +5 V cable detection interrupt for INT2	
HDMI_ENCRPT_A_MB1			R/W
0x73	00000000	This control is used to set the INT1 interrupt mask for the Port A encryption detection interrupt. When set, the Port A encryption detection interrupt triggers the INT1 interrupt and hdmi_encrpt_a_st indicates the interrupt status. 0 - Disable Port A HDMI encryption detection interrupt for INT1 1 - Enable Port A HDMI encryption detection interrupt for INT1	
HDMI_ENCRPT_B_MB1			R/W
0x73	00000000	This control is used to set the INT1 interrupt mask for the Port B encryption detection interrupt. When set, the Port B encryption detection interrupt triggers the INT1 interrupt and hdmi_encrpt_b_st indicates the interrupt status. 0 - Disable Port B HDMI encryption detection interrupt for INT1 1 - Enable Port B HDMI encryption detection interrupt for INT1	
HDMI_ENCRPT_C_MB1			R/W
0x73	00000000	This control is used to set the INT1 interrupt mask for the Port C encryption detection interrupt. When set, the Port C encryption detection interrupt triggers the INT1 interrupt and hdmi_encrpt_c_st indicates the interrupt status. 0 - Disable Port C HDMI encryption detection interrupt for INT1 1 - Enable Port C HDMI encryption detection interrupt for INT1	

Reg	Bits	Description	
HDMI_ENCRPT_D_MB1			R/W
0x73	000 <u>0</u> 0000	This control is used to set the INT1 interrupt mask for the Port D encryption detection interrupt. When set, the Port D encryption detection interrupt triggers the INT1 interrupt and hdmi_encrpt_d_st indicates the interrupt status. 0 - Disable Port D HDMI encryption detection interrupt for INT1 1 - Enable Port D HDMI encryption detection interrupt for INT1	
CABLE_DET_A_MB1			R/W
0x73	0000 <u>0</u> 000	This control is used to set the INT1 interrupt mask for the Port A +5 V cable detection interrupt. When set, the Port A +5 V cable detection interrupt triggers the INT1 interrupt and cable_det_a_st indicates the interrupt status. 0 - Disable Port A +5 V cable detection interrupt for INT1 1 - Enable Port A +5 V cable detection interrupt for INT1	
CABLE_DET_B_MB1			R/W
0x73	00000 <u>0</u> 00	This control is used to set the INT1 interrupt mask for the Port B +5 V cable detection interrupt. When set, the Port B +5 V cable detection interrupt triggers the INT1 interrupt and cable_det_b_st indicates the interrupt status. 0 - Disable Port B +5 V cable detection interrupt for INT1 1 - Enable Port B +5 V cable detection interrupt for INT1	
CABLE_DET_C_MB1			R/W
0x73	000000 <u>0</u> 0	This control is used to set the INT1 interrupt mask for the Port C +5 V cable detection interrupt. When set, the Port C +5 V cable detection interrupt triggers the INT1 interrupt and cable_det_c_st indicates the interrupt status. 0 - Disable Port C +5 V cable detection interrupt for INT1 1 - Enable Port C +5 V cable detection interrupt for INT1	
CABLE_DET_D_MB1			R/W
0x73	0000000 <u>0</u>	This control is used to set the INT1 interrupt mask for the Port D +5 V cable detection interrupt. When set, the Port D +5 V cable detection interrupt triggers the INT1 interrupt and cable_det_d_st indicates the interrupt status. 0 - Disable Port D +5 V cable detection interrupt for INT1 1 - Enable Port D +5 V cable detection interrupt for INT1	
VIDEO_3D_RAW			R
0x74	00000 <u>0</u> 00	This readback indicates the raw status of the Video 3D signal. 0 - Video 3D not detected 1 - Video 3D detected	
V_LOCKED_RAW			R
0x74	000000 <u>0</u> 0	This readback indicates the raw status of the vertical sync filter locked signal. 0 - Vertical sync filter not locked and vertical sync parameters not valid 1 - Vertical sync filter locked and vertical sync parameters are valid	
DE_REGEN_LCK_RAW			R
0x74	0000000 <u>0</u>	This readback indicates the raw status of the DE regeneration lock signal. 0 - DE regeneration block not locked to incoming DE signal 1 - DE regeneration block locked to incoming DE signal	
VIDEO_3D_ST			R
0x75	00000 <u>0</u> 00	This readback indicates the latched status for the Video 3D interrupt. Once set, this bit remains high until the interrupt is cleared via video_3d_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - video_3d_raw not changed, interrupt not generated 1 - video_3d_raw changed, interrupt generated	
V_LOCKED_ST			R
0x75	000000 <u>0</u> 0	This readback indicates the latched status of the vertical sync filter locked interrupt. Once set, this bit remains high until the interrupt is cleared via v_locked_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - v_locked_raw not changed, interrupt not generated 1 - v_locked_raw changed, interrupt generated	
DE_REGEN_LCK_ST			R
0x75	0000000 <u>0</u>	This readback indicates the latched status of the DE regeneration lock interrupt signal. Once set, this bit remains high until the interrupt is cleared via de_regen_lck_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - de_regen_lck_raw not changed, interrupt not generated 1 - de_regen_lck_raw changed, interrupt generated	

Reg	Bits	Description	
VIDEO_3D_CLR			SC
0x76	00000000	This control is used to clear the Video 3D interrupt. This is a self clearing bit. 0 - Do not clear video_3d_st 1 - Clear video_3d_st	
V_LOCKED_CLR			SC
0x76	00000000	This control is used to clear the vertical sync filter locked interrupt. This is a self clearing bit. 0 - Do not clear v_locked_st 1 - Clear v_locked_st	
DE_REGEN_LCK_CLR			SC
0x76	00000000	This control is used to clear the DE regeneration lock interrupt signal. This is a self clearing bit. 0 - Do not clear de_regen_lck_st 1 - Clear de_regen_lck_st	
VIDEO_3D_MB2			R/W
0x77	00000000	This control is used to set the INT2 interrupt mask for the Video 3D interrupt. When set, the Video 3D interrupt triggers the INT2 interrupt and video_3d_st indicates the interrupt status. 0 - Disable Video 3D interrupt on INT2 1 - Enable Video 3D interrupt on INT2	
V_LOCKED_MB2			R/W
0x77	00000000	This control is used to set the INT2 interrupt mask for the vertical sync filter locked interrupt. When set, the vertical sync filter locked interrupt triggers the INT2 interrupt and v_locked_st indicates the interrupt status. 0 - Disable vertical sync filter lock interrupt on INT2 1 - Enable vertical sync filter lock interrupt on INT2	
DE_REGEN_LCK_MB2			R/W
0x77	00000000	This control is used to set the INT2 interrupt mask for the DE regeneration lock interrupt. When set, the DE regeneration lock interrupt triggers the INT2 interrupt and de_regen_lck_st indicates the interrupt status. 0 - Disable DE regeneration lock interrupt on INT2 1 - Enable DE regeneration lock interrupt on INT2	
VIDEO_3D_MB1			R/W
0x78	00000000	This control is used to set the INT1 interrupt mask for the Video 3D interrupt. When set, the Video 3D interrupt triggers the INT1 interrupt and video_3d_st indicates the interrupt status. 0 - Disable Video 3D interrupt on INT1 1 - Enable Video 3D interrupt on INT1	
V_LOCKED_MB1			R/W
0x78	00000000	This control is used to set the INT1 interrupt mask for the vertical sync filter locked interrupt. When set, the vertical sync filter locked interrupt triggers the INT1 interrupt and v_locked_st indicates the interrupt status. 0 - Disable Vertical Sync Filter lock interrupt on INT1 1 - Enable Vertical Sync Filter lock interrupt on INT1	
DE_REGEN_LCK_MB1			R/W
0x78	00000000	This control is used to set the INT1 interrupt mask for the DE regeneration lock interrupt. When set, the DE regeneration lock interrupt triggers the INT1 interrupt and de_regen_lck_st indicates the interrupt status. 0 - Disable DE regeneration lock interrupt on INT1 1 - Enable DE regeneration lock interrupt on INT1	
NEW_ISRC2_PCKT_RAW			R
0x79	00000000	This readback indicates the status of the New ISRC2 interrupt signal. When set to 1, it indicates that an ISRC2 packet was received with new contents. Once set, this bit remains high until it is cleared via new_isrc2_pckt_clr. 0 - No new ISRC2 packet received 1 - ISRC2 packet with new content received	
NEW_ISRC1_PCKT_RAW			R
0x79	00000000	This readback indicates the status of the New ISRC1 interrupt signal. When set to 1, it indicates that an ISRC1 packet was received with new contents. Once set, this bit remains high until it is cleared via new_isrc1_pckt_clr. 0 - No new ISRC1 packet received 1 - ISRC1 packet with new content received	
NEW_ACP_PCKT_RAW			R
0x79	00000000	This readback indicates the status of the new ACP packet interrupt signal. When set to 1, it indicates that an ACP packet was received with new contents. Once set, this bit remains high until it is cleared via new_acp_pckt_clr. 0 - No new ACP packet received 1 - ACP packet with new content received	

Reg	Bits	Description	
NEW_VS_INFO_RAW			R
0x79	000 <u>0</u> 0000	This readback indicates the status of the new vendor specific InfoFrame interrupt signal. When set to 1, it indicates that a vendor specific InfoFrame was received with new contents. Once set, this bit remains high until it is cleared via new_vs_info_clr. 0 - No new VS packet received 1 - VS packet with new content received	
NEW_MS_INFO_RAW			R
0x79	0000 <u>0</u> 000	This readback indicates the status of the new MPEG source InfoFrame interrupt signal. When set to 1, it indicates that an MPEG source InfoFrame was received with new contents. Once set, this bit remains high until it is cleared via new_ms_info_clr. 0 - No new MPEG source InfoFrame received 1 - MPEG source InfoFrame with new content received	
NEW_SPD_INFO_RAW			R
0x79	00000 <u>0</u> 00	This readback indicates the status of the new source product descriptor packet interrupt signal. When set to 1, it indicates that a source product descriptor packet was received with new contents. Once set, this bit remains high until it is cleared. 0 - No new SPD InfoFrame received 1 - SPD InfoFrame with new content received	
NEW_AUDIO_INFO_RAW			R
0x79	000000 <u>0</u>	This readback indicates the status of the new audio InfoFrame interrupt signal. When set to 1, it indicates that an audio InfoFrame was received with new contents. Once set, this bit remains high until it is cleared via new_audio_info_clr. 0 - No new audio InfoFrame received 1 - Audio InfoFrame with new content received	
NEW_AVI_INFO_RAW			R
0x79	000000 <u>0</u>	This readback indicates the status of the new AVI InfoFrame interrupt signal. When set to 1, it indicates that an AVI InfoFrame was received with new contents. Once set, this bit remains high until the interrupt is cleared via new_avi_info_clr. 0 - No new AVI InfoFrame received 1 - AVI InfoFrame with new content received	
NEW_ISRC2_PCKT_ST			R
0x7A	<u>0</u> 0000000	This readback indicates the latched status for the new ISRC2 packet interrupt. Once set, this bit remains high until the interrupt is cleared via new_isrc2_pckt_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No new ISRC2 packet received, interrupt not generated 1 - ISRC2 packet with new content received, interrupt generated	
NEW_ISRC1_PCKT_ST			R
0x7A	<u>0</u> 0000000	This readback indicates the latched status for the new ISRC1 packet interrupt. Once set, this bit remains high until the interrupt is cleared via new_isrc1_pckt_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No new ISRC1 packet received, interrupt not generated 1 - ISRC1 packet with new content received, interrupt generated	
NEW_ACP_PCKT_ST			R
0x7A	<u>0</u> 0000000	This readback indicates the latched status for the new ACP packet interrupt. Once set, this bit remains high until the interrupt is cleared via new_acp_pckt_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No new ACP packet received, interrupt not generated 1 - ACP packet with new content received, interrupt generated	
NEW_VS_INFO_ST			R
0x7A	000 <u>0</u> 0000	This readback indicates the latched status for the new vendor specific InfoFrame interrupt. Once set, this bit remains high until the interrupt is cleared via new_vs_info_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No new VS packet received, interrupt not generated 1 - VS packet with new content received, interrupt generated	
NEW_MS_INFO_ST			R
0x7A	0000 <u>0</u> 000	This readback indicates the latched status for the New MPEG Source InfoFrame interrupt. Once set, this bit remains high until the interrupt is cleared via new_ms_info_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No new MPEG source InfoFrame received, interrupt not generated 1 - MPEG source InfoFrame with new content received, interrupt generated	

Reg	Bits	Description	
NEW_SPD_INFO_ST			R
0x7A	00000000	This readback indicates the latched status for the new source product descriptor InfoFrame interrupt. Once set, this bit remains high until the interrupt is cleared via new_spd_info_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No new SPD InfoFrame received. Interrupt has not been generated. 1 - SPD InfoFrame with new content received, interrupt generated	
NEW_AUDIO_INFO_ST			R
0x7A	00000000	This readback indicates the latched status for the new audio InfoFrame interrupt. Once set, this bit remains high until the interrupt is cleared via new_audio_info_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No new Audio InfoFrame received, interrupt not generated 1 - Audio InfoFrame with new content received, interrupt generated	
NEW_AVI_INFO_ST			R
0x7A	00000000	This readback indicates the latched status for new_avi_info_raw. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. Once set, this bit remains high until the interrupt is cleared via new_avi_info_clr. 0 - new_avi_info_raw not changed state 1 - new_avi_info_raw changed state	
NEW_ISRC2_PCKT_CLR			SC
0x7B	00000000	This control is used to clear the new_isrc2_pckt_raw and new_isrc2_pckt_st bits. This is a self clearing bit. 0 - No function 1 - Clear new_isrc2_pckt_raw and new_isrc2_pckt_st	
NEW_ISRC1_PCKT_CLR			SC
0x7B	00000000	This control is used to clear the new_isrc1_pckt_raw and new_isrc1_pckt_st bits. This is a self clearing bit. 0 - No function 1 - Clear new_isrc1_pckt_raw and new_isrc1_pckt_st	
NEW_ACP_PCKT_CLR			SC
0x7B	00000000	This control is used to clear the new_acp_pckt_raw and new_acp_pckt_st bits. This is a self clearing bit. 0 - No function 1 - Clear new_acp_pckt_raw and new_acp_pckt_st	
NEW_VS_INFO_CLR			SC
0x7B	00000000	This control is used to clear the new_vs_info_raw and new_vs_info_st bits. This is a self clearing bit. 0 - No function 1 - Clear new_vs_info_raw and new_vs_info_st	
NEW_MS_INFO_CLR			SC
0x7B	00000000	This control is used to clear the new_ms_info_raw and new_ms_info_st bits. This is a self clearing bit. 0 - No function 1 - Clear new_ms_info_raw and new_ms_info_st	
NEW_SPD_INFO_CLR			SC
0x7B	00000000	This control is used to clear the new_spd_info_raw and new_spd_info_st bits. This is a self clearing bit. 0 - No function 1 - Clear new_spd_info_raw and new_spd_info_st	
NEW_AUDIO_INFO_CLR			SC
0x7B	00000000	This control is used to clear the new_audio_info_raw and new_audio_info_st bits. This is a self clearing bit. 0 - No function 1 - Clear new_audio_info_raw and new_audio_info_st	
NEW_AVI_INFO_CLR			SC
0x7B	00000000	This control is used to clear the new_avi_info_raw and new_avi_info_st bits. This is a self clearing bit. 0 - No function 1 - Clear new_avi_info_raw and new_avi_info_st	
NEW_ISRC2_PCKT_MB2			R/W
0x7C	00000000	This control is used to set the INT2 interrupt mask for the new ISRC2 packet interrupt. When set, the new ISRC2 interrupt triggers the INT2 interrupt and new_isrc2_st indicates the interrupt status. 0 - Disable new ISRC2 packet interrupt for INT2 1 - Enable new ISRC2 packet interrupt for INT2	

Reg	Bits	Description	
NEW_ISRC1_PCKT_MB2			R/W
0x7C	00000000	This control is used to set the INT2 interrupt mask for the new ISRC1 packet interrupt. When set, the new ISRC2 interrupt triggers the INT2 interrupt and new_isrc1_st indicates the interrupt status. 0 - Disable new ISRC1 packet interrupt for INT2 1 - Enable new ISRC1 packet interrupt for INT2	
NEW_ACP_PCKT_MB2			R/W
0x7C	00000000	This control is used to set the INT2 interrupt mask for the new ACP packet interrupt. When set, the new ACP interrupt triggers the INT2 interrupt and new_acp_st indicates the interrupt status. 0 - Disable new ACP packet interrupt for INT2 1 - Enable new ACP packet interrupt for INT2	
NEW_VS_INFO_MB2			R/W
0x7C	00000000	This control is used to set the INT2 interrupt mask for the new vendor specific InfoFrame interrupt. When set, the new vendor specific InfoFrame interrupt triggers the INT2 interrupt and new_vs_info_st indicates the interrupt status. 0 - Disable new VS InfoFrame interrupt for INT2 1 - Enable new VS InfoFrame interrupt for INT2	
NEW_MS_INFO_MB2			R/W
0x7C	00000000	This control is used to set the INT2 interrupt mask for the new MPEG source InfoFrame interrupt. When set, the new MPEG source InfoFrame interrupt triggers the INT2 interrupt and new_ms_info_st indicates the interrupt status. 0 - Disable new MS InfoFrame interrupt for INT2 1 - Enable new MS InfoFrame interrupt for INT2	
NEW_SPD_INFO_MB2			R/W
0x7C	00000000	This control is used to set the INT2 interrupt mask for the new source product descriptor InfoFrame interrupt. When set, the new source product descriptor InfoFrame interrupt triggers the INT2 interrupt and new_spd_info_st indicates the interrupt status. 0 - Disable new SPD InfoFrame interrupt for INT2 1 - Enable new SPD InfoFrame interrupt for INT2	
NEW_AUDIO_INFO_MB2			R/W
0x7C	00000000	This control is used to set the INT2 interrupt mask for the New Audio InfoFrame interrupt. When set, the new audio InfoFrame interrupt triggers the INT2 interrupt and new_audio_info_st indicates the interrupt status. 0 - Disable new audio InfoFrame interrupt for INT2 1 - Enable new audio InfoFrame interrupt for INT2	
NEW_AVI_INFO_MB2			R/W
0x7C	00000000	This control is used to set the INT2 interrupt mask for the new AVI InfoFrame detection interrupt. When set, a new AVI InfoFrame detection event causes new_avi_info_st to be set and an interrupt to be generated on INT2. 0 - Disable new AVI InfoFrame interrupt for INT2 1 - Enable new AVI InfoFrame interrupt for INT2	
NEW_ISRC2_PCKT_MB1			R/W
0x7D	00000000	This control is used to set the INT1 interrupt mask for the new ISRC2 packet interrupt. When set, the new ISRC2 interrupt triggers the INT1 interrupt and new_isrc2_st indicates the interrupt status. 0 - Disable new ISRC2 packet interrupt for INT1 1 - Enable new ISRC2 packet interrupt for INT1	
NEW_ISRC1_PCKT_MB1			R/W
0x7D	00000000	This control is used to set the INT1 interrupt mask for the new ISRC1 packet interrupt. When set, the New ISRC2 interrupt triggers the INT1 interrupt and new_isrc1_st indicates the interrupt status. 0 - Disable new ISRC1 packet interrupt for INT1 1 - Enable new ISRC1 packet interrupt for INT1	
NEW_ACP_PCKT_MB1			R/W
0x7D	00000000	This control is used to set the INT1 interrupt mask for the new ACP packet interrupt. When set, the new ACP interrupt triggers the INT1 interrupt and new_acp_st indicates the interrupt status. 0 - Disable new ACP packet interrupt for INT1 1 - Enable new ACP packet interrupt for INT1	
NEW_VS_INFO_MB1			R/W
0x7D	00000000	This control is used to set the INT1 interrupt mask for the new vendor specific InfoFrame interrupt. When set, the new vendor specific InfoFrame interrupt triggers the INT1 interrupt and new_vs_info_st indicates the interrupt status. 0 - Disable new VS InfoFrame interrupt for INT1 1 - Enable new VS InfoFrame interrupt for INT1	

Reg	Bits	Description	
NEW_MS_INFO_MB1			R/W
0x7D	00000000	This control is used to set the INT1 interrupt mask for the new MPEG source InfoFrame interrupt. When set, the new MPEG source InfoFrame interrupt triggers the INT1 interrupt and new_ms_info_st indicates the interrupt status. 0 - Disable new MPEG source InfoFrame interrupt for INT1 1 - Enable new MS InfoFrame interrupt for INT1	
NEW_SPD_INFO_MB1			R/W
0x7D	00000000	This control is used to set the INT1 interrupt mask for the new source product descriptor InfoFrame interrupt. When set, the new source product descriptor InfoFrame interrupt triggers the INT1 interrupt and new_spd_info_st indicates the interrupt status. 0 - Disable new SPD InfoFrame interrupt for INT1 1 - Enable new SPD InfoFrame interrupt for INT1	
NEW_AUDIO_INFO_MB1			R/W
0x7D	00000000	This control is used to set the INT1 interrupt mask for the new audio InfoFrame interrupt. When set, the new audio InfoFrame interrupt triggers the INT1 interrupt and new_audio_info_st indicates the interrupt status. 0 - Disable new audio InfoFrame interrupt for INT1 1 - Enable new audio InfoFrame interrupt for INT1	
NEW_AVI_INFO_MB1			R/W
0x7D	00000000	This control is used to set the INT1 interrupt mask for the new AVI InfoFrame detection interrupt. When set, a new AVI InfoFrame detection event will cause new_avi_info_st to be set and an interrupt will be generated on INT1. 0 - Disable new AVI InfoFrame interrupt for INT1 1 - Enable new AVI InfoFrame interrupt for INT1	
FIFO_NEAR_OVFL_RAW			R
0x7E	00000000	This readback indicates the status of the audio FIFO near overflow interrupt signal. When set to 1, it indicates the audio FIFO is near overflow as the number of FIFO registers containing stereo data is greater or equal to the value set in audio_fifo_almost_full_threshold. Once set, this bit will remain high until it is cleared via FIFO_NEAR_OVFL_CLR. 0 - Audio FIFO not reached high threshold defined in audio_fifo_almost_full_threshold[5:0] 1 - Audio FIFO reached high threshold defined in audio_fifo_almost_full_threshold[5:0]	
FIFO_UNDERFLO_RAW			R
0x7E	00000000	This readback indicates the status of audio FIFO underflow interrupt signal. When set to 1, it indicates the Audio FIFO read pointer has reached the write pointer causing the audio FIFO to underflow. Once set, this bit remains high until it is cleared. 0 - Audio FIFO not underflowed 1 - Audio FIFO underflowed	
FIFO_OVERFLOW_RAW			R
0x7E	00000000	This readback indicates the status of the audio FIFO overflow interrupt signal. When set to 1, it indicates the audio FIFO write pointer has reached the read pointer causing the audio FIFO to overflow. Once set, this bit remains high until it is cleared. 0 - Audio FIFO not overflowed 1 - Audio FIFO overflowed	
CTS_PASS_THRSH_RAW			R
0x7E	00000000	This readback indicates the status of the ACR CTS value exceed threshold interrupt signal. When set to 1, it indicates the CTS value of the ACR packets has exceeded the threshold set by cts_change_threshold. Once set, this bit remains high until it is cleared. 0 - Audio clock regeneration CTS value not passed threshold 1 - Audio clock regeneration CTS value changed more than threshold	
CHANGE_N_RAW			R
0x7E	00000000	This readback indicates the status of the ACR N value changed interrupt signal. Once set to 1, it indicates the N value of the ACR packets has changed. Once set, this bit remains high until it is cleared via change_n_clr. 0 - Audio clock regeneration N value not changed 1 - Audio clock regeneration N value changed	
PACKET_ERROR_RAW			R
0x7E	00000000	This readback indicates the status of the packet error interrupt signal. When set to 1, it indicates that an any packet was received with an uncorrectable EEC error in either the header or body. Once set, this bit remains high until it is cleared. 0 - No uncorrectable error detected in packet header 1 - Uncorrectable error detected in an unknown packet (error in packet header)	

Reg	Bits	Description	
AUDIO_PCKT_ERR_RAW			R
0x7E	000000 <u>00</u>	This readback indicates the status of the audio packet error interrupt signal. When set to 1, it indicates that an audio packet was received with an uncorrectable error. Once set, this bit remains high until it is cleared via <code>audio_pckt_err_clr</code> . 0 - No uncorrectable error detected in audio packets, interrupt not generated 1 - Uncorrectable error detected in audio packet, interrupt generated	
NEW_GAMUT_MDATA_RAW			R
0x7E	000000 <u>00</u>	This readback indicates the status of the new gamut metadata packet interrupt signal. When set to 1, it indicates a that a gamut metadata packet was received with new contents. Once set, this bit remains high until it is cleared via <code>new_gamut_mdata_pckt_clr</code> . 0 - No new gamut metadata packet received or no change, interrupt not generated 1 - New gamut metadata packet received, interrupt generated	
FIFO_NEAR_OVFL_ST			R
0x7F	<u>0</u> 0000000	This readback indicates the latched status for the audio FIFO near overflow interrupt. Once set, this bit remains high until the interrupt is cleared via <code>fifo_ovfl_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - Audio FIFO not reached high threshold 1 - Audio FIFO reached high threshold	
FIFO_UNDERFLO_ST			R
0x7F	<u>0</u> 0000000	This readback indicates the latched status for the audio FIFO underflow interrupt. Once set, this bit remains high until the interrupt is cleared via <code>fifo_underflo_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - Audio FIFO not underflowed 1 - Audio FIFO underflowed	
FIFO_OVERFLOW_ST			R
0x7F	<u>0</u> 0000000	This readback indicates the latched status for the audio FIFO overflow interrupt. Once set, this bit remains high until the interrupt is cleared via <code>fifo_overflow_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - Audio FIFO not overflowed 1 - Audio FIFO overflowed	
CTS_PASS_THRSH_ST			R
0x7F	000 <u>0</u> 0000	This readback indicates the latched status for the ACR CTS value exceed threshold interrupt. Once set, this bit remains high until the interrupt is cleared via <code>cts_pass_thrsh_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - Audio clock regeneration CTS value not passed the threshold 1 - Audio clock regeneration CTS value changed more than threshold	
CHANGE_N_ST			R
0x7F	0000 <u>0</u> 000	This readback indicates the latched status for the ACR N value changed interrupt. Once set, this bit remains high until the interrupt is cleared via <code>change_n_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - Audio clock regeneration N value not changed 1 - Audio clock regeneration N value changed	
PACKET_ERROR_ST			R
0x7F	00000 <u>0</u> 00	This readback indicates the latched status for the packet error interrupt. Once set, this bit remains high until the interrupt is cleared via <code>packet_error_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No uncorrectable error detected in packet header, interrupt not generated 1 - Uncorrectable error detected in unknown packet (in packet header), interrupt generated	
AUDIO_PCKT_ERR_ST			R
0x7F	00000 <u>0</u> 00	This readback indicates the latched status for the audio packet error interrupt. Once set, this bit remains high until the interrupt is cleared via <code>audio_pckt_err_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No uncorrectable error detected in audio packets, interrupt not generated 1 - Uncorrectable error detected in audio packet, interrupt generated	
NEW_GAMUT_MDATA_ST			R
0x7F	000000 <u>0</u> 0	This readback indicates the latched status for the new gamut metadata packet interrupt. Once set, this bit remains high until the interrupt is cleared via <code>new_gamut_mdata_pckt_clr</code> . This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No new gamut metadata packet received or no change, interrupt not generated 1 - New gamut metadata packet received, interrupt generated	

Reg	Bits	Description	
FIFO_NEAR_OVFL_CLR			SC
0x80	00000000	This control is used to clear the audio FIFO near overflow interrupt. This is a self clearing bit. 0 - Do not clear 1 - Clear	
FIFO_UNDERFLO_CLR			SC
0x80	00000000	This control is used to clear the audio FIFO underflow interrupt. This is a self clearing bit. 0 - Do not clear fifo_underflo_st 1 - Clear fifo_underflo_st	
FIFO_OVERFLOW_CLR			SC
0x80	00000000	This control is used to clear the audio FIFO overflow interrupt. This is a self clearing bit. 0 - Do not clear fifo_overflow_st 1 - Clear fifo_overflow_st	
CTS_PASS_THRSH_CLR			SC
0x80	00000000	This control is used to clear the ACR CTS value exceed threshold interrupt. This is a self clearing bit. 0 - Do not clear 1 - Clear cts_pass_thrsh_st	
CHANGE_N_CLR			SC
0x80	00000000	This control is used to clear the ACR N value changed interrupt. This is a self clearing bit. 0 - Do not clear change_n_st 1 - Clear change_n_st	
PACKET_ERROR_CLR			SC
0x80	00000000	This control is used to clear the packet error interrupt. This is a self clearing bit. 0 - Do not clear packet_error_st 1 - Clear packet_error_st	
AUDIO_PCKT_ERR_CLR			SC
0x80	00000000	This control is used to clear the audio packet error interrupt. This is a self clearing bit. 0 - Do not clear audio_pckt_err_st 1 - Clear audio_pckt_err_st	
NEW_GAMUT_MDATA_CLR			SC
0x80	00000000	This control is used to clear the new gamut metadata packet interrupt. This is a self clearing bit. 0 - Do not clear new_gamut_mdata_st 1 - Clear new_gamut_mdata_st	
FIFO_NEAR_OVFL_MB2			R/W
0x81	00000000	This control is used to set the INT2 interrupt mask for the audio FIFO near overflow interrupt. When set, the audio FIFO near overflow interrupt triggers the INT2 interrupt and fifo_near_ovfl_st indicates the interrupt status. 0 - Disable audio FIFO near overflow interrupt on INT2 1 - Enable audio FIFO near overflow interrupt on INT2	
FIFO_UNDERFLO_MB2			R/W
0x81	00000000	This control is used to set the INT2 interrupt mask for the audio FIFO underflow interrupt. When set, the audio FIFO underflow interrupt triggers the INT2 interrupt and fifo_underflo_st indicates the interrupt status. 0 - Disable audio FIFO underflow interrupt on INT2 1 - Enable audio FIFO underflow interrupt on INT2	
FIFO_OVERFLOW_MB2			R/W
0x81	00000000	This control is used to set the INT2 interrupt mask for the audio FIFO overflow interrupt. When set, the audio FIFO overflow interrupt triggers the INT2 interrupt and fifo_overflow_st indicates the interrupt status. 0 - Disable audio FIFO overflow interrupt on INT2 1 - Enable audio FIFO overflow interrupt on INT2	
CTS_PASS_THRSH_MB2			R/W
0x81	00000000	This control is used to set the INT2 interrupt mask for the ACR CTS value exceed threshold interrupt. When set, the ACR CTS value exceed threshold interrupt triggers the INT2 interrupt and cts_pass_thrsh_st indicates the interrupt status. 0 - Disable ACR CTS value exceed threshold interrupt on INT2 1 - Enable ACR CTS value exceed threshold interrupt on INT2	

Reg	Bits	Description	
CHANGE_N_MB2			R/W
0x81	00000000	This control is used to set the INT2 interrupt mask for the ACR N value changed interrupt. When set, the ACR N value changed interrupt triggers the INT2 interrupt and change_n_st indicates the interrupt status. 0 - Disable ACR N value changed interrupt for INT2 1 - Enable ACR N value changed interrupt for INT2	
PACKET_ERROR_MB2			R/W
0x81	00000000	This control is used to set the INT2 interrupt mask for the packet error interrupt. Once set, the audio packet error interrupt triggers the INT2 interrupt and packet_error_st indicates the interrupt status. 0 - Disable audio packet error interrupt for INT2 1 - Enable packet error interrupt for INT2	
AUDIO_PCKT_ERR_MB2			R/W
0x81	00000000	This control is used to set the INT2 interrupt mask for the audio packet error interrupt. When set, the audio packet error interrupt triggers the INT2 interrupt and audio_pckt_err_st indicates the interrupt status. 0 - Disable audio packet error interrupt for INT2 1 - Enable audio packet error interrupt for INT2	
NEW_GAMUT_MDATA_MB2			R/W
0x81	00000000	This control is used to set the INT2 interrupt mask for the new gamut metadata packet interrupt. When set, the new gamut metadata packet interrupt triggers the INT2 interrupt and new_gamut_mdata_pckt_st indicates the interrupt status. 0 - Disable new gamut metadata InfoFrame interrupt for INT2 1 - Enable new gamut metadata InfoFrame interrupt for INT2	
FIFO_NEAR_OVFL_MB1			R/W
0x82	00000000	This control is used to set the INT1 interrupt mask for the audio FIFO near overflow interrupt. When set, the audio FIFO overflow interrupt triggers the INT1 interrupt and fifo_near_ovfl_st indicates the interrupt status. 0 - Disable audio FIFO overflow interrupt on INT1 1 - Enable audio FIFO overflow interrupt on INT1	
FIFO_UNDERFLO_MB1			R/W
0x82	00000000	This control is used to set the INT1 interrupt mask for the audio FIFO overflow interrupt. When set, the audio FIFO overflow interrupt triggers the INT1 interrupt and fifo_underflo_st indicates the interrupt status. 0 - Disable audio FIFO overflow interrupt on INT1 1 - Enable audio FIFO overflow interrupt on INT1	
FIFO_OVERFLOW_MB1			R/W
0x82	00000000	This control is used to set the INT1 interrupt mask for the audio FIFO overflow interrupt. When set, the audio FIFO overflow interrupt triggers the INT1 interrupt and fifo_overflow_st indicates the interrupt status. 0 - Disable audio FIFO overflow interrupt on INT1 1 - Enable audio FIFO overflow interrupt on INT1	
CTS_PASS_THRSH_MB1			R/W
0x82	00000000	This control is used to set the INT1 interrupt mask for the ACR CTS value exceed threshold interrupt. When set, the ACR CTS value exceed threshold interrupt triggers the INT1 interrupt and cts_pass_thrsh_st indicates the interrupt status. 0 - Disable ACR CTS value exceed threshold interrupt on INT1 1 - Enable ACR CTS value exceed threshold interrupt on INT1	
CHANGE_N_MB1			R/W
0x82	00000000	This control is used to set the INT1 interrupt mask for the ACR N value changed interrupt. When set, the ACR N value changed interrupt triggers the INT1 interrupt and change_n_st indicates the interrupt status. 0 - Disable ACR N value changed interrupt for INT1 1 - Enable ACR N value changed interrupt for INT1	
PACKET_ERROR_MB1			R/W
0x82	00000000	This control is used to set the INT1 interrupt mask for the packet error interrupt. When set, the audio packet error interrupt triggers the INT1 interrupt and packet_error_st indicates the interrupt status. 0 - Disable packet error interrupt for INT1 1 - Enable packet error interrupt for INT1	
AUDIO_PCKT_ERR_MB1			R/W
0x82	00000000	This control is used to set the INT1 interrupt mask for the audio packet error interrupt. When set, the audio packet error interrupt triggers the INT1 interrupt and audio_pckt_err_st indicates the interrupt status. 0 - Disable audio packet error interrupt for INT1 1 - Enable audio packet error interrupt for INT1	

Reg	Bits	Description	
NEW_GAMUT_MDATA_MB1			R/W
0x82	00000000	This control is used to set the INT1 interrupt mask for the new gamut metadata packet interrupt. When set, the new gamut metadata packet interrupt triggers the INT1 interrupt and new_gamut_mdata_pckt_st indicates the interrupt status. 0 - Disable new gamut metadata InfoFrame interrupt for INT1 1 - Enable new gamut metadata InfoFrame interrupt for INT1	
DEEP_COLOR_CHNG_RAW			R
0x83	00000000	This readback indicates the status of deep color mode change interrupt signal. When set to 1, it indicates a change in the deep color mode has been detected. Once set, this bit remains high until it is cleared via deep_color_chng_clr. 0 - Deep color mode not changed 1 - Change in deep color triggered this interrupt	
VCLK_CHNG_RAW			R
0x83	00000000	This readback indicates the status of the video clock change interrupt signal. When set to 1, it indicates that irregular or missing pulses are detected in the TMDS clock. Once set, this bit remains high until it is cleared via vclk_chng_clr. 0 - No irregular or missing pulse detected in TMDS clock 1 - Irregular or missing pulses detected in TMDS clock triggered this interrupt	
AUDIO_MODE_CHNG_RAW			R
0x83	00000000	This readback indicates the status of the audio mode change interrupt signal. When set to 1, it indicates that the type of audio packet received has changed. The following are considered audio modes; no audio packets, Audio Sample Packet, DSD packet, HBR Packet or DST Packet. Once set, this bit will remain high until it is cleared via AUDIO_MODE_CHNG_CLR. 0 - Audio mode not changed. 1 - Audio mode changed.	
PARITY_ERROR_RAW			R
0x83	00000000	This readback indicates the status of the parity error interrupt signal. When set to 1, it indicates an audio sample packet was received with parity error. Once set, this bit remains high until it is cleared via parity_error_clr. 0 - No parity error detected in audio packets 1 - Parity error detected in audio packet	
NEW_SAMP_RT_RAW			R
0x83	00000000	This readback indicates the status of the new sampling rate interrupt signal. When set to 1, it indicates that the audio sampling frequency field in the channel status data has changed. Once set, this bit remains high until it is cleared via new_samp_rt_clr. 0 - Sampling rate bits of the channel status data on audio channel 0 not changed 1 - Sampling rate bits of the channel status data on audio channel 0 changed	
AUDIO_FLT_LINE_RAW			R
0x83	00000000	This readback indicates the status of the audio flat line interrupt signal. When set to 1, it indicates an audio sample packet was received with the flat line bit set to 1. Once set, this bit remains high until it is cleared via audio_flat_line_clr. 0 - Audio sample packet with flat line bit set not received 1 - Audio sample packet with flat line bit set received	
NEW_TMDS_FRQ_RAW			R
0x83	00000000	This readback indicates the status of the new TMDS frequency interrupt signal. When set to 1, it indicates the TMDS frequency has changed by more than the tolerance set in freqtolerance[3:0]. Once set, this bit remains high until it is cleared via new_tmds_freq_clr. 0 - TMDS frequency not changed by more than tolerance set in freqtolerance[3:0] in HDMI Map 1 - TMDS frequency changed by more than tolerance set in freqtolerance[3:0] in HDMI Map	
FIFO_NEAR_UFLO_RAW			R
0x83	00000000	This readback indicates the status of the audio FIFO near underflow interrupt signal. When set to 1, it indicates the audio FIFO near underflow as the number of FIFO registers containing stereo data less or equal to the value set in audio_fifo_almost_empty_threshold. 0 - Audio FIFO not reached low threshold defined in audio_fifo_almost_empty_threshold[5:0] 1 - Audio FIFO reached low threshold defined in audio_fifo_almost_empty_threshold[5:0]	
DEEP_COLOR_CHNG_ST			R
0x84	00000000	This readback indicates the latched status of the deep color mode change interrupt. Once set, this bit remains high until the interrupt is cleared via deep_color_chng_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - Deep color mode not changed 1 - Change in deep color detected	

Reg	Bits	Description	
VCLK_CHNG_ST			R
0x84	00000000	This readback indicates the latched status of the video clock change interrupt. Once set, this bit remains high until the interrupt is cleared via vclk_chng_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No irregular or missing pulse detected in TMDS clock 1 - Irregular or missing pulses detected in TMDS clock	
AUDIO_MODE_CHNG_ST			R
0x84	00000000	This readback indicates the latched status of the audio mode change interrupt. Once set, this bit remains high until the interrupt is cleared via audio_mode_chng_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - Audio mode not changed 1 - Audio mode changed. The following are considered audio modes; no audio, PCM, DSD, HBR and DST.	
PARITY_ERROR_ST			R
0x84	00000000	This readback indicates the latched status of the parity error interrupt. Once set, this bit remains high until the interrupt is cleared via parity_error_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No parity error detected in audio packets 1 - Parity error detected in audio packet	
NEW_SAMP_RT_ST			R
0x84	00000000	This readback indicates the latched status of the new sample rate interrupt. Once set, this bit remains high until the interrupt is cleared via new_samp_rt_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - Sampling rate bits of channel status data on audio channel 0 not changed 1 - Sampling rate bits of channel status data on audio channel 0 changed	
AUDIO_FLT_LINE_ST			R
0x84	00000000	This readback indicates the latched status of the new TMDS frequency interrupt. Once set, this bit remains high until the interrupt is cleared via new_tmds_freq_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - Audio sample packet with flat line bit set not received 1 - Audio sample packet with flat line bit set received	
NEW_TMDS_FRQ_ST			R
0x84	00000000	This readback indicates the latched status of the new TMDS frequency interrupt. Once set, this bit remains high until the interrupt is cleared via new_tmds_freq_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - TMDS frequency not changed by more than tolerance 1 - TMDS frequency changed by more than tolerance	
FIFO_NEAR_UFLO_ST			R
0x84	00000000	This readback indicates the latched status for the audio FIFO near underflow interrupt. Once set, this bit remains high until the interrupt is cleared via FIFO_UFLO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - Audio FIFO not reached low threshold 1 - Audio FIFO reached low threshold	
DEEP_COLOR_CHNG_CLR			SC
0x85	00000000	This control is used to clear the deep color mode change interrupt. This is a self clearing bit. 0 - Do not clear deep_color_chng_st 1 - Clear deep_color_chng_st	
VCLK_CHNG_CLR			SC
0x85	00000000	This control is used to clear the video clock change interrupt. This is a self clearing bit. 0 - Do not clear vclk_chng_st 1 - Clear vclk_chng_st	
AUDIO_MODE_CHNG_CLR			SC
0x85	00000000	This control is used to clear the audio mode change interrupt. This is a self clearing bit. 0 - Do not clear audio_mode_chng_st 1 - Clear audio_mode_chng_st	
PARITY_ERROR_CLR			SC
0x85	00000000	This control is used to clear the parity error interrupt. This is a self clearing bit. 0 - Do not clear 1 - Clear	

Reg	Bits	Description	
NEW_SAMP_RT_CLR			SC
0x85	00000 <u>000</u>	This control is used to clear the new sample rate interrupt. This is a self clearing bit. 0 - Do not clear new_samp_rt_st 1 - Clear new_samp_rt_st	
AUDIO_FLT_LINE_CLR			SC
0x85	00000 <u>000</u>	This control is used to clear the audio flat line interrupt. This is a self clearing bit. 0 - Do not clear 1 - Clear audio_ft_line_st	
NEW_TMDS_FREQ_CLR			SC
0x85	000000 <u>00</u>	This control is used to clear the new TMDS frequency interrupt. This is a self clearing bit. 0 - Do not clear new_tmds_freq_st 1 - Clear new_tmds_freq_st	
FIFO_NEAR_UFLO_CLR			SC
0x85	0000000 <u>0</u>	This control is used to clear the audio FIFO near underflow interrupt. This is a self clearing bit. 0 - Do not clear 1 - Clear FIFO_NEAR_UFLO_ST	
DEEP_COLOR_CHNG_MB2			R/W
0x86	0 <u>0000000</u>	This control is used to set the INT2 interrupt mask for the deep color mode change interrupt. When set, the deep color mode change interrupt triggers the INT2 interrupt and deep_color_chng_st indicates the interrupt status. 0 - Disable deep color mode change interrupt on INT2 1 - Enable deep color mode change interrupt on INT2	
VCLK_CHNG_MB2			R/W
0x86	0 <u>0000000</u>	This control is used to set the INT2 interrupt mask for the video clock change interrupt. When set, the video clock change interrupt triggers the INT2 interrupt and vclk_chng_st indicates the interrupt status. 0 - Disable video clock change interrupt on INT2 1 - Enable video clock change interrupt on INT2	
AUDIO_MODE_CHNG_MB2			R/W
0x86	00 <u>000000</u>	This control is used to set the INT2 interrupt mask for the audio mode change interrupt. When set, the audio mode change interrupt triggers the INT2 interrupt and audio_mode_chng_st indicates the interrupt status. 0 - Disable audio mode change interrupt on INT2 1 - Enable audio mode change interrupt on INT2	
PARITY_ERROR_MB2			R/W
0x86	000 <u>00000</u>	This control is used to set the INT2 interrupt mask for the parity error interrupt. When set, the parity error interrupt triggers the INT2 interrupt and parity_error_st indicates the interrupt status. 0 - Disable parity error interrupt on INT2 1 - Enable parity error interrupt on INT2	
NEW_SAMP_RT_MB2			R/W
0x86	00000 <u>000</u>	This control is used to set the INT2 interrupt mask for the new sample rate interrupt. When set, the new sample rate interrupt triggers the INT2 interrupt and new_samp_rt_st indicates the interrupt status. 0 - Disable new sample rate interrupt on INT2 1 - Enable new sample rate interrupt on INT2	
AUDIO_FLT_LINE_MB2			R/W
0x86	00000 <u>000</u>	This control is used to set the INT2 interrupt mask for the audio flat line interrupt. When set, the audio flat line interrupt triggers the INT2 interrupt and audio_ft_line_st indicates the interrupt status. 0 - Disable audio flat line interrupt on INT2 1 - Enable audio flat line interrupt on INT2	
NEW_TMDS_FREQ_MB2			R/W
0x86	000000 <u>00</u>	This control is used to set the INT2 interrupt mask for the new TMDS frequency interrupt. When set, the new TMDS frequency interrupt triggers the INT2 interrupt and new_tmds_freq_st indicates the interrupt status. 0 - Disable new TMDS frequency interrupt on INT2 1 - Enable new TMDS frequency interrupt on INT2	
FIFO_NEAR_UFLO_MB2			R/W
0x86	0000000 <u>0</u>	This control is used to set the INT2 interrupt mask for the audio FIFO near underflow interrupt. When set, the audio FIFO near underflow interrupt triggers the INT2 interrupt and fifo_near_uflo_st indicates the interrupt status. 0 - Disable audio FIFO near underflow interrupt on INT2 1 - Enable audio FIFO near underflow interrupt on INT2	

Reg	Bits	Description	
DEEP_COLOR_CHNG_MB1			R/W
0x87	00000000	This control is used to set the INT1 interrupt mask for the deep color mode change interrupt. When set, the deep color mode change interrupt triggers the INT1 interrupt and deep_color_chng_st indicates the interrupt status. 0 - Disable deep color mode change interrupt on INT1 1 - Enable deep color mode change interrupt on INT1	
VCLK_CHNG_MB1			R/W
0x87	00000000	This control is used to set the INT1 interrupt mask for the video clock change interrupt. When set, the video clock change interrupt triggers the INT1 interrupt and vclk_chng_st indicates the interrupt status. 0 - Disable video clock change interrupt on INT1 1 - Enable video clock change interrupt on INT1	
AUDIO_MODE_CHNG_MB1			R/W
0x87	00000000	This control is used to set the INT1 interrupt mask for the audio mode change interrupt. When set, the audio mode change interrupt triggers the INT1 interrupt and audio_mode_chng_st indicates the interrupt status. 0 - Disable audio mode change interrupt on INT1 1 - Enable audio mode change interrupt on INT1	
PARITY_ERROR_MB1			R/W
0x87	00000000	This control is used to set the INT1 interrupt mask for the parity error interrupt. When set, the parity error interrupt triggers the INT1 interrupt and parity_error_st indicates the interrupt status. 0 - Disable parity error interrupt on INT1 1 - Enable parity error interrupt on INT1	
NEW_SAMP_RT_MB1			R/W
0x87	00000000	This control is used to set the INT1 interrupt mask for the new sample rate interrupt. When set, the new sample rate interrupt triggers the INT1 interrupt and new_samp_rt_st indicates the interrupt status. 0 - Disable new sample rate interrupt on INT1 1 - Enable new sample rate interrupt on INT1	
AUDIO_FLT_LINE_MB1			R/W
0x87	00000000	This control is used to set the INT1 interrupt mask for the audio flat line interrupt. When set, the audio flat line interrupt triggers the INT1 interrupt and audio_flat_line_st indicates the interrupt status. 0 - Disable audio flat line interrupt on INT1 1 - Enable audio flat line interrupt on INT1	
NEW_TMDS_FRQ_MB1			R/W
0x87	00000000	This control is used to set the INT1 interrupt mask for the new TMDS frequency interrupt. When set, the new TMDS frequency interrupt triggers the INT1 interrupt and new_tmds_freq_st indicates the interrupt status. 0 - Disable new TMDS frequency interrupt on INT1 1 - Enable new TMDS frequency interrupt on INT1	
FIFO_NEAR_UFLO_MB1			R/W
0x87	00000000	This control is used to set the INT1 interrupt mask for the audio FIFO near underflow interrupt. When set, the audio FIFO near underflow interrupt triggers the INT1 interrupt and fifo_near_uflo_st indicates the interrupt status. 0 - Disable audio FIFO near underflow interrupt on INT1 1 - Enable audio FIFO near underflow interrupt on INT1	
MS_INF_CKS_ERR_RAW			R
0x88	00000000	This readback indicates the status of the MPEG source InfoFrame checksum error interrupt signal. When set to 1, it indicates that a checksum error was detected for an MPEG source InfoFrame. Once set, this bit remains high until it is cleared via ms_inf_ck_clr. 0 - No MPEG source InfoFrame checksum error occurred 1 - MPEG source InfoFrame checksum error occurred	
SPD_INF_CKS_ERR_RAW			R
0x88	00000000	This readback displays the status of the SPD InfoFrame checksum error interrupt signal. When set to 1, it indicates that a checksum error was detected for an SPD InfoFrame. Once set, this bit remains high until it is cleared via spd_inf_cks_err_clr. 0 - No SPD InfoFrame checksum error occurred 1 - SPD InfoFrame checksum error occurred	
AUD_INF_CKS_ERR_RAW			R
0x88	00000000	This readback displays the status of the audio InfoFrame checksum error interrupt signal. When set to 1, it indicates that a checksum error was detected for an audio InfoFrame. Once set, this bit remains high until it is cleared via audio_inf_cks_err_clr. 0 - No audio InfoFrame checksum error occurred 1 - Audio InfoFrame checksum error occurred	

Reg	Bits	Description	
AVI_INF_CKS_ERR_RAW			R
0x88	000 <u>0</u> 0000	This readback displays the status of the AVI InfoFrame checksum error interrupt signal. When set to 1, it indicates that a checksum error was detected for an AVI InfoFrame. Once set, this bit remains high until it is cleared via avi_inf_cks_err_clr. 0 - No AVI InfoFrame checksum error occurred 1 - An AVI InfoFrame checksum error occurred	
AKSV_UPDATE_A_RAW			R
0x88	0000 <u>0</u> 000	Status of Port A AKSV update interrupt signal. When set to 1, it indicates that transmitter has written its AKSV into HDCP registers for Port A. Once set, this bit remains high until it is cleared via aksv_update_a_clr. 0 - No AKSV updates on Port A 1 - Detected a write access to the AKSV register on Port A	
AKSV_UPDATE_B_RAW			R
0x88	0000 <u>0</u> 00	This readback displays the status of the Port B AKSV update interrupt signal. When set to 1, it indicates that the transmitter has written its AKSV into the HDCP registers for Port B. Once set, this bit remains high until it is cleared via aksv_update_b_clr. 0 - No AKSV updates on Port B 1 - Detected write access to AKSV register on Port B	
AKSV_UPDATE_C_RAW			R
0x88	0000 <u>0</u> 0	This readback displays the status of the Port C AKSV update interrupt signal. When set to 1, it indicates that the transmitter has written its AKSV into the HDCP registers for Port C. Once set, this bit remains high until it is cleared via aksv_update_c_clr. 0 - No AKSV updates on Port C 1 - Detected write access to AKSV register on Port C	
AKSV_UPDATE_D_RAW			R
0x88	0000 <u>0</u> 0	This readback displays the status of the Port D AKSV update interrupt signal. When set to 1, it indicates that the transmitter has written its AKSV into the HDCP registers for Port D. Once set, this bit remains high until it is cleared via aksv_update_d_clr. 0 - No AKSV updates on Port D 1 - Detected write access to AKSV register on Port D	
MS_INF_CKS_ERR_ST			R
0x89	<u>0</u> 0000000	This readback indicates the latched status of the MPEG Source InfoFrame checksum error interrupt. Once set, this bit remains high until the interrupt is cleared via ms_inf_cks_err_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No change in MPEG source InfoFrame checksum error 1 - MPEG source InfoFrame checksum error triggered this interrupt	
SPD_INF_CKS_ERR_ST			R
0x89	<u>0</u> 0000000	This readback indicates the latched status of the SPD InfoFrame checksum error interrupt. Once set, this bit remains high until the interrupt is cleared via spd_inf_cks_err_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No change in SPD InfoFrame checksum error 1 - SPD InfoFrame checksum error triggered this interrupt	
AUD_INF_CKS_ERR_ST			R
0x89	<u>0</u> 0000000	This readback indicates the latched status of the audio InfoFrame checksum error interrupt. Once set, this bit remains high until the interrupt is cleared via audio_inf_cks_err_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No change in audio InfoFrame checksum error 1 - Audio InfoFrame checksum error triggered this interrupt	
AVI_INF_CKS_ERR_ST			R
0x89	<u>0</u> 0000000	This readback indicates the latched status of the AVI InfoFrame checksum error interrupt. Once set, this bit remains high until the interrupt is cleared via avi_inf_cks_err_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No change in AVI InfoFrame checksum error 1 - AVI InfoFrame checksum error triggered this interrupt	
AKSV_UPDATE_A_ST			R
0x89	0000 <u>0</u> 00	This readback indicates the latched status of Port A AKSV update interrupt. Once set, this bit remains high until the interrupt is cleared via aksv_update_a_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No AKSV updates on Port A 1 - Detected a write access to the AKSV register on Port A	

Reg	Bits	Description	
AKSV_UPDATE_B_ST			R
0x89	00000 <u>0</u> 00	This readback indicates the latched status of Port B AKSV update interrupt. Once set, this bit remains high until the interrupt is cleared via (No Suggestions). This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No AKSV updates on Port B 1 - Detected a write access to the AKSV register on Port B	
AKSV_UPDATE_C_ST			R
0x89	000000 <u>0</u> 0	This readback indicates the latched status of Port C AKSV update interrupt. Once set, this bit remains high until the interrupt is cleared via aksv_update_c_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit 0 - No AKSV updates on Port C 1 - Detected a write access to the AKSV register on Port C	
AKSV_UPDATE_D_ST			R
0x89	0000000 <u>0</u>	This readback indicates the latched status of Port D AKSV update interrupt. Once set, this bit remains high until the interrupt is cleared via aksv_update_d_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No AKSV updates on Port D 1 - Detected a write access to AKSV register on Port D	
MS_INF_CKS_ERR_CLR			SC
0x8A	<u>0</u> 0000000	This control is used to clear the MPEG source InfoFrame checksum error interrupt. This is a self clearing bit. 0 - Do not clear ms_inf_cks_err_st 1 - Clear ms_inf_cks_err_st	
SPD_INF_CKS_ERR_CLR			SC
0x8A	<u>0</u> 0000000	This control is used to clear the SPD InfoFrame checksum error interrupt. This is a self clearing bit. 0 - Do not clear spd_inf_cks_err_st 1 - Clear spd_inf_cks_err_st	
AUD_INF_CKS_ERR_CLR			SC
0x8A	<u>0</u> 0000000	This control is used to clear the Audio InfoFrame checksum error interrupt. This is a self clearing bit. 0 - Do not clear 1 - Clear	
AVI_INF_CKS_ERR_CLR			SC
0x8A	<u>0</u> 0000000	This control is used to clear the AVI InfoFrame checksum error interrupt. This is a self clearing bit. 0 - Do not clear avi_inf_cks_err_st 1 - Clear avi_inf_cks_err_st	
AKSV_UPDATE_A_CLR			SC
0x8A	0000 <u>0</u> 000	This control is used to clear the Port A AKSV update interrupt. This is a self clearing bit. 0 - Do not clear 1 - Clear aksv_update_a_st	
AKSV_UPDATE_B_CLR			SC
0x8A	00000 <u>0</u> 00	This control is used to clear the Port B AKSV update interrupt. This is a self clearing bit. 0 - Do not clear aksv_update_b_st 1 - Clear aksv_update_b_st	
AKSV_UPDATE_C_CLR			SC
0x8A	000000 <u>0</u> 0	This control is used to clear the Port C AKSV update interrupt. This is a self clearing bit. 0 - Do not clear AKSV_update_C_st 1 - Clear AKSV_update_C_st	
AKSV_UPDATE_D_CLR			SC
0x8A	0000000 <u>0</u>	This control is used to clear the Port D AKSV update interrupt. This is a self clearing bit. 0 - Do not clear aksv_update_d_st 1 - Clear aksv_update_d_st	
MS_INF_CKS_ERR_MB2			R/W
0x8B	<u>0</u> 0000000	This control is used to set the INT2 interrupt mask for the MPEG source InfoFrame checksum error interrupt. When set, the MPEG source InfoFrame checksum error interrupt triggers the INT2 interrupt and ms_inf_cks_err_st indicates the interrupt status. 0 - Disable MPEG source InfoFrame checksum error interrupt on INT2 1 - Enable MPEG source InfoFrame checksum error interrupt on INT2	

Reg	Bits	Description	
SPD_INF_CKS_ERR_MB2			R/W
0x8B	00000000	This control is used to set the INT2 interrupt mask for the SPD InfoFrame checksum error interrupt. When set, the SPD InfoFrame checksum error interrupt triggers the INT2 interrupt and spd_inf_cks_err_st indicates the interrupt status. 0 - Disable SPD InfoFrame checksum error interrupt on INT2 1 - Enable SPD InfoFrame checksum error interrupt on INT2	
AUD_INF_CKS_ERR_MB2			R/W
0x8B	00000000	This control is used to set the INT2 interrupt mask for the audio InfoFrame checksum error interrupt. When set, the audio InfoFrame checksum error interrupt triggers the INT2 interrupt and audio_inf_cks_err_st indicates the interrupt status. 0 - Disable audio InfoFrame checksum error interrupt on INT2 1 - Enable audio InfoFrame checksum error interrupt on INT2	
AVI_INF_CKS_ERR_MB2			R/W
0x8B	00000000	This control is used to set the INT2 interrupt mask for the AVI InfoFrame checksum error interrupt. When set, the AVI InfoFrame checksum error interrupt triggers the INT2 interrupt and avi_inf_cks_err_st indicates the interrupt status. 0 - Disable AVI InfoFrame checksum error interrupt on INT2 1 - Enable AVI InfoFrame checksum error interrupt on INT2	
AKSV_UPDATE_A_MB2			R/W
0x8B	00000000	This control is used to set the INT2 interrupt mask for the Port A AKSV update interrupt. When set, the Port A AKSV update interrupt triggers the INT2 interrupt and aksv_update_a_st indicates the interrupt status. 0 - Disable Port A AKSV update interrupt on INT2 1 - Enable Port A AKSV update interrupt on INT2	
AKSV_UPDATE_B_MB2			R/W
0x8B	00000000	This control is used to set the INT2 interrupt mask for the Port B AKSV update interrupt. When set, the Port B AKSV update interrupt triggers the INT2 interrupt and aksv_update_b_st indicates the interrupt status. 0 - Disable Port B AKSV update interrupt on INT2 1 - Enable Port B AKSV update interrupt on INT2	
AKSV_UPDATE_C_MB2			R/W
0x8B	00000000	This control is used to set the INT2 interrupt mask for the Port C AKSV update interrupt. When set, the Port C AKSV update interrupt triggers the INT2 interrupt and aksv_update_c_st indicates the interrupt status. 0 - Disable Port C AKSV update interrupt on INT2 1 - Enable Port C AKSV update interrupt on INT2	
AKSV_UPDATE_D_MB2			R/W
0x8B	00000000	This control is used to set the INT2 interrupt mask for the Port D AKSV update interrupt. When set, the Port D AKSV update interrupt triggers the INT2 interrupt and aksv_update_d_st indicates the interrupt status. 0 - Disable Port D AKSV update interrupt on INT2 1 - Enable Port D AKSV update interrupt on INT2	
MS_INF_CKS_ERR_MB1			R/W
0x8C	00000000	This control is used to set the INT1 interrupt mask for the MPEG Source InfoFrame checksum error interrupt. When set, the MPEG Source InfoFrame checksum error interrupt triggers the INT1 interrupt and ms_inf_cks_err_st indicates the interrupt status. 0 - Disable MPEG source InfoFrame checksum error interrupt on INT1 1 - Enable MPEG source InfoFrame checksum error interrupt on INT1	
SPD_INF_CKS_ERR_MB1			R/W
0x8C	00000000	This control is used to set the INT1 interrupt mask for the SPD InfoFrame checksum error interrupt. When set, the SPD InfoFrame checksum error interrupt triggers the INT1 interrupt and spd_inf_cks_err_st indicates the interrupt status. 0 - Disable SPD InfoFrame checksum error interrupt on INT1 1 - Enable SPD InfoFrame checksum error interrupt on INT1	
AUD_INF_CKS_ERR_MB1			R/W
0x8C	00000000	This control is used to set the INT1 interrupt mask for the audio InfoFrame checksum error interrupt. When set, the audio InfoFrame checksum error interrupt triggers the INT1 interrupt and audio_inf_cks_err_st indicates the interrupt status. 0 - Disable audio InfoFrame checksum error interrupt on INT1 1 - Enable audio InfoFrame checksum error interrupt on INT1	
AVI_INF_CKS_ERR_MB1			R/W
0x8C	00000000	This control is used to set the INT1 interrupt mask for the AVI InfoFrame checksum error interrupt. When set, the AVI InfoFrame checksum error interrupt triggers the INT1 interrupt and avi_inf_cks_err_st indicates the interrupt status. 0 - Disable AVI InfoFrame checksum error interrupt on INT1 1 - Enable AVI InfoFrame checksum error interrupt on INT1	

Reg	Bits	Description	
AKSV_UPDATE_A_MB1			R/W
0x8C	0000 <u>0</u> 000	This control is used to set the INT1 interrupt mask for the Port A AKSV update interrupt. When set, the Port A AKSV update interrupt triggers the INT1 interrupt and aksv_update_a_st indicates the interrupt status. 0 - Disable Port A AKSV update interrupt on INT1 1 - Enable Port A AKSV update interrupt on INT1	
AKSV_UPDATE_B_MB1			R/W
0x8C	0000 <u>0</u> 000	This control is used to set the INT1 interrupt mask for the Port B AKSV update interrupt. When set, the Port B AKSV update interrupt triggers the INT1 interrupt and aksv_update_b_st indicates the interrupt status. 0 - Disable Port B AKSV update interrupt on INT1 1 - Enable Port B AKSV update interrupt on INT1	
AKSV_UPDATE_C_MB1			R/W
0x8C	0000 <u>0</u> 00	This control is used to set the INT1 interrupt mask for the Port C AKSV update interrupt. When set, the Port C AKSV update interrupt triggers the INT1 interrupt and aksv_update_c_st indicates the interrupt status. 0 - Disable Port C AKSV update interrupt on INT1 1 - Enable Port C AKSV update interrupt on INT1	
AKSV_UPDATE_D_MB1			R/W
0x8C	0000 <u>0</u> 00	This control is used to set the INT1 interrupt mask for the Port D AKSV update interrupt. When set, the Port D AKSV update interrupt triggers the INT1 interrupt and aksv_update_d_st indicates the interrupt status. 0 - Disable Port D AKSV update interrupt on INT1 1 - Enable Port D AKSV update interrupt on INT1	
RI_EXPIRED_A_RAW			R
0x8D	<u>0</u> 0000000	This readback indicates the status of the Port A Ri expired interrupt signal. When set to 1, it indicates that HDCP cipher Ri value for Port A expired. Once set, this bit remains high until it is cleared via ri_expired_a_clr. 0 - No Ri expired on Port A 1 - Ri expired on Port A	
RI_EXPIRED_B_RAW			R
0x8D	<u>0</u> 0000000	This readback indicates the status of the Port B Ri expired interrupt signal. When set to 1, it indicates that HDCP cipher Ri value for Port B expired. Once set, this bit remains high until it is cleared via ri_expired_b_clr. 0 - No Ri expired on Port B 1 - Ri expired on Port B	
RI_EXPIRED_C_RAW			R
0x8D	<u>0</u> 0000000	Status of Port C Ri expired interrupt signal. When set to 1, it indicates that HDCP cipher Ri value for Port C expired. Once set, this bit remains high until it is cleared via ri_expired_c_clr. 0 - No Ri expired on Port C 1 - Ri expired on Port C	
RI_EXPIRED_D_RAW			R
0x8D	<u>0</u> 0000000	This readback indicates the status of the Port D Ri expired interrupt signal. When set to 1, it indicates that HDCP cipher Ri value for Port D expired. Once set, this bit remains high until it is cleared via ri_expired_a_clr. 0 - No Ri expired on Port D 1 - Ri expired on Port D	
BG_MEAS_DONE_RAW			R
0x8D	0000 <u>0</u> 00	This readback indicates the status of the background port measurement completed interrupt signal. When set to 1, it indicates that measurements of the TMDS frequency and video parameters on the selected background port are completed. 0 - Measurements of TMDS frequency and video parameters of background port not finished or not requested. 1 - Measurements of TMDS frequency and video parameters of background port ready	
VS_INF_CKS_ERR_RAW			R
0x8D	0000 <u>0</u> 00	This readback indicates the status of the vendor specific InfoFrame checksum error interrupt signal. When set to 1, it indicates that a checksum error was detected for a vendor specific InfoFrame. Once set, this bit remains high until it is cleared. 0 - No vendor specific InfoFrame checksum error occurred 1 - Vendor specific InfoFrame checksum error occurred	
RI_EXPIRED_A_ST			R
0x8E	<u>0</u> 0000000	This readback indicates the latched status of the Port A Ri expired interrupt. Once set, this bit remains high until the interrupt is cleared via ri_expired_a_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No Ri expired on Port A 1 - Ri expired on Port A	

Reg	Bits	Description	
RI_EXPIRED_B_ST			R
0x8E	00000000	This readback indicates the latched status of the Port B Ri expired interrupt. Once set, this bit remains high until the interrupt is cleared via ri_expired_b_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No Ri expired on Port B 1 - Ri expired on Port B	
RI_EXPIRED_C_ST			R
0x8E	00000000	This readback indicates the latched status of the Port C Ri expired interrupt. Once set, this bit remains high until the interrupt is cleared via ri_expired_c_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No Ri expired on Port C 1 - Ri expired on Port C	
RI_EXPIRED_D_ST			R
0x8E	00000000	This readback indicates the latched status of the Port D Ri expired interrupt. Once set, this bit remains high until the interrupt is cleared via ri_expired_a_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No Ri expired on Port D 1 - Ri expired on Port D	
BG_MEAS_DONE_ST			R
0x8E	00000000	This readback indicates the latched status of the background port measurement completed interrupt. Once set, this bit remains high until the interrupt is cleared via bg_meas_done_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - Measurements of TMDS frequency and video parameters of background port not finished or not requested. 1 - Measurements of TMDS frequency and video parameters of background port ready	
VS_INF_CKS_ERR_ST			R
0x8E	00000000	This readback indicates the latched status of vendor specific InfoFrame checksum error interrupt. Once set, this bit remains high until the interrupt is cleared via vs_inf_cks_err_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No change in vendor specific InfoFrame checksum error 1 - Vendor specific InfoFrame checksum error triggered this interrupt	
RI_EXPIRED_A_CLR			SC
0x8F	00000000	This control is used to clear the Port A Ri expired interrupt. This is a self clearing bit. 0 - Do not clear ri_expired_a_st 1 - Clear ri_expired_a_st	
RI_EXPIRED_B_CLR			SC
0x8F	00000000	This control is used to clear the Port B Ri expired interrupt. This is a self clearing bit. 0 - Do not clear ri_expired_b_st 1 - Clear ri_expired_b_st	
RI_EXPIRED_C_CLR			SC
0x8F	00000000	This control is used to clear the Port C Ri expired interrupt. This is a self clearing bit. 0 - Do not clear ri_expired_c_st 1 - Clear ri_expired_c_st	
RI_EXPIRED_D_CLR			SC
0x8F	00000000	This control is used to clear the Port D Ri expired interrupt. This is a self clearing bit. 0 - Do not clear ri_expired_d_st 1 - Clear ri_expired_d_st	
BG_MEAS_DONE_CLR			SC
0x8F	00000000	This control is used to clear the background port measurement completed interrupt. This is a self clearing bit. 0 - Do not clear bg_meas_done_st 1 - Clear bg_meas_done_st	
VS_INF_CKS_ERR_CLR			SC
0x8F	00000000	This control is used to clear the vendor specific InfoFrame checksum error interrupt. This is a self clearing bit. 0 - Do not clear 1 - Clear vs_inf_cks_err_st	

Reg	Bits	Description	
RI_EXPIRED_A_MB2			R/W
0x90	00000000	This control is used to set the INT2 interrupt mask for the Port A Ri expired interrupt. When set, the Port A Ri expired interrupt triggers the INT2 interrupt and ri_expired_a_st indicates the interrupt status. 0 - Disable Port A Ri expired interrupt on INT2 1 - Enable Port A Ri expired interrupt on INT2	
RI_EXPIRED_B_MB2			R/W
0x90	00000000	This control is used to set the INT2 interrupt mask for the Port B Ri expired interrupt. When set, the Port B Ri expired interrupt triggers the INT2 interrupt and ri_expired_b_st indicates the interrupt status. 0 - Disable Port B Ri expired interrupt on INT2 1 - Enable Port B Ri expired interrupt on INT2	
RI_EXPIRED_C_MB2			R/W
0x90	00000000	This control is used to set the INT2 interrupt mask for the Port C Ri expired interrupt. When set, the Port C Ri expired interrupt triggers the INT2 interrupt and ri_expired_c_st indicates the interrupt status. 0 - Disable Port C Ri expired interrupt on INT2 1 - Enable Port C Ri expired interrupt on INT2	
RI_EXPIRED_D_MB2			R/W
0x90	00000000	This control is used to set the INT2 interrupt mask for the Port D Ri expired interrupt. When set, the Port D Ri expired interrupt triggers the INT2 interrupt and ri_expired_d_st indicates the interrupt status. 0 - Disable Port D Ri expired interrupt on INT2 1 - Enable Port D Ri expired interrupt on INT2	
BG_MEAS_DONE_MB2			R/W
0x90	00000000	This control is used to set the INT2 interrupt mask for the background port measurement completed interrupt. When set, the background port measurement completed interrupt triggers the INT2 interrupt and bg_meas_done_st indicates the interrupt status. 0 - Disable background port measurement completed interrupt on INT2 1 - Enable background port measurement completed interrupt on INT2	
VS_INF_CKS_ERR_MB2			R/W
0x90	00000000	This control is used to set the INT2 interrupt mask for the vendor specific InfoFrame checksum error interrupt. When set, the vendor specific InfoFrame checksum error interrupt triggers the INT2 interrupt and vs_inf_cks_err_st indicates the interrupt status. 0 - Disable vendor specific InfoFrame checksum error interrupt on INT2 1 - Enable vendor specific InfoFrame checksum error interrupt on INT2	
RI_EXPIRED_A_MB1			R/W
0x91	00000000	This control is used to set the INT1 interrupt mask for the Port A Ri expired interrupt. When set, the Port A AKSV update interrupt triggers the INT1 interrupt and ri_expired_a_st indicates the interrupt status. 0 - Disable Port A Ri expired interrupt on INT1 1 - Enable Port A Ri expired interrupt on INT1	
RI_EXPIRED_B_MB1			R/W
0x91	00000000	This control is used to set the INT1 interrupt mask for the Port B Ri expired interrupt. When set, the Port B AKSV update interrupt triggers the INT1 interrupt and ri_expired_b_st indicates the interrupt status. 0 - Disable Port B Ri expired interrupt on INT1 1 - Enable Port B Ri expired interrupt on INT1	
RI_EXPIRED_C_MB1			R/W
0x91	00000000	This control is used to set the INT1 interrupt mask for the Port C Ri expired interrupt. When set, the Port C AKSV update interrupt triggers the INT1 interrupt and ri_expired_c_st indicates the interrupt status. 0 - Disable Port C Ri expired interrupt on INT1 1 - Enable Port C Ri expired interrupt on INT1	
RI_EXPIRED_D_MB1			R/W
0x91	00000000	This control is used to set the INT1 interrupt mask for the Port D Ri expired interrupt. When set, the Port D AKSV update interrupt triggers the INT1 interrupt and ri_expired_d_st indicates the interrupt status. 0 - Disable Port D Ri expired interrupt on INT1 1 - Enable Port D Ri expired interrupt on INT1	
BG_MEAS_DONE_MB1			R/W
0x91	00000000	This control is used to set the INT1 interrupt mask for the background port measurement completed interrupt. When set, the background port measurement completed interrupt triggers the INT1 interrupt and bg_meas_done_st indicates the interrupt status. 0 - Disable background port measurement completed interrupt on INT1 1 - Enable background port measurement completed interrupt on INT1	

Reg	Bits	Description	
VS_INF_CKS_ERR_MB1			R/W
0x91	00000000	This control is used to set the INT1 interrupt mask for the vendor specific InfoFrame checksum error interrupt. When set, the vendor specific InfoFrame checksum error interrupt triggers the INT1 interrupt and vs_inf_cks_err_st indicates the interrupt status. 0 - Disable vendor specific checksum error interrupt on INT1 1 - Enable vendor specific checksum error interrupt on INT1	
SDP_STD_CHANGED_RAW			R
0x9C	00000000	This readback indicates the raw status of the SDP standard changed signal. 1 - SDP auto detect result changed 0 - No change on SDP auto detect result	
SDP_BURST_LOCKED_RAW			R
0x9C	00000000	This readback indicates the raw status of the SDP burst lock signal. 1 - SDP color locked 0 - SDP not color locked	
SDP_VIDEO_DETECTED_RAW			R
0x9C	00000000	This readback indicates the raw status of the video detected signal. 1 - Video detected at SDP input 0 - Video not detected at SDP input	
SDP_STD_CHANGED_ST			R
0x9D	00000000	This readback indicates the latched status for the SDP standard changed interrupt signal. Once set, this bit remains high until the interrupt is cleared via sdp_std_changed_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No change, interrupt not generated 1 - sdp_std_changed_raw changed and generated interrupt	
SDP_BURST_LOCKED_ST			R
0x9D	00000000	This readback indicates the latched status for the SDP burst lock interrupt signal. Once set, this bit remains high until the interrupt is cleared via sdp_burst_locked_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No change, interrupt not generated 1 - sdp_burst_locked_raw changed and generated interrupt	
SDP_VIDEO_DETECTED_ST			R
0x9D	00000000	This readback indicates the latched status for the SDP video detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via sdp_video_detected_clr. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. 0 - No change, interrupt not generated 1 - sdp_video_detected_raw changed and generated interrupt	
SDP_STD_CHANGED_CLR			SC
0x9E	00000000	This control is used to clear the SDP standard detection change interrupt. This is a self clearing bit. 0 - Do not clear sdp_std_changed_st 1 - Clear sdp_std_changed_st	
SDP_BURST_LOCKED_CLR			SC
0x9E	00000000	This control is used to clear the SDP burst lock interrupt. This is a self clearing bit. 0 - Do not clear sdp_burst_locked_st 1 - Clear sdp_burst_locked_st	
SDP_VIDEO_DETECTED_CLR			SC
0x9E	00000000	This control is used to clear the SDP video detected interrupt. This is a self clearing bit. 0 - Do not clear sdp_video_detected_st 1 - Clear sdp_video_detected_st	
SDP_STD_CHANGED_MB2			R/W
0x9F	00000000	This control is used to set the INT2 interrupt mask for the SDP standard detection change interrupt. When set, the SDP standard detection change interrupt triggers the INT2 interrupt and sdp_std_changed_st indicates the interrupt status. 0 - Disable SDP standard detection change interrupt on INT2 1 - Enable SDP standard detection change interrupt on INT2	

Reg	Bits	Description	
SDP_BURST_LOCKED_MB2			R/W
0x9F	000000 <u>00</u>	This control is used to set the INT2 interrupt mask for the SDP burst lock interrupt. When set, the SDP burst lock interrupt triggers the INT2 interrupt and sdp_burst_lock_st indicates the interrupt status. 0 - Disable SDP burst lock interrupt on INT2 1 - Enable SDP burst lock interrupt on INT2	
SDP_VIDEO_DETECTED_MB2			R/W
0x9F	000000 <u>00</u>	This control is used to set the INT2 interrupt mask for the SDP video detected interrupt. When set, the SDP video detected interrupt triggers the INT2 interrupt and sdp_video_detected_st indicates the interrupt status. 0 - Disable SDP video detected interrupt on INT2 1 - Enable SDP video detected interrupt on INT2	
SDP_STD_CHANGED_MB1			R/W
0xA0	0000 <u>0000</u>	This control is used to set the INT1 interrupt mask for the SDP standard detection change interrupt. When set, the SDP standard detection change interrupt triggers the INT1 interrupt and sdp_std_changed_st indicates the interrupt status. 0 - Disable SDP standard detection change interrupt on INT1 1 - Enable SDP standard detection change interrupt on INT1	
SDP_FIFO_CRISIS_MB1			R/W
0xA0	0000 <u>0000</u>	This control is used to set the INT1 interrupt mask for the SDP FIFO crisis interrupt. When set, the SDP FIFO crisis interrupt triggers the INT1 interrupt and sdp_fifo_crisis_st indicates the interrupt status. 0 - Disable SDP FIFO crisis interrupt on INT1 1 - Enable SDP FIFO crisis interrupt on INT1	
SDP_BURST_LOCKED_MB1			R/W
0xA0	0000 <u>0000</u>	This control is used to set the INT1 interrupt mask for the SDP burst lock interrupt. When set, the SDP burst lock interrupt triggers the INT1 interrupt and sdp_burst_lock_st indicates the interrupt status. 0 - Disable SDP burst lock interrupt on INT1 1 - Enable SDP burst lock interrupt on INT1	
SDP_VIDEO_DETECTED_MB1			R/W
0xA0	000000 <u>00</u>	This control is used to set the INT1 interrupt mask for the SDP video detected interrupt. When set, the SDP video detected interrupt triggers the INT1 interrupt and sdp_video_detected_st indicates the interrupt status. 0 - Disable SDP video detected interrupt on INT1 1 - Enable SDP video detected interrupt on INT1	
ARC_PWRDN_D[1]			R/W
0xAC	0000 <u>1111</u>	This control is used to power down the ARC transmitter. 0 - Power up ARC Tx channel D 1 - Power down ARC Tx channel D	
ARC_PWRDN_C[1]			R/W
0xAC	0000 <u>1111</u>	This control is used to power down the ARC transmitter. 0 - Power up ARC Tx channel C 1 - Power down ARC Tx channel C	
ARC_PWRDN_B[1]			R/W
0xAC	0000 <u>1111</u>	This control is used to power down the ARC transmitter. 0 - Power up ARC Tx channel B 1 - Power down ARC Tx channel B	
ARC_PWRDN_A[1]			R/W
0xAC	0000 <u>1111</u>	This control is used to power down the ARC transmitter. 0 - Power up ARC Tx channel A 1 - Power down ARC Tx channel A	
INV_SPDIF_IN_D			R/W
0xAD	<u>0</u> 0000000	This control is used to invert the SPDIF input to the ARC transmitter. 1 - Invert SPDIF input to ARC Tx channel D	
INV_SPDIF_IN_C			R/W
0xAD	<u>0</u> 0000000	This control is used to invert the SPDIF input to the ARC transmitter. 1 - Invert SPDIF input to ARC Tx channel C	
INV_SPDIF_IN_B			R/W
0xAD	<u>0</u> 0000000	This control is used to invert the SPDIF input to the ARC transmitter. 1 - Invert SPDIF input to ARC Tx channel B	

Reg	Bits	Description	
INV_SPDIF_IN_A			R/W
0xAD	000 <u>0</u> 0000	This control is used to invert the SPDIF input to the ARC transmitter. 1 - Invert SPDIF input to ARC Tx channel A	
ZERO_SPDIF_IN_D			R/W
0xAD	0000 <u>0</u> 000	This control is used to zero the SPDIF input to the ARC transmitter. 1 - Zero SPDIF input to ARC Tx channel D	
ZERO_SPDIF_IN_C			R/W
0xAD	00000 <u>0</u> 00	This control is used to zero the SPDIF input to the ARC transmitter. 1 - Zero SPDIF input to ARC Tx channel C	
ZERO_SPDIF_IN_B			R/W
0xAD	000000 <u>0</u> 0	This control is used to zero the SPDIF input to the ARC transmitter. 1 - Zero SPDIF input to ARC Tx channel B	
ZERO_SPDIF_IN_A			R/W
0xAD	0000000 <u>0</u>	This control is used to zero the SPDIF input to the ARC transmitter. 1 - Zero SPDIF input to ARC Tx channel A	
ARC_TX_AMPL[2:0]			R/W
0xAE	00000 <u>11</u> 0	This control is used to set the output level of the ARC signal. 110 - Default	
RD_INFO[15:0]			R
0xE1 0xE2	00000000 00000000	This readback displays the chip revision code. 0x2101 - Version Number	
CLOCK POLARITY			R/W
0xE4	000000 <u>0</u>	This control is used to adjust the clock polarity for the SPI Interface (CPOL). 0 - Normal polarity 1 - Inverted polarity	
CLOCK PHASE			R/W
0xE4	0000000 <u>0</u>	This control is used to adjust the clock phase control for SPI. 0 - Data captured on rising edge of SPI clock 1 - Data captured on falling edge of SPI clock	
AUDIO_CODEC_SLAVE_ADDR[6:0]			R/W
0xE7	0000000 <u>0</u>	This control is used to program the I2C slave address for the Audio Codec Map.	
XMEM_GAMMA_SLAVE_ADDR[6:0]			R/W
0xEB	0000000 <u>0</u>	This control is used to program the I2C slave address for the xmem_gamma Map.	
VFE_SLAVE_ADDR[6:0]			R/W
0xEC	0000000 <u>0</u>	This control is used to program the I2C slave address for the VFE Map.	
TX_EDID_SLAVE_ADDR[6:0]			R/W
0xF0	0000000 <u>0</u>	This control is used to program the I2C slave address for the TX EDID Map.	
SDP_SLAVE_ADDR[6:0]			R/W
0xF1	0000000 <u>0</u>	This control is used to program the I2C slave address for the SDP Map.	
SDP_IO_SLAVE_ADDR[6:0]			R/W
0xF2	0000000 <u>0</u>	This control is used to program the I2C slave address for the SDP_IO Map.	
INFOFRAME_SLAVE_ADDR[6:0]			R/W
0xF5	0000000 <u>0</u>	This control is used to program the I2C slave address for the InfoFrame Map.	
AFE_SLAVE_ADDR[6:0]			R/W
0xF8	0000000 <u>0</u>	This control is used to program the I2C slave address for the AFE Map.	

Reg	Bits	Description	
KSV_SLAVE_ADDR[6:0]			R/W
0xF9	00000000	This control is used to program the I2C slave address for the KSV Map.	
EDID_SLAVE_ADDR[6:0]			R/W
0xFA	00000000	This control is used to program the I2C slave address for the EDID Map.	
HDMI_SLAVE_ADDR[6:0]			R/W
0xFB	00000000	This control is used to program the I2C slave address for the HDMI Map.	
CP_SLAVE_ADDR[6:0]			R/W
0xFD	00000000	This control is used to program the I2C slave address for the CP Map.	
VDP_SLAVE_ADDR[6:0]			R/W
0xFE	00000000	This control is used to program the I2C slave address for the VDP Map.	
MAIN_RESET			SC
0xFF	00000000	This control is used to apply a main reset where I2C registers will be reset to their default values. This is a self clearing bit. 0 - Normal operation 1 - Apply main I2C reset	
VDP_RESET			SC
0xFF	00000000	This control is used to apply a VDP FIFO and a controller reset. This is a self clearing bit. 0 - Not reset 1 - Apply VDP reset	
SDP_RESET			SC
0xFF	00000000	This control is used to apply a SDP reset. This is a self clearing bit. 0 - Not reset 1 - Apply SDP reset	
SDP_MEM_RESET			SC
0xFF	00000000	This control is used to apply a memory interface reset. This is a self clearing bit. 0 - Not reset 1 - Apply SDP memory reset	

2.2 ADDR 4C (AFE)

Reg	Bits	Description	
PDN_ADC3			R/W
0x00	0000 <u>1</u> 111	This control is used to power down ADC3. 0 - Power up 1 - Power down	
PDN_ADC2			R/W
0x00	0000 <u>1</u> 111	This control is used to power down ADC2. 0 - Power up 1 - Power down	
PDN_ADC1			R/W
0x00	0000 <u>1</u> 111	This control is used to power down ADC1. 0 - Power up 1 - Power down	
PDN_ADC0			R/W
0x00	0000 <u>1</u> 111	This control is used to power down ADC0. 0 - Power up 1 - Power down	
PDN_AOUT2			R/W
0x01	00000 <u>1</u> 1	This control is used to power down the analog output buffer2. 0 - Power up 1 - Power down	
PDN_AOUT1			R/W
0x01	00000 <u>1</u> 1	This control is used to power down the analog output buffer1. 0 - Power up 1 - Power down	
ADC_SWITCH_MAN			R/W
0x02	<u>0</u> 0000000	This control is used to enable manual input muxing to the ADCs. 0 - Automatic muxing 1 - Manual muxing	
EMB_SYNC_SEL_MAN_EN			R/W
0x02	<u>0</u> 0000000	This control is used to enable manual selection of embedded synchronization inputs to synchronization strippers. In automatic mode, ain_sel[3:0] makes the selection. In manual mode, emb_sync_1_selman[1:0] and emb_sync_2_selman[1:0] makes the selection. 0 - Automatic sync selection 1 - Manual sync selection	
AIN_SEL[2:0]			R/W
0x02	00000 <u>0</u> 00	This control is used to select the analog input muxing mode. Code - ADC0 ADC1 ADC2 ADC3 EMB_SYNC_SEL1 EMB_SYNC_SEL2 000 - NC Ain1 Ain2 Ain3 Sync1 Sync2 001 - NC Ain4 Ain5 Ain6 Sync2 Sync1 010 - Ain10 Ain7 Ain8 Ain9	
ADC0_SW_MAN[3:0]			R/W
0x03	<u>0</u> 0000000	This control is used to manually route analog inputs to ADC0. 0101 - Ain5 1010 - Ain10 1011 - Ain11 1100 - Ain12 1101 - Ain13 All others - Reserved	
ADC1_SW_MAN[3:0]			R/W
0x03	<u>0</u> 0000000	This control is used to manually route analog inputs to ADC 1. 0001 - Ain1 0100 - Ain4 0111 - Ain7 1011 - Ain11 All others - Reserved	

Reg	Bits	Description	
ADC2_SW_MAN[3:0]			R/W
0x04	00000000	This control is used to manually route analog inputs to ADC2. 0010 - Ain2 0101 - Ain5 1000 - Ain8 1011 - Ain11 All others - Reserved	
ADC3_SW_MAN[3:0]			R/W
0x04	00000000	This control is used to manually route analog inputs to ADC3. 0011 - Ain3 0110 - Ain6 1001 - Ain9 All others - Reserved	
AA_FILTER_EN3			R/W
0x05	00000000	This control is used to enable the anti-aliasing filter on ADC3. 0 - Disable 1 - Enable	
AA_FILTER_EN2			R/W
0x05	00000000	This control is used to enable the anti-aliasing filter on ADC2. 0 - Disable 1 - Enable	
AA_FILTER_EN1			R/W
0x05	00000000	This control is used to enable the anti-aliasing filter on ADC1. 0 - Disable 1 - Enable	
AA_FILTER_EN0			R/W
0x05	00000000	This control is used to enable the anti-aliasing filter on ADC0. 0 - Disable 1 - Enable	
AA_FILT_HIGH_BW[1:0]			R/W
0x06 0x07	00000000 00000000	This control is used to program the anti-alias bandwidth on the ADCs. aa_filt_prog_bw[1:0] combined with aa_filt_high_bw[1:0] controls the anti-aliasing filter response. 00 - Default, passband < 17 MHz 01 - Passband < 42 MHz 10 - Passband < 92 MHz 11 - Passband < 146 MHz	
AA_FILT_PROG_BW[1:0]			R/W
0x07	00000000	This control is used to program the anti-alias bandwidth. It is used in conjunction with aa_filt_high_bw[1:0]. 00 - Default	
FB_SELECT[3:0]			R/W
0x14	00000000	This control is used to select the trilevel input to use as fast blank. 0000 - TRI1 0001 - TRI2 0010 - TRI3 0011 - TRI4 0100 - TRI5/HS_IN2 0101 - TRI6/VS_IN2 0110 - TRI7/HS_IN1 0111 - TRI8/VS_IN1 1xxx - Reserved	
EMB_SYNC_1_SEL_MAN[1:0]			R/W
0x15	00001010	This control is used to select a manual embedded synchronization for emb_sync1. 00 - Sync1 pin 01 - Sync2 pin 10 - Sync3 pin 11 - Reserved	

Reg	Bits	Description	
EMB_SYNC_2_SEL_MAN[1:0]			R/W
0x15	00 <u>00</u> 1010	This control is used to select a manual embedded synchronization for emb_sync2. 00 - Sync1 pin 01 - Sync2 pin 10 - Sync3 pin 11 - Reserved	
SYNC1_FILTER_SEL[1:0]			R/W
0x15	0000 <u>10</u> 10	This control is used to select the clamp filter on sync channel 1. 00 - No filter 01 - Sync > 250 ns 10 - Sync > 1 us 11 - Sync > 2.5 us	
SYNC2_FILTER_SEL[1:0]			R/W
0x15	0000 <u>10</u> 10	This control is used to select the clamp filter on sync channel 2. 00 - No filter 01 - Sync > 250 ns 10 - Sync > 1 us 11 - Sync > 2.5 us	
SLICE_LEVEL[4:0]			R/W
0x16	100 <u>11</u> 000	This control is used to set the slice level in the synchronization strippers. A smaller value corresponds to a higher slice level. For a clamp at 300 mV, the slice level is equal to 600 mV - (slice_level + 1) * 9.375 mV). 00000 - Highest slice level XXXXX - Clamp at 300 mV and slice at 600 mV - (XXXXX + 1) * 9.375 mV 11000 - Default 11111 - Lowest slice level	
TRI1_INT_MASKB[1:0]			R/W
0x17	<u>00</u> 000000	This control is used to enable the interrupts on the Tri1 input. 00 - No interrupt 01 - Interrupt on lower slice level only 10 - Interrupt on upper slice level only 11 - Interrupt on both slice levels	
TRI2_INT_MASKB[1:0]			R/W
0x17	<u>00</u> 000000	This control is used to enable the interrupts on the Tri2 input. 00 - No interrupt 01 - Interrupt on lower slice level only 10 - Interrupt on upper slice level only 11 - Interrupt on both slice levels	
TRI3_INT_MASKB[1:0]			R/W
0x17	00000 <u>00</u>	This control is used to enable the interrupts on the Tri3 input. 00 - No interrupt 01 - Interrupt on lower slice level only 10 - Interrupt on upper slice level only 11 - Interrupt on both slice levels	
TRI4_INT_MASKB[1:0]			R/W
0x17	000000 <u>00</u>	This control is used to enable the interrupts on the Tri4 input. 00 - No interrupt 01 - Interrupt on lower slice level only 10 - Interrupt on upper slice level only 11 - Interrupt on both slice levels	
TRI5_INT_MASKB[1:0]			R/W
0x18	<u>00</u> 000000	This control is used to enable the interrupts on the Tri5 input. 00 - No interrupt 01 - Interrupt on lower slice level only 10 - Interrupt on upper slice level only 11 - Interrupt on both slice levels	

Reg	Bits	Description	
TRI6_INT_MASKB[1:0]			R/W
0x18	00 <u>000000</u>	This control is used to enable the interrupts on the Tri6 input. 00 - No interrupt 01 - Interrupt on lower slice level only 10 - Interrupt on upper slice level only 11 - Interrupt on both slice levels	
TRI7_INT_MASKB[1:0]			R/W
0x18	000000 <u>00</u>	This control is used to enable the interrupts on the Tri7 input. 00 - No interrupt 01 - Interrupt on lower slice level only 10 - Interrupt on upper slice level only 11 - Interrupt on both slice levels	
TRI8_INT_MASKB[1:0]			R/W
0x18	000000 <u>00</u>	This control is used to enable the interrupts on the Tri8 input. 00 - No interrupt 01 - Interrupt on lower slice level only 10 - Interrupt on upper slice level only 11 - Interrupt on both slice levels	
TRI1_INT_CLEAR[1:0]			SC
0x19	<u>00</u> 000000	This control is used to clear the interrupts on the Tri1 input. This is a self-clearing bit. 00 - None 01 - Clear lower slice level interrupt 10 - Clear upper slice level interrupt 11 - Clear both interrupts	
TRI2_INT_CLEAR[1:0]			SC
0x19	<u>00</u> 000000	This control is used to clear the interrupts on the Tri2 input. This is a self-clearing bit. 00 - None 01 - Clear lower slice level interrupt 10 - Clear upper slice level interrupt 11 - Clear both interrupts	
TRI3_INT_CLEAR[1:0]			SC
0x19	000000 <u>00</u>	This control is used to clear the interrupts on the Tri3 input. This is a self-clearing bit. 00 - None 01 - Clear lower slice level interrupt 10 - Clear upper slice level interrupt 11 - Clear both interrupts	
TRI4_INT_CLEAR[1:0]			SC
0x19	000000 <u>00</u>	This control is used to clear the interrupts on the Tri4 input. This is a self-clearing bit. 00 - None 01 - Clear lower slice level interrupt 10 - Clear upper slice level interrupt 11 - Clear both interrupts	
TRI5_INT_CLEAR[1:0]			SC
0x1A	<u>00</u> 000000	This control is used to clear the interrupts on the Tri5 input. This is a self-clearing bit. 00 - None 01 - Clear lower slice level interrupt 10 - Clear upper slice level interrupt 11 - Clear both interrupts	
TRI6_INT_CLEAR[1:0]			SC
0x1A	<u>00</u> 000000	This control is used to clear the interrupts on the Tri6 input. This is a self-clearing bit. 00 - None 01 - Clear lower slice level interrupt 10 - Clear upper slice level interrupt 11 - Clear both interrupts	

Reg	Bits	Description	
TRI7_INT_CLEAR[1:0]			SC
0x1A	0000 <u>00</u> 00	This control is used to clear the interrupts on the Tri7 input. This is a self-clearing bit. 00 - None 01 - Clear lower slice level interrupt 10 - Clear upper slice level interrupt 11 - Clear both interrupts	
TRI8_INT_CLEAR[1:0]			SC
0x1A	0000 <u>00</u> 00	This control is used to clear the interrupts on the Tri8 input. This is a self-clearing bit. 00 - None 01 - Clear lower slice level interrupt 10 - Clear upper slice level interrupt 11 - Clear both interrupts	
TRI1_INT_STATUS[1:0]			R
0x1B	<u>00</u> 000000	This readback displays the Tri1 interrupt status. 00 - No signal change detected 01 - Signal crossed lower slice level 10 - Signal crossed upper slice level 11 - Signal crossed both slice levels	
TRI2_INT_STATUS[1:0]			R
0x1B	<u>00</u> 000000	This readback displays the Tri2 interrupt status. 00 - No signal change detected 01 - Signal crossed lower slice level 10 - Signal crossed upper slice level 11 - Signal crossed both slice levels	
TRI3_INT_STATUS[1:0]			R
0x1B	0000 <u>00</u> 00	This readback displays the Tri3 interrupt status. 00 - No signal change detected 01 - Signal crossed lower slice level 10 - Signal crossed upper slice level 11 - Signal crossed both slice levels	
TRI4_INT_STATUS[1:0]			R
0x1B	0000 <u>00</u> 00	This readback displays the Tri4 interrupt status. 00 - No signal change detected 01 - Signal crossed lower slice level 10 - Signal crossed upper slice level 11 - Signal crossed both slice levels	
TRI5_INT_STATUS[1:0]			R
0x1C	<u>00</u> 000000	This readback displays the Tri5 interrupt status. 00 - No signal change detected 01 - Signal crossed lower slice level 10 - Signal crossed upper slice level 11 - Signal crossed both slice levels	
TRI6_INT_STATUS[1:0]			R
0x1C	<u>00</u> 000000	This readback displays the Tri6 interrupt status. 00 - No signal change detected 01 - Signal crossed lower slice level 10 - Signal crossed upper slice level 11 - Signal crossed both slice levels	
TRI7_INT_STATUS[1:0]			R
0x1C	0000 <u>00</u> 00	This readback displays the Tri7 interrupt status. 00 - No signal change detected 01 - Signal crossed lower slice level 10 - Signal crossed upper slice level 11 - Signal crossed both slice levels	

Reg	Bits	Description	
TRI8_INT_STATUS[1:0]			R
0x1C	00000 <u>00</u>	This readback displays the Tri8 interrupt status. 00 - No signal change detected 01 - Signal crossed lower slice level 10 - Signal crossed upper slice level 11 - Signal crossed both slice levels	
TRI1_SLICER_PWRDN			R/W
0x1D	0 <u>1</u> 101101	This control is used to power down the Tri1 slicer. 0 - Power up 1 - Power down	
TRI1_BILEVEL_SLICE_EN			R/W
0x1D	0 <u>1</u> 101101	This control is used to enable bilevel slicing on the Tri1 input. 0 - Bilevel slicing 1 - Trilevel slicing	
TRI1_UPPER_SLICE_LEVEL[2:0]			R/W
0x1D	0 <u>11</u> 101101	This control is used to set the upper slice level on the Tri1 input. 000 - 75 mV 001 - 225 mV 010 - 375 mV 011 - 525 mV 100 - 675 mV 101 - 825 mV 110 - 975 mV 111 - 1.125 V	
TRI1_LOWER_SLICE_LEVEL[1:0]			R/W
0x1D	0110 <u>11</u> 01	This control is used to set the lower slice level on the Tri1 input. 00 - 75 mV 01 - 225 mV 10 - 375 mV 11 - 525 mV	
TRI2_SLICER_PWRDN			R/W
0x1E	0 <u>1</u> 101101	This control is used to power down the Tri2 slicer. 0 - Power up 1 - Power down	
TRI2_BILEVEL_SLICE_EN			R/W
0x1E	0 <u>1</u> 101101	This control is used to enable bilevel slicing on the Tri2 input. 0 - Bilevel slicing 1 - Trilevel slicing	
TRI2_UPPER_SLICE_LEVEL[2:0]			R/W
0x1E	0 <u>11</u> 101101	This control is used to set the upper slice level on the Tri2 input. 000 - 75 mV 001 - 225 mV 010 - 37 mV 011 - 525 mV 100 - 675 mV 101 - 825 mV 110 - 975 mV 111 - 1.125 V	
TRI2_LOWER_SLICE_LEVEL[1:0]			R/W
0x1E	0110 <u>11</u> 01	This control is used to set the lower slice level on the Tri2 input. 00 - 75 mV 01 - 225 mV 10 - 375 mV 11 - 525 mV	
TRI3_SLICER_PWRDN			R/W
0x1F	0 <u>1</u> 101101	This control is used to power down the Tri3 slicer. 0 - Power up 1 - Power down	

Reg	Bits	Description	
TRI3_BILEVEL_SLICE_EN			R/W
0x1F	01 <u>1</u> 01101	This control is used to enable bilevel slicing on the Tri3 input. 0 - Bilevel slicing 1 - Trilevel slicing	
TRI3_UPPER_SLICE_LEVEL[2:0]			R/W
0x1F	011 <u>011</u> 01	This control is used to set the upper slice level on the Tri3 input. 000 - 75 mV 001 - 225 mV 010 - 375 mV 011 - 525 mV 100 - 675 mV 101 - 825 mV 110 - 975 mV 111 - 1.125 V	
TRI3_LOWER_SLICE_LEVEL[1:0]			R/W
0x1F	011011 <u>01</u>	This control is used to set the lower slice level on the Tri3 input. 00 - 75 mV 01 - 225 mV 10 - 375 mV 11 - 525 mV	
TRI4_SLICER_PWRDN			R/W
0x20	01101101	This control is used to power down the Tri4 slicer. 0 - Power up 1 - Power down	
TRI4_BILEVEL_SLICE_EN			R/W
0x20	01 <u>1</u> 01101	This control is used to enable bilevel slicing on the Tri4 input. 0 - Bilevel slicing 1 - Trilevel slicing	
TRI4_UPPER_SLICE_LEVEL[2:0]			R/W
0x20	011 <u>011</u> 01	This control is used to set the upper slice level on the Tri4 input. 000 - 75 mV 001 - 225 mV 010 - 375 mV 011 - 525 mV 100 - 675 mV 101 - 825 mV 110 - 975 mV 111 - 1.125 V	
TRI4_LOWER_SLICE_LEVEL[1:0]			R/W
0x20	011011 <u>01</u>	This control is used to set the lower slice level on the Tri4 input. 00 - 75 mV 01 - 225 mV 10 - 375 mV 11 - 525 mV	
TRI5_SLICER_PWRDN			R/W
0x21	01101101	This control is used to power down the Tri5 slicer. 0 - Power up 1 - Power down	
TRI5_BILEVEL_SLICE_EN			R/W
0x21	01 <u>1</u> 01101	This control is used to enable bilevel slicing on the Tri5 input. 0 - Bilevel slicing 1 - Trilevel slicing	

Reg	Bits	Description	
TRI5_UPPER_SLICE_LEVEL[2:0]			R/W
0x21	011 <u>011</u> 01	This control is used to set the upper slice level on the Tri5 input. 000 - 75 mV 001 - 225 mV 010 - 375 mV 011 - 525 mV 100 - 675 mV 101 - 825 mV 110 - 975 mV 111 - 1.125 V	
TRI5_LOWER_SLICE_LEVEL[1:0]			R/W
0x21	011011 <u>01</u>	This control is used to set the lower slice level on the Tri5 input. 00 - 75 mV 01 - 225 mV 10 - 375 mV 11 - 525 mV	
TRI6_SLICER_PWRDN			R/W
0x22	01 <u>1</u> 01101	This control is used to power down the Tri6 slicer. 0 - Power up 1 - Power down	
TRI6_BILEVEL_SLICE_EN			R/W
0x22	01 <u>1</u> 01101	This control is used to enable bilevel slicing on the Tri6 input. 0 - Bilevel slicing 1 - Trilevel slicing	
TRI6_UPPER_SLICE_LEVEL[2:0]			R/W
0x22	011 <u>011</u> 01	This control is used to set the upper slice level on the Tri6 input. 000 - 75 mV 001 - 225 mV 010 - 375 mV 011 - 525 mV 100 - 675 mV 101 - 825 mV 110 - 975 mV 111 - 1.125 V	
TRI6_LOWER_SLICE_LEVEL[1:0]			R/W
0x22	011011 <u>01</u>	This control is used to set the lower slice level on the Tri6 input. 00 - 75 mV 01 - 225 mV 10 - 375 mV 11 - 525 mV	
TRI7_SLICER_PWRDN			R/W
0x23	01 <u>1</u> 01101	This control is used to power down the Tri7 slicer. 0 - Power up 1 - Power down	
TRI7_BILEVEL_SLICE_EN			R/W
0x23	01 <u>1</u> 01101	This control is used to enable bilevel slicing on the Tri7 input. 0 - Bilevel slicing 1 - Trilevel slicing	
TRI7_UPPER_SLICE_LEVEL[2:0]			R/W
0x23	011 <u>011</u> 01	This control is used to set the upper slice level on the Tri7 input. 000 - 75 mV 001 - 225 mV 010 - 375 mV 011 - 525 mV 100 - 675 mV 101 - 825 mV 110 - 975 mV 111 - 1.125 V	

Reg	Bits	Description	
TRI7_LOWER_SLICE_LEVEL[1:0]			R/W
0x23	011011 <u>01</u>	This control is used to set the lower slice level on the Tri7 input. 00 - 75 mV 01 - 225 mV 10 - 375 mV 11 - 525 mV	
TRI8_SLICER_PWRDN			R/W
0x24	0 <u>1</u> 101101	This control is used to power down the Tri8 slicer. 0 - Power up 1 - Power down	
TRI8_BILEVEL_SLICE_EN			R/W
0x24	01 <u>1</u> 01101	This control is used to enable bilevel slicing on the Tri8 input. 0 - Bilevel slicing 1 - Trilevel slicing	
TRI8_UPPER_SLICE_LEVEL[2:0]			R/W
0x24	011 <u>011</u> 01	This control is used to set the upper slice level on the Tri8 input. 000 - 75 mV 001 - 225 mV 010 - 375 mV 011 - 525 mV 100 - 675 mV 101 - 825 mV 110 - 975 mV 111 - 1.125 V	
TRI8_LOWER_SLICE_LEVEL[1:0]			R/W
0x24	011011 <u>01</u>	This control is used to set the lower slice level on the Tri8 input. 00 - 75 mV 01 - 225 mV 10 - 375 mV 11 - 525 mV	
TRI1_READBACK[1:0]			R
0x27	<u>00</u> 000000	This readback displays Tri1 DC levels. 1x - Signal higher than upper level 0x - Signal lower than upper level x1 - Signal higher than lower level x0 - Signal lower than lower level	
TRI2_READBACK[1:0]			R
0x27	<u>00</u> 000000	This readback displays Tri2 DC levels. 1x - Signal higher than upper level 0x - Signal lower than upper level x1 - Signal higher than lower level x0 - Signal lower than lower level	
TRI3_READBACK[1:0]			R
0x27	0000 <u>00</u> 00	This readback displays Tri3 DC levels. 1x - Signal higher than upper level 0x - Signal lower than upper level x1 - Signal higher than lower level x0 - Signal lower than lower level	
TRI4_READBACK[1:0]			R
0x27	000000 <u>00</u>	This readback displays Tri4 DC levels. 1x - Signal higher than upper level 0x - Signal lower than upper level x1 - Signal higher than lower level x0 - Signal lower than lower level	

Reg	Bits	Description	
TRI5_READBACK[1:0]			R
0x28	00000000	This readback displays Tri5 DC levels. 1x - Signal higher than upper level 0x - Signal lower than upper level x1 - Signal higher than lower level x0 - Signal lower than lower level	
TRI6_READBACK[1:0]			R
0x28	00000000	This readback displays Tri6 DC levels. 1x - Signal higher than upper level 0x - Signal lower than upper level x1 - Signal higher than lower level x0 - Signal lower than lower level	
TRI7_READBACK[1:0]			R
0x28	00000000	This readback displays Tri7 DC levels. 1x - Signal higher than upper level 0x - Signal lower than upper level x1 - Signal higher than lower level x0 - Signal lower than lower level	
TRI8_READBACK[1:0]			R
0x28	00000000	This readback displays Tri8 DC levels. 1x - Signal higher than upper level 0x - Signal lower than upper level x1 - Signal higher than lower level x0 - Signal lower than lower level	
VOUT2_SEL[3:0]			R/W
0x2C	00000000	This control is used to switch analog inputs to Vout2. 0100 - Ain4 1011 - Ain11 1100 - Ain12 All others - Reserved	
VOUT1_SEL[3:0]			R/W
0x2C	00000000	This control is used to switch analog inputs to Vout1. 0101 - Ain5 1010 - Ain10 1011 - Ain11 1100 - Ain12 1101 - Ain13 All others - Reserved	

2.3 ADDR 8A (MEMORY)

Reg	Bits	Description	
SDRAM_SIZE[3:0]			R/W
0x11	00010010	This control is used to set the size of the SDRAM memory. 000 - Reserved 001 - 256 Mb 010 - 512 Mb 011 - 1 Gb 100 - 2 Gb 101 - 4 Gb All others - Reserved	
RW_CTRL_OE			R/W
0x28	00000000	This control is used to enable the external memory read/write signals, e.g. ras, cas, clock, and address. 0 - Input 1 - Output	
DDR2_CK_OE			R/W
0x28	00000000	This control is used to enable the external memory clock signal. 0 - Input 1 - Output	
MEM_RW_CTRL_DRV_STR[1:0]			R/W
0x28	00000000	This control is used to adjust the drive strength setting for the read/write control signals to the DDR2 memory, e.g. ras, cas, wr, and cke. 00 - Minimum drive strength 11 - Maximum drive strength	
MEM_SM_RESET			R/W
0x2B	00101001	This control is used to reset the memory controller. It is a self-clearing control. 1 - Reset memory controller	
CK_DRV_STR[7:0]			R/W
0x37	10101010	This control is used to adjust the drive strength setting for the clock output to the DDR2 memory. 00 - Minimum drive strength FF - Maximum drive strength	
DQS_DRV_STR[7:0]			R/W
0x38	01010101	This control is used to adjust the drive strength setting for the lower DQS outputs to the DDR2 memory. 00 - Minimum drive strength FF - Maximum drive strength	
DQS_DRV_STR[7:0]			R/W
0x39	01010101	This control is used to adjust the drive strength setting for the upper DQS outputs to the DDR2 memory. 00 - Minimum drive strength FF - Maximum drive strength	

2.4 ADDR 44 (CP)

Reg	Bits	Description	
RB_CSC_SCALE[1:0]			R
0x0B	00000000	This readback displays the CSC scale applied to CSC coefficients. xx - Readback value	
RB_A4[12:0]			R
0x0B 0x0C	00000000 00000000	This readback displays the CSC coefficient A4 modified by the video adjustment block. xxxxxxxxxxxx - Readback value	
RB_A3[12:0]			R
0x0D 0x0E	00000000 00000000	This readback displays the CSC coefficient A3 modified by the video adjustment block. xxxxxxxxxxxx - Readback value	
RB_A2[12:0]			R
0x0E 0x0F 0x10	00000000 00000000 00000000	This readback displays the CSC coefficient A2 modified by the video adjustment block. xxxxxxxxxxxx - Readback value	
RB_A1[12:0]			R
0x10 0x11	00000000 00000000	This readback displays the CSC coefficient A1 modified by the video adjustment block. xxxxxxxxxxxx - Readback value	
RB_B4[12:0]			R
0x12 0x13	00000000 00000000	This readback displays the CSC coefficient B4 modified by the video adjustment block. xxxxxxxxxxxx - Readback value	
RB_B3[12:0]			R
0x14 0x15	00000000 00000000	This readback displays the CSC coefficient B3 modified by the video adjustment block. xxxxxxxxxxxx - Readback value	
RB_B2[12:0]			R
0x15 0x16 0x17	00000000 00000000 00000000	This readback displays the CSC coefficient B2 modified by the video adjustment block. xxxxxxxxxxxx - Readback value	
RB_B1[12:0]			R
0x17 0x18	00000000 00000000	This readback displays the CSC coefficient B1 modified by the video adjustment block. xxxxxxxxxxxx - Readback value	
RB_C4[12:0]			R
0x19 0x1A	00000000 00000000	This readback displays the CSC coefficient C4 modified by the video adjustment block. xxxxxxxxxxxx - Readback value	
RB_C3[12:0]			R
0x1B 0x1C	00000000 00000000	This readback displays the CSC coefficient C3 modified by the video adjustment block. xxxxxxxxxxxx - Readback value	
RB_C2[12:0]			R
0x1C 0x1D 0x1E	00000000 00000000 00000000	This readback displays the CSC coefficient C2 modified by the video adjustment block. xxxxxxxxxxxx - Readback value	
RB_C1[12:0]			R
0x1E 0x1F	00000000 00000000	This readback displays the CSC coefficient C1 modified by the video adjustment block. xxxxxxxxxxxx - Readback value	
CP_START_HS[12:0]			R/W
0x22 0x23	00000000 00000000	This control is used to set the position of the start of the Hsync output signal in the CP core in autographic mode only. Programming of this control is optional and should only be performed when the part is set in autographics mode. The value is unsigned. 0x0000 - Default	

Reg	Bits	Description	
CP_END_HS[12:0]			R/W
0x24 0x25	00000000 00000000	This control is used to set the position of the end of the HSync output signal in the CP core in autographics mode only. Programming of this control is optional and should only be performed when the part is set in autographics mode. The value is unsigned. 0x0000 - Default	
CP_START_SAV[12:0]			R/W
0x26 0x27	00000000 00000000	This control is used to set a manual value for the Start of Active Video (SAV) position. It is used to set the total number of pixels between the start of non active video and the start of active video. Programming is optional and should only be performed when the part is set in autographics mode. The value is unsigned. 0x0000 - Default	
CP_START_EAV[12:0]			R/W
0x28 0x29	00000000 00000000	This control is used to set a manual value for the Start of Active Video (SAV) position. It is used to set the total number of pixels between the start of non active video and the start of active video. Programming is optional and should only be performed when the part is set in autographics mode. The value is unsigned. 0x0000 - Default	
CP_START_VBI_R[11:0]			R/W
0x2A 0x2B	00000000 00000000	This control is used to manually set the value for the start position of the VBI region. This is the extra blank region preceding the odd right (R) field in the 3D TV field alternative packing format supported by HDMI. It is not required to set this value. In normal operation, this parameter is automatically calculated from the input.	
CP_END_VBI_R[11:0]			R/W
0x2B 0x2C	00000000 00000000	This control is used to manually set the value for the end of VBI position. This is the extra blank region preceding the odd right field in the 3D TV field alternative packing format supported by HDMI. It is not required to set this value. In normal operation, this parameter is automatically calculated from the input.	
CP_START_VBI_EVEN_R[11:0]			R/W
0x2D 0x2E	00000000 00000000	This control is used to manually set the value for the start position of the VBI region. This is the extra blank region preceding the even right field in the 3D TV field alternative packing format supported by HDMI. It is not required to set this value. In normal operation, this parameter is automatically calculated from the input.	
CP_END_VBI_EVEN_R[11:0]			R/W
0x2E 0x2F	00000000 00000000	This control is used to manually set the value for the start position of the VBI region. This is the extra blank region preceding the even right field in the 3D TV field alternative packing format supported by HDMI. It is not required to set this value. In normal operation, this parameter is automatically calculated from the input.	
DE_V_START_R[3:0]			R/W
0x30	00000000	This control is used to vary the position of the start of the extra VBI region between the left and right fields during the odd field in the field alternative packing in 3D TV video format. It stores a signed value represented in a twos complement format. The unit of de_v_end_even[9:0] is one line. 1000 to 1111 - -8 lines to -1 line 0000 - Default (0 lines) 0001 to 0111 - 1 line to 7 lines	
DE_V_END_R[3:0]			R/W
0x30	00000000	This control is used to vary the position of the start of the extra VBI region between the left and right fields during the odd field in the field alternative packing in 3D TV video format. It stores a signed value represented in a twos complement format. The unit of de_v_end_even[9:0] is one line. 1000 to 1111 - -8 lines to -1 line 0000 - Default (0 lines) 0001 to 0111 - 1 line to 7 lines	
DE_V_START_EVEN_R[3:0]			R/W
0x31	00000000	This control is used to vary the position of the start of the extra VBI region between L and R fields during the even field in the field alternative packing in 3D TV video format through HDMI. It stores a signed value represented in a twos complement format. The unit of de_v_end_even[9:0] is one line. 1000 to 1111 - -8 lines to -1 line 0000 - Default (0 lines) 0001 to 0111 - 1 line to 7 lines	
DE_V_END_EVEN_R[3:0]			R/W
0x31	00000000	This control is used to vary the position of the end of the extra VBI region between L and R fields during the even field in the field alternative packing in 3D TV video format through HDMI. It stores a signed value represented in a twos complement format. The unit of de_v_end_even[9:0] is one line. 1000 to 1111 - -8 lines to -1 line 0000 - Default (0 lines) 0001 to 0111 - 1 line to 7 lines	

Reg	Bits	Description	
CP_CONTRAST[7:0]			R/W
0x3A	10000000	This control is used to set the contrast. It is an unsigned value represented in a 1.7 binary format. The MSB represents the integer part of the contrast value, which is either 0 or 1. The seven LSBs represents the fractional part of the contrast value. The fractional part has the range [0 to 0.99]. This control is functional if vid_adj_en is set to 1. 00000000 - Contrast set to minimum 10000000 - Default 11111111 - Contrast set to maximum	
CP_SATURATION[7:0]			R/W
0x3B	10000000	This control is used to set the saturation. It is an unsigned value represented in a 1.7 binary format. The MSB represents the integer part of the saturation value, which is either 0 or 1. The seven LSBs represent the fractional part of the saturation value. The fractional part has a [0 to 0.99] range. This control is functional if vid_adj_en is set to 1. 00000000 - Saturation set to minimum 10000000 - Default 11111111 - Saturation set to maximum	
CP_BRIGHTNESS[7:0]			R/W
0x3C	00000000	This control is used to set the brightness. It is a signed value. The effective brightness value applied to the luma is obtained by multiplying the programmed value cp_brightness with a gain of 4. The brightness applied to the luma has a range of [-512 to 508]. This control is functional if vid_adj_en is set to 1. 00000000 - Offset applied to luma is 0. 01111111 - Offset applied to luma is 508d. This value corresponds to brightest setting. 11111111 - Offset applied to luma is -512d. This value corresponds to darkest setting.	
CP_HUE[7:0]			R/W
0x3D	00000000	This control is used to set the hue. This control represents an unsigned value which provides hue adjustment. The effective hue applied to the chroma is $[(cp_hue[7:0] * 180) / 256 - 90]$. The range of the effective hue applied to the chroma is [-90° to 90°]. 00000000 - Hue of -90° applied to chroma 00001111 - Hue of 0° applied to chroma 11111111 - Hue of 90° applied to chroma	
VID_ADJ_EN			R/W
0x3E	00000000	This control is used to enable video adjustment. It is used to select whether or not the color controls feature is enabled. The color controls feature is configured via the parameters cp_contrast[7:0], cp_saturation[7:0], cp_brightness[7:0] and cp_hue[7:0]. The CP CSC must also be enabled for the color controls to be effective. 0 - Disable color controls 1 - Enable color controls	
CP_MODE_GAIN_ADJ_EN			R/W
0x3E	00000000	This control is used to enable pregain. 0 - Pregain block is bypassed 1 - Pregain block is enabled	
ALT_SAT_UV_MAN			R/W
0x3E	00000000	This control is used to define the U and V saturation range. 0 - Range of saturator on Cr and Cb channels determined by op_656_range and alt_data_sat 1 - Range of saturator on Cr and Cb channels determined by alt_sav_uv if op_656_range or alt_data_sat set to 0	
ALT_SAT_UV			R/W
0x3E	00000000	This control is used to define the Cr and Cb saturation range. Refer to the description of alt_sat_uv_man for additional details. 0 - Range of saturators on channels Cr and Cb is 15 to 235 1 - Range of saturators on channels Cr and Cb is 16 to 240	
CP_MODE_GAIN_ADJ[7:0]			R/W
0x40	01011100	This control is used for pregain adjustment to compensate for the gain of the Analog Front End. It stores a value in a 1.7 binary format. 0xxxxxxx - Gain of $(0 + (xxxxxxx / 128))$ 10000000 - Default pregain (pregain of 1.0) 1xxxxxxx - Gain of $(1 + (xxxxxxx / 128))$	
CH2_POL_MAN_EN			R/W
0x41	00000010	This control is used to override the polarity detection by sync channel 2 SSPD. 0 - Use result from sync channel 2 SSPD autodetection 1 - Use ch2_pol_vs and ch2_pol_hs	

Reg	Bits	Description	R/W
CH2_POL_VS			
0x41	00 <u>0000</u> 10	This control is used to override the polarity of VSync by sync channel 2 SSPD. ch2_pol_man_en must be set to 1 for this control to be active. 0 - VSync input to sync channel 2 carries negative polarity signal 1 - VSync input to sync channel 2 carries positive polarity signal	R/W
CH2_POL_HSCS			
0x41	00 <u>0000</u> 10	This control is used to override the polarity of HSync by sync channel 2 SSPD. ch2_pol_man_en must be set to 1 for this control to be active. 0 - HSync input to sync channel 2 carries negative polarity signal (HSync or CSync) 1 - HSync input to sync channel 2 carries positive polarity signal (HSync or CSync)	R/W
CH2_SYNC_SRC[1:0]			
0x41	00 <u>00</u> 010	This control is used to select the synchronization signals processed by sync channel 2 SSPD. 00 - Autodetection mode for synchronization source. Use results of autodetection for synchronization signal routing. Result can be read back via ch2_cur_sync[1:0] bits. 01 - Manual setting: separate HSync and VSync to sync channel 2 SSPD. 10 - Manual sett	R/W
CH2_TRIG_SSPD			
0x41	0000 <u>0</u> 10	This control is used to trigger a synchronization source and polarity detector for sync channel 2 SSPD. A 0 to 1 transition in this bit restarts the autosync detection algorithm. This is not a self clearing bit and must be set to 0 to prepare for the next trigger. 0 - Default - transition 0 to 1 restarts autosync detection algorithm 1 - Transition 0 to 1 restarts autosync detection algorithm	R/W
CH2_SSPD_CONT			
0x41	00000 <u>0</u> 10	This control is used to set the synchronization source polarity detection mode for sync channel 2 SSPD. 0 - Sync channel 2 SSPD works in one-shot mode (triggered by a 0 to 1 transition on ch2_trig_sspd bit) 1 - Sync channel 2 SSPD works in continuous mode	R/W
CH2_SSPD_PP_EN			
0x41	00000 <u>0</u> 10	This control is used to enable sync channel 2 SSPD post processing. Activity on the embedded signal input to sync channel 2 SSPD is reported by ch2_rs_active. Post processing of the synchronization signal input to sync channel 2 SSPD works only if the embedded synchronization signal and the Hsync/CSync and Vsync signals have the same timing. 0 - Disable post processing of synchronization signals input to sync channel 2 SSPD 1 - Check for activity on embedded synchronization signal input to sync channel 2 SSPD when it detects activity on HSync/CSync and VSync	R/W
CH2_TRIG_STDI			
0x42	0011 <u>10</u> 11	This control is used to trigger the standard identification of sync channel 2 STDI. A 0 to 1 transition triggers the STDI measurements. This is not a self clearing bit and must be set to 0 to prepare for the next STDI measurements. 0 - Default - transition 0 to 1 restarts autosync detection algorithm 1 - Transition 0 to 1 restarts autosync detection algorithm	R/W
CH2_STDI_CONT			
0x42	0011 <u>10</u> 11	This control is used to select the sync channel 2 STDI mode of operation. 0 - Sync channel 2 STDI block operates in single-shot mode. 0 to 1 transition on ch2_trig_stdi triggers measurement of sync channel 2 STDI block. 1 - Sync channel 2 STDI runs in continuous mode.	R/W
CH2_FL_FR_THRESHOLD[2:0]			
0x43	<u>110</u> 10100	This control is used to define the threshold of the difference between the input video field length and the internally stored standard to enter and exit free run. It is used for the sync channel 2 STDI. 000 - Minimum difference to switch into free run is 36 lines. Maximum difference to switch out of free run is 31 lines. 001 - Minimum difference to switch into free run is 18 lines. Maximum difference to switch out of free run is 15 lines. 010 - Minimum d	R/W
CH2_F_RUN_THR[2:0]			
0x43	<u>110</u> 10100	This control is used to select the free run threshold for sync channel 2. It determines the horizontal conditions under which free run mode is entered or left. The length of the incoming video line is measured based on the crystal clock and compared to an internally stored parameter. The magnitude of the difference decides whether or not sync channel 2 will enter free run mode. 000 - Minimum difference to switch into free run is 2. Maximum difference to switch out of free run is 1. 001 - Minimum difference to switch into free run is 256. Maximum difference to switch out of free run is 200. 010 - Minimum difference to switch into	R/W

Reg	Bits	Description	
CH2_FR_FIELD_LENGTH[11:0]			R/W
0x46 0x47	00000000 00000000	This code is used to define the ideal number of lines per field used by the CP core for the free run decision for sync channel 2. If set to 0, the ideal number of lines per field is dictated by cp_lcount_max[11:0]. 0x000 - Default	
CH2_FR_LL[10:0]			R/W
0x47 0x48	00000000 00000000	This control is used to define the free run line length in the number of crystal clock cycles in one line of video for sync channel 2 STDI. This control should only be programmed for video standards that are not supported by prim_mode[3:0] and vid_std[5:0]. 0x000 - Actually used internal free run line length decoded from prim_mode[3:0] and vid_std[5:0]. All other values - Number of crystal clocks in ideal line length. Used to enter or exit free run mode.	
CH2_STDI_DVALID			R
0x49	00000000	This control is set when the measurements performed by sync channel 2 STDI are completed. A high level signals validity for the ch2_bll, ch2_lcf, ch2_lcv, ch2_fcl, and ch2_stdi_intlcd controls. To prevent false readouts, especially during signal acquisition, ch2_sdti_dvalid is set to 1 only after four fields with the same length are recorded. As a result, STDI measurements can take up to five fields to finish. 0 - Sync channel 2 STDI measurement not valid 1 - Sync channel 2 STDI measurement valid	
CH2_STDI_INTLCD			R
0x49	00000000	This readback displays interlaced versus progressive mode detected by sync channel 2 STDI. The readback is valid if ch2_stdi_dvalid is set to 1. 0 - Indicates video signal on sync channel 2 with non interlaced timing 1 - Indicates signal on sync channel 2 with interlaced timing	
CH2_BL[13:0]			R
0x49 0x4A	00000000 00000000	This readback displays the sync channel 2 block length. It displays the number of crystal cycles in a block of eight lines of incoming video. The readback is valid if ch2_stdi_dvalid is set to 1. xxxxxxxxxxxx - Readback value	
CH2_LCVS[4:0]			R
0x4B	00000000	This readback displays the sync channel 2 line count in a VSync. It displays the number of lines in a VSync period measured on sync channel 2. The readback is valid if ch2_stdi_dvalid is set to 1. xxxxx - Readback value	
CH2_LCF[11:0]			R
0x4B 0x4C 0x4D	00000000 00000000 00000000	This readback displays the sync channel 2 line count in a field. It displays the number of lines between two VSynCs measured on sync channel 2. The readback is valid if ch2_stdi_dvalid is set to 1. xxxxxxxxxxxx - Readback value	
CH2_FCL[12:0]			R
0x4D 0x4E	00000000 00000000	This readback displays the sync channel 2 field count length. The number of crystal clock cycles between successive VSynCs is measured by sync channel 2 STDI or in 1/256th of a field. The readback is valid if ch2_stdi_dvalid is set to 1. xxxxxxxxxxxx - Readback value	
CH2_SSPD_DVALID			R
0x4F	00000000	This control is set to 1 when the readbacks from the SSPD section of sync channel 2 are valid. It is set to 1 after 2 ²² crystal clock periods following a reset of the CP section. It is set to 0 when the DUT is reset. 0 - Sync channel 2 SSPD results not valid for readback 1 - Sync channel 2 SSPD results valid (detection finished)	
CH2_VS_ACT			R
0x4F	00000000	This readback indicates the activity on the VSync input to sync channel 2 SSPD. 0 - No activity detected on VSync input to sync channel 2 SSPD 1 - VSync input to sync channel 2 SSPD carries an active signal	
CH2_CUR_POL_VS			R
0x4F	00000000	This readback displays the polarity of the VSync input to sync channel 2 SSPD. 0 - VSync input to sync channel 2 SSPD has negative polarity signal 1 - VSync input to sync channel 2 SSPD has positive polarity signal	
CH2_HS_ACT			R
0x4F	00000000	This readback displays activity on the HSync/CSync input to sync channel 2 SSPD. 0 - No activity detected on HSync/CSync input to sync channel 2 SSPD 1 - HSync/CSync input to sync channel 2 SSPD carries an active signal	

Reg	Bits	Description	
CH2_CUR_POL_HS			R
0x4F	00000 <u>000</u>	This readback displays the polarity of the HSync/CSync input to sync channel 2 SSPD. 0 - HSync CSync input to sync channel 2 SSPD has negative polarity 1 - HSync CSync input to sync channel 2 SSPD has positive polarity	
CH2_RS_ACTIVE			R
0x4F	00000 <u>000</u>	This readback displays activity in an embedded synchronization signal input to sync channel 2 SSPD. ch2_sspd_pp_en must be set to 1 and ch2_sspd_dvalid must return 1 for this readback to be valid. This readback is only valid when there is an Hsync and Vsync signal present. It is not valid to use this control when only an embedded signal is present. The purpose of this control is to indicate that the user can switch to embedded sync if using Hsync and Vsync inputs. 0 - Activity detected on embedded signal input to sync channel 2 SSPD 1 - No activity detected on embedded signal input to sync channel 2 SSPD	
CH2_CUR_SYNC_SRC[1:0]			R
0x4F	00000 <u>00</u>	This readback displays the current synchronization source detected by sync channel 2 SSPD. 00 - Not used 01 - Activity detected on HSync and VSync input to sync channel 2 SSPD 10 - CSync detected in HSync input to sync channel 2 SSPD 11 - Activity detected on embedded synchronization input to sync channel 2 SSPD	
CSC_SCALE[1:0]			R/W
0x52	<u>01</u> 000000	This control is used to set the CSC coefficient scalar. 00 - CSC scalar set to 1 01 - CSC scalar set to 2 10 - Reserved 11 - Reserved	
A4[12:0]			R/W
0x52 0x53	<u>010</u> 00000 <u>00000000</u>	This control is used to set the CSC coefficient A4. It contains a 13-bit A4 coefficient for the A channel. 0x0000 - Default	
A3[12:0]			R/W
0x54 0x55	<u>00000000</u> <u>00000000</u>	This control is used to set the CSC coefficient A3. It contains a 13-bit A3 coefficient for the A channel. 0x0000 - Default	
A2[12:0]			R/W
0x55 0x56 0x57	<u>00000000</u> <u>00000000</u> <u>00001000</u>	This control is used to set the CSC coefficient A2. It contains a 13-bit A2 coefficient for the A channel. 0x0000 - Default	
A1[12:0]			R/W
0x57 0x58	<u>00001000</u> <u>00000000</u>	This control is used to set the CSC coefficient A1. It contains a 13-bit A1 coefficient for the A channel. 0x0800 - Default	
B4[12:0]			R/W
0x59 0x5A	<u>00000000</u> <u>00000000</u>	This control is used to set the CSC coefficient B4. It contains a 13-bit B4 coefficient for the B channel. 0x0000 - Default	
B3[12:0]			R/W
0x5B 0x5C	<u>00000000</u> <u>00000001</u>	This control is used to set the CSC coefficient B3. It contains a 13-bit B3 coefficient for the B channel. 0x0000 - Default	
B2[12:0]			R/W
0x5C 0x5D 0x5E	<u>00000001</u> <u>00000000</u> <u>00000000</u>	This control is used to set the CSC coefficient B2. It contains a 13-bit B2 coefficient for the B channel. 0x0800 - Default	
B1[12:0]			R/W
0x5E 0x5F	<u>00000000</u> <u>00000000</u>	This control is used to set the CSC coefficient B1. It contains a 13-bit B1 coefficient for the B channel. 0x0000 - Default	

Reg	Bits	Description	
C4[12:0]			R/W
0x60 0x61	00000000 00000000	This control is used to set the CSC coefficient C4. It contains a 13-bit C4 coefficient for the C channel. 0x0000 - Default	
C3[12:0]			R/W
0x62 0x63	00100000 00000000	This control is used to set the CSC coefficient C3. It contains a 13-bit C3 coefficient for the C channel. 0x0800 - Default	
C2[12:0]			R/W
0x63 0x64 0x65	00000000 00000000 00000000	This control is used to set the CSC coefficient C2. It contains a 13-bit C2 coefficient for the C channel. 0x0000 - Default	
C1[12:0]			R/W
0x65 0x66	00000000 00000000	This control is used to set the CSC coefficient C1. It contains a 13-bit C1 coefficient for the C channel. 0x0000 - Default	
EMB_SYNC_ON_ALL			R/W
0x67	00000000	This control is used to alter the gain computed by the AGC based on the presence of an embedded synchronization on channels A, B and C. It is used only in the case of RGB input and RGB output with color controls enabled. 0 - Embedded synchronization present only on luma channel (i.e. channel A) 1 - All three input channels have embedded synchronization	
CSC_COEFF_SEL[3:0]			R/W
0x68	11110000	This control is used to select the mode in which the CP CSC operates. 0000 - CP CSC configuration in manual mode 1111 - CP CSC configured in automatic mode xxxx - Reserved	
MAN_CP_CSC_EN			R/W
0x69	00000100	This control is used to manually enable the CP CSC. By default, the CP CSC is automatically enabled in the case where either a color space conversion or video adjustment (hue, saturation, contrast, or brightness) is determined to be required due to other I2C settings. If man_cp_csc_en is set to 1, the CP CSC is forced into the enabled state. 0 - CP CSC automatically enabled if required 1 - Manual override to force CP CSC to be enabled	
EIA_861_COMPLIANCE			R/W
0x69	00000100	This control is used to implement compliance to the CEA 861 standard for 525p inputs. It affects the start of the VBI for the 525p standard only. 0 - VBI region starts on line 1 1 - VBI region starts on line 523 (compliant with CEA 861 specification)	
CLMP_A_MAN			R/W
0x6C	00010000	This control is used to enable manual clamping for channel A. 0 - Use digital fine clamp value determined by on-chip clamp loop 1 - Ignore internal digital fine clamp loop result, use clmp_a[11:0]	
CLMP_BC_MAN			R/W
0x6C	00010000	This control is used to enable manual clamping for channels B and C. 0 - Use digital fine clamp value determined by on-chip clamp loop 1 - Ignore internal digital fine clamp loop result, use clmp_b[11:0] for channel B and clmp_c[11:0] for channel C	
CLMP_FREEZE			R/W
0x6C	00010000	This control is used to stop the digital fine clamp loops for channels A, B and C from updating. 0 - Clamp value updated on every active video line 1 - Clamp loops stopped and not updated	
CLMP_A[11:0]			R/W
0x6C 0x6D	00010000 00000000	This control is used to set the manual clamp value for channel A. It is an unsigned 12-bit value to be subtracted from the incoming video signal. The value programmed in this control is effective if clmp_a_man is set to 1. To change the clmp_a[11:0], the control addresses 0x6C and 0x6D must be updated with the desired clamp value written to in this order and with no other I2C access inbetween. 0x000 - Minimum range, - ... 0xFFFF - Maximum range	

Reg	Bits	Description	
CLMP_B[11:0]			R/W
0x6E 0x6F	00000000 00000000	This control is used to set the manual clamp value for channel B. This is an unsigned 12-bit value to be subtracted from the incoming video signal. The value programmed in this control is effective if clmp_bc_man is set to 1. To change clmp_b[11:0], the control addresses 0x6E and 0x6F must be updated with the desired clamp value written to in this order and with no other I2C access inbetween. 0x000 - Minimum range, - ... 0xFFFF - Maximum range	
CLMP_C[11:0]			R/W
0x6F 0x70	00000000 00000000	This control is used to set the manual clamp value for channel C. This is an unsigned 12-bit value to be subtracted from the incoming video signal. The value programmed in this control is effective if clmp_bc_man is set to 1. To change clmp_c[11:0], the control addresses 0x6F and 0x70 must be updated with the desired clamp value written to in this order and with no other I2C access inbetween. 0x000 - Minimum range, - ... 0xFFFF - Maximum range	
AGC_TAR[9:0]			R/W
0x71 0x72	00000000 00000000	This control is used to enable the manual AGC target value. It is used to set the target value for the horizontal synchronization depth after gain is applied. It is an unsigned value. This control is used to set the manual AGC target value. See the descriptions of agc_tar_man, agc_freeze and agc_tim. 0x000 - Minimum range, - ... 0x3FF - Maximum range	
AGC_TAR_MAN			R/W
0x71	00000000	This control is used to enable the manual target level. 0 - AGC operates based on 300 mV or 286 mV horizontal synchronization depth, use hs_norm to select 1 - AGC operates based on agc_tar[9:0]	
AGC_FREEZE			R/W
0x71	00000000	This control is used to enable AGC freeze. 0 - AGC loop operational. 1 - AGC loop frozen and not updated further. Last gain value becomes static.	
HS_NORM			R/W
0x71	00000000	This control is used to select the nominal HSync depth. 0 - AGC target scales video as per 300 mV horizontal synchronization depth 1 - AGC target scales video as per 286 mV horizontal synchronization depth	
AGC_TIM[2:0]			R/W
0x71	00000000	This control is used to select the AGC time constant. 000 - 100 lines 001 - 1 frame 010 - 0.5 sec 011 - 1 sec 100 - 2 sec 101 - 3 sec 110 - 5 sec 111 - 7 sec	
GAIN_MAN			R/W
0x73	00010000	This control is used to enable the gain factor to be set by the AGC or manually. 0 - AGC controls gain for all three channels 1 - Manual gains used for all three channels	
AGC_MODE_MAN			R/W
0x73	00010000	This control is used to set how the gain for all three channels is configured. 0 - Gain dependant on type of input and op_656_range 1 - Gain operation controlled by gain_man	
A_GAIN[9:0]			R/W
0x73 0x74	00010000 00000100	This control is used to set the manual gain value for channel A. It is an unsigned value in a 2.8 binary format. To change it, the control at addresses 0x73 and 0x74 must be written to in this order with no I2C access inbetween. 0x000 - Gain of 0 0x100 - Unity gain 0x3FF - Gain of 3.99	

Reg	Bits	Description	R/W
B_GAIN[9:0]			R/W
0x74 0x75	00000100 00000001	This control is used to set the manual gain value for channel B. It stores an unsigned value in a 2.8 binary format. To change it, the control at addresses 0x74 and 0x75 must be written to in this order with no I2C access inbetween. 0x000 - Gain of 0 0x100 - Unity gain 0x3FF - Gain of 3.99	
C_GAIN[9:0]			R/W
0x75 0x76	00000001 00000000	This control is used to set the manual gain value for channel C. It stores an unsigned value in a 2.8 binary format. To change it, the control at addresses 0x75 and 0x76 must be written to in this order with no I2C access inbetween. 0x000 - Gain of 0 0x100 - Unity gain 0x3FF - Gain of 3.99	
A_OFFSET[9:0]			R/W
0x77 0x78	11111111 11111111	This control is used to set the manual offset for channel A. This field stores an unsigned value. To change it, the register addresses 0x77 and 0x78 must be written to in this order with no I2C access inbetween. 0x3FF - Auto offset to channel A Any other value - Channel A offset	
B_OFFSET[9:0]			R/W
0x78 0x79	11111111 11111111	This control is used to set the manual offset for channel B. This field stores an unsigned value. To change it, the register addresses 0x77 and 0x78 must be written to in this order with no I2C access inbetween. 0x3FF - Auto offset to channel B Any other value - Channel B offset	
C_OFFSET[9:0]			R/W
0x79 0x7A	11111111 11111111	This control is used to set the manual offset for channel C. This field stores an unsigned value. To change it, the register addresses 0x79 and 0x7A must be written to in this order with no I2C access inbetween. 0x3FF - Auto offset to channel C Any other value - Channel C offset	
CP_INV_HS			R/W
0x7C	10000000	A control to set the polarity of the HSync/CSync output by the CP core. This control is not recommended for use. INV_HS_POL in IO Map, Register 0x06 [1] should be used instead. 0 - The CP outputs a HSync CSync with negative polarity 1 - The CP outputs a HSync CSync with positive polarity	
CP_INV_VS			R/W
0x7C	10000000	A control to set the polarity of the VSync output by the CP core. This control is not recommended for use. INV_VS_POL in IO Map, Register 0x06 [2] should be used instead. 0 - The CP outputs a VSync with negative polarity 1 - The CP outputs a VSync with positive polarity	
CP_INV_DE			R/W
0x7C	10000000	A control to set the polarity of the FIELD/DE output by the CP core. This control is not recommended for use. INV_F_POL in IO Map, Register 0x06 [3] should be used instead. 0 - The CP outputs FIELD/DE with negative polarity 1 - The CP outputs FIELD/DE with positive polarity	
START_HS[9:0]			R/W
0x7C 0x7E	11000000 00000000	This control is used to shift the position of the leading edge of the HSync output by the CP core. It stores a signed value in a twos complement format. This control is the number of pixel clocks by which the leading edge of the HSync is shifted (e.g. 0x3FF corresponds to a shift of one pixel clock away from the active video, 0x005 corresponds to a shift of five pixel clocks towards the active video). 0x000 - Default 0x000 to 0x1FF - Leading edge of HSync shifted towards active video 0x200 to 0x3FF - Leading edge of HSync shifted away from active video	
END_HS[9:0]			R/W
0x7C 0x7D	11000000 00000000	This control is used to shift the position of the trailing edge of the HSync output by the CP core. It stores a signed value in a twos complement format. This control is the number of pixel clocks by which the trailing edge of the HSync is shifted (e.g. 0x3FF corresponds to a shift of one pixel clock away from the active video, 0x005 corresponds to a shift of five pixel clocks towards the active video). 0x000 - Default 0x000 to 0x1FF - Trailing edge of HSync shifted towards active video 0x200 to 0x3FF - Trailing edge of HSync shifted away from active video	

Reg	Bits	Description	
START_VS[3:0]			R/W
0x7F	00000000	This control is used to shift the position of the leading edge of the Vsync output by the CP core. It stores a signed value in a twos complement format. This control is the number of lines by which the leading edge of the Vsync is shifted (e.g. 0x0F corresponds to a shift by one line towards the active video, 0x01 corresponds to a shift of one line away from the active video). 0x0 - Default 0x0 to 0x7 - Leading edge of VSync shifted towards active video 0x8 to 0xF - Leading edge of VSync shifted away from active video	
END_VS[3:0]			R/W
0x7F	00000000	This control is used to shift the position of the trailing edge of the Vsync output by the CP core. It stores a signed value in a twos complement format. This control is the number of lines by which the trailing edge of the Vsync is shifted (e.g. 0x0F corresponds to a shift of one line towards the active video, 0x01 corresponds to a shift of one line away from the active video). 0x0 - Default 0x0 to 0x7 - Trailing edge of VSync shifted towards active video 0x8 to 0xF - Trailing edge of VSync shifted away from active video	
MEAS_WL[1:0]			R/W
0x81	11000000	This control is used to set the width of the window length used for noise calibration measurements. The unit is a pixel clock cycle. Refer to noise[7:0] and calib[10:0]. 00 - Window length of 128 LLC clock cycles 01 - Window length of 64 LLC clock cycles 10 - Window length of 32 LLC clock cycles 11 - Window length of 16 LLC clock cycles	
GR_AV_BL_EN			R/W
0x81	11000000	This control is used to enable the insertion of data blanking and AV codes for autographic mode. 0 - Disable data blanking and AV code insertion for autographic mode 1 - Enable data blanking and AV code insertion for autographic mode	
MEAS_WS[11:0]			R/W
0x81 0x82	11000000 00000100	This control is used to set the start value of the measurement window use for noise and calibration. The unit is a pixel clock cycle. Refer to noise[7:0] and calib[10:0]. A value of 0 positions the start of the window at the trailing edge of the incoming Hsync. 0x000 - Start value (in LLC clock cycles) of measurement window 0x004 - Default	
ISD_THR[7:0]			R/W
0x83	00000000	This control is used to set the threshold used for the ISD measurement. Isd_thr[7:0] stores a 12-bit unsigned value. 0x00 - Calculate threshold automatically and set to (level of HSync tip) + 0.5 * (HSync depth) >0x01 - Set threshold to (isd_thr[7:0] * 8)	
CP_GAIN_FILT[3:0]			R/W
0x84	00001100	This control is used to set the coefficient A of the IIF filter to filter the gain applied to the video signal when the gain is set manually. The value set in this control is effective only when manual gain is enabled. The filter is designed as an IIR filter with a transfer function of the form $Y[N] = (1-A)y[N-1] + A * X[N]$. 0000 - No filtering, i.e. coefficient A = 1 0001 - Coefficient A = 1/128 lines 0010 - Coefficient A = 1/256 lines 0011 - Coefficient A = 1/512 lines 0100 - Coefficient A = 1/1024 lines 0101 - Coefficient A = 1/2048 lines 0110 - Coefficient A = 1/4096 line	
CH1_SSPD_PP_EN			R/W
0x84	00001100	This control is used to enable sync channel 1 SSPD post processing. 0 - Disable post processing of synchronization signals input to sync channel 1 SSPD 1 - Check for activity on embedded synchronization signal input to sync channel 1 SSPD when it detects activity on HSync, CSync and VSync. Activity on embedded signal input	
IFSD_AVG			R/W
0x84	00001100	This control is used to set the averaging mode used to compute ifsd[8:0]. 0 - ifsd[8:0] averaged over 128 lines of video to generate ifsd[8:0] 1 - ifsd[8:0] averaged over 256 lines of video to generate ifsd[8:0]	

Reg	Bits	Description	
CH1_POL_MAN_EN			R/W
0x85	00000011	This control is used to override for polarity detection by sync channel 1 SSPD. ch1_pol_man_en must be set to 1 for this control to become active. 0 - Use result from sync channel 1 SSPD polarity autodetection 1 - Manual override, use ch1_pol_vs and ch1_pol_hs	
CH1_POL_VS			R/W
0x85	00000011	This control is used to override the polarity of VSync by sync channel 1 SSPD. 0 - VSync input to sync channel 1 carries negative polarity signal 1 - VSync input to sync channel 1 carries positive polarity signal	
CH1_POL_HSCS			R/W
0x85	00000011	This control is used to override the polarity of HSync by sync channel 1 SSPD. ch1_pol_man_en must be set to 1 for this control to become active. 0 - HSync input to sync channel 1 carries negative polarity signal (HSync or CSync) 1 - HSync input to sync channel 1 carries positive polarity signal (HSync or CSync)	
CH1_SYNC_SRC[1:0]			R/W
0x85	00000011	This control is used to select the synchronization signals processed by sync channel 1 SSPD. 00 - Autodetect mode for synchronization source. Use results of autodetection for synchronization signal routing. Result can be read back via ch1_cur_sync[1:0] bits. 01 - Manual setting: separate HSync and VSync to sync channel 1 SSPD. 10 - Manual setting	
CH1_TRIG_SSPD			R/W
0x85	00000011	This control is used to trigger a synchronization source and polarity detector for sync channel 1 SSPD. A 0 to 1 transition in this bit restarts the autosync detection algorithm. This is not a self clearing bit and must be set to 0 to prepare for the next trigger. 0 - Default - transition 0 to 1 restarts autosync detection algorithm 1 - Transition 0 to 1 restarts autosync detection algorithm	
CH1_SSPD_CONT			R/W
0x85	00000011	This control is used to set the synchronization source polarity detection mode for sync channel 1 SSPD. 0 - Sync channel 1 SSPD works in one-shot mode (triggered by 0 to 1 transition on ch1_trig_sspd bit) 1 - Sync channel 1 SSPD works in continuous mode	
CH1_TRIG_STDI			R/W
0x86	00001011	This control is used to trigger a synchronization source and polarity detector for sync channel 1 STDI. A 0 to 1 transition in this bit restarts the autosync detection algorithm. This is not a self clearing bit and must be set to 0 to prepare for the next trigger. 0 - Default - transition 0 to 1 restarts autosync detection algorithm 1 - Reset to zero to prepare for next trigger	
CH1_STDI_CONT			R/W
0x86	00001011	This control is used to set the synchronization source polarity detection mode for sync channel 1 STDI 0 - Sync channel 1 STDI works in one-shot mode (triggered by 0 to 1 transition on ch1_trig_sspd) 1 - Sync channel 1 STDI works in continuous mode	
DE_V_START_EVEN[5:0]			R/W
0x87	00000000	This control is used to vary the start position of the VBI region in an even field. It stores a signed value represented in a twos complement format. The unit of adjustment is one line. 100000...111111 - -32 lines ... -1 line 000000 - Default (0 lines) 000000...011111 - 1 line ... 31 lines	
DE_V_END_EVEN[5:0]			R/W
0x88	00000000	This control is used to vary the position of the end of the VBI region in an even field. It stores a signed value represented in a twos complement format. The unit of adjustment is one line. 100000...111111 - -32 lines ... -1 line 000000 - Default (0 lines) 000000...011111 - 1 line ... 31 lines	

Reg	Bits	Description	
START_VS_EVEN[3:0]			R/W
0x89	00000000	This control is used to shift the position of the leading edge of the VSync output by the CP core. It stores a signed value in a twos complement format. start_vs_even[3:0] is the number of lines by which the leading edge of the VSync is shifted (e.g. 0x0F corresponds to a shift by one line towards the active video, 0x01 corresponds to a shift of one line away from the active video). 0x0 to 0x7 - Leading edge of even VSync shifted towards active video 0x8 to 0xF - Leading edge of even VSync shifted away from active video	
END_VS_EVEN[3:0]			R/W
0x89	00000000	This control is used to shift the position of the trailing edge of the VSync output by the CP core. It stores a signed value in a twos complement format. end_vs_even[3:0] is the number of lines by which the trailing edge of the VSync is shifted (e.g. 0x0F corresponds to a shift by one line towards the active video, 0x01 corresponds to a shift of one line away from the active video). 0x0 to 0x7 - Trailing edge of even VSync shifted towards active video 0x8 to 0xF - Trailing edge of even VSync shifted away from active video	
IGNR_CLMP_VS_MAR_END[4:0]			R/W
0x8A	00100000	This control is used to set the end of the window during which the clamp is ignored. It stores the unsigned number of pixel clocks between the end position of the window relative to the trailing edge of the Vsync. This control should only be used if vid_std[5:0] is set for autographics mode. 0x04 - Default	
IGNR_CLMP_VS_MAR_START[4:0]			R/W
0x8A 0x8B	00100000 01000000	This control is used to set the start of the window during which the clamp is ignored. It stores the unsigned number of pixel clocks between the start position of the window relative to the leading edge of the VSync. This control should only be used if vi 0x04 - Default	
DE_H_START[9:0]			R/W
0x8B 0x8D	01000000 00000000	This control is used to vary the leading edge position of the DE signal output by the CP core. It stores a signed value in a twos complement format. The unit of de_h_start[9:0] is one pixel clock. 0x200 - -512 pixels of shift 0x3FF - -1 pixel of shift 0x000 - Default (no shift) 0x001 - +1 pixel of shift 0x1FF - +511 pixels	
DE_H_END[9:0]			R/W
0x8B 0x8C	01000000 00000000	This control is used to vary the trailing edge position of the DE signal output by the CP core. It stores a signed value in a twos complement format. The unit of de_h_end[9:0] is one pixel clock. 0x200 - -512 pixels of shift 0x3FF - -1 pixel of shift 0x000 - Default (no shift) 0x001 - +1 pixel of shift 0x1FF - +511 pixels	
CH1_FR_LL[10:0]			R/W
0x8F 0x90	00000000 00000000	This control is used to set the free run line length in a number of crystal clock cycles in one line of video for sync channel 1 STD1. It should be programmed only with video standards that are not supported by prim_mode[3:0] and vid_std[5:0]. 0x000 - Internal free run line length decoded from prim_mode[3:0] and vid_std[5:0]. All other values - Number of crystal clocks in ideal line length. Used to enter or exit free run mode.	
MAN_PARM			R/W
0x91	01000000	This control is used to enable the CP output timing controls in autographics mode. 1 - Use manual parameters programmed 0 - Use parameters from internal ROM	
INTERLACED			R/W
0x91	01000000	This control is used to set the interlaced or progressive mode of the incoming video processed in CP mode. 0 - CP core expects video mode is progressive 1 - CP core expects video mode is interlaced	

Reg	Bits	Description	
DE_V_START[5:0]			R/W
0x98	00000000	This control is used to vary the start position of the VBI region. It stores a signed value represented in a twos complement format. The unit of de_v_start[5:0] is one line. 100000 --32 lines of shift 1111 11 --1 line of shift 000000 - Default 000001 - +1 line of shift 011111 - +31 lines of shift	
DE_V_END[5:0]			R/W
0x99	00000000	This control is used to vary the position of the end of the VBI region. It stores a signed value represented in a twos complement format. The unit of de_v_end[5:0] is one line. 100000 --32 lines of shift 1111 11 --1 line of shift 000000 - Default 000001 - +1 line of shift 011111 - +31 lines of shift	
CP_START_VS[5:0]			R/W
0x9A	00000000	This control is used to set the position of the start of the VSync output signal in the CP core in autographics mode only. In the case of an interlaced signal, this control adjusts the odd VS signal. Programming of this control is optional and should only be performed when the part is set in autographics mode. The value is unsigned. 000000 - Default	
CP_END_VS[5:0]			R/W
0x9B	00000000	This control is used to set the position of the end of the Vsync output signal in the CP core in autographics mode only. In the case of an interlaced signal, this control adjusts the odd VS signal. Programming of this control is optional and should only be performed when the part is set in autographics mode. The value is unsigned. 000000 - Default	
CP_START_VS_EVEN[10:0]			R/W
0x9C 0x9D	00000000 00000000	This control is used to set the position of the start of the even VSync output signal in the CP core in autographics mode only. Programming of this control is optional and should only be performed when the part is set in autographic mode. The value is unsigned. 0x000 - Default	
CP_END_VS_EVEN[10:0]			R/W
0x9D 0x9E	00000000 00000000	This control is used to set the position of the end of the even VSync output signal in the CP core in autographic mode only. Programming of this control is optional and should only be performed when the part is set in autographic mode. The value is unsigned. 0x000 - Default	
CP_START_F_ODD[10:0]			R/W
0x9F 0xA0	00000000 00000000	This control is used to set the position of the end of the odd field output signal in the CP core in autographic mode only. Programming of this control is optional and should only be performed when the part is set in autographic mode. The value is unsigned. 0x000 - Default	
CP_START_F_EVEN[10:0]			R/W
0xA0 0xA1	00000000 00000000	This control is used to set the position of the end of the even field output signal in the CP core in autographic mode only. Programming of this control is optional and should only be performed when the part is set in autographic mode. The value is unsigned. 0x000 - Default	
CH1_LCF[11:0]			R
0xA3 0xA4	00000000 00000000	This readback displays the sync channel 1 line count in a field. The number of lines between two VSynCs is measured on sync channel 1. The readback is valid if ch1_std_dvalid is set to 1. xxxxxxxxxx - Readback value	
CP_START_VBI[11:0]			R/W
0xA5 0xA6	00000000 00000000	This control is used to set the manual value for the start of the VBI region position (of odd fields in case of interlaced output). This is an unsigned value. It sets the total number of lines at the start of a frame of non interlaced standard video. Programming is optional and should only be performed when the part is set in autographics mode. 0x000 - Default	

Reg	Bits	Description	
CP_END_VBI[11:0]			R/W
0xA6 0xA7	00000000 00000000	This control is used to set a manual value for the end of the VBI region position (of odd fields in the case of interlaced output). It is an unsigned value. It sets the total number of lines at the end of a frame of noninterlaced standard video. It sets the total number of lines at the end of the odd frame of interlaced standard video. Programming is optional and should only be performed when the part is set in autographics mode. 0x000 - Default	
CP_START_VBI_EVEN[11:0]			R/W
0xA8 0xA9	00000000 00000000	This control is used to set a manual value for the start of the VBI in even fields. It is an unsigned value. It sets the total number of lines at the start of the even frame of interlaced standard. Programming is optional and should only be performed when the part is set in autographics mode. 0x000 - Default	
CP_END_VBI_EVEN[11:0]			R/W
0xA9 0xAA	00000000 00000000	This control is used to set the manual value for the end of the VBI region position for even fields. It is an unsigned value. It sets the total number of lines at the end of the even frame of interlaced standard. Programming is optional and should only be performed when the part is set in autographics mode. 0x000 - Default	
CP_LCOUNT_MAX[11:0]			R/W
0xAB 0xAC	00000000 00000000	This control is used to set a manual value for the total number of lines in a frame expected by the CP core. This control is used for the manual configuration of the free run feature. The value programmed here is used for sync channel 1 and is also used for sync channel 2 if ch2_fr_field_length[10:0] is set to 0x000. It is an unsigned value. 0x000 - Ideal number of lines per frame decoded from prim_mode[3:0] and vid_std[5:0] for sync channel 1 All other values - Use programmed value as ideal number of lines per frame in free run decision for sync channel 1	
CH1_STDI_DVALID			R
0xB1	00000000	This readback is set when the measurements performed by sync channel 1 STDI are completed. A high level indicates ch1_bl, ch1_lcf, ch1_lcv, ch1_fcl, and chi_stdi_intlcd are valid readback. To prevent false readouts, especially during signal acquisition, ch1_stdi_dvalid is set to 1 only after four fields with the same length are recorded. As a result, STDI measurements can take up to five fields to finish. 0 - Sync channel 1 STDI measurement not valid 1 - Sync channel 1 STDI measurement valid	
CH1_STDI_INTLCD			R
0xB1	00000000	This readback displays interlaced versus progressive mode detected by sync channel 1 STDI. The readback is valid if ch1_stdi_dvalid is set to 1. 0 - Indicates video signal on sync channel 1 with non interlaced timing 1 - Indicates signal on sync channel 1 with interlaced timing	
CH1_BL[13:0]			R
0xB1 0xB2	00000000 00000000	This readback displays the block length for sync channel 1. It displays the number of crystal clock cycles in a block of eight lines of incoming video. This readback is valid if ch1_stdi_dvalid is set to 1. xxxxxxxxxxxx - Readback value	
CH1_LCVS[4:0]			R
0xB3	00000000	This readback displays the sync channel 1 line count in a VSync. It displays the number of lines in a VSync period measured on sync channel 1. The readback is valid if ch1_stdi_dvalid is set to 1. xxxxx - Readback value	
CH1_SSPD_DVALID			R
0xB5	00000000	This control is set to 1 when the readbacks from the SSPD section of the synchronization sync channel 1 are valid. It is set to 1 after 2 ²² crystal clock periods following a reset of the CP section. It is set to 0 when the device is reset. 0 - Sync channel 1 SSPD results not valid for readback 1 - Sync channel 1 SSPD results valid	
CH1_VS_ACT			R
0xB5	00000000	This readback indicates activity on VSync input to sync channel 1 SSPD. 0 - No activity detected on VSync input to sync channel 1 SSPD 1 - VSync input to sync channel 1 SSPD carries an active signal	
CH1_CUR_POL_VS			R
0xB5	00000000	This readback indicates polarity on the HSync/CSync input to sync channel 1 SSPD. 0 - VSync input to sync channel 1 SSPD has negative polarity signal 1 - VSync input to sync channel 1 SSPD has positive polarity signal	

Reg	Bits	Description	
CH1_HS_ACT			R
0xB5	000 <u>00000</u>	This readback indicates activity on the HSync/CSync input to sync channel 1 SSPD. 0 - No activity detected on HSync/CSync input to sync channel 1 SSPD 1 - HSync/CSync input to sync channel 1 SSPD carries an active signal	
CH1_CUR_POL_HS			R
0xB5	0000 <u>0000</u>	This readback indicates the polarity of the HSync/CSync input to the sync channel 1 SSPD. 0 - Negative polarity on HSync/CSync input to sync channel 1 SSPD 1 - Positive polarity on HSync/CSync input to sync channel 1 SSPD	
CH1_RS_ACTIVE			R
0xB5	0000 <u>0000</u>	This readback indicates activity in the embedded synchronization signal input to sync channel 1 SSPD. ch1_sspd_pp_en must be set to 1 and ch1_sspd_dvalid must return 1 for this readback to be valid. 0 - Activity detected on embedded signal input to sync channel 1 SSPD 1 - No activity detected on embedded signal input to sync channel 1 SSPD	
CH1_CUR_SYNC_SRC[1:0]			R
0xB5	0000 <u>0000</u>	This readback displays the current synchronization source detected by sync channel 1 SSPD. 00 - Not used 01 - Activity detected on HSync and VSync input to sync channel 1 SSPD 10 - CSync detected on HSync input to sync channel 1 SSPD 11 - Activity detected on embedded synchronization input to sync channel 1 SSPD	
CH1_FCL[12:0]			R
0xB8 0xB9	000 <u>00000</u> 00000000	This readback displays the sync channel 1 field count length. It displays the number of crystal clock cycles between successive VSynCs measured by sync channel 1 STDI or in 1/256th of a field. The readback from this field is valid if ch1_stdi_dvalid is set. xxxxxxxxxxxx - Readback value	
HDMI_FRUN_MODE			R/W
0xBA	00000 <u>001</u>	This control is used to configure the free run feature in HDMI mode. 0 - HDMI free run mode 0. Part free runs when TMDS clock not detected on selected HDMI port. 1 - HDMI free run mode 1. CP core free runs when TMDS clock not detected on selected HDMI port or if video resolution of HDMI stream processed by part does not m	
HDMI_FRUN_EN			R/W
0xBA	000000 <u>01</u>	This control is used to enable free run in HDMI mode. 0 - Disable free run feature in HDMI mode 1 - Enable free run feature in HDMI mode	
DLY_A			R/W
0xBE	<u>0</u> 0000100	This control is used to delay the data on channel A by one pixel clock cycle. 1 - Delay data of channel A by one pixel clock cycle 0 - Do not delay data of channel A	
DLY_B			R/W
0xBE	<u>00</u> 000100	This control is used to delay the data on channel B by one pixel clock cycle. 1 - Delay data of channel B by one pixel clock cycle 0 - Do not delay data of channel B	
DLY_C			R/W
0xBE	00 <u>00</u> 0100	This control is used to delay the data on channel C by one pixel clock cycle. 1 - Delay data of channel C by one pixel clock cycle 0 - Do not delay data of channel C	
HCOUNT_ALIGN_ADJ[4:0]			R/W
0xBE 0xBF	0000 <u>0100</u> <u>000</u> 10010	This control is used to manually adjust for internally generated hcount offset. The control allows an adjustment of 15 pixels to the left or to the right. The MSB sets the direction (left or right) and the four LSBs set the number of pixels to move. 00000 - Default	
CP_DEF_COL_MAN_VAL			R/W
0xBF	0001 <u>0010</u>	This control is used to enable the manual selection of the color used when the CP core free runs. 0 - Use default color blue 1 - Output default colors as given in cp_def_col_cha, cp_def_col_chb and cp_def_col_chc	

Reg	Bits	Description	
CP_DEF_COL_AUTO			R/W
0xBF	00010010	This control is used to enable the insertion of the default color when the CP free runs. 0 - Disable automatic insertion of default color 1 - Output default colors when CP free runs	
CP_FORCE_FREERUN			R/W
0xBF	00010010	This control is used to force the CP to free run. 0 - Do not force CP core free run 1 - Force CP core to free run	
DEF_COL_CHA[7:0]			R/W
0xC0	00000000	This control is used to set the default color for channel A. It is used if cp_def_col_man_val is set at 1. 0x00 - Default	
DEF_COL_CHB[7:0]			R/W
0xC1	00000000	This control is used to set the default color for channel B. It is used if cp_def_col_man_val is set at 1. 0x00 - Default	
DEF_COL_CHC[7:0]			R/W
0xC2	00000000	This control is used to set the default color for channel C. It is used if cp_def_col_man_val is set at 1. 0x00 - Default	
CLAMP_AVG_FCTR[1:0]			R/W
0xC5	10010001	This control is used to set the coefficient A of the IIR filter used for aut clamp mode. The function transfer is $Y[N]=(1-A)*Y[N-1]+A*X[N]$. 00 - No filtering, A=1 01 - Clamp is averaged over 8 lines, A=1/8 10 - Clamp is averaged over 16 lines, A=1/16 11 - Clamp is averaged over 32 lines, A=1/32	
CP_ANVC_POS_START[12:0]			R/W
0xC6 0xC9 0xCA	00000000 00101100 00000000	This control is used to set the start of the window for analog voltage clamp measurement (new clamping scheme). It is unsigned. 0x0000 - Default	
CP_ANVC_POS_DURATION[7:0]			R/W
0xC7	00000000	This control is used to set the duration of the window for analog voltage clamp measurement (new clamping scheme). It is unsigned. 0x0000 - Default	
CP_DFC_POS_START[12:0]			R/W
0xC8 0xC9 0xCA	00000000 00101100 00000000	This control is used to set the start of the window for digital fine clamp measurement (new clamping scheme). It is unsigned. 0x0000 - Default	
DIS_AUTO_PARAM_BUFF			R/W
0xC9	00101100	This control is used to disable the buffering of the timing parameters used for free run in HDMI mode. 0 - Buffer last measured parameters in HDMI mode used to determine video resolution into which part free runs. 1 - Disable buffering of measured parameters in HDMI mode. Free run standard determined by prim_mode[3:0], vid_std[5:0] and v_freq[2:0].	
HDMI_CP_LOCK_THRESHOLD[1:0]			R/W
0xCB	01100000	This control is used to show the locking time of the filter used for the buffering of timing parameters in HDMI mode. 00 - Slowest locking time 01 - Medium locking time 10 - Fastest locking time 11 - Fixed step size of 0.5 pixel	
PW_WIN_MAN			R/W
0xDA	00000000	This control is used to configure the peak white window. 0 - Use active window generated for peak white measurement 1 - Use specified manual peak white window	
PW_SHOW_WIN			R/W
0xDA	00000000	This control is used to show the peak white window. 0 - Do not show peak white window 1 - Show peak white window	

Reg	Bits	Description	
PW_VB[7:0]			R/W
0xDB	00011001	This control is used to show the value of the beginning of the peak white window in a field. It stores an unsigned value. 0x19 - Default	
PW_VL[7:0]			R/W
0xDC	01100100	This control is used to show the value of the end of the peak white window in a field. It stores an unsigned value. 0x64 - Default	
PW_HB[11:0]			R/W
0xDD 0xDE	00010010 11000101	This control is used to show the value of the beginning of the peak white window in a line. It stores an unsigned value. 0x12C - Default	
PW_HL[11:0]			R/W
0xDE 0xDF	11000101 01111000	This control is used to show the value of the end of the peak white window in a line. It stores an unsigned value. 0x578 - Default	
HDMI_CP_AUTOPARM_LOCKED			R
0xE0	00000000	This readback indicates the lock status of the parameter buffering in HDMI mode. 0 - Do not lock parameter buffering block to synchronization signal from HDMI core 1 - Lock parameter buffering block to synchronization signal from HDMI core	
HDMI_AUTOPARM_STS[1:0]			R
0xE0	00000000	This readback indicates the CP status in HDMI mode. 00 - CP free running according to timing parameters programmed in prim_mode[3] and vid_std[5] 01 - Timing buffer filter locked to HDMI input 10 - CP free running according to HDMI buffered parameters 11 - Reserved	
CP_AGC_GAIN[9:0]			R
0xE0 0xE1	00000000 00000000	This readback displays the value of the gain used on the data of channel A. This value is in a 1.9 binary format and is composed of one integer and nine fractional bits. xxxxxxxx - Readback value of gain	
NOISE[7:0]			R
0xE2	00000000	This readback displays the noise value measured on the luma channel (i.e. channel A). It provides an unsigned value representing the difference between the maximum and minimum value measured during the window configured by meas_ws[11:0] and meas_wl[1:0]. xxxxxxxx - Readback value	
CALIB[10:0]			R
0xE3 0xE6	00000000 00000000	This readback displays the calibration value measured on the luma channel (i.e. channel A). It provides a signed value representing the average level over the extent of the window configured by meas_ws[11:0] and meas_wl[1:0]. xxxxxxxxxx - Readback value	
IFSD[8:0]			R
0xE3 0xE5	00000000 00000000	This readback displays the average value of the ISD measurement over 128 or 256 lines. The number of lines used to compute ifsd[8:0] is set in ifsd_avg. xxxxxxxx - Readback value	
ISD[8:0]			R
0xE3 0xE4	00000000 00000000	This readback represents the area of the HSync that falls below the slicing threshold set by isd_thr[7:0]. A high value indicates robust locking. xxxxxxxx - Readback value	
HSD_CHC[9:0]			R
0xE7 0xEA	00000000 00000000	This readback displays the measured value of the HSync depth on channel C before the gain multiplier. The value is presented in 1.9 binary format. xxxxxxxxxx - Readback for measured value of HSync depth on channel C	
HSD_CHB[9:0]			R
0xE7 0xE9	00000000 00000000	This readback displays the measured value of the HSync depth on channel B before the gain multiplier. The value is presented in 1.9 binary format. xxxxxxxxxx - Readback for measured value of HSync depth on channel B	

Reg	Bits	Description	
HSD_CHA[9:0]			R
0xE7 0xE8	00000000 00000000	This readback displays the measured value of the HSync depth on channel A before the gain multiplier. The value is presented in 1.9 binary format. xxxxxxxx - Readback for measured value of HSync depth on channel A	
HSD_FB[11:0]			R
0xEB 0xEC	00000000 00000000	This readback displays the measured value of Hsync depth on channel A, after gain multiplier, for an external feedback loop. The value is presented in twos complement form. This means that only a standard adder is needed to subtract the actual Hsync depth (as per hsd_fb) from a nominal value, as the hsd_hb value is already in negative format. xxxxxxxx - Readback value	
PKV_CHA[9:0]			R
0xED 0xEE	00000000 00000000	This readback displays the maximum signal level measured during the active video on channel A. xxxxxxxx - Readback value	
PKV_CHB[9:0]			R
0xED 0xEF	00000000 00000000	This readback displays the maximum signal level measured during the active video on channel B. xxxxxxxx - Readback value	
PKV_CHC[9:0]			R
0xED 0xF0	00000000 00000000	This readback displays the maximum signal level measured during the active video on channel C. xxxxxxxx - Readback value	
CH1_FL_FR_THRESHOLD[2:0]			R/W
0xF3	11010100	This readback indicates the threshold for the difference between the input video field length and the internally stored standard to enter and exit free run. 000 - Minimum difference to switch into free run is 36 lines. Maximum difference to switch out of free run is 31 lines. 001 - Minimum difference to switch into free run is 18 lines. Maximum difference to switch out of free run is 15 lines. 010 - Minimum d	
CH1_F_RUN_THR[2:0]			R/W
0xF3	11010100	This control is used to select the free run threshold for sync channel 1. It determines the horizontal conditions under which free run mode is entered or left. The length of the incoming video line is measured based on the crystal clock and is compared to an internally stored parameter. The magnitude of the difference decides whether or not sync channel 1 will enter free run mode. 000 - Minimum difference to switch into free run is 2. Maximum difference to switch out of free run is 1. 001 - Minimum difference to switch into free run is 256. Maximum difference to switch out of free run is 200. 010 - Minimum difference to switch into	
CSC_COEFF_SEL_RB[3:0]			R
0xF4	00000000	This readback displays the CP CSC conversion when configured in automatic mode. 0000 - CSC bypassed 0001 - YPbPr 601 to RGB 0011 - YPbPr 709 to RGB 0101 - RGB to YPbPr 601 0111 - RGB to YPbPr 709 1001 - YPbPr 709 to YPbPr 601 1010 - YPbPr 601 to YPbPr 709 1111 - CSC in manual mode xxxx - Reserved	
WD_TIMER_DIS			R/W
0xF5	00000000	This control is used to disable the watchdog timer. The watchdog timer is used for generating pulses in the absence of a frame start detection pulse when parameters like pll_div_ratio are to be updated on the VSync. 0 - Enable watchdog timer 1 - Disable watchdog timer	
DIG_SYNC DEGLITCH REDUCE			R/W
0xF5	00000000	This control is used to configure the deglitch filters that process synchronization signals before they are input to the SSPD section. The value set is effective if dig_sync_deglitch_reduce_man is set to 1. 1 - Remove 2 xtal clock wide glitches from synchronization signals input to SSPD sections 0 - Remove 5 xtal clock wide glitches from synchronization signals input to SSPD sections	

Reg	Bits	Description	
DIG_SYNC_DEGLITCH_REDUCE_MAN			R/W
0xF5	00000000	This control is used to manually configure the deglitch filters that process synchronization signals input to the SSPD sections. 1 - Manual configuration: deglitch filters configured via dig_sync_deglitch_reduce 0 - Automatic configuration: deglitch filters remove 5 xtal clock wide glitches from synchronization signals input to SSPD section	
BYPASS_STDI1_LOCKING			R/W
0xF5	00000000	This control is used to bypass STDI locking for sync channel 1. 0 - Update ch1_bl, ch1_lcf and ch1_lcv. Only sync channel 1 STDI locks and ch1_stdi_dvalid set to 1. 1 - Update ch1_bl, ch1_lcf and ch1_lcv from sync channel 1 STDI as they are measured.	
BYPASS_STDI2_LOCKING			R/W
0xF5	00000000	This control is used to bypass STDI locking for sync channel 2. 0 - Update ch2_bl, ch2_lcf and ch2_lcv. Only sync channel 2 STDI locks and ch2_stdi_dvalid set to 1. 1 - Update ch2_bl, ch2_lcf and ch2_lcv from sync channel 2 STDI as they are measured.	
MV_PS_DET			R
0xFF	00000000	This readback indicates the Macrovision pseudo pulses detection status. 0 - No Macrovision pseudo synchronization pulses detected 1 - Detected Macrovision pseudo synchronization pulses	
MV_AGC_DET			R
0xFF	00000000	This readback indicates the Macrovision AGC pulses detection status. 0 - Macrovision AGC pulses not detected by CP 1 - CP detected Macrovision AGC pulses	
CP_FREE_RUN			R
0xFF	00000000	This readback indicates the component processor free run status. 0 - CP not free running 1 - CP free running	

2.5 ADDR 48 (VDP)

Reg	Bits	Description	
VDP_CGMS_TYPEB_DATA[7:0]			R
0x3C	00000000	This readback displays byte 1 of decoded CGMS type B data. xxxxxxx - Byte 1 of decoded CGMS type B data	
VDP_CGMS_TYPEB_DATA[15:8]			R
0x3D	00000000	This readback displays byte 2 of decoded CGMS type B data. xxxxxxx - Byte 2 of decoded CGMS type B data	
VDP_CGMS_TYPEB_DATA[23:16]			R
0x3E	00000000	This readback displays byte 3 of decoded CGMS type B data. xxxxxxx - Byte 3 of decoded CGMS type B data	
VDP_CGMS_TYPEB_DATA[31:24]			R
0x3F	00000000	This readback displays byte 4 of decoded CGMS type B data. xxxxxxx - Byte 4 of decoded CGMS type B data	
VDP_STATUS_TTXT			R
0x40	00000000	This readback displays the Teletext detection status. 0 - Teletext not detected 1 - Teletext detected	
VDP_STATUS_VITC			R
0x40	00000000	This readback displays the VITC detection status. 0 - VITC data not detected 1 - VITC data detected	
VDP_STATUS_GEMS_TYPE			R
0x40	00000000	This readback displays the Gemstar type. 0 - Gemstar 1X detected 1 - Gemstar 2X detected	
VDP_STATUS_GS_VPS_PDC_UTC_CGMSTB			R
0x40	00000000	This readback displays the Gemstar, VPS, PDC, UTC, and CGMS type B data detection status. 0 - Gemstar, VPS, PDC, UTC, and CGMS type B data not detected 1 - Gemstar, VPS, PDC, UTC, and CGMS type B data detected	
VDP_STATUS_WSS_CGMS			R
0x40	00000000	This readback displays the WSS or CGMS type A data detection status. 0 - WSS or CGMS type A data not detected 1 - WSS or CGMS type A data detected	
VDP_STATUS_CCAP_EVEN_FIELD			R
0x40	00000000	This readback displays the closed caption data in the even field status. 0 - Closed caption data not detected in even field 1 - Closed caption data detected in even field	
VDP_STATUS_CCAP			R
0x40	00000000	This readback displays the closed caption data detection status. 0 - Closed caption data not detected 1 - Closed caption data detected	
VDP_CCAP_DATA[7:0]			R
0x41	00000000	This readback displays byte 1 of the decoded closed caption data. xxxxxxx - Byte 1 of decoded closed caption data	
VDP_CCAP_DATA[15:8]			R
0x42	00000000	This readback displays byte 2 of the decoded closed caption data. xxxxxxx - Byte 2 of decoded closed caption data	
VDP_CGMS_WSS_DATA[23:0]			R
0x43	00000000	This readback displays decoded data for CGMS type A and WSS. vdp_cgms_wss_data[23:0] - decoded CGMS[23:0] data vdp_cgms_wss_data[13:0] - decoded WSS[13:0] data	
0x44	00000000		
0x45	00000000		

Reg	Bits	Description	
VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[95:0]			R
0x47	00000000	This readback displays the decoded Gemstar, PDC, VPS, UTC, or CGMS type B data.	
0x48	00000000		
0x49	00000000		
0x4A	00000000		
0x4B	00000000		
0x4C	00000000		
0x4D	00000000		
0x4E	00000000		
0x4F	00000000		
0x50	00000000		
0x51	00000000		
0x52	00000000		
VDP_GS_VPS_PDC_UTC_CGMSTB_DATA[103:96]			R
0x53	00000000	This readback displays decoded Gemstar, PDC, VPS, UTC or CGMS type B data. xxxxxxx - Readback value	
VDP_VITC_DATA[71:0]			R
0x55	00000000	This readback displays decoded VITC data.	
0x56	00000000		
0x57	00000000		
0x58	00000000		
0x59	00000000		
0x5A	00000000		
0x5B	00000000		
0x5C	00000000		
0x5D	00000000		
VDP_VITC_CALC_CRC[7:0]			R
0x5E	00000000	This readback indicates the calculated CRC value for decoded VITC data. xxxxxxx - Readback value	
EN_FC_WINDOW_AFTER_CRI_DET			R/W
0x60	00001000	This control is used to select between the different methods of clock run in detection. Scheme 1 specifies a large timing window in which color burst, CRI, and FC must be accommodated. Scheme 2 specifies a timing window for framing code detection only. Th 1 - Default	
VDP_TTXT_TYPE_MAN_EN			R/W
0x60	00001000	This control is used to enable the manual programming of Teletext decoding. 0 - Manual programming of Teletext disabled 1 - Manual programming of Teletext enabled	
VDP_TTXT_TYPE[1:0]			R/W
0x60	00001000	This readback indicates the Teletext type detected. It is functional only if vdp_ttxt_type_man_en is set to 1. 00 - ITU_BT.653-625/50-A - for PAL 01 - ITU_BT.653-625/50-B(WST) - for PAL; ITU_BT.653-525/60-B - for NTSC 10 - ITU_BT.653-625/50-C(WST) - for PAL; ITU_BT.653-525/60-C or EIA516(NABTS) - for NTSC 11 - ITU_BT.653-625/50-D - for PAL; ITU_BT.653-525/60-D -	
VDP_CP_CLAMP_AVG			R/W
0x61	00011000	This control is used to set the amount of samples taken to calculate clamp levels. 0 - 16 samples taken for averaging 1 - 32 samples taken for averaging	
NOISE_CLK_DISABLE			R/W
0x61	00011000	This control is used to detect the noise clock feature for Clock Run In (CRI). 0 - Enable noise clock feature for CRI detection 1 - Disable noise clock feature for CRI detection	
AUTO_DETECT_GEM			R/W
0x61	00011000	This control is used for the autodetection of the Gemstar type. 0 - Disable autodetection of Gemstar type 1 - Enable autodetection of Gemstar type	

Reg	Bits	Description	
VITC_STRIP_SYNC_DISABLE			R/W
0x61	00011000	This control is used for sync stripping on the VITC input. 0 - Disable stripping of 10 syncs from VITC input signal 1 - Enable stripping of 10 syncs from VITC input signal	
BIPHASE_DECODE_DISABLE			R/W
0x61	00011000	This control is used for the biphase decoding of the incoming VPS or WSS signal. 0 - Enable biphase decoding of incoming VPS or WSS signal 1 - Disable biphase decoding of incoming VPS or WSS signal	
VDP_MAN_LINE_1_21[7:0]			R/W
0x64	00000000	This control is used to set the configuration register for manual VDP control for lines 1 and 21.	
VDP_MAN_LINE_2_22[7:0]			R/W
0x65	00000000	This control is used to set the configuration register for manual VDP control for lines 2 and 22.	
VDP_MAN_LINE_3_23[7:0]			R/W
0x66	00000000	This control is used to set the configuration register for manual VDP control for line 3 and 23.	
VDP_MAN_LINE_4_24[7:0]			R/W
0x67	00000000	This control is used to set the configuration register for manual VDP control for line 4 and 24.	
VDP_MAN_LINE_5_25[7:0]			R/W
0x68	00000000	This control is used to set the configuration register for manual VDP control for line 5 and 25.	
VDP_MAN_LINE_6_26[7:0]			R/W
0x69	00000000	This control is used to set the configuration register for manual VDP control for line 6 and 26.	
VDP_MAN_LINE_7_27[7:0]			R/W
0x6A	00000000	This control is used to set the configuration register for manual VDP control for line 7 and 27.	
VDP_MAN_LINE_8_28[7:0]			R/W
0x6B	00000000	This control is used to set the configuration register for manual VDP control for line 8 to 28.	
VDP_MAN_LINE_9_29[7:0]			R/W
0x6C	00000000	This control is used to set the configuration register for manual VDP control line 9 and 29.	
VDP_MAN_LINE_10_30[7:0]			R/W
0x6D	00000000	This control is used to set the configuration register for manual VDP control for line 10 and 30.	
VDP_MAN_LINE_11_31[7:0]			R/W
0x6E	00000000	This control is used to set the configuration register for manual VDP control for line 11 and 31.	
VDP_MAN_LINE_12_32[7:0]			R/W
0x6F	00000000	This control is used to set the configuration register for manual VDP control for line 12 and 32.	
VDP_MAN_LINE_13_33[7:0]			R/W
0x70	00000000	This control is used to set the configuration register for manual VDP control for line 13 and 33.	
VDP_MAN_LINE_14_34[7:0]			R/W
0x71	00000000	This control is used to set the configuration register for manual VDP control for line 14 and 34.	
VDP_MAN_LINE_15_35[7:0]			R/W
0x72	00000000	This control is used to set the configuration register for manual VDP control for line 15 and 35.	
VDP_MAN_LINE_16_36[7:0]			R/W
0x73	00000000	This control is used to set the configuration register for manual VDP control for line 16 and 36.	

Reg	Bits	Description	
VDP_MAN_LINE_17_37[7:0]			R/W
0x74	00000000	This control is used to set the configuration register for manual VDP control for line 17 and 37.	
VDP_MAN_LINE_18_38[7:0]			R/W
0x75	00000000	This control is used to set the configuration register for manual VDP control for line 18 and 38.	
VDP_MAN_LINE_19_39[7:0]			R/W
0x76	00000000	This control is used to set the configuration register for manual VDP control for line 19 and 38.	
VDP_MAN_LINE_20_40[7:0]			R/W
0x77	00000000	This control is used to set the configuration register for manual VDP control for line 20 and 40.	
STATUS_CLEAR_TTXT			SC
0x78	00000000	This control is used to refresh the Teletext status registers. This is a self-clearing bit. 0 - Do not refresh Teletext status registers 1 - Refresh Teletext status registers	
STATUS_CLEAR_VITC			SC
0x78	00000000	This control is used to refresh the VITC status registers. This is a self-clearing bit. 0 - Do not refresh VITC status registers 1 - Refresh VITC status registers	
STATUS_CLEAR_GEMS_VPS			SC
0x78	00000000	This control is used to refresh the Gemstar and VPS status registers. This is a self-clearing bit. 0 - Do not refresh VPS status registers 1 - Refresh VPS readback registers	
STATUS_CLEAR_WSS_CGMS			SC
0x78	00000000	This control is used to refresh the WSS and CGMS readback registers. This is a self-clearing bit. 0 - Do not refresh WSS and CGMS readback registers 1 - Refresh WSS and CGMS readback registers	
STATUS_CLEAR_CCAP			SC
0x78	00000000	This control is used to refresh the CCAP status registers. This is a self-clearing bit. 0 - Do not refresh CCAP status registers 1 - Refresh CCAP status registers	
LOW_DATA_STD_FILTER_EN			R/W
0x98	10001000	This control is used to enable the low data rate filter. 0 - Disable filter for low data rate 1 - Enable filter for low data rate	
ADAP1_SL_CONFIG_EN			R/W
0x98	10001000	This control is used to enable the duty-cycle based slicer calculator. 0 - Disable duty-cycle based slicer calculator 1 - Enable duty-cycle based slicer calculator	
ADAP2_SL_CONFIG_EN			R/W
0x98	10001000	This control is used to enable the peak tracking slicer. 0 - Disable peak tracking slicer 1 - Enable peak tracking slicer	
ADAP2_TTXT_STD_EN			R/W
0x99	11011101	This control is used to enable standard adaptive slicing for Teletext. 0 - Do not enable Teletext standard 1 - Enable Teletext standard	
ADAP2_VITC_STD_EN			R/W
0x99	11011101	This control is used to enable standard adaptive slicing for VITC. 0 - Do not enable VITC standard 1 - Enable VITC standard	
ADAP2_GEMS_STD_EN			R/W
0x99	11011101	This control is used to enable standard adaptive slicing for Gemstar. 0 - Do not enable GEMSTAR-1x, GEMSTAR-2x standard 1 - Enable GEMSTAR-1x, GEMSTAR-2x standard	

Reg	Bits	Description	
ADAP2_VPS_STD_EN			R/W
0x99	11011101	This control is used to enable standard adaptive slicing for VPS. 0 - Do not enable VPS standard 1 - Enable VPS standard	
ADAP2_WSS_CGMS_STD_EN			R/W
0x99	11011101	This control is used to enable standard adaptive slicing for CGMS and WSS. 0 - Do not enable WSS-CGMS standard 1 - Enable WSS-CGMS standard	
ADAP2_CCAP_STD_EN			R/W
0x99	11011101	This control is used to enable standard adaptive slicing for closed captioning. 0 - Do not enable CCAP standard 1 - Enable CCAP standard	
GS_VPS_PDC_UTC_CB_CHANGE			R/W
0x9C	00100000	This control is used to allow content based updates of VPS, PDC and UTC data. 0 - Disable content based update of VPS, PDC, UTC data 1 - Enable content based update of UTC, PDC, UTC data	
WSS_CGMS_CB_CHANGE			R/W
0x9C	00100000	This control is used to allow content based updates of WSS and CGMS type A data. 0 - Disable content based update of WSS and CGMS type A data 1 - Enable content based update of WSS and CGMS type A data	
RAW_STATUS_ENABLE			R/W
0x9C	00100000	This control is used to convert the latched status signals into raw status signals. 0 - Disable raw status and data 1 - Enable raw status and data	
GS_VPS_PDC_UTC_CGMSTB[2:0]			R/W
0x9C	00100000	The readback registers for VPS, PDC, UTC and CGMS type B are shared. This control is used to identify which type of data is to be written to the shared registers. 000 - Gemstar 1x/2x 001 - VPS 010 - PDC 011 - UTC 100 - CGMS type B 101 - Reserved 110 - Reserved 111 - Reserved	
SLICE_CORRECTOR_EN			R/W
0x9D	00000010	This control is used to enable the slice corrector. This feature is designed to improve the handling of nonstandard data. 0 - Disable slice corrector feature 1 - Enable slice corrector feature	
ADAP2_VPS_CTB_FAST_LEARN_EN			R/W
0x9E	00000000	This control is used to enable the slice level calculation based on the fast learn approach. 0 - Disable slice level calculation using fast learn approach for VPS and CGMS type B data standard 1 - Enable slice level calculation using fast learn approach for VPS and CGMS type B data standard	
VDP_USE_PREDEF_FREQ			R/W
0xA5	10010000	If the video standard is not correctly identified, this control is used to force a predefined bit frequency for the PAL standard. 0 - Use bit frequency sent by vdp_parm 1 - Use predefined bit frequency (PAL, XTAL 27 MHz)	
VDP_CRI_TOLERANCE			R/W
0xA5	10010000	This control is used to allow tolerance in CRI detection. 0 - No tolerance 1 - Allow 1-bit tolerance in CRI detection	
VDP_FRM_CODE_TOLERANCE			R/W
0xA5	10010000	This control is used to remove tolerance in framing code detection. 0 - No tolerance 1 - Allow 1-bit tolerance in framing code detection	

Reg	Bits	Description	
VDP_CRI_8BIT			R/W
0xA5	10010000	This control sets the number of CRI bits that must be detected for a robust detection. 0 - Search for six bits of CRI 1 - Search for eight bits	
VDP_INVERT_EVEN_FIELD			R/W
0xA6	00000000	This control is used to set the even_field signal polarity, as seen by the VDP. 0 - Use default even field polarity 1 - Invert even field polarity	
VDP_MANUAL_TTXC			R/W
0xA8	00001000	This control is used to force the VDP block to try and detect Teletext type C. 0 - Try to detect only the type of ttxt which vdp_parm decides 1 - Try to detect TTX type C even when ttx_type given out by vdp_parm is TTX type B	
VDP_CRI_MAG_TRESH[7:0]			R/W
0xAC	11001000	This control is used to set the threshold of the CRI detection. In order to be detected, the magnitude of CRI peaks must be more than the threshold defined in this control. 0x00 - Minimum threshold 0xC8 - Default threshold 0xFF - Maximum threshold	
VDP_FAST_REG_CONF_CUS2			R/W
0xC0	00000000	This control is used to select the VBI data that is available through the SPI interface. 0 - Default	
VDP_FAST_REG_CONF_CUST			R/W
0xC0	00000000	This control is used to select the VBI data that is available through the SPI interface. 0 - Default	
VDP_FAST_REG_CONF_CCAP			R/W
0xC0	00000000	This control is used to select the VBI data that is available through the SPI interface. 0 - Default	
VDP_FAST_REG_CONF_GEM1X_2X			R/W
0xC0	00000000	This control is used to select the VBI data that is available through the SPI interface. 0 - Default	
VDP_FAST_REG_CONF_CGMS_WSS			R/W
0xC0	00000000	This control is used to select the VBI data that is available through the SPI interface. 0 - Default	
VDP_FAST_REG_CONF_VITC			R/W
0xC0	00000000	This control is used to select the VBI data that is available through the SPI interface. 0 - Default	
VDP_FAST_REG_CONF_VPS_CGMSTB			R/W
0xC0	00000000	This control is used to select the VBI data that is available through the SPI interface. 0 - Default	
VDP_FAST_REG_CONF_TTXT			R/W
0xC0	00000000	This control is used to select the VBI data that is available through the SPI interface. 0 - Default	

Reg	Bits	Description	
VDP_FAST_VBI_STD[3:0]			R
0xC2	00000000	<p>This readback displays the VBI standard in the SPI registers.</p> <p>0001 - Teletext 0010 - VPS 0011 - VITC 0100 - WSS/CGMS type A 0101 - Gemstar 1X 0110 - Gemstar 2X 0111 - CCAP 1000 - CGMS type B 1001 - Reserved 1010 - Reserved 1011 - Reserved 1100 - Reserved 1101 - Custom 1 1110 - Custom 2 1111 - Reserved</p>	
VDP_FAST_PACKET_SIZE[7:0]			R
0xC3	00000000	<p>This readback displays the number of bytes contained in the SPI registers.</p> <p>xxxxxxx - Number of bytes contained in fast I2C registers</p>	

2.6 ADDR A0 (VFE)

Reg	Bits	Description	R/W
VID_STD[5:0]			R/W
0x00	00001000	This control is used to set the input video standards and oversampling mode. Its configuration is dependant on prim_mode[3:0]. 000010 - Default	
V_FREQ[2:0]			R/W
0x01	00000110	This control is used to set the vertical frequency of HD component standards. 000 - 60 Hz 001 - 50 Hz 010 - 30 Hz 011 - 25 Hz 100 - 24 Hz 101 - Reserved 110 - Reserved 111 - Reserved	
PRIM_MODE[3:0]			R/W
0x01	00000110	This control is used to select the primary mode of operation of the decoder. It is to be used with vid_std[5:0]. 0000 - SDP mode 0001 - Component mode 0010 - Graphics mode 0011 - Reserved 0100 - Reserved 0101 - HDMI-Comp 0110 - HDMI-GR 0111 - 1111 - Reserved	
INP_COLOR_SPACE[3:0]			R/W
0x02	11110000	This control is used to set the color space of the input video. It is to be used in conjunction with alt_gamma and rgb_out to configure the color space converter. A value of 4'b1111 selects automatic setting of the input color space base on the primary mode and video standard settings. Settings 1000 to 1110 are undefined. 0000 - Force RGB (range 16 to 235) input 0001 - Force RGB (range 0 to 255) input 0010 - Force YCrCb input (601 color space) (range 16 to 235) 0011 - Force YCrCb input (709 color space) (range 16 to 235) 0100 - Force XYVCC 601 0101 - Force XYVCC 709 0110 -	
ALT_GAMMA			R/W
0x02	11110000	This control is used to select the type of YPbPr color space conversion. It is to be used in conjunction with inp_color_space[3:0] and rgb_out. If alt_gamma is set to 1 and rgb_out is set to 0, a color space conversion is applied to convert from 601 to 709 or 709 to 601. It is valid only if rgb_out is set to 0. 0 - No conversion 1 - Apply YUV601 to YUV709 conversion if input is YUV601, apply YUV709 to YUV601 conversion if input is YUV709	
OP_656_RANGE			R/W
0x02	11110000	This control is used to set the output range of the digital data. It also automatically sets the gain setting, the offset setting, and the data saturator setting. 0 - Enable full output range (0 to 255) 1 - Enable limited output range (16 to 235)	
RGB_OUT			R/W
0x02	11110000	This control is used to select the output color space and the correct digital blank level and offsets on the RGB or YPrPb outputs. It is used in conjunction with inp_color_space[3:0] and alt_gamma to select the applied CSC. 0 - YPbPr color space output 1 - RGB color space output	
ALT_DATA_SAT			R/W
0x02	11110000	This control is used to disable the data saturator that limits the output range independently of op_656_range. It is used to support extended data range modes. 0 - Enable/disable data saturator according to op_656_range setting 1 - Reverse op_656_range decision to enable or disable data saturator	

Reg	Bits	Description	
OP_SWAP_CB_CR			R/W
0x05	00101100	This control is used to swap the Cr and Cb data on the output bus. 0 - Output Cr and Cb as per default 1 - Invert order of Cb and Cr in interleaved data stream	
CP_PWRDN			R/W
0x0C	00000010	This control is used to power down the clock to the CP core. 0 - Power up clock to CP core. 1 - Power down clock to CP core. VDP, DPP and HDMI blocks not affected.	
VDP_PDN			R/W
0x0C	00000010	This control is used to power down the VDP. It is recommended to power down the VDP when this feature is not required. 0 - Power up VDP section 1 - Power down VDP section	
PLL_DIV_MAN_EN			R/W
0x16	01000011	This control is used to manually override the PLL divider ratio value. 0 - Disable manual PLL divider ratio settings. PLL divider ratio set by prim_mode[3:0] and vid_std[5:0]. 1 - Set pll_div ratio manually as defined by pll_div[12:0].	
PLL_DIV_RATIO[12:0]			R/W
0x16 0x17	01000011 01011010	This control is used to set the manual PLL divide ratio. It is sequenced and requires sequential writes for the desired value to be updated. xxxxxxxxxxxx - Synthesizer feedback value. pll_man_val_en must be set for this value to be active.	
COEFF_PART_WR			SC
0x19	00000000	This control is used to write the coefficients for the DCM filters. It is self clearing. 1 - Enable write to DCM coefficients	
DCM_CONFIG_EN			R/W
0x21	00000000	This control is used to enable channel selection for DCM filters. 1 - Enable channel selection for DCM filters 0 - Disable channel selection	
DCM_CH_SEL[2:0]			R/W
0x21	00000000	This control is used to select a channel for DCM filters. It allows the dcm_mode control to be selected for the particular channel. 000 - Channel 1 001 - Channel 2 010 - Channel 3 011 - Channel 4 All others - Reserved	
DCM_FILT_EN			R/W
0x21	00000000	This control is used to manually enable the DCM filter block. 1 - Enable manual DCM filter control 0 - Automatic control	
DCM_FILT_SEL[2:0]			R/W
0x21	00000000	This control is used to manually select a filter for the DCM filter block. The particular channel should be selected by filt_sel before this control is set. 000 - Reserved 001 - Filter with auto coefficients 010 - Filter with manual coefficients 011 - Filter bypass with delay 100 - Filter complete bypass All others - Reserved	
DCM_MODE[2:0]			R/W
0x22	00000000	A control to configure the DCM filter block 000 - Reserved 001 - 1x1 modes 010 - 2x2 modes 011 - 4x1 modes All others - Reserved	

Reg	Bits	Description	
DCM_FILT_SIZE[1:0]			R/W
0x22	000 <u>00</u> 000	A control to configure the DCM filter block 00 - Reserved 01 - 19/20 tap filter 10 - 29/40 tap filter 11 - Reserved	
DCM_BANDWIDTH[2:0]			R/W
0x22	00000 <u>000</u>	A control to configure the DCM filter block 000 - Reserved 001 - Fs/2 010 - Fs/4 011 - Fs/8 All others - Reserved	
DCM_CH_EN			R/W
0x23	<u>0</u> 0000000	This control is used to provide manual control of the DCM channels. 1 - Manual channel power up control 0 - Automatic power up	
DCM_CH3_EN			R/W
0x23	00000 <u>000</u>	This control is used to power up a particular channel. 1 - Power up channel 4 0 - Power down channel 4	
DCM_CH2_EN			R/W
0x23	00000 <u>000</u>	This control is used to power up a particular channel. 1 - Power up channel 3 0 - Power down channel 3	
DCM_CH1_EN			R/W
0x23	000000 <u>00</u>	This control is used to power up a particular channel. 1 - Power up channel 2 0 - Power down channel 2	
DCM_CH0_EN			R/W
0x23	0000000 <u>0</u>	This control is used to power up a particular channel. 1 - Power up channel 1 0 - Power down channel 1	
DCM_FILT_GAIN[3:0]			R/W
0x24	0000 <u>0000</u>	This control is used to program the DCM filter gain. 0000 - Default	
FILT_SEL[3:0]			R/W
0x25	<u>0000</u> 0000	This control is used to select the DCM filter to be programmed. 0000 - No filter selected 0001 - Select channel 1 0010 - Select channel 2 0100 - Select channel 3 1000 - Select channel 4	
COEFF_PART_SEL[11:0]			R/W
0x27	00000000	This control is used to set the manual coefficients for the DCM filter.	
0x28	00000000		
0x29	00000000		
0x2A	00000000		
0x2B	00000000		
0x2C	00000000		
0x2D	00000000		
0x2E	00000000		
0x2F	00000000		
0x30	00000000		
0x31	00000000		
0x32	00000000		
0x33	00000000		
0x34	00000000		

Reg	Bits	Description	R/W
COEFF_PART			R/W
0xBF	00000000	This control is used for power reduction. It should be set to 1 when the input video is above 170 MHz. 1 - Bypass CP core 0 - Enable normal mode	

2.7 ADDR 90 (SDP)

Reg	Bits	Description	
SDP_AD_SECAM_EN			R/W
0x00	00 <u>0000</u> 10	This control is used to enable autodetection of the SECAM standard. Setting this bit to 1 enables the corresponding standard to be detected. In order to force the part into a particular standard, only the corresponding enable bit for that standard should be enabled. To allow full autodetection, all standards should be enabled via the respective bit. 1 - Enable SECAM to be detected 0 - Do not enable SECAM to be detected	
SDP_AD_N443_EN			R/W
0x00	00 <u>0000</u> 10	This control is used to enable autodetection of the NTSC-443 standard. Setting this bit to 1 enables the corresponding standard to be detected. In order to force the part into a particular standard, only the corresponding enable bit for that standard should be enabled. To allow full autodetection, all standards should be enabled via the respective bit. 1 - Enable NTSC-443 to be detected 0 - Do not enable NTSC-443 to be detected	
SDP_AD_PAL60_EN			R/W
0x00	000 <u>000</u> 10	This control is used to enable autodetection of the PAL-60 standard. Setting this bit to 1 enables the corresponding standard to be detected. In order to force the part into a particular standard, only the corresponding enable bit for that standard should be enabled. To allow full autodetection, all standards should be enabled via the respective bit. 1 - Enable PAL-60 to be detected 0 - Do not enable PAL-60 to be detected	
SDP_AD_PALCN_EN			R/W
0x00	0000 <u>00</u> 10	This control is used to enable autodetection of the PAL-CombN standard. Setting this bit to 1 enables the corresponding standard to be detected. In order to force the part into a particular standard, only the corresponding enable bit for that standard should be enabled. To allow full autodetection, all standards should be enabled via the respective bit. 1 - Enable PAL-CombN to be detected 0 - Do not enable PAL-CombN to be detected	
SDP_AD_PALM_EN			R/W
0x00	00000 <u>0</u> 10	This control is used to enable autodetection of the PAL-M standard. Setting this bit to 1 enables the corresponding standard to be detected. In order to force the part into a particular standard, only the corresponding enable bit for that standard should be enabled. To allow full autodetection, all standards should be enabled via the respective bit. 1 - Enable PAL-M to be detected 0 - Do not enable PAL-M to be detected	
SDP_AD_NTSC_EN			R/W
0x00	000000 <u>0</u> 10	This control is used to enable autodetection of the NTSC-M standard. Setting this bit to 1 enables the corresponding standard to be detected. In order to force the part into a particular standard, only the corresponding enable bit for that standard should be enabled. To allow full autodetection, all standards should be enabled via the respective bit. 1 - Enable NTSC-M to be detected 0 - Do not enable NTSC-M to be detected	
SDP_AD_PAL_EN			R/W
0x00	000000 <u>0</u> 10	This control is used to enable autodetection of the PAL-BGHID standard. Setting this bit to 1 enables the corresponding standard to be detected. In order to force the part into a particular standard, only the corresponding enable bit for that standard should be enabled. To allow full autodetection, all standards should be enabled via the respective bit. 1 - Enable PAL-BGHID to be detected 0 - Do not enable PAL-BGHID to be detected	
SDP_SECAM_PED_EN			R/W
0x01	00 <u>110</u> 110	This control is used to force the part to assume that the corresponding standard has a pedestal. Standards with a pedestal are clamped to the pedestal level; standards without a pedestal are clamped to the back porch level. 1 - Assume SECAM inputs have a pedestal 0 - Assume SECAM inputs do not have a pedestal	
SDP_N443_PED_EN			R/W
0x01	00 <u>110</u> 110	This control is used to force the part to assume that the corresponding standard has a pedestal. Standards with a pedestal are clamped to the pedestal level; standards without a pedestal are clamped to the back porch level. 1 - Assume NTSC-443 inputs have a pedestal 0 - Assume NTSC-443 inputs do not have a pedestal	
SDP_PAL60_PED_EN			R/W
0x01	001 <u>10</u> 110	This control is used to force the part to assume that the corresponding standard has a pedestal. Standards with a pedestal are clamped to the pedestal level; standards without a pedestal are clamped to the back porch level. 1 - Assume PAL-60 inputs have a pedestal 0 - Assume PAL-60 inputs do not have a pedestal	

Reg	Bits	Description	
SDP_PALCN_PED_EN			R/W
0x01	00110110	This control is used to force the part to assume that the corresponding standard has a pedestal. Standards with a pedestal are clamped to the pedestal level; standards without a pedestal are clamped to the back porch level. 1 - Assume PAL-CombN inputs have a pedestal 0 - Assume PAL-CombN inputs do not have a pedestal	
SDP_PALM_PED_EN			R/W
0x01	00110110	This control is used to force the part to assume that the corresponding standard has a pedestal. Standards with a pedestal are clamped to the pedestal level; standards without a pedestal are clamped to the back porch level. 1 - Assume PAL-M inputs have a pedestal 0 - Assume PAL-M inputs do not have a pedestal	
SDP_NTSC_PED_EN			R/W
0x01	00110110	This control is used to force the part to assume that the corresponding standard has a pedestal. Standards with a pedestal are clamped to the pedestal level; standards without a pedestal are clamped to the back porch level. 1 - Assume NTSC-M inputs have a pedestal 0 - Assume NTSC-M inputs do not have a pedestal	
SDP_PAL_PED_EN			R/W
0x01	00110110	This control is used to force the part to assume that the corresponding standard has a pedestal. Standards with a pedestal are clamped to the pedestal level; standards without a pedestal are clamped to the back porch level. 1 - Assume PAL-BGHID inputs have a pedestal 0 - Assume PAL-BGHID inputs do not have a pedestal	
SDP_CR_MODE_EN			R/W
0x02	00100111	This control is used to enable contrast reduction. This is only valid in fast blanking modes. 1 - Enable contrast reduction 0 - Ignore contrast reduction	
SDP_Y_AGC_EN			R/W
0x03	11000100	This control is used to select between automatic and manual luma gain control. 1 - Enable automatic luma gain based on sync 0 - Enable manual luma gain, set by sdp_y_gain_man	
SDP_PW_EN			R/W
0x03	11000100	This control is used to enable the peak white luma gain feature. 1 - Enable peak white luma gain control 0 - Disable peak white luma gain control	
SDP_MAN_GAIN_VCR			R/W
0x03	11000100	This control is used to select the gain method used when a VCR input is detected. 1 - Manual gain used for VCR inputs value is sdp_y_gain_man 0 - Automatic gain used for VCR inputs (valid only if sdp_y_agc_en set to 1)	
SDP_Y_GAIN_MAN[12:0]			R/W
0x03 0x04	11000100 00001011	This control is used to adjust the manual luma gain value. It is used if sdp_y_agc_en is set to 0. It also applies to the G channel in component modes. The control has a range of 0.5 to 4. 0x0558 - Default	
SDP_C_AGC_EN			R/W
0x05	11000011	This control is used to select between automatic and manual chroma gain (C/U/V/R/B channels also used for G in the case of SCART). 1 - Enable automatic chroma gain based on burst power 0 - Enable manual chroma gain, gain value set by sdp_c_gain_act_man	
SDP_PC_EN			R/W
0x05	11000011	This control is used to enable the peak-color chroma gain feature. Peak-color chroma overrides and reduces the gain of the chroma AGC if the chroma signal path becomes larger than a set threshold. Peak chroma can only act to reduce the AGC gain. When there are no more violations of the peak white threshold, the peak chrome algorithm allows the chroma AGC to restore the gain (based on the synchronization depth). The recovery rate of the AGC gain is set by the peak chroma recovery register. 1 - Enable peak color chroma gain 0 - Disable peak color override of chroma gain	

Reg	Bits	Description	
SDP_C_GAIN_ACT_MAN[12:0]			R/W
0x05 0x06	11000011 11000000	This control is used to adjust the manual chroma gain value. It used if sdp_c_agc_en is set to 0. It also applies to the U, V, R, and B channels in component modes. The control has a range of 0.5 to 8. 0x05[4:0] - sdp_c_gain_act_man[12:8] 0x06[7:0] - sdp_c_gain_act_man[7:0]	
SDP_CKILL_EN			R/W
0x07	10001011	This control is used to enable the color kill feature. 1 - Enable color kill feature 0 - Disable color kill feature	
SDP_CK_LOW_THR[6:0]			R/W
0x07	10001011	This control is used to set the color kill low threshold. If the burst power is below this threshold, it enters color kill mode. 00001011 - Color kill low threshold	
SDP_CK_HIGH_THR[7:0]			R/W
0x08	00011010	This control is used to set the color kill high threshold. If the burst power is above this threshold, it enters color kill mode. 00011010 - Color kill high threshold	
SDP_DGAIN_SPEED[4:0]			R/W
0x0A	11100101	This control is used to adjust the speed of luma digital gain operation. Only values of 1 to 6 are within a valid range. 0x00 - Freeze digital gain 0x05 - Default Valid range - 0x01 to 0x06 All other values - Reserved	
SDP_C_DGAIN_SPEED[4:0]			R/W
0x0B	11100101	This control is used to adjust the speed of chroma digital gain operation. Only values of 1 to 6 are within a valid range. This register has an effect only if sdp_c_agc_en is set to 1. 00000 - Freeze clamp gain Valid range - 1 to 6 All other values - Reserved	
SDP_DCLP_SPEED[4:0]			R/W
0x0C	11100101	This control is used to adjust the speed of digital clamp operation. 00000 - Freeze digital clamp Valid range - 1 to 6 All other values - Reserved	
SDP_ACLP_SPEED[4:0]			R/W
0x0D	11100100	This control is used to adjust the speed of the analog clamp operation. 00000 - Freeze analog clamp Valid range - 1 to 6 All other values - Reserved	
SDP_SCM_CTI_EN			R/W
0x0E	00110001	This control is used to enable CTI in SECAM modes. 1 - Enable extra CTI in SECAM modes 0 - Disable extra CTI in SECAM modes	
SDP_Y_2D_PK_EN			R/W
0x0E	00110001	This control is used to enable the horizontal peaking filter on the 2D combed output. This peaking filter is applied to the 2D portion of the image before it is mixed with the 3D. It is important to note that it will always be applied to the 2D portion regardless of whether or not 3D comb is enabled. The purpose of this control is that where 3D comb is enabled, 2D peaking reduces the sharpness/resolution difference perceived in areas where motion occurs. 3D areas are always very sharp due to temporal comb; 2D areas need to be peaked to compensate for softness of 2D/1D separation. 1 - Enable horizontal peaking 0 - Disable horizontal peaking	
SDP_V_PK_EN			R/W
0x0E	00110001	This control is used to enable the vertical peaking filter. 1 - Enable vertical peaking 0 - Disable vertical peaking	

Reg	Bits	Description	
SDP_H_PK_EN			R/W
0x0E	001100 <u>01</u>	This control is used to enable the horizontal peaking filter. This is a universal peaking control applied after 2D/3D mixing. It is applied whether or not 3D has been enabled. 1 - Enable horizontal peaking 0 - Disable horizontal peaking	
SDP_LTI_EN			R/W
0x0E	001100 <u>01</u>	This control is used to enable Luma Transient Improvement (LTI). 1 - Enable LTI 0 - Disable LTI	
SDP_CTI_EN			R/W
0x0E	001100 <u>01</u>	This control is used to enable Chroma Transient Improvement (CTI). 1 - Enable CTI 0 - Disable CTI	
SDP_PC_REC_RATE[11:0]			R/W
0x0F 0x11	<u>00000000</u> <u>00010000</u>	This control is used to adjust the peak chroma gain recovery speed, that is, the speed at which the chroma gain is increased following a gain reduction due to peak color violation. A larger value corresponds to a faster speed. 0x0F[7:4] - sdp_pc_rec_rate[12:8] 0x11[7:0] - sdp_pc_rec_rate[7:0]	
SDP_PW_REC_RATE[11:0]			R/W
0x0F 0x10	<u>00000000</u> <u>00000001</u>	This control is used to adjust the peak white gain recovery speed, that is, the speed at which the luma gain is increased following a gain reduction to a peak white violation. A larger value corresponds to a faster speed. 0x0F[3:0] - sdp_pw_rec_rate[12:8] 0x10[7:0] - sdp_pw_rec_rate[7:0]	
SDP_FR_TBC_EN			R/W
0x12	00000 <u>001</u>	This control is used to enable frame Time Based Correction (TBC). 1 - Enable frame TBC 0 - Disable frame TBC	
SDP_3D_COMB_EN			R/W
0x12	000000 <u>01</u>	This control is used to disable the 3D comb filter. When the 3D comb is enabled, automatic 2D/3D comb switching is applied based on the detected video type. When the 3D comb is disabled, 2D combing only is applied. 1 - Enable 3D comb filter 0 - Disable 3D comb filter, enable 2D comb mode only	
SDP_CONTRAST[9:0]			R/W
0x13 0x17	<u>10000000</u> <u>00000000</u>	This control is used to set the contrast level (luma gain). This control has a range of 0 to 2. It is an unsigned number and has a range from 0x000 (lowest contrast, all black) to 0x3FF (highest contrast). 0x000 - Lowest contrast 0x080 - Default contrast 0x3FF - Highest contrast	
SDP_BRIGHTNESS[9:0]			R/W
0x14 0x17	<u>00000000</u> <u>00000000</u>	This control is used to set the brightness level (luma offset). It is a twos complement number and has a range of 0x200 (darkest) to 0x1FF (brightest). 0x200 - Darkest 0x000 - Default brightness 0x1FF - Brightest	
SDP_SATURATION[9:0]			R/W
0x15 0x17	<u>10000000</u> <u>00000000</u>	This control is used to set the saturation level (chroma gain). It has a valid range of 0 to 1.75. It is an unsigned number and has a range of 0x000 (lowest saturation, no color) to 0x3FF (highest saturation). 0x000 - Lowest saturation (no color) 0x3FF - Highest saturation	
SDP_HUE[9:0]			R/W
0x16 0x17	<u>00000000</u> <u>00000000</u>	This control is used to set the hue (chroma phase rotation). It is a twos complement number and has a range of 0x200 (-180 degrees) to 0x1FF (+180 degrees). 0x1FF - +180° 0x000 - 0° 0x200 - -180°	

Reg	Bits	Description	
SDP_BLANK_C_VBI			R/W
0x18	11111111	This control is used to set sdp_blank_c_vbi. When this control is set to 1, the Cr and Cb values of all VBI lines are blanked. This is done so that any data that comes during VBI is not decoded as color and output through Cr and Cb. As a result, it should 1 - Blank color during VBI lines 0 - Pass through color as decoded during VBI lines	
SDP_FORCE_CKILL_HQI			R/W
0x18	11111111	This control is used to force the use of the HQI Y shaping filter when color kill is active. When this control is disabled, the autoselection of the Y shaping filter does not consider color kill mode. 1 - Force use of HQI Y shaping filter when color kill active 0 - HQI Y shaping filter not used when color kill active	
SDP_Y_SHAPE_SEL_VBI[5:0]			R/W
0x18	11111111	This control is used to select the Y shaping filter for the VBI region. Refer to the Hardware Manual for details on Y shaping filters. 111111 - Default	
SDP_Y_SHAPE_AUTO_EN			R/W
0x19	11001101	This control is used to allow manual or automatic selection of the Y shaping filter. In manual mode, the Y shaping filter is determined by the value of using sdp_y_shape_sel_hqi[5:0]. 1 - Enable automatic selection of Y shaping filter 0 - Enable manual selection of Y shaping filter	
SDP_FORCE_COMP_HQI			R/W
0x19	11001101	This control is used to force the use of a HQI Y shaping filter when a component input is applied. When this bit is disabled, the autoselection of the Y shaping filter is employed. 1 - Force Y shaping filter selection to use HQI filter selection in component modes 0 - Automatic selection of Y shaping filter used in component modes	
SDP_Y_SHAPE_SEL_HQI[5:0]			R/W
0x19	11001101	This control is used to select the manual Y shaping filter for high quality input signals. 001101 - Default	
SDP_HQI_REQ_STD			R/W
0x1A	10010101	This control sets criteria for the selection of the HQI shaping filter. 1 - HQI requires both stable and standard (nominal) timebase 0 - HQI requires only stable timebase	
SDP_Y_SHAPE_SEL_LQI[5:0]			R/W
0x1A	10010101	This control is used to select manually the Y shaping filter for low quality inputs (LQI). 010101 - Default	
SDP_Y_SHAPE_SEL_SCM[5:0]			R/W
0x1B	00011110	This control is used to select manually the Y shaping filter for SECAM input signals. 011110 - Default	
SDP_C_SHAPE_AUTO_EN			R/W
0x1C	11000100	This control is used to allow manual or automatic selection of the C shaping filter. Manual selection is determined by sdp_c_shape_sel_hqi[4:0]. 1 - Enable automatic selection of C shaping filter 0 - Enable manual selection of C shaping filter	
SDP_CSH_WBW_AUTO			R/W
0x1C	11000100	This control allows automatic selection of the C shaping filter to be influenced by motion detection. In areas where motion is detected and 2D combing is in operation, a narrow C shaping filter is used. For still areas where no motion is detected and 3D combing is in operation, a wide C shaping filter is applied. 1 - Enable auto C shaping filter selection based on motion 0 - Disable auto C shaping filter selection based on motion, select default C shaping filter	
SDP_C_SHAPE_SEL_HQI[4:0]			R/W
0x1C	11000100	This control is used to manually select a C shaping filter for high quality inputs (HQI). 00100 - Default	
SDP_C_SHAPE_SEL_HQI_ADJ[2:0]			R/W
0x1D	00000010	This signed adjustment control is used to increase or decrease the C shaping filter bandwidth for 3D combed pixels. It is only valid when enabled. 000 - Default	

Reg	Bits	Description	
SDP_C_SHAPE_SEL_LQI[4:0]			R/W
0x1D	00000010	This control is used to allow selection of the C shaping filter for low quality inputs (LQI). 00010 - Default	
SDP_C_SHAPE_SEL_SCM[4:0]			R/W
0x1E	00000100	This control is used to allow selection of the C shaping filter for SECAM input signals. 00100 - Default	
SDP_IF_FILTER_SEL[4:0]			R/W
0x20	00000000	This control is used to compensate for SAW filter characteristics on a composite input as would be observed on a tuner output. 00000 - Default	
SDP_U_DEL_LINE_EN			R/W
0x21	11111111	This control is used to enable a delay line, in the form of a 2-tap vertical filter for the U component. 1 - Enable delay line for U component 0 - Disable delay line for U component	
SDP_V_DEL_LINE_EN			R/W
0x21	11111111	This control is used to enable a delay line, in the form of a 2-tap vertical filter for the V component. 1 - Enable delay line for V component 0 - Disable delay line for V component	
SDP_H_PK_INV			R/W
0x22	00100000	This control is used to enable an inverse horizontal peaking filter operation. 1 - Inverse peaking (attenuate HF) 0 - Normal (gain HF)	
SDP_H_PK_GAIN[3:0]			R/W
0x22	00100000	This control is used to adjust the gain of the horizontal peaking filter. The peaking filter can visually improve the picture by showing more definition on the picture details that contain frequency components around 3 MHz. The filter response is also user selectable using the sdp_h_pk_band and sdp_h_pk_inv. It has a range of 0 to 4 or 0 to -4 depending on sdp_h_pk_inv. 0100 - Default gain	
SDP_H_PK_CORE[2:0]			R/W
0x22	00100000	This control is used to select the horizontal threshold from the eight possible values listed in the following table. If the filtered output is less than the coring threshold, no high frequency is added back to the input. If the filter output is greater than the core threshold, it is passed through unchanged to the next stage. 000 - 0 001 - 8 010 - 16 011 - 24 100 - 32 101 - 40 110 - 48 111 - 56	
SDP_V_PK_INV			R/W
0x23	00010000	This control is used to enable an inverse vertical peaking filter operation. 1 - Inverse peaking (attenuate HF) 0 - Normal (gain HF)	
SDP_V_PK_GAIN[3:0]			R/W
0x23	00010000	This control is used to adjust the gain for the vertical peaking filter. The user can select to boost or attenuate the mid region of the Y spectrum around 3 MHz. The peaking filter can visually improve the picture by showing more definition on the picture details that contain frequency components around 3 MHz. It is to be used in conjunction with an sdp_v_pk_inv range of 0 to 4 or 0 to -4, depending on sdp_v_pk_inv. 0010 - Default gain	

Reg	Bits	Description	
SDP_V_PK_CORE[2:0]			R/W
0x23	00010000	This control is used to set the coring threshold for a vertical filter. Signals in the output of the filter that are below this level are cored to 0. 000 - 0 001 - 8 010 - 16 011 - 24 100 - 32 101 - 40 110 - 48 111 - 56	
SDP_V_PK_FLIP[2:0]			R/W
0x24	01001100	This control is used to set the upper convergence limit. Filtered input signal amplitude above this threshold receive no peaking enhancement. 000 - 64 001 - 128 010 - 256 011 - 512 100 - 1024 101 - 2048 110 - 3072 111 - 4095	
SDP_V_PK_CLIP[1:0]			R/W
0x24	01001100	This control is used to set the maximum amount of enhancement that can be added before the gain is applied. The saturation threshold is set on the output of the peaking filter. It is to be used in conjunction with sdp_v_pk_clip. 000 - Flip threshold divided by 2 001 - Flip threshold divided by 7/16 010 - Flip threshold divided by 3/8 011 - Flip threshold divided by 4	
SDP_H_PK_BAND[1:0]			R/W
0x24	01001100	This control is used to set a horizontal peaking filter band. 0 - No filtering 1 - Highpass 2 - Bandpass peaking 3 - Alternative bandpass peaking	
SDP_LTI_FILT_SEL			R/W
0x25	00000000	This control is used to select one of two filter responses available in LTI operation. 1 - Select filter response 1 as part of LTI 0 - Select filter response 0 as part of LTI	
SDP_LTI_LEVEL[6:0]			R/W
0x25	00000000	This control is used to set the amount of LTI applied. A larger value corresponds to the sharpening of luma transients. Bigger values - More sharpening of luma transients 0 - No transient improvement	
SDP_CTI_FILT_SEL			R/W
0x26	10001111	This control is used to select one of two filter responses available for CTI operation. 1 - Select filter response 1 as part of CTI 0 - Select filter response 0 as part of CTI	
SDP_CTI_FILT_SEL_422			R/W
0x26	10001111	This control is used to select the filter of high gain for 422 CTI data operation. 0 - Select filter response with gain double 1 - Select filter response for optimum 422 operation	
SDP_CTI_LEVEL[5:0]			R/W
0x26	10001111	This control is used to set the amount of CTI applied. A larger value corresponds to the sharpening of chroma transients. Bigger values - More sharpening of chroma transients 0 - No transient improvement	

Reg	Bits	Description	
SDP_CTI_FLIP[1:0]			R/W
0x27	<u>10</u> 101010	This control is used to select the amplitude of the filtered input signal. Amplitudes above this threshold receive no CTI edge enhancement. 00 - 128 01 - 512 10 - 1024 11 - 4096	
SDP_LTI_FLIP[1:0]			R/W
0x27	1010 <u>10</u> 10	This control is used to select the amplitude of the filtered input signal. Amplitudes above this threshold receive no LTI edge enhancement. 00 - 128 01 - 512 10 - 1024 11 - 4096	
SDP_SCM_CTI_GAIN[1:0]			R/W
0x28	00000 <u>010</u>	This control is used to change the gain used for CTI (SECAM modes). 0 - *0.125 1 - *0.25 2 - *0.375 3 - *0.5	
SDP_MAN_FB			R/W
0x2A	<u>0</u> 0000000	This control is used to select a video source for fast blank operation. This control is only valid sdp_man_fb_en is set to 1. 1 - Select RGB 0 - Select CVBS	
SDP_RGB_DELAY_ADJ[2:0]			R/W
0x2A	<u>000</u> 00000	This signed control is used to advance or delay for SCART RGB signals in increments of one burst-locked pixel. 000 - No delay 001 - Delay by 1 pixel 010 - Delay by 2 pixels 011 - Delay by 3 pixels 100 - No advance 101 - Advance by 1 pixel 110 - Advance by 2 pixels 111 - Advance by 3 pixels	
SDP_MAN_FB_EN			R/W
0x2A	00000 <u>000</u>	This control is used to select between manual fast blank control via sdp_man_fb and automatic fast blank control via the FB signal (refer to fb_select in the AFE Map). 1 - Allow manual control of FB signal 0 - Auto fast blank controlled by FB signal	
SDP_FB_DELAY_ADJ[2:0]			R/W
0x2A	00000 <u>000</u>	This signed control is used to advance or delay for FB signal in increments of one burst-locked pixel. 000 - No delay 001 - Delay by 1 pixel 010 - Delay by 2 pixels 011 - Delay by 3 pixels 100 - No advance 101 - Advance by 1 pixel 110 - Advance by 2 pixels 111 - Advance by 3 pixels	
SDP_TBC_EN			R/W
0x34	<u>1</u> 0100000	This control is used to enable line TBC. When enabled, it only becomes active in VCR trick modes. 1 - Enable line TBC (time base correction) 0 - Disable line TBC (time base correction)	
SDP_LBOX_BLK_TOP[7:0]			R
0x4C	<u>00000000</u>	This readback is used to indicate the number of black lines detected at the top of the field.	
SDP_LBOX_BLK_BOT[7:0]			R
0x4D	<u>00000000</u>	This readback is used to indicate the number of black lines detected at the bottom of the field.	

Reg	Bits	Description	
SDP_LBOX_BLK_SUB_BOT[7:0]			R
0x4E	00000000		
SDP_SYNCTIP_NOISE[11:0]			R
0x4F 0x53	00000000 00000000	This readback indicates the noise level on the synctip of the video signal. 0x53[7:4] - sdp_synctip_noise[11:8] 0x4F[7:0] - sdp_synctip_noise[7:0]	
SDP_MV_AGC_DETECTED			R
0x50	00000000	This readback displays the detection of Macrovision AGC pulses. 1 - Macrovision AGC pulses part of AGC process detected 0 - Macrovision AGC pulses part of AGC process not detected	
SDP_MV_PS_DETECTED			R
0x50	00000000	This readback displays the detection of Macrovision AGC pseudo syncs. 1 - Macrovision pseudo sync part of AGC process detected 0 - Macrovision pseudo sync part of AGC process not detected	
SDP_MVCS_TYPE3			R
0x50	00000000	This readback displays the detection of a Macrovision type 3 color stripe process. 1 - Macrovision type 3 color stripe process detected, only valid if sdp_mvcs_detect = 1 0 - Macrovision type 3 color stripe process not detected	
SDP_MVCS_DETECT			R
0x50	00000000	This readback displays the detection of the color stripe process. 1 - Macrovision color stripe process detected 0 - Macrovision color stripe process not detected	
SDP_BP_TOTAL_PULSE_BEG[3:0]			R
0x51	00000000	This readback displays the total Macrovision back porch pulses detected at the beginning of the field.	
SDP_BP_TOTAL_PULSES_END[3:0]			R
0x51	00000000	This readback displays the total Macrovision back porch pulses detected at the end of the field.	
SDP_STD[3:0]			R
0x52	00000000	This readback displays the current active standard in autodetection mode. 0x00 - NTSC-M/J 0x02 - NTSC-443 0x03 - 60HzSECAM 0x04 - PAL-M 0x06 - PAL-60 0x0C - PAL-CombN 0x0E - PAL-BGHID 0x0F - SECAM	
SDP_NOISY_IP			R
0x54	00000000	This readback displays the detection of a noisy input signal. 1 - Noisy input detected 0 - Noisy input not detected	
SDP_VERY_NOISY_IP			R
0x54	00000000	This readback displays the detection of a very noisy input signal. 1 - Very noisy input detected 0 - Very noisy input not detected	
SDP_C_CHAN_ACTIVE			R
0x54	00000000	This readback displays the result of the CVBS/YC detection feature. 1 - Y/C input detected 0 - CVBS input detected	
SDP_Y_GAIN_MAN_RB[12:0]			R
0x54 0x55	00000000 00000000	This readback provides the current luma gain. 0x54[4:0] - sdp_y_gain_man_rb[12:8] 0x55[7:0] - sdp_y_gain_man_rb[7:0]	

Reg	Bits	Description	
SDP_HSWITCH_PRESENT			R
0x56	00000000	This readback displays the result of head switch detection using algorithm 1. 1 - Head switch detected by algorithm 1 0 - Head switch not detected by algorithm 1	
SDP_BLK_NSTD			R
0x56	00000000	This readback displays the length of a 192 line block of pixels in clock cycles if within the set threshold. 1 - Length of 192 line block of pixels in clock cycles not within +- sdp_frm_nstd_thr of nominal value 0 - Length of 192 line block of pixels in clock cycles within +- sdp_frm_nstd_thr of nominal value	
SDP_FLD_NSTD			R
0x56	00000000	This readback indicates if the field length in clock cycles is within the threshold set by sdp_frm_nstd_thr of a nominal value. 1 - Field length in clock cycles not within +- sdp_frm_nstd_thr of nominal value 0 - Field length in clock cycles within +- sdp_frm_nstd_thr of nominal value	
SDP_FRM_NSTD			R
0x56	00000000	This readback indicates if the frame length in clock cycles is within the threshold set by sdp_frm_nstd_thr. 1 - Frame length in clock cycles not within +- sdp_frm_nstd_thr of nominal value 0 - Frame length in clock cycles within +- sdp_frm_nstd_thr of nominal value	
SDP_LC_NSTD			R
0x56	00000000	This readback indicates if the field length varies by more than one line from field to field. 1 - Field length in terms of number of lines varies by more than one line from field to field 0 - Field length in terms of number of lines does not vary by more than one line from field to field	
SDP_ALLOW_MED_PLL			R
0x56	00000000	This readback indicates if the input could be from a VCR source. It is valid only if sdp_allow_slow_pll is set to 0. It is ignored if sdp_allow_slow_pll is set to 1. 1 - Input may be a VCR; medium HSync PLL speed used 0 - Input is a VCR; fast HSync PLL speed used	
SDP_ALLOW_SLOW_PLL			R
0x56	00000000	This readback indicates if the input could be from a VCR source. It is to be used in conjunction with sdp_allow_med_pll. 1 - Input not a VCR; slow HSync PLL speed used 0 - Input may be a VCR; refer to sdp_allow_med_pll	
SDP_FREE_RUN			R
0x56	00000000	This readback indicates free run status. If set to 1, the part is free running due to no video detected on the input or forced free run mode. 1 - Part free running 0 - Part not free running	
SDP_CKILL_ACT			R
0x57	00000000	This readback displays the color kill status. 1 - Color kill is active (and enabled) 0 - Color kill is not active	
SDP_VS_STD_MODE			R
0x57	00000000	This readback indicates the detection of regular frame lengths on the input. 1 - Regular frame lengths detected on input 0 - Regular frame lengths not detected on input	
SDP_ALLOW_3D_COMB			R
0x57	00000000	This readback indicates the suitability of the input for 3D combing. 1 - Standard input detected, 3d comb allowed 0 - Nonstandard input detected, 3d comb not allowed, 2d comb used	
SDP_INTERLACED			R
0x57	00000000	This readback indicates the detection of an interlaced format on the input. 1 - Alternating field sequence detected on input 0 - Alternating field sequence not detected on input	
SDP_TRICK_MODE			R
0x57	00000000	This readback indicates the detection of a VCR trick mode operation on the input. 1 - VCR trick mode detected, line TBC allowed if enabled 0 - VCR trick mode not detected, line TBC not allowed	

Reg	Bits	Description	
SDP_PR_DETECTED_IN_SD			R
0x58	00000000	This readback indicates the detection of a progressive input to the SD core. 1 - SDP detects progressive input 0 - Normal operation	
SDP_BURST_LOCKED_RB			R
0x59	00000000	This readback displays the status of the burst locking loop. 1 - Burst locking loop locked 0 - Burst locking loop not locked	
SDP_AD_50_60_HZ			R
0x59	00000000	This readback displays the result of the field rate detection on the input. 1 - Field rate of 50 Hz detected on input 0 - Field rate of 60 Hz detected on input	
SDP_PAL_SW_LOCKED			R
0x59	00000000	This readback indicates the detection of a PAL swinging burst sequence on the input. 1 - PAL swinging burst sequence detected 0 - PAL swinging burst sequence not detected	
SDP_FSC_FREQ_OK			R
0x59	00000000	This readback indicates the status of the subcarrier frequency detected on the input if it is close to that of the selected standard, 3.58 MHz or 4.43 MHz; or the subcarrier frequency is running in 4.43 MHz input mode and input is 3.58 MHz or vice versa. 1 - Detected fact frequency close to that of selected standard 0 - Detected fact frequency not close to that of selected standard	
SDP_SCM_LOCKED			R
0x59	00000000	This readback indicates the detection of a SECAM input. 1 - SECAM detected on input 0 - SECAM not detected on input	
SDP_VIDEO_DETECTED			R
0x5A	00000000	This readback indicates the detection of a valid video input. 1 - Indicates valid SD/PR video input detected 0 - Input invalid or no input connected	
SDP_EXTEND_VS_MAX_FREQ			R/W
0x7B	01101001	This control is used to extend the minimum frequency VSync lock range. 1 - Extended minimum frequency VSync lock range 0 - Normal minimum frequency VSync lock range	
SDP_EXTEND_VS_MIN_FREQ			R/W
0x7B	01101001	This control is used to extend the maximum frequency VSync lock range. 1 - Extended maximum frequency VSync lock range 0 - Normal maximum frequency VSync lock range	
SDP_LIMIT_Y_GAIN			R/W
0x89	00000011	This control is used to limit the luma gain. 1 - Limit luma gain to range of 50% to 200% 0 - Normal operation	
SDP_LIMIT_C_GAIN			R/W
0x89	00000011	This control is used to limit the chroma gain. 1 - Limit chroma gain to range of 50% to 200% 0 - Normal operation	
SDP_LIMIT_UV_GAIN			R/W
0x89	00000011	This control is used to limit U/V gain. 1 - Limit U/V gain to range of 50% to 200% 0 - Normal operation	
SDP_LIMIT_G_GAIN			R/W
0x89	00000011	This control is used to limit the SD SCART FB RGB gain. 1 - Limit SD (FB) RGB gain to range of 50% to 200% 0 - Normal operation	

Reg	Bits	Description	
SHAPE_1D_AUTO			R/W
0x96	10011000	This control is used to enable a 1D shaping filter when a nonstandard line frequency input is detected. 0 - Disable auto-1D shape filter selection 1 - Enable auto-1D shape filter selection	
SHAPE_1D_FORCE			R/W
0x96	10011000	This control is used to select between an automatic selection of the 1D shaping filter or to force a 1D notch filter. 0 - Automatic filter selection 1 - Force 1D shaping filter	
Y_SHAPE_SEL_1D[5:0]			R/W
0x96	10011000	This control is used to select the Y shaping filter for the 1D inputs. Refer to the Hardware Manual for details on Y shaping filters. 011000 - Default	
C_SHAPE_SEL_1D[4:0]			R/W
0x97	00000010	This control is used to select the C shaping filter for the 1D inputs. Refer to the Hardware Manual for details on C shaping filters. 00010 - Default	
SDP_NSY_DIS_SFS_STD			R/W
0x98	10111111	This control is used to enable an HQI shaping filter when a noisy input is detected. 1 - Disable HQI shape filter if noisy input detected 0 - Allow HQI shape filter even if noisy input detected	
SDP_HSW2_DIS_SFS_STD			R/W
0x98	10111111	This control is used to enable an HQI shaping filter when a head switch is detected on the input by head switch algorithm 2. 1 - Disable HQI shape filter if head switch detection algorithm 2 detects head switches 0 - Allow HQI shape filter even if head switch detection algorithm 2 detects head switches	
SDP_HSW1_DIS_SFS_STD			R/W
0x98	10111111	This control is used to enable an HQI shaping filter when a head switch is detected on the input by head switch algorithm 1. 1 - Disable HQI shape filter if head switch detection algorithm 1 detects head switches. 0 - Allow HQI shape filter even if head switch detection algorithm 1 detects head switches.	
SDP_LC_DIS_SFS_STD			R/W
0x98	10111111	This control is used to enable an HQI shaping filter when an incorrect number of lines per frame is detected. 1 - Disable HQI shape filter if clean and incorrect lines per frame detected 0 - Allow HQI shape filter even if incorrect number of lines per frame detected	
SDP_BLK_DIS_SFS_STD			R/W
0x98	10111111	This control is used to enable an HQI shaping filter when a nonstandard block length is detected. 1 - Disable HQI shape filter if clean input and sdp_blk_nstd detected 0 - Allow HQI shape filter even if sdp_blk_nstd detected	
SDP_FLD_SFS_STD			R/W
0x98	10111111	This control is used to enable an HQI shaping filter when a nonstandard field is detected. 1 - Disable HQI shape filter if clean input and sdp fld_nstd detected 0 - Allow HQI shape filter even if sdp fld_nstd detected	
SDP_FRM_DIS_SFS_STD			R/W
0x98	10111111	This control is used to enable an HQI shaping filter when a nonstandard frame is detected. 1 - Disable HQI shape filter if clean input and sdp_frm_nstd detected 0 - Allow HQI shape filter even if sdp_frm_nstd detected	
SDP_VNSY_DIS_SFS_STD			R/W
0x98	10111111	This control is used to enable an HQI shaping filter when a very noisy input is detected. 1 - Disable HQI shape filter if very noisy input detected 0 - Allow HQI shape filter even if noisy input detected	

Reg	Bits	Description	
SDP_SHAPE_STD_FILT_SEL[2:0]			R/W
0x99	00010000	This control is used to select the amount of filtering. 000 - No filtering 001 - 0.25 sec 010 - 0.55 sec 011 - 0.81 sec 100 - 1.10 sec 101 - 1.36 sec 110 - 1.63 sec 111 - 2.00 sec	
SDP_ALLOW_3D_FILT_SEL[2:0]			R/W
0xA9	00000001	This control is used to set the time constant applied to the deglitching filter for the 3D comb decision. 000 - No filtering 001 - 0.25 sec 010 - 0.55 sec 011 - 0.81 sec 100 - 1.10 sec 101 - 1.36 sec 110 - 1.63 sec 111 - 2.00 sec	
SDP_NOISY_THR[7:0]			R/W
0xA1	01010000	This control is used to set the threshold for input to be detected as noisy. A higher value reduces the possibility of detecting an input as noisy.	
SDP_VERY_NOISY_THR[7:0]			R/W
0xA2	10100000	This control is used to set the threshold for input to be detected as very noisy. A higher valued reduces the possibility of detecting the input to be very noisy.	
SDP_CKILL_DIS_3D			R/W
0xA3	10111110	This control is used to enable 3D combing if color kill mode is active. 1 - Disable 3D comb if color kill active 0 - Allow 3D comb even if color kill active	
SDP_CKILL_DIS_2D			R/W
0xA4	10111111	This control is used to enable 2D combing even if color kill mode is active. This would effectively be pass through mode. 1 - Disable 2D comb if color kill active 0 - Use 2D comb even if color kill active	
SDP_NOISY_HSW2_DIS_3D			R/W
0xA4	10111111	This control is used to enable 3D combing if a noisy input is detected and headswitch is detected on the input by algorithm 2. 1 - Disable 3D comb if noisy input detected and head switch detection algorithm 2 detects head switches 0 - Allow 3D comb if noisy input detected even if head switch detection algorithm 2 detects head switches	
SDP_NOISY_HSW1_DIS_3D			R/W
0xA4	10111111	This control is used to enable 3D combing if a noisy input is detected and a headswitch is detected on the input by algorithm 1. 1 - Disable 3D comb if noisy input detected and head switch detection algorithm 1 detects head switches 0 - Allow 3D comb if noisy input detected even if head switch detection algorithm 1 detects head switches	
SDP_NOISY_LC_DIS_3D			R/W
0xA4	10111111	This control is used to enable 3D combing if a noisy input is detected and a nonstandard number of lines per frame is detected on the input. 1 - Disable 3D comb if noisy input detected and incorrect lines per frame detected 0 - Allow 3D comb if noisy input detected even if incorrect number of lines per frame detected	
SDP_NOISY_BLK_DIS_3D			R/W
0xA4	10111111	This control is used to enable 3D combing if a noisy input is detected and a nonstandard block length is detected on the input. 1 - Disable 3D comb if noisy input detected and sdp_blk_nstd detected 0 - Allow 3D comb if noisy input detected even if sdp_blk_nstd detected	
SDP_NOISY_FLD_DIS_3D			R/W
0xA4	10111111	This control is used to enable 3D combing if a noisy input is detected and a nonstandard field length is detected. 1 - Disable 3D comb if noisy input detected and sdp fld_nstd detected 0 - Allow 3D comb if noisy input detected even if sdp fld_nstd detected	

Reg	Bits	Description	
SDP_NOISY_FRM_DIS_3D			R/W
0xA4	101111 <u>1</u>	This control is used to enable 3D combing if a noisy input is detected and a nonstandard frame length is detected. 1 - Disable 3D comb if noisy input detected and sdm_frm_nstd detected 0 - Allow 3D comb if noisy signal even if sdm_frm_nstd detected	
SDP_NOISY_DIS_3D			R/W
0xA4	101111 <u>1</u>	This control is used to enable 3D combing if a noisy input is detected. 1 - Disable 3D comb if noisy input detected 0 - Allow 3D comb if noisy input detected	
SDP_P60_N443_DIS_3D			R/W
0xA5	<u>1</u> 0111111	This control is used to enable 3D combing for PAL-60 and NTSC-443 even though it does not work perfectly due to a suboptimal mathematical relationship of subcarrier frequency versus horizontal frequency for those standards. 1 - Disable 3D comb for PAL-60 and NTSC-443 inputs 0 - Use 3D comb on PAL-60 and NTSC-443 inputs	
SDP_VNOISY_HSW2_DIS_3D			R/W
0xA5	<u>1</u> 0111111	This control is used to enable 3D combing if a very noisy input is detected and head switch is detected on the input by algorithm 2. 1 - Disable 3D comb if very noisy input detected and head switch detection algorithm 2 detects head switches 0 - Allow 3D comb if very noisy input detected even if head switch detection algorithm 2 detects head switches	
SDP_VNOISY_HSW1_DIS_3D			R/W
0xA5	10 <u>1</u> 11111	This control is used to enable 3D combing if a very noisy input is detected and head switch is detected on the input by algorithm 1. 1 - Disable 3D comb if very noisy input detected and head switch detection algorithm 1 detects head switches 0 - Allow 3D comb if very noisy input detected even if head switch detection algorithm 1 detects head switches	
SDP_VNOISY_LC_DIS_3D			R/W
0xA5	101 <u>1</u> 1111	This control is used to enable 3D combing if a very noisy input is detected and an incorrect frame length is detected on the input. 1 - Disable 3D comb if very noisy input detected and incorrect lines per frame detected 0 - Allow 3D comb if very noisy input detected even if incorrect number of lines per frame detected	
SDP_VNOISY_BLK_DIS_3D			R/W
0xA5	1011 <u>1</u> 111	This control is used to enable 3D combing if a very noisy input is detected and a nonstandard block length is detected on the input. 1 - Disable 3D comb if very noisy input detected and sdm_blk_nstd detected 0 - Allow 3D comb if very noisy input detected even if sdm_blk_nstd detected	
SDP_VNOISY_FLD_DIS_3D			R/W
0xA5	10111 <u>1</u> 11	This control is used to enable 3D combing if a very noisy input is detected and a nonstandard field length is detected on the input. 1 - Disable 3D comb if very noisy input detected and sdm fld_nstd detected 0 - Allow 3D comb if very noisy input detected even if sdm fld_nstd detected	
SDP_VNOISY_FRM_DIS_3D			R/W
0xA5	101111 <u>1</u>	This control is used to enable 3D combing if a very noisy input is detected and a nonstandard frame length is detected on the input. 1 - Disable 3D comb if very noisy input and sdm_frm_nstd detected 0 - Allow 3D comb if very noisy signal even if sdm_frm_nstd detected	
SDP_VNOISY_DIS_3D			R/W
0xA5	1011111 <u>1</u>	This control is used to enable 3D combing if a very noisy input is detected. 1 - Disable 3d comb if very noisy input detected 0 - Allow 3d comb if very noisy input detected	
SDP_3D_COMB_NOISE_SNS[6:0]			R/W
0xA8	<u>0</u> 1000000	This control is used to set the 3D comb noise sensitivity. Larger values allow more temporal comb for noisy RF signals but may also introduce motion error. This is an unsigned control. 1000000 - Smaller values increase 3D processing	
SDP_3D_COMB_CHROMA_CORE[3:0]			R/W
0xA9	<u>1</u> 0001000	This control is used to set 3D comb chroma coring. Larger values decrease 3D comb motion detection sensitivity to chroma motion and noise. This is an unsigned control. 1000 - Larger values increase 3D processing	

Reg	Bits	Description	
SDP_3D_COMB_CHROMA_SNS[3:0]			R/W
0xA9	10001000	This control is used to set 3D comb chroma sensitivity. Larger values increase 3D comb motion detection sensitivity to chroma motion and noise. This is an unsigned control. 1000 - Smaller values increase 3D processing	
SDP_3D_COMB_LUMA_CORE[3:0]			R/W
0xAA	10001000	This control is used to set the 3D comb luma coring. Larger values decrease 3D comb motion detection sensitivity to luma motion and noise. This is an unsigned control. 1000 - Larger values increase 3D processing	
SDP_3D_COMB_LUMA_SNS[3:0]			R/W
0xAA	10001000	This control is used to set the 3D comb luma sensitivity. Larger values increase 3D comb motion detection sensitivity to luma motion and noise. This is an unsigned control. 1000 - Smaller values increase 3D processing	
SDP_LBOX_END_DEL[3:0]			R/W
0xDB	10001000	This control is used to set the letterbox detection end line versus the default position. 1000 - Letterbox detection ends with last active line of video on field	
SDP_LBOX_BEG_DEL[3:0]			R/W
0xDB	10001000	This control is used to set the letterbox detection begin line versus the default position. 1000 - Letterbox detection aligned with start line of active video. Window starts after VBI data line.	
SDP_LBOX_BLK_LVL[2:0]			R/W
0xDC	00000010	This control is used to set the expected blank level in the lbox detection block. A larger value corresponds to a higher blank level. 000 - None 001 - None 010 - None 011 - None 100 - None 101 - None 110 - None 111 - None	
SDP_LBOX_THR[4:0]			R/W
0xDC	00000010	This control is used to set the threshold for black line detection in letterbox detection. A larger value increases the possibility of detecting a line as black. 00010 - Default threshold for detection of black lines	
SDP_FREE_RUN_AUTO			R/W
0xDD	10111100	This control is used to enable automatic free run operation. The part enters free run if no valid input video is detected. 1 - Free run if no valid input video detected 0 - Do not free run even if no valid input video detected	
SDP_FREE_RUN_MAN_COL_EN			R/W
0xDD	10111100	This control is used to enable the manual setting of video data output in video mode. If in free run, luma and chroma values are set by sdp_free_run_y, sdp_free_run_v, and sdp_free_run_u. 1 - If in free run, output manual luma and chroma values set by sdp_free_run_y, sdp_free_run_v, and sdp_free_run_u 0 - If in free run, output decoded video data	
SDP_FREE_RUN_CBAR_EN			R/W
0xDD	10111100	This control is used to select the color bar pattern to be output in manual free run mode. 1 - If in free run mode, output color bar data 0 - If in free run mode, output free run mode data	
SDP_FORCE_FREE_RUN			R/W
0xDD	10111100	This control is used to force free run mode irrespective of the input lock status. 1 - Force free run 0 - Normal operation	
SDP_FREE_RUN_Y[7:0]			R/W
0xDE	00100011	This control is used to set the luma level to output in free run mode if sdp_free_run_man_col_en is set to 1.	
SDP_FREE_RUN_V[3:0]			R/W
0xDF	01111101	This control is used to set the V level to output in free run mode if sdp_free_run_man_col_en is set to 1.	

Reg	Bits	Description	
	SDP_FREE_RUN_U[3:0]		R/W
0xDF	01111101	This control is used to set the U level to output in free run mode if sdp_free_run_man_col_en is set to 1.	

2.8 ADDR 94 (SDP_IO)

Reg	Bits	Description	
FIELD_2_FLAG			R
0x38	00000000	This readback indicates if the current field is Field 1 or Field 2 for interlaced standards. 0 - Field is field 1 1 - Field is field 2	
FIELD_1_LENGTH[9:0]			R
0x38	00000000	This readback indicates the length of Field 1 in number of lines.	
0x39	00000000		
FIELD_2_LENGTH[9:0]			R
0x3A	00000000	This readback indicates the length of Field 2 in number of lines.	
0x3B	00000000		
H_ERR_1D_ON[7:0]			R/W
0x3C	00010000	This control is used to set the threshold for turning on 1D filtering. If the unsigned HSync period error is greater than this value multiplied by 16, 1D filtering will be enabled. 00010000 - Default	
H_ERR_1D_OFF[7:0]			R/W
0x3D	00001000	This control is used to set the threshold for turning off 1D filtering. If the unsigned HSync period error is less than this value multiplied by 16, 1D filtering will be disabled. 00001000 - Default	
H_ERR_CGAIN_OVR_ON[7:0]			R/W
0x3E	00001100	This control is used to set the threshold for turning on the C active gain override. If the unsigned HSync period error is greater than this value multiplied by 16, the C active gain will be overridden by c_ad_gain. 00001100 - Default	
H_ERR_CGAIN_OVR_OFF[7:0]			R/W
0x3F	00001011	This control is used to set the threshold for turning off the C active gain override. If the unsigned HSync period error is less than this value multiplied by 16, the C active gain will be overridden by c_ad_gain. 00001011 - Default	
C_GAIN_ACT[12:0]			R
0x40	00000000	This readback indicates the current active path chroma gain. 0xXXX - Chroma Gain readback value	
0x41	00000000		
C_GAIN_AD[12:0]			R
0x42	00000000	This readback indicates the current detect path chroma gain. 0xXXX - Chroma Gain Readback value	
0x43	00000000		
BURST_POWER_ACT[11:0]			R
0x44	00000000	This readback displays the active path burst power measurement. 0xXXX - Burst Power Readback value	
0x45	00000000		
BURST_POWER_AD[11:0]			R
0x46	00000000	This readback displays the autodetect path burst power measurement. 0xXXX - Burst Power Readback value	
0x47	00000000		
AUTO_CGAIN_OVR_EN			R/W
0x49	10111000	This control is used to enable the C active gain control. 0 - Disable C active gain override 1 - Enable automatic override of C active gain with c_ad_gain based on HSync period error	
FORCE_CGAIN_OVR_EN			R/W
0x49	10111000	This control is used to force the C active gain control. 0 - Do not force C active gain to be overwritten by c_ad_gain 1 - Force override of C active gain with c_ad_gain	
AUTO_C_COMB_1D			R/W
0x49	10111000	This control is used to select automatic C 1D combing. 0 - Disable automatic C 1D combing based on HSync period error 1 - Allow automatic C 1D comb based on HSync period error	

Reg	Bits	Description	
AUTO_Y_COMB_1D			R/W
0x49	10111000	This control is used to select automatic Y 1D combing. 0 - Disable automatic Y 1D combing based on HSync period error 1 - Allow automatic Y 1D comb based on HSync period error	
AUTO_1D_YC_SEP_EN			R/W
0x49	10111000	This control is used to select automatic 1D YC separation. 0 - Disable automatic 1D YC separation based on HSync period error 1 - Enable automatic 1D YC separation based on HSync period error	
FORCE_Y_1D			R/W
0x49	10111000	This control is used to force 1D filtering on the Y channel. 1 - Force 1D filtering on Y	
FORCE_C_1D			R/W
0x49	10111000	This control is used to force 1D filtering on the C channel. 1 - Force 1D filtering on C	
HS_PERIOD_ERR_RAW[11:0]			R
0x4A 0x4B	00000000 00000000	This readback displays the raw HSync period error. 0xXXX - Raw HS readback value	
HS_PERIOD_ERR_FILT[11:0]			R
0x4C 0x4D	00000000 00000000	This readback displays the filtered HSync period error. 0xXXX - Filtered HS readback value	
BURST_DETECTED			R
0x4E	00000000	This readback displays the burst detected flag. 0 - No color burst detected 1 - Color burst detected	
BURST_4_43_DET			R
0x4E	00000000	This readback displays the burst frequency measurement. It is valid only if burst_4_43_valid is set to 1. 0 - Burst frequency is close to 3.58 MHz 1 - Burst is close to 4.43 MHz	
BURST_4_43_VALID			R
0x4E	00000000	This readback displays the burst frequency measurement valid flag. 0 - burst_4_43_det readback invalid 1 - burst_4_43_det readback valid	
HS_PERIOD_VALID			R
0x4E	00000000	This readback displays the HSync period measurement valid flag. 0 - hs_period_err_filt readback invalid 1 - hs_period_err_filt readback valid	
UPD_SDP_RB			SC
0x4F	00000000	This control is used to update the c_gain_act, c_gain_ad, burst_power_act, burst_power_ad, hs_period_err_raw and hs_period_err_filt readback registers. 0 - Freeze SDP multiregister readbacks 1 - Update SDP multiregister readbacks	
SDP_RING_RED_EN			R/W
0x51	00000000	This control is used to enable the ringing reduction block to remove a ringing artifact from around sharp edges. 0 - Disable ringing reduction block 1 - Enable ringing reduction block	
SDP_RING_RED_LEVEL[6:0]			R/W
0x51	00000000	This control is used to provide level control for the ringing reduction algorithm. Higher values give a more dramatic ringing reduction. 0000000 - No ringing reduction	
SDP_CSC_SCALE			R/W
0xE0	01000111	This control is used to set the CSC gain. 0 - CSC scaler set to 1 1 - CSC scaler set to 2	

Reg	Bits	Description	
SDP_CSC_AUTO			R/W
0xE0	01000111	This control is used to select the CSC operation. 0 - Use manual CSC coefficients 1 - Use automatic CSC coefficients	
SDP_A1[12:0]			R/W
0xE0 0xE1	01000111 11010010	This control is used to set the CSC A1 coefficient for the SDP output color space converter. 0x07D2 - Default	
SDP_A2[12:0]			R/W
0xE2 0xE3	00000000 00000000	This control is used to set the CSC A2 coefficient for the SDP output color space converter. 0x0000 - Default	
SDP_A3[12:0]			R/W
0xE4 0xE5	00000000 01000000	This control is used to set the CSC A3 coefficient for the SDP output color space converter. 0x0040 - Default	
SDP_A4[14:0]			R/W
0xE6 0xE7	01111111 00000000	This control is used to set the CSC A4 coefficient for the SDP output color space converter. 0x7F00 - Default	
SDP_B1[12:0]			R/W
0xE8 0xE9	00000000 00000000	This control is used to set the CSC B1 coefficient for the SDP output color space converter. 0x0000 - Default	
SDP_B2[12:0]			R/W
0xEA 0xEB	00001001 00100110	This control is used to set the CSC B2 coefficient for the SDP output color space converter. 0x0926 - Default	
SDP_B3[12:0]			R/W
0xEC 0xED	00000000 00000000	This control is used to set the CSC B3 coefficient for the SDP output color space converter. 0x0000 - Default	
SDP_B4[14:0]			R/W
0xEE 0xEF	00000000 00000000	This control is used to set the CSC B4 coefficient for the SDP output color space converter. 0x0000 - Default	
SDP_C1[12:0]			R/W
0xF0 0xF1	00000000 00000000	This control is used to set the CSC C1 coefficient for the SDP output color space converter. 0x0000 - Default	
SDP_C2[12:0]			R/W
0xF2 0xF3	00000000 00000000	This control is used to set the CSC C2 coefficient for the SDP output color space converter. 0x0000 - Default	
SDP_C3[12:0]			R/W
0xF4 0xF5	00000110 10000001	This control is used to set the CSC C3 coefficient for the SDP output color space converter. 0x0681 - Default	
SDP_C4[14:0]			R/W
0xF6 0xF7	00000000 00000000	This control is used to set the CSC C4 coefficient for the SDP output color space converter. 0x0000 - Default	

2.9 ADDR 68 (HDMI)

Reg	Bits	Description	
HDCP_A0			R/W
0x00	00000000	This control is used to set the second LSB of the HDCP port I2C address. 0 - I2C address for HDCP port is 0x74. Used for single-link mode or 1st receiver in dual-link mode. 1 - I2C address for HDCP port is 0x76. Used only for 2nd receiver dual-link mode.	
HDCP_ONLY_MODE			R/W
0x00	00000000	This control is used to configure a HDCP only mode for simultaneous analog and HDMI modes. Refer to the <code>adc_hdmi_simultaneous_mode</code> bit. By selecting HDCP only mode, HDMI activity is reduced and it can be used as a power saving feature in simultaneous analog and HDMI operation. 0 - Normal operation 1 - HDCP only mode	
BG_MEAS_PORT_SEL[2:0]			R/W
0x00	00000000	This control is used to select a background port on which HDMI measurements are to be made and provided in the background measurement registers. The port in question must be set as a background port in order for this setting to be effective. There is no conflict if this matches the port selected by <code>hdmi_port_select</code> . 000 - Port A 001 - Port B 010 - Port C 011 - Port D	
HDMI_PORT_SELECT[2:0]			R/W
0x00	00000000	This control is used to select the HDMI primary port. 000 - Port A 001 - Port B 010 - Port C 011 - Port D	
MUX_DSD_OUT			R/W
0x01	00000000	This control is used to set the override for the DSD output. 0 - Override by outputting I2S data 1 - Override by outputting DSD/DST data	
OVR_AUTO_MUX_DSD_OUT			R/W
0x01	00000000	This control is used to override the DSD/DST output control. In automatic control, DSD or I2S interface is selected according to the type of packet received. The DSD/DST interface is enabled if the part receives DSD or DST audio sample packet. The I2S interface is enabled when the part receives audio sample packets or when no packet is received. In manual mode, <code>mux_dsd_out</code> selects the output interface. 0 - Automatic DSD/DST output control 1 - Override DSD/DST output control	
OVR_MUX_HBR			R/W
0x01	00000000	This control is used to select automatic or manual configuration for HBR outputs. Automatically, HBR outputs are encoded as SPDIF streams. In manual mode, <code>mux_hbr_out</code> selects the audio output interface. 0 - Automatic HBR output control 1 - Manual HBR output control	
MUX_HBR_OUT			R/W
0x01	00000000	This control is used to manually select the audio output interface for HBR data. It is valid when <code>ovr_mux_hbr</code> is set to 1. 0 - Override by outputting I2S data 1 - Override by outputting SPDIF data	
TERM_AUTO			R/W
0x01	00000000	This control is used to select automatic or manual control of clock termination. If automatic mode termination is enabled, then the termination on the port selected via <code>hdmi_port_select[1:0]</code> is enabled. The termination is disabled on all other ports. 0 - Disable termination automatic control 1 - Enable termination automatic control	
EN_BG_PORT_D			R/W
0x02	00000000	This control is used to set Port D in background mode to establish a HDCP link with its source even if the port is not selected by <code>hdmi_port_select</code> . This control has no effect if the port is selected by <code>hdmi_port_select</code> . 0 - Disable port unless selected with <code>hdmi_port_select</code> 1 - Enable port in background mode	

Reg	Bits	Description	
EN_BG_PORT_C			R/W
0x02	000000 <u>00</u>	This control is used to set Port C in background mode to establish a HDCP link with its source, even if the port is not selected by hdmi_port_select. This control has no effect if the port is selected by hdmi_port_select. 0 - Disable port disabled unless selected with hdmi_port_select 1 - Enable port in background mode	
EN_BG_PORT_B			R/W
0x02	000000 <u>00</u>	This control is used to set Port B in background mode to establish a HDCP link with its source even if the port is not selected by hdmi_port_select. This control has no effect if the port is selected by hdmi_port_select. 0 - Disable port unless selected with hdmi_port_select 1 - Enable port in background mode	
EN_BG_PORT_A			R/W
0x02	000000 <u>00</u>	This control is used to set Port A in background mode to establish a HDCP link with its source even if the port is not selected by hdmi_port_select. This control has no effect if the port is selected by hdmi_port_select. 0 - Disable port unless selected with hdmi_port_select 1 - Enable port in background mode	
I2SOUTMODE[1:0]			R/W
0x03	<u>00</u> 11000	This control is used to configure the I2S output interface. 00 - I2S mode 01 - Right justified 10 - Left justified 11 - Raw SPDIF (IEC60958) Mode	
I2SBITWIDTH[4:0]			R/W
0x03	000 <u>11</u> 000	This control is used to adjust the bit width for right justified mode on the I2S interface. xxxxx - Number of bits 00000 - 0 bit 00001 - 1 bit 00010 - 2 bits 11000 - 24 bits 11110 - 30 bits 11111 - 31 bits	
AV_MUTE			R
0x04	<u>00</u> 000000	This readback displays the avmute status received in the last general control packet received. 0 - avmute not set 1 - avmute set	
HDCP_KEYS_READ			R
0x04	<u>00</u> 000000	This readback indicates a successful read of the HDCP keys and/or KSV from the internal HDCP key OTP ROM. A logic high is returned when the read is successful. 0 - HDCP keys and/or KSV not yet read 1 - HDCP keys and/or KSV HDCP keys read	
HDCP_KEY_ERROR			R
0x04	<u>000</u> 00000	This readback indicates if a checksum error occurred while reading the HDCP and/or KSV from the HDCP key ROM. A high is returned when the HDCP key master encounters an error while reading the HDCP key OTP ROM. 0 - No error occurred while reading HDCP keys 1 - HDCP keys read error	
HDCP_RI_EXPIRED			R
0x04	00000 <u>0000</u>	This readback is set high when a calculated Ri has not been read by the source TX on the active port. It remains high until the next Aksv update.	
TMDS_PLL_LOCKED			R
0x04	000000 <u>00</u>	This readback indicates if the TMDS PLL is locked to the TMDS clock input of the selected HDMI port. 0 - TMDS PLL not locked 1 - TMDS PLL locked to TMDS clock input of selected HDMI port	
AUDIO_PLL_LOCKED			R
0x04	0000000 <u>00</u>	This readback indicates the audio DPLL lock status. 0 - Audio DPLL not locked 1 - Audio DPLL locked	

Reg	Bits	Description	
HDMI_MODE			R
0x05	00000000	This readback indicates whether the stream processed by the HDMI core is a DVI or an HDMI stream. 0 - DVI mode detected 1 - HDMI mode detected	
HDMI_CONTENT_ENCRYPTED			R
0x05	00000000	This readback indicates if the input stream processed by the HDMI core is HDCP encrypted or not. 0 - Input stream processed by HDMI core not HDCP encrypted 1 - Input stream processed by HDMI core HDCP encrypted	
DVI_HSYNC_POLARITY			R
0x05	00000000	This readback indicates the polarity of the HSync encoded in the input stream. 0 - HSync active low 1 - HSync active high	
DVI_VSYNC_POLARITY			R
0x05	00000000	This readback indicates the polarity of the VSync encoded in the input stream. 0 - VSync active low 1 - VSync active high	
HDMI_PIXEL_REPETITION[3:0]			R
0x05	00000000	This readback provides the current HDMI pixel repetition value decoded from the AVI InfoFrame received. The HDMI receiver automatically discards repeated pixel data and divides the pixel clock frequency appropriately as per the pixel repetition value. 0000 - 1x 0001 - 2x 0010 - 3x 0011 - 4x 0100 - 5x 0101 - 6x 0110 - 7x 0111 - 8x 1000 - 9x 1001 - 10x 1010 - 1111 - Reserved	
VERT_FILTER_LOCKED			R
0x07	00000000	This readback indicates whether or not the vertical filter is locked and the vertical synchronization parameter measurements are valid for readback. 0 - Vertical filter not locked 1 - Vertical filter locked	
AUDIO_CHANNEL_MODE			R
0x07	00000000	This readback flags stereo or multichannel audio packets. Note that stereo packets may carry compressed multichannel audio. 0 - Stereo audio (may be compressed multichannel) 1 - Multichannel uncompressed audio detected (3-8 channels)	
DE_REGEN_FILTER_LOCKED			R
0x07	00000000	This readback displays the DE regeneration filter lock status. It indicates if the DE regeneration section has locked to the received DE and if the horizontal synchronization parameter measurements are valid for readback. 0 - DE regeneration not locked 1 - DE regeneration locked to incoming DE	
LINE_WIDTH[12:0]			R
0x07 0x08	00000000 00000000	This readback displays the number of active pixels in a line. Line width is a horizontal synchronization measurement. This measurement is only valid when the DE regeneration filter is locked. 000000000000 - Number of active pixels per line xxxxxxxxxxx - Number of active pixels per line	
FIELD0_HEIGHT[12:0]			R
0x09 0x0A	00000000 00000000	This readback displays the number of active lines in field 0. Field 0 height is a vertical filter measurement. This measurement is valid only when the vertical filter has locked. 000000000000 - Number of active lines in Field 0 xxxxxxxxxxxxx - Number of active lines in Field 0	

Reg	Bits	Description	
DEEP_COLOR_MODE[1:0]			R
0x0B	00000000	This readback displays the deep color mode information extracted from the general control packet. 00 - 8 bits per channel 01 - 10 bits per channel 10 - 12 bits per channel 11 - 16 bits per channel (not supported)	
HDMI_INTERLACED			R
0x0B	00000000	This readback indicates the HDMI input interlace status, a vertical filter measurement. 0 - Progressive input 1 - Interlaced input	
FIELD1_HEIGHT[12:0]			R
0x0B 0x0C	00000000 00000000	This readback displays the number of active lines in field 1. Field 1 height is a vertical filter measurement. This readback gives the number of active lines in field. This measurement is valid only when the vertical filter has locked. Field 1 height is a vertical filter measurement. 000000000000 - Number of active lines in Field 1 xxxxxxxxxxxx - Number of active lines in Field 1	
HDMI_PORT_SELECT_TX_B[2:0]			R/W
0x0D	0000100	This control is used to select the HDMI primary port for Tx B. 000 - Port A 001 - Port B 010 - Port C 011 - Port D	
FREQTOLERANCE[3:0]			R/W
0x0D	0000100	This control is used to set the tolerance in MHz for a new TMDS frequency detection. This tolerance is used for the audio mute mask <code>mt_msk_vclk_chng</code> and the HDMI status bit <code>new_tmds_frq_raw</code> . 0100 - Default tolerance in MHz for new TMDS frequency detection xxxx - Tolerance in MHz for new TMDS frequency detection	
CTS_CHANGE_THRESHOLD[5:0]			R/W
0x10	00100101	This control is used to set the tolerance for change in the CTS value. This tolerance is used for the audio mute mask, <code>mt_msk_new_cts</code> ; the HDMI status bit, <code>cts_pass_thrsh_raw</code> ; and the HDMI interrupt status bit, <code>cts_pass_thrsh_st</code> . It controls the amounts of LSBs that the CTS can change before an audio mute, status change or interrupt is triggered. 100101 - Default tolerance of CTS value for <code>cts_pass_thrsh_raw</code> and <code>mt_msk_new_cts</code> xxxxxx - Tolerance of CTS value for <code>cts_pass_thrsh_raw</code> and <code>mt_msk_new_cts</code>	
AUDIO_FIFO_ALMOST_FULL_THRESHOLD[6:0]			R/W
0x11	01111101	This control is used to set the threshold used for <code>fifo_near_ovrfl_raw</code> . The <code>fifo_near_ovrfl_st</code> interrupt is triggered if audio FIFO reaches this level. 1111101 - Default	
AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[6:0]			R/W
0x12	0000010	This control is used to set the threshold used for <code>fifo_near_uflo_raw</code> . The <code>fifo_near_uflo_st</code> interrupt is triggered if audio FIFO goes below this level. 0000010 - Default	
AC_MSK_VCLK_CHNG			R/W
0x13	01111111	This control is used to set the audio coast mask for a TMDS clock change. When set, the audio DPLL coasts if the TMDS clock has any irregular/missing pulses. 1 - Audio DPLL coasts if TMDS clock contains irregular/missing pulses 0 - Audio DPLL does not coast if TMDS clock contains irregular/missing pulses	
AC_MSK_VPLL_UNLOCK			R/W
0x13	01111111	This control is used to set the audio coast mask for TMDS PLL unlock. When set, the audio DPLL coasts if the TMDS PLL unlocks. 1 - Audio DPLL coasts if TMDS DPLL unlocks 0 - Audio DPLL does not coast if TMDS DPLL unlocks	
AC_MSK_NEW_CTS			R/W
0x13	01111111	This control is used to set the audio coast mask for a new ACR CTS value. When set the audio DPLL coasts if CTS changes by more than the threshold defined in <code>cts_change_threshold[5:0]</code> . 1 - Audio DPLL coasts if CTS changes by more than the threshold set in register <code>cts_change_threshold[5:0]</code> . 0 - Audio DPLL does not coast if CTS changes by more than the threshold set in register <code>cts_change_threshold[5:0]</code> .	

Reg	Bits	Description	R/W
AC_MSK_NEW_N			R/W
0x13	01111111	This control is used to set the audio coast mask for a new ACR N value. When set, the audio DPLL coasts if a N value changes. 1 - Audio DPLL coasts if a change in the N value occurs. 0 - Audio DPLL does not coast if a change in the N value occurs.	
AC_MSK_CHNG_PORT			R/W
0x13	01111111	This control is used to set the audio coast mask for an HDMI port change. When set, the audio DPLL coasts if a change in the active port occurs. 1 - Audio DPLL coasts if the active port is changed. 0 - Audio DPLL does not coast if the active port is changed	
AC_MSK_VCLK_DET			R/W
0x13	01111111	This control is used to set the audio coast mask for a TMDS clock detection. It sets the audio PLL to coast if no TMDS clock is detected on the active port. 1 - Audio DPLL coasts if a TMDS clock is not detected on the active port. 0 - Audio DPLL does not coast if a TMDS clock is not detected on the active port.	
MT_MSK_COMPRS_AUD			R/W
0x14	00111111	This control is used to set the audio coast mask for compressed audio. It sets the audio mutes if the audio received is in a compressed format. 1 - Audio mute occurs if audio is received in compressed format.	
MT_MSK_AUD_MODE_CHNG			R/W
0x14	00111111	This control is used to set the audio mute mask for an audio mode change. It sets the audio mutes if audio changes between any of the following: PCM, DSD, HBR or DST formats. 1 - Audio mute occurs if audio changes between any of the following: PCM, DSD, HBR or DST formats	
MT_MSK_PARITY_ERR			R/W
0x14	00111111	This control is used to set the audio mute mask for a parity error. It sets the audio mutes if an audio sample packet is received with an incorrect parity bit. 1 - Audio mute occurs if audio sample packet is received with incorrect parity bit.	
MT_MSK_VCLK_CHNG			R/W
0x14	00111111	This control is used to set the audio mute mask for a TMDS clock change. It sets the audio mutes if the TMDS clock has irregular/missing pulses. 1 - Audio mute occurs if the TMDS clock has irregular/missing pulses	
MT_MSK_APLL_UNLOCK			R/W
0x15	11111111	This control is used to set the audio mute mask for an audio PLL unlock. It sets the audio mutes if the audio PLL unlocks. 1 - Audio mute occurs if the audio PLL unlocks	
MT_MSK_VPLL_UNLOCK			R/W
0x15	11111111	This control is used to set the audio mute mask for a TMDS PLL unlock. When set, audio mutes if the TMDS PLL unlocks. 1 - Audio mute occurs if the TMDS PLL unlocks.	
MT_MSK_ACR_NOT_DET			R/W
0x15	11111111	This control is used to set the audio mute mask for an ACR packet. When set, the audio mutes if an ACR packet is not received within one VSync. 1 - Audio mute occurs if ACR packet not received within one VSync	
MT_MSK_FLATLINE_DET			R/W
0x15	11111111	This control is used to set the audio mute mask for the flatline bit. When set, the audio mutes if an audio packet is received with the flatline bit set. 1 - Audio mute occurs if audio packet received with flatline bit set	
MT_MSK_FIFO_UNDERFLOW			R/W
0x15	11111111	This control is used to set the audio mute mask for FIFO underflow. 1 - Audio mute occurs if FIFO underflows	
MT_MSK_FIFO_OVERFLOW			R/W
0x15	11111111	This control is used to set the audio mute mask for FIFO overflow. 1 - Audio mute occurs if FIFO overflows	
MT_MSK_AVMUTE			R/W
0x16	11111111	This control is used to set the audio mute mask for avmute. When set, the audio mutes if a general control packet is received with set_avmute set. 1 - Audio mute occurs if avmute set by general control packet	

Reg	Bits	Description	
MT_MSK_NOT_HDMIMODE			R/W
0x16	11111111	This control is used to set the audio mute mask for a non HDMI input stream. When set, the audio mutes if hdmi_mode goes low. 1 - Audio mute occurs if HDMI mode bit goes low	
MT_MSK_NEW_CTS			R/W
0x16	11111111	This control is used to set the audio mute mask for a change of ACR CTS. When set, the audio mutes if the CTS changes by more than the specified threshold set by cts_change_threshold. 1 - Audio mute occurs if CTS changes	
MT_MSK_NEW_N			R/W
0x16	11111111	This control is used to set the audio mute mask for a new ACR N. If set, the audio mutes if there is a change in the N value. 1 - Audio mute occurs if N changes	
MT_MSK_CHMODE_CHNG			R/W
0x16	11111111	This control is used to set the audio mute mask for an audio channel mode change. When set, the audio mutes if the channel mode changes between stereo and multichannel. 1 - Audio mute occurs if channel mode changes	
MT_MSK_APCKT_ECC_ERR			R/W
0x16	11111111	This control is used to set the audio mute mask for an audio packet ECC error. When set, the audio mutes if an uncorrectable error is detected in an audio packet by the ECC block. 1 - Audio mute occurs if uncorrectable error detected in audio packet by ECC block	
MT_MSK_CHNG_PORT			R/W
0x16	11111111	This control is used to set the audio mute mask for an HDMI port change. When set, the audio mutes if the HDMI port selection is changed. 1 - Audio mute occurs if HDMI port selection changed	
MT_MSK_VCLK_DET			R/W
0x16	11111111	This control is used to set the audio mute mask for a TMDS clock. When set, the audio mutes if a TMDS clock is not detected. 1 - Audio mute occurs if TMDS is not detected	
HBR_AUDIO_PCKT_DET			R
0x18	00000000	This control is used to detect an HBR packet. It resets to 0 on the 11th HSync leading edge following an HBR packet if a subsequent HBR packet is not detected. It also resets if an audio, DSD or DST packet sample packet is received, or after an HDMI reset condition. 0 - No HBR audio packet received within last 10 HSyncs 1 - HBR audio packet received within last 10 HSyncs	
DST_AUDIO_PCKT_DET			R
0x18	00000000	This control is used to detect a DST audio packet. It resets to 0 on the 11th HSync leading edge following an DST packet if a subsequent DST is not received; or if an Audio, DSD or HBR packet sample packet was received or after an HDMI reset condition. 0 - No DST packet received within last 10 HSyncs 1 - DST packet received within last 10 HSync	
DSD_PACKET_DET			R
0x18	00000000	This control is used to detect a DSD audio packet. It resets to 0 on the 11th HSync leading edge following a DSD packet or if an audio, DST or HBR packet sample packet was received or after an HDMI reset condition. 0 - No DSD packet received within last 10 HSync 1 - DSD packet received within last 10 HSync	
AUDIO_SAMPLE_PCKT_DET			R
0x18	00000000	This control is used to detect an audio sample packet. It resets to 0 on the 11th HSync leading edge following an audio packet if a subsequent audio sample packet is not received or if a DSD, DST or HBR audio packet sample packet was received. 0 - No I_pcm or IEC 61937 compressed audio sample packet received within last 10 HSyncs 1 - I_pcm or IEC 61937 compressed audio sample packet received within last 10 HSync	
DST_DOUBLE			R
0x19	00000000	This readback indicates when the DST audio is double data rate. 0 - No DST double data rate audio detected 1 - DST double data rate audio detected	

Reg	Bits	Description	
IGNORE_PARITY_ERR			R/W
0x1A	10000000	This control is used to select the processing of audio samples even when they have a parity error. 0 - Discard audio sample packets that have invalid parity bit 1 - Process audio sample packets that have invalid parity bit	
MUTE_AUDIO			R/W
0x1A	10000000	This control is used to force an internal mute independently of the mute mask conditions 0 - Audio in normal operation 1 - Force audio mute	
WAIT_UNMUTE[2:0]			R/W
0x1A	10000000	This control is used to delay audio unmute. Once all mute conditions are inactive, wait_unmute[2:0] can specify a further delay time before unmuting. not_auto_unmute must be set to 0 for this control to be effective. 000 - Disable/cancel delayed unmute; audio unmutes directly after all mute conditions become inactive 001 - Unmute 250 ms after all mute conditions become inactive 010 - Unmute 500 ms after all mute conditions become inactive 011 - Unmute 750 ms after al	
NOT_AUTO_UNMUTE			R/W
0x1A	10000000	This control is used to disable the auto unmute feature. When set to 1, audio can be unmuted manually if all mute conditions are inactive by setting not_auto_unmute to 0 and then back to 1. 0 - Audio unmutes following a delay set by wait_unmute after all mute conditions become inactive 1 - Prevents audio from unmuting automatically	
DCFIFO_RESET_ON_LOCK			R/W
0x1B	00011000	This control is used to enable the reset/recentering of video FIFO on video PLL unlock. 0 - Do not reset on video PLL lock 1 - Reset FIFO on video PLL lock	
DCFIFO_KILL_NOT_LOCKED			R/W
0x1B	00011000	This control is used to determine whether or not the output of the video FIFO is set to 0 when the video PLL is unlocked. 0 - FIFO data output regardless of video PLL lock status 1 - FIFO output is set to 0 if video PLL unlocked	
DCFIFO_KILL_DIS			R/W
0x1B	00011000	This control is used to determine whether or not the video FIFO output is zeroed if there is more than one resynchronization of the pointers within two FIFO cycles. 0 - FIFO output set to 0 if more than one resynchronization necessary during two FIFO cycles 1 - FIFO output never set to 0 regardless of how many resynchronizations occur	
DCFIFO_LOCKED			R
0x1C	00000000	This readback indicates if video FIFO is locked. 0 - Video FIFO not locked; video FIFO had to resynchronize between previous two VSyncs 1 - Video FIFO is locked; video FIFO did not have to resynchronize between previous two VSyncs	
DCFIFO_LEVEL[2:0]			R
0x1C	00000000	This readback indicates the distance between the read and write pointers. Overflow/underflow would read as level 0. Ideal centered functionality would read as 0b100. 000 - FIFO underflowed or overflowed 001 - FIFO about to overflow 010 - FIFO has some margin 011 - FIFO has some margin 100 - FIFO perfectly balanced 101 - FIFO has some margin 110 - FIFO has some margin 111 - FIFO about to underflow	
PDN_PKT_PROCESSOR			R/W
0x1D	00000000	This control is used to disable the clocking of the tmds rate section of the packet processor. Note that the audio clocking can be stopped separately, from the digital PLL (clock generator). 0 - Packet processor active 1 - Packet processor stopped, i.e. powered down	
UP_CONVERSION_MODE			R/W
0x1D	00000000	This control is used to select linear or interpolated 4:2:2 to 4:4:4 conversion. A 4:2:2 incoming stream is always upconverted to a 4:4:4 stream before being sent to the CP. 0 - Cr and Cb samples repeated in their respective channel 1 - Interpolate Cr and Cb values	

Reg	Bits	Description	
TOTAL_LINE_WIDTH[13:0]			R
0x1E 0x1F	00000000 00000000	This readback displays the total number of pixels per line. The total line width is a horizontal synchronization measurement. This measurement is valid only when the DE regeneration filter has locked. xxxxxxxxxxxxx - Total number of pixels per line	
HSYNC_FRONT_PORCH[12:0]			R
0x20 0x21	00000000 00000000	This readback displays the total number of pixels in the front porch. The HSync front porch width is a horizontal synchronization measurement. The unit of this measurement is unique pixels. This measurement is valid only when the DE regeneration filter is locked. Hsync front porch width is a horizontal synchronization measurement. xxxxxxxxxxxxx - Total number of pixels in front porch	
HSYNC_PULSE_WIDTH[12:0]			R
0x22 0x23	00000000 00000000	This readback displays the total number of pixels in the HSync pulse. The HSync pulse width is a horizontal synchronization measurement. The unit of this measurement is unique pixels. This measurement is valid only when the DE regeneration filter has locked. xxxxxxxxxxxxx - Total number of pixels in HSync pulse	
HSYNC_BACK_PORCH[12:0]			R
0x24 0x25	00000000 00000000	This readback displays the total number of pixels in the back porch. The HSync back porch width is a horizontal synchronization measurement. The unit of this measurement is unique pixels. This measurement is valid only when the DE regeneration filter has locked. xxxxxxxxxxxxx - Total number of pixels in back porch	
FIELD0_TOTAL_HEIGHT[13:0]			R
0x26 0x27	00000000 00000000	This readback displays the total number of half lines in Field 0. The Field 0 total height is a vertical synchronization measurement. This measurement is valid only when the vertical filter has locked. 00000000000000 - Total number of half lines in Field 0 (divide readback by 2 to get number of lines) xxxxxxxxxxxxxxx - Total number of half lines in Field 0 (divide readback by 2 to get number of lines)	
FIELD1_TOTAL_HEIGHT[13:0]			R
0x28 0x29	00000000 00000000	This readback displays the total number of half lines in Field 1. The Field 1 total height is a vertical synchronization measurement. This measurement is valid only when the vertical filter has locked. Field 1 measurements are valid when hdmi_interlaced is set to 1. Field 1 total height is a vertical synchronization measurement. 00000000000000 - Total number of half lines in Field 1 (divide readback by 2 to get number of lines) xxxxxxxxxxxxxxx - Total number of half lines in Field 1 (divide readback by 2 to get number of lines)	
FIELD0_VS_FRONT_PORCH[13:0]			R
0x2A 0x2B	00000000 00000000	This readback displays the total number of half lines in the VSync front porch of Field 0. The Field 0 VSync front porch width is a vertical synchronization measurement. The unit of this measurement is half lines. This measurement is valid only when the v 00000000000000 - Total number of half lines in VSync front porch of Field 0 (divide readback by 2 to get number of lines) xxxxxxxxxxxxxxx - Total number of half lines in the VSync front porch of Field 0 (divide readback by 2 to get number of lines)	
FIELD1_VS_FRONT_PORCH[13:0]			R
0x2C 0x2D	00000000 00000000	This readback displays the total number of half lines in the VSync front porch of Field 1. The Field 1 VSync front porch width is a vertical synchronization measurement. The unit of this measurement is half lines. This measurement is valid only when the vertical filter has locked. 00000000000000 - Total number of half lines in VSync front porch of Field 1 (divide readback by 2 to get number of lines) xxxxxxxxxxxxxxx - Total number of half lines in VSync front porch of Field 1 (divide readback by 2 to get number of lines)	
FIELD0_VS_PULSE_WIDTH[13:0]			R
0x2E 0x2F	00000000 00000000	This readback displays the total number of half lines in the VSync pulse of Field 0. The Field 0 VSync width is a vertical synchronization measurement. The unit for this measurement is half lines. This measurement is valid only when the vertical filter has locked. 00000000000000 - Total number of half lines in VSync pulse of Field 0 (divide readback by 2 to get number of lines) xxxxxxxxxxxxxxx - Total number of half lines in VSync pulse of Field 0 (divide readback by 2 to get number of lines)	
FIELD1_VS_PULSE_WIDTH[13:0]			R
0x30 0x31	00000000 00000000	This readback displays the total number of half lines in the VSync pulse of Field 1. The Field 1 VSync width is a vertical synchronization measurement. The unit for this measurement is half lines. This measurement is valid only when the vertical filter has locked. 00000000000000 - Total number of half lines in VSync pulse of Field 1 (divide readback by 2 to get number of lines) xxxxxxxxxxxxxxx - Total number of half lines in VSync pulse of Field 1 (divide readback by 2 to get number of lines)	

Reg	Bits	Description	
FIELD0_VS_BACK_PORCH[13:0]			R
0x32 0x33	00000000 00000000	This readback displays the total number of half lines in the VSync back porch of Field 0. The Field 0 VSync back porch width is a vertical synchronization measurement. The unit for this measurement is half lines. 00000000000000 - Total number of half lines in VSync back porch of Field 0 (divide readback by 2 to get number of lines) xxxxxxxxxxxxxx - Total number of half lines in VSync back porch of Field 0 (divide readback by 2 to get number of lines)	
FIELD1_VS_BACK_PORCH[13:0]			R
0x34 0x35	00000000 00000000	This readback displays the total number of half lines in the VSync back porch of Field 1. The Field 1 VSync back porch width is a vertical synchronization measurement. The unit for this measurement is half lines. This measurement is valid only when the vertical filter has locked. 00000000000000 - Number of half lines in VSync back porch of Field 1 (divide readback by 2 to get number of lines) xxxxxxxxxxxxxx - Number of half lines in VSync back porch of Field 1 (divide readback by 2 to get number of lines)	
CS_DATA[39:0]			R
0x36 0x37 0x38 0x39 0x3A	00000000 00000000 00000000 00000000 00000000	This readback displays the channel status data bits collected from audio channel 0.	
OVERRIDE_DEEP_COLOR_MODE			R/W
0x40	00000000	This control is used to override the deep color mode. 0 - HDMI section unpacks video data according to deep color information extracted from general control packets (normal operation). 1 - Override deep color mode extracted from the general control packet. HDMI section unpacks video data according to deep	
DEEP_COLOR_MODE_USER[1:0]			R/W
0x40	00000000	This control is used to manually set the deep color mode. The value set in this control is effective when override_deep_color_mode is set to 1. 00 - 8 bits per channel 01 - 10 bits per channel 10 - 12 bits per channel 11 - 16 bits per channel (not supported)	
DEREP_N_OVERRIDE			R/W
0x41	01000000	This control allows the user to override the pixel repetition factor. derep_n[3:0] is used instead of hdmi_pixel_repetition[3:0] to discard video pixel data from the incoming HDMI stream. 0 - Automatic detection and processing of pixel repeated modes using AVI InfoFrame information 1 - Enables manual setting of pixel repetition factor as per derep_n[3:0]	
DEREP_N[3:0]			R/W
0x41	01000000	This control is used to set the derepetition value if derepetition is overridden by setting derep_n_override. 0000 - derep_n+1 indicates pixel and clock discard factor xxxx - derep_n+1 indicates pixel and clock discard factor	
QZERO_ITC_DIS			R/W
0x47	00000000	This control is used to manually select the RGB colorimetry when the AVI InfoFrame field q[1:0]=00. It is to be used in conjunction with qzero_rgb_full. 0 - AVI InfoFrame ITC bit decides RGB-full or limited range in case q[1:0]=00 1 - Manual RGB range as per qzero_rgb_full.	
QZERO_RGB_FULL			R/W
0x47	00000000	This control is used to manually select the HDMI colorimetry when AVI InfoFrame field q[1:0]=00. It is valid only when qzero_itc_dis is set to 1. 0 - RGB-limited range when q[1:0]=00 1 - RGB-full when Q[1:0]=00	
ALWAYS_STORE_INF			R/W
0x47	00000000	This control is used to force InfoFrames with checksum errors to be stored. 0 - Store data from received InfoFrames only if their checksum correct 1 - Always store data from received InfoFrame regardless of their checksum	

Reg	Bits	Description	
DIS_PWRDNB			R/W
0x48	00000000	This control is used to disable the effect of the PWRDN1 pin. dis_pwr دنب should be set to 1 if the PWRDN1 pin is unused and unconnected. 0 - PWRDN1 pin used to set power mode of part (e.g. power down mode or normal mode). 1 - PWRDN1 pin has no effect	
DIS_CABLE_DET_RST			R/W
0x48	00000000	This control is used to disable the reset effects of cable detection. dis_cable_det_rst should be set to 1 if the +5 V pins are unused and left unconnected. 0 - Reset HDMI section if 5 V input pin corresponding to selected HDMI port (e.g. RXA_5V for port A) inactive 1 - Do not use 5 V input pins as reset signal for HDMI section	
GAMUT_IRQ_NEXT_FIELD			R/W
0x50	00000000	This control is used to set the new_gamut_mdata_raw interrupt to detect when the new contents are applicable to the next field or to indicate that the gamut packet is new. This is done using the header information of the gamut packet. 0 - Interrupt flag indicates that gamut packet is new 1 - Interrupt flag indicates that gamut packet is to be applied to next field	
CS_COPYRIGHT_MANUAL			R/W
0x50	00000000	This control is used to select an automatic or manual setting of the copyright value of the channel status bit that is passed to the SPDIF output. Manual control is set with the cs_copyright_value bit. 0 - Automatic CS copyright control 1 - Manual CS copyright control	
CS_COPYRIGHT_VALUE			R/W
0x50	00000000	This control is used to set the CS copyright value when in manual configuration of the CS copyright bit that is passed to the SPDIF output. 0 - Copyright value of channel status bit is 0. Valid only if cs_copyright_manual is set to 1. 1 - Copyright value of channel status bit is 1. Valid only if cs_copyright_manual is set to 1.	
TMDSFREQ[8:0]			R
0x51 0x52	00000000 00000000	This readback provides a full precision integer TMDS frequency measurement. 00000000 - Output 9-bit TMDS frequency measurement in MHz xxxxxxx - Output 9-bit TMDS frequency measurement in MHz	
TMDSFREQ_FRAC[6:0]			R
0x52	00000000	This readback indicates the fractional bits of the measured frequency of the PLL recovered TMDS clock. The unit is 1/128 MHz. 0000000 - Output 7-bit TMDS fractional frequency measurement in 1/128 MHz xxxxxxx - Output 7-bit TMDS fractional frequency measurement in 1/128 MHz	
HDMI_COLORSPACE[3:0]			R
0x53	00000000	This readback displays the HDMI input color space decoded from the AVI InfoFrame. 0000 - rgb_limited 0001 - rgb_full 0010 - yuv_601 0011 - yuv_709 0100 - xyvcc_601 0101 - xyvcc_709 0110 - yuv_601_FULL 0111 - yuv_709_FULL 1000 - sYCC 601 1001 - Adobe YCC 601 1010 - Adobe RGB	
FILT_5V_DET_DIS			R/W
0x56	01011000	This control is used to disable the digital glitch filter on the HDMI 5 V detect signals. The filtered signals are used as interrupt flags, and also used to reset the HDMI section. The filter works from an internal ring oscillator clock and is, therefore, 0 - Enable 1 - Disable	
FILT_5V_DET_TIMER[6:0]			R/W
0x56	01011000	This control is used to set the timer for the digital glitch filter on the HDMI +5 V detect inputs. The unit of this parameter is 2 clock cycles of the ring oscillator (~47 ns). The input must be constantly high for the duration of the timer, otherwise th 1011000 - Approximately 4.2 us. xxxxxxx - Time duration of +5 V deglitch filter. The unit of this parameter is 2 clock cycles of ring oscillator (~ 47 ns)	

Reg	Bits	Description	
LOAD_EQ_STAT			SC
0x5A	00000000	Load pulse to store static values from EQ_STAT_G/ZCTRL into the hidden registers corresponding to the port identified with EQ_STAT_ADDRESS	
HDCP_I2C_RESET_TX			SC
0x5A	00000000	This control is used to reset the HDCP engine of the HDMI transmitter so that it restarts the authentication. This is a self clearing bit. 1 - Reset HDCP engine	
BG_MEAS_REQ			SC
0x5A	00000000	This control is used in order to obtain the correct measurements of the selected background port. Setting this control sends a request to update the synchronization parameter measurements of the currently selected background port. The port on which the measurement will be made is selected by bg_meas_port_sel[1:0]. It is a self clearing control. 0 - No request to update selected background port synchronization parameter measurements 1 - Requests update of selected background port synchronization parameter measurements	
HDCP_REPT_EDID_RESET			SC
0x5A	00000000	This control is used to reset the E-EDID/repeater controller. When asserted, it resets the E-EDID/repeater controller. This is a self clearing bit. 0 - Normal operation 1 - Reset E-EDID/repeater controller	
DCFIFO_RECENTER			SC
0x5A	00000000	This control is used to recenter the video FIFO. This is a self clearing bit. 0 - Video FIFO normal operation 1 - Video FIFO to recenter	
FORCE_N_UPDATE			SC
0x5A	00000000	This control is used to force an N and CTS value update to the audio DPLL. The audio DPLL regenerates the audio clock. This is a self clearing bit. 0 - No effect 1 - Force update on N and CTS values for audio clock regeneration	
CTS[19:0]			R
0x5B 0x5C 0x5D	00000000 00000000 00000000	This readback indicates the CTS value received in the HDMI datastream. 00000000000000000000 - Default CTS value readback from HDMI stream xxxxxxxxxxxxxxxxxxxx - CTS value readback from HDMI stream	
N[19:0]			R
0x5D 0x5E 0x5F	00000000 00000000 00000000	This readback indicates the N value received in the HDMI datastream. 00000000000000000000 - Default N value readback from HDMI stream xxxxxxxxxxxxxxxxxxxx - N value readback from HDMI stream	
HPA_DELAY_SEL[3:0]			R/W
0x6C	10100011	This control is used to set a delay between +5 V detection and hot plug assertion on the HPA output pins, in increments of 100 ms per bit. 0000 - No delay 0001 - 100 ms delay 0010 - 200 ms delay 1010 - 1 s delay 1111 - 1.5 s delay	
HPA_OVR_TERM			R/W
0x6C	10100011	This control is used to set the termination control to be overridden by the HPA setting. When this bit is set, termination on a specific port is set according to the HPA status of that port. 0 - Automatic or manual I2C control of port termination 1 - Termination controls disabled and overridden by HPA controls	
HPA_MANUAL			R/W
0x6C	10100011	This control is used to manually enable the Hot Plug Assert output pins. By setting this bit, any automatic control of these pins is disabled. Manual control is determined by the hpa_man_value_x (where X = A, B, C or D) 0 - HPA takes its value based on hpa_auto_int_edid 1 - HPA takes its value from hpa_man_value_x	

Reg	Bits	Description	
I2S_SPDIF_MAP_INV			R/W
0x6D	00000000	This control is used to invert the arrangement of the I2S/SPDIF interface on the audio output port pins. Note the arrangement of the I2S/SPDIF interface on the audio output port pins is determined by i2s_spdif_map_rot. 0 - Do not invert arrangement of I2S/SPDIF channels in audio output port pins 1 - Invert arrangement of I2S/SPDIF channels in audio output port pins	
I2S_SPDIF_MAP_ROT[1:0]			R/W
0x6D	00000000	This control is used to select the arrangement of the I2S/SPDIF interface on the audio output port pins. 00 - [I2S0/SPDIF0 on AP1] [I2S1/SPDIF1 on AP2] [I2S2/SPDIF2 on AP3] [I2S3/SPDIF3 on AP4] 01 - [I2S3/SPDIF3 on AP1] [I2S0/SPDIF0 on AP2] [I2S1/SPDIF1 on AP3] [I2S2/SPDIF2 on AP4] 10 - [I2S2/SPDIF2 on AP1] [I2S3/SPDIF3 on AP2] [I2S0/SPDIF0 on AP3] [I2S1/SPDIF1 on AP4]	
DSD_MAP_INV			R/W
0x6D	00000000	This control is used to invert the arrangement of the DSD interface on the audio output port pins. Note the arrangement of the DSD interface on the audio output port pins is determined by dsd_map_rot. 0 - Do not invert arrangement of DSD channels on audio output port pins 1 - Invert arrangement of DSD channels on audio output port pins	
DSD_MAP_ROT[2:0]			R/W
0x6D	00000000	This control is used to select the arrangement of the DSD interface on the audio output port pins. 000 - [DSD0A on AP0] [DSD0B on AP1] [DSD1A on AP2] [DSD1B on AP3] [DSD2A on AP4] [DSD2B on AP5] 001 - [DSD2B on AP0] [DSD0A on AP1] [DSD0B on AP2] [DSD1A on AP3] [DSD1B on AP4] [DSD2A on AP5] 010 - [DSD2A on AP0] [DSD2B on AP1] [DSD0A on AP2] [DSD0B on AP3]	
DST_MAP_ROT[2:0]			R/W
0x6E	00000100	This control is used to select the arrangement of the DST interface on the audio output port pins. 000 - [DST_S on AP0] [DST_FF on AP5] 001 - [DST_S on AP1] [DST_FF on AP5] 010 - [DST_S on AP2] [DST_FF on AP5] 011 - [DST_S on AP3] [DST_FF on AP5] 100 - [DST_S on AP4] [DST_FF on AP5] 101 - Reserved 110 - Reserved 111 - Reserved	
EDID_PWRSW3P3[1:0]			R/W
0x71	00000000	Controls the switch related to EDID power domain taking the system or the cable supply. Dedicated control for the 3.3V domain 00 - Power switch always takes the cable supply 01 - Power switch takes the system supply, whenever it is available, otherwise the cable supply 10 - Power switch takes the cable supply whenever it is available, otherwise the system supply 11 - Power switc	
EDID_PWRSW1P8[1:0]			R/W
0x71	00000000	Controls the switch related to EDID power domain taking the system or the cable supply. Dedicated control for the 1.8V domain 00 - Power switch always takes the cable supply 01 - Power switch takes the system supply, whenever it is available, otherwise the cable supply 10 - Power switch takes the cable supply whenever it is available, otherwise the system supply 11 - Power switc	
VGA_PWRDN			R/W
0x72	00000100	This control is used to power down the VGA EDID pads. 0 - Power up VGA EDID pads 1 - Power down VGA EDID pads	
DDC_PWRDN[7:0]			R/W
0x73	00000000	This control is used to power down the DDC pads. 0 - Power up DDC pads 1 - Power down DDC pads	
CLOCK_TERM_DISABLE			R/W
0x83	11111111	This control is used to disable clock termination on Port D. It can be used when term_auto is set to 0. 0 - Enable termination Port D 1 - Disable termination Port D	

Reg	Bits	Description	
CLOCK_TERMC_DISABLE			R/W
0x83	11111111	This control is used to disable clock termination on Port C. It can be used when term_auto is set to 0. 0 - Enable termination Port C 1 - Disable termination Port C	
CLOCK_TERM_B_DISABLE			R/W
0x83	11111111	This control is used to disable clock termination on Port B. It can be used when term_auto is set to 0. 0 - Enable termination Port B 1 - Disable termination Port B	
CLOCK_TERM_A_DISABLE			R/W
0x83	11111111	This control is used to disable clock termination on Port A. It can be used when term_auto is set to 0. 0 - Enable termination Port A 1 - Disable termination Port A	
EQ_BYPASS_MODE			R/W
0x85	00010110	This control is used to bypass the equalizer 0 - Functional mode 1 - Equalizer bypass	
EQ_AGC_MODE[3:0]			R/W
0x85	00010110	AGC adaptation control mode 0000 - Automatic Gain 0001 - Automatic GCTRL, Manual ZCTRL 0010 - Manual GCTRL, Automatic ZCTRL 0011 - Manual GCTRL, Manual ZCTRL	
EQ_AGC_READBACK_SEL[1:0]			R/W
0x87	00000000	This control selects the readback value seen in EQ_AGC_READBACK register. 00 - GCTRL Value 01 - Reserved 10 - Reserved 11 - ZCTRL value	
EQ_AGC_READBACK[7:0]			R
0x88	00000000	See EQ_AGC_READBACK_SEL[1:0] for details. xxxxxxxx - Automatic Equaliser value based on EQ_AGC_READBACK_SEL[1:0]	
EQ_STAT_PORT_SEL[2:0]			R/W
0x91	00000000	Select the HDMI port for control via the rest of EQ_STAT values.	
EQ_STAT_GCTRL[4:0]			R/W
0x92	00001000	Manual value for GCTRL (low frequency equalizer adaptation) when automatic control is disabled.	
EQ_STAT_ZCTRL[7:0]			R/W
0x93	00000000	Manual value for ZCTRL (high frequency equalizer adaptation) when the automatic control is disabled.	
BG_TMDSFREQ[8:0]			R
0xE0 0xE1	00000000 00000000	This readback provides a precision integer TMDs frequency measurement on the background port selected by bg_meas_port_sel. The value provided is the result of a single measurement of the TMDs PLL frequency in MHz. The value provided is the result of a single measurement of the TMDs PLL frequency in MHz. This value is updated when an update request is made via bg_meas_req. This measurement is valid only when bg_param_lock is set to 1. 00000000 - Output 9-bit TMDs frequency measurement in MHz xxxxxxxx - Output 9-bit TMDs frequency measurement in MHz	
BG_TMDSFREQ_FRAC[6:0]			R
0xE1	00000000	This readback provides a precision fractional measurement of the TMDs frequency on the background port selected by bg_meas_port_sel. The unit is 1/128 MHz and the value is updated when an update request is made via bg_meas_req control. This measurement is valid only when bg_param_lock is set to 1. 00000000 - Output 7-bit TMDs fractional frequency measurement in 1/128MHz xxxxxxx - Output 7-bit TMDs fractional frequency measurement in 1/128MHz	

Reg	Bits	Description	
BG_LINE_WIDTH[12:0]			R
0xE2 0xE3	00000000 00000000	This readback displays a value representing the number of active pixels in a line and is updated when an update request is made via bg_meas_req. The background port line width is a horizontal synchronization measurement for the background HDMI port determined by bg_meas_port_sel[1:0]. The value represents the number of active pixels in a line and is updated when an update request is made via bg_meas_req control. 000000000000 - Number of active pixels per line on background measurement port xxxxxxxxxxxx - Number of active pixels per line on background measurement port	
BG_TOTAL_LINE_WIDTH[13:0]			R
0xE4 0xE5	00000000 00000000	This readback displays the total number of pixels per line on the background measurement port. The background port total line width is a horizontal synchronization measurement for the background HDMI port determined by bg_meas_port_sel[1:0]. The value represents the total number of pixels in a line and is updated when an update request is made via bg_meas_req control. This measurement is valid only when bg_param_lock is set to 1. xxxxxxxxxxxx - Total number of pixels per line on background measurement port	
BG_FIELD_HEIGHT[12:0]			R
0xE6 0xE7	00000000 00000000	This readback displays the number of active lines in a Field on the background measurement port. The background port field height is a vertical synchronization measurement for a background HDMI port determined by bg_meas_port_sel[1:0]. The value represents the number of active pixels in a line and is updated when an update request is made via bg_meas_req control. 000000000000 - Number of active lines in a Field on background measurement port xxxxxxxxxxxx - Number of active lines in a Field on background measurement port	
BG_TOTAL_FIELD_HEIGHT[12:0]			R
0xE8 0xE9	00000000 00000000	This readback displays the total number of lines in a Field on the background measurement port. The background port total field height is a vertical synchronization measurement for the background HDMI port determined by bg_meas_port_sel[1:0]. The value represents the total number of lines in a field and is updated when an update request is made via bg_meas_req control. 000000000000 - Total number of lines in Field on background measurement port xxxxxxxxxxxx - Total number of lines in Field on background measurement port	
BG_PIX_REP[3:0]			R
0xEA	00000000	This readback indicates the background port pixel repetition status for the background HDMI port determined by bg_meas_port_sel[1:0]. It provides the pixel repetition value in AVI InfoFrame and is updated when an update request is made via bg_meas_req. This measurement is valid only when bg_param_lock is set to 1. 0000 - 1x 0001 - 2x 0010 - 3x 0011 - 4x 0100 - 5x 0101 - 6x 0110 - 7x 0111 - 8x 1000 - 9x 1001 - 10x 1010 - 1111 - Reserved	
BG_DEEP_COLOR_MODE[1:0]			R
0xEA	00000000	This readback provides the deep color status for the background HDMI port determined by bg_meas_port_sel[1:0]. The readback provides the HDMI color depth and is updated when an update request is made via bg_meas_req. This measurement is valid only when bg_param_lock is set to 1. 00 - 8-bit color per channel 01 - 10-bit color per channel 10 - 12-bit color per channel 11 - 16-bit color per channel	
BG_PARAM_LOCK			R
0xEA	00000000	This readback indicates if vertical and horizontal parameters were locked during a background measurement. 0 - Horizontal and vertical not locked when measurement taken for select background HDMI port 1 - Horizontal and vertical locked when measurement taken for select background HDMI port	
BG_HDMI_INTERLACED			R
0xEA	00000000	This readback indicates the background port HDMI input interlace status. The background port HDMI input interlace status is a vertical filter measurement for a background HDMI port determined by bg_meas_port_sel[1:0]. The status readback is updated when an update request is made via bg_meas_req control. This measurement is valid only when bg_param_lock is set to 1. 0 - Progressive input 1 - Interlaced input	

Reg	Bits	Description	
BG_HDMI_MODE			R
0xEB	00000000	This readback provides the HDMI/DVI mode status of the background port determined by bg_meas_port_sel[1:0] and is updated continuously. 0 - DVI mode detected on selected BG port 1 - HDMI mode detected on selected BG port	
BG_DST_DOUBLE			R
0xEE	00000000	This readback indicates whether DST audio is sampled at a single or double transfer rate in the background port with bg_meas_port_sel. It is only valid when bg_audio_detected indicates DST packets were received. 0 - DST sample rate equals transfer rate 1 - DST sample rate doubles transfer rate	
BG_AUDIO_DETECTED[3:0]			R
0xEE	00000000	This readback indicates if audio samples were received on the background port and, if so, their type. 0000 - No audio samples detected 0001 - Audio sample detected 0010 - DSD audio detected 0100 - DST audio detected 1000 - HBR audio detected	
BG_HEADER_REQUESTED[7:0]			R/W
0xEF	10000010	This control is used to select the type of InfoFrame/packet to be provided for readback in the background port header and packet registers (0xF0 to 0xF5). The value set in this register is compared against the detected InfoFrame or packet header byte 0. If they match, header byte 1 and data bytes 1 to 5 are stored. The default value of 0x82 is the InfoFrame type of the AVI InfoFrame. xxxxxxx - Header value requested. This will be compared with detected packet headers. If a match is found, data is stored in registers 0xF0 to 0xF5.	
BG_HEADER_BYTE1[7:0]			R
0xF0	00000000	This readback displays byte 1 of the header for the InfoFrame/packet selected to be read in the background port. xxxxxxx - Header byte 1 data. Only valid if bg_valid_packet is high.	
BG_PACKET_BYTE1[7:0]			R
0xF1	00000000	This readback displays byte 1 of the packet for the InfoFrame/packet selected to be read in the background port. xxxxxxx - Packet byte 1 data. Only valid if bg_valid_packet is high.	
BG_PACKET_BYTE2[7:0]			R
0xF2	00000000	This readback displays byte 2 of the packet for the InfoFrame/packet selected to be read in the background port. xxxxxxx - Packet byte 2 data. Only valid if bg_valid_packet is high.	
BG_PACKET_BYTE3[7:0]			R
0xF3	00000000	This readback displays byte 3 of the packet for the InfoFrame/packet selected to be read in background port. xxxxxxx - Packet byte 3 data. Only valid if bg_valid_packet is high.	
BG_PACKET_BYTE4[7:0]			R
0xF4	00000000	This readback displays byte 4 of the packet for the InfoFrame/packet selected to be read in the background port. xxxxxxx - Packet byte 4 data. Only valid if bg_valid_packet is high.	
BG_PACKET_BYTES[7:0]			R
0xF5	00000000	This readback displays byte 5 of the packet for the InfoFrame/packet selected to be read in the background port. xxxxxxx - Packet byte 5 data. Only valid if bg_valid_packet is high.	
BG_VALID_PACKET			R
0xF6	00000000	This readback indicates if the background header and packet information is valid. 0 - Background header and packet readbacks not valid 1 - Background header and packet readbacks valid	

2.10 ADDR 64 (REPEATER)

Reg	Bits	Description	
BKSV[39:0]			R
0x00	00000000	The HDMI receiver Key Selection Vector (bksv) can be read back once the part has successfully accessed the HDCP ROM. The following registers contain the bksv read from the EEPROM: 0x00[7:0] = bksv[7:0], 0x01[7:0] = bksv[15:8], 0x02[7:0] = bksv[23:16], 0x03[7:0] = bksv[31:24] and 0x04[7:0] = bksv[39:32].	
0x01	00000000		
0x02	00000000		
0x03	00000000		
0x04	00000000		
RI[15:0]			R
0x08	00000000	This readback displays the Ri generated by the HDCP core.	
0x09	00000000		
PJ[7:0]			R
0x0A	00000000	This readback displays the Pj generated by the HDCP core.	
AKSV[39:0]			R/W
0x10	00000000	This readback indicates the aksv value. The aksv of the transmitter attached to the active HDMI port can be read back after an aksv update. The following registers contain the aksv written by the Tx. 0x10[7:0] = aksv[7:0], 0x11[7:0] = aksv[15:8], 0x12[7:0]	
0x11	00000000		
0x12	00000000		
0x13	00000000		
0x14	00000000		
AINFO[7:0]			R/W
0x15	00000000	This readback indicates the AINFO written by TX.	
AINFO_RB[7:0]			R
0x16	00000000	This readback indicates the effective Ainfo value; the value in the previous address is cleared after an aksv update.	
AN[63:0]			R/W
0x18	00000000	This readback indicates the AN written by TX.	
0x19	00000000		
0x1A	00000000		
0x1B	00000000		
0x1C	00000000		
0x1D	00000000		
0x1E	00000000		
0x1F	00000000		
SHA_A[31:0]			R/W
0x20	00000000	This readback indicates the SHA Hash Part A generated by on chip micro.	
0x21	00000000		
0x22	00000000		
0x23	00000000		
SHA_B[31:0]			R/W
0x24	00000000	This readback indicates the SHA Hash Part B generated by on chip micro	
0x25	00000000		
0x26	00000000		
0x27	00000000		
SHA_C[31:0]			R/W
0x28	00000000	This readback indicates the SHA Hash Part C generated by on chip micro	
0x29	00000000		
0x2A	00000000		
0x2B	00000000		
SHA_D[31:0]			R/W
0x2C	00000000	This readback indicates the SHA Hash Part D generated by on chip micro	
0x2D	00000000		
0x2E	00000000		
0x2F	00000000		

Reg	Bits	Description	
SHA_E[31:0]			R/W
0x30	00000000	This readback indicates the SHA Hash Part E generated by inchip micro	
0x31	00000000		
0x32	00000000		
0x33	00000000		
BCAPS[7:0]			R/W
0x40	10000011	This control is used to set the bcaps register which is presented to the TX attached to the active HDMI port. 10000011 - Default bcaps register value presented to the Tx xxxxxxx - bcaps register value presented to the Tx	
BSTATUS[15:0]			R/W
0x41	00000000	This control is used to set the bstatus information presented to the active HDMI port. Bits [11:0] must be set by the system software acting as a repeater. 0x41[7:0] = bstatus[7:0], 0x42[7:0] = bstatus[15:8]. xxxxxxxxxxxxxxxx - bstatus register presented to Tx 0000000000000000 - Reset value. bstatus register is reset only after power up.	
0x42	00000000		
SPA_PORT_B[15:0]			R/W
0x52	00000000	This control is used to define the source physical address for Port B. This is used for CEC and is located in the HDMI vendor specific data block in the E-EDID. 0000000000000000 - Default xxxxxxxxxxxxxxxx - Source physical address of Port B	
0x53	00000000		
SPA_PORT_C[15:0]			R/W
0x54	00000000	This control is used to define the source physical address for Port C. This is used for CEC and is located in the HDMI vendor specific data block in the E-EDID. 0000000000000000 - Default xxxxxxxxxxxxxxxx - Source physical address of Port C	
0x55	00000000		
SPA_PORT_D[15:0]			R/W
0x56	00000000	This control is used to define the source physical address for Port D. This is used for CEC and is located in the HDMI vendor specific data block in the E-EDID. 0000000000000000 - Default xxxxxxxxxxxxxxxx - Source physical address of Port D	
0x57	00000000		
PORT_B_CHECKSUM[7:0]			R/W
0x61	00000000	This control is used to set the checksum for the second half of the Port B EDID. This is calculated automatically. xxxxxxx - Checksum for E-EDID block containing SPA for Port B 00000000 - Default	
PORT_C_CHECKSUM[7:0]			R/W
0x62	00000000	This control is used to set the checksum for the second half of the Port C EDID. This is calculated automatically. 00000000 - Default xxxxxxx - Checksum for E-EDID block containing SPA for Port C	
PORT_D_CHECKSUM[7:0]			R/W
0x63	00000000	This control is used to set the checksum for the second half of the Port D EDID. This is calculated automatically. 00000000 - Default xxxxxxx - Checksum for E-EDID block containing SPA for Port D	
SPA_LOCATION[7:0]			R/W
0x70	11000000	This control is used to set the location in the E-EDID record where the SPA is located. 11000000 - Default xxxxxxx - Location of source physical address in internal E-EDID of Ports B, C and D	
KSV_LIST_READY			R/W
0x71	00000000	The system sets this bit in order to indicate that the KSV list has been read from the Tx IC(s) and written into the Repeater Map. The system must also set bits [11:0] of Bstatus before setting this bit. 0 - Not ready 1 - Ready	
SPA_LOCATION_MSB			R/W
0x71	00000000	This control is used to set the additional MSB bit of spa_location. For example, spa_location[8] is needed to point to SPAs stored in the second segment.	

Reg	Bits	Description	
EXT_EEPROM_TRI			R/W
0x72	00000000	This control is used to tristate the output pins to the external SPI EEPROM. 0 - Enable SPI interface outputs 1 - Tristate SPI interface outputs	
EXT_EEPROM_MAN_SELECT			R/W
0x72	00000000	This control is used to override the external EEPROM memory size. 0 - Detect automatically external EEPROM type (1024 or 512 bytes) 1 - Manually override type of external EEPROM (to be used with register ext_eeprom_man_value)	
EXT_EEPROM_MAN_VALUE			R/W
0x72	00000000	This control is used to override the external EEPROM memory size 0 - External EEPROM 1024 bytes 1 - External EEPROM 512 bytes	
VGA_EDID_ENABLED			R
0x73	00000000	This readback displays the I2C enable status for EDID access on the VGA port after a combination of manual and automatic functions. 0 - Disabled 1 - Enabled	
MAN_EDID_D_ENABLE			R/W
0x74	00000000	This control is used to manually enable I2C access to the internal EDID ram from DDC Port D, when the load_edid and cksum_calc operations are finished. 0 - Manual enable not active for E-EDID on Port D 1 - Manual enable active for E-EDID on Port D	
MAN_EDID_C_ENABLE			R/W
0x74	00000000	This control is used to manually enable I2C access to the internal EDID ram from DDC Port C, when the load_edid and cksum_calc operations are finished. 0 - Manual enable not active for E-EDID on Port C 1 - Manual enable active for E-EDID on Port C	
MAN_EDID_B_ENABLE			R/W
0x74	00000000	This control is used to manually enable I2C access to the internal EDID ram from DDC Port B, when the load_edid and cksum_calc operations are finished. 0 - Manual enable not active for E-EDID on Port B 1 - Manual enable active for E-EDID on Port B	
MAN_EDID_A_ENABLE			R/W
0x74	00000000	This control is used to manually enable I2C access to the internal EDID ram from DDC port A, when the load_edid and cksum_calc operations are finished. 0 - Manual enable not active for E-EDID on Port A 1 - Manual enable active for E-EDID on Port A	
EDID_D_ENABLED			R
0x76	00000000	This readback displays the resulting I2C enable readback for EDID access on port D, after a combination of manual and automatic functions. 0 - Disabled 1 - Enabled	
EDID_C_ENABLED			R
0x76	00000000	This readback displays the resulting I2C enable readback for EDID access on Port C, after a combination of manual and automatic functions. 0 - Disabled 1 - Enabled	
EDID_B_ENABLED			R
0x76	00000000	This readback displays the resulting I2C enable readback for EDID access on Port B, after a combination of manual and automatic functions. 0 - Disabled 1 - Enabled	
EDID_A_ENABLED			R
0x76	00000000	This readback displays the resulting I2C enable readback for EDID access on Port A, after a combination of manual and automatic functions. 0 - Disabled 1 - Enabled	

Reg	Bits	Description	
CLEAR_KSV_LIST			SC
0x77	00000 <u>0</u> 00	This control is used to clear the KSV list from memory. 0 - No effect 1 - Clear KSV list	
CKSUM_CALC			SC
0x77	00000 <u>0</u> 00	This control is used to force a full recalculation of all checksums for the internal E-EDID for all ports. 0 - No effect 1 - Calculate checksums of all internal EDID contents for all ports	
LOAD_EDID			SC
0x77	00000 <u>0</u> 00	This control is used to force the loading of internal E-EDID RAM with external SPI EEPROM contents. This automatically triggers a cksum_calc event. 0 - No effect 1 - Load internal E-EDID with SPI EEPROM contents	
STORE_EDID			SC
0x77	00000 <u>0</u> 00	This control is used to write the contents of the internal E-EDID RAM to the external SPI EEPROM. It is a self clearing control. 0 - No effect 1 - Write contents of internal E-EDID to SPI EEPROM	
KSV_LIST_READY_CLR_D			SC
0x78	00000 <u>0</u> 00	This control is used to clear the BCAPS KSV list ready bit in Port D. This is a self clearing bit. 0 - No effect 1 - Clears BCAPS KSV list ready bit	
KSV_LIST_READY_CLR_C			SC
0x78	00000 <u>0</u> 00	This control is used to clear the BCAPS KSV list ready bit in Port C. This is a self clearing bit. 0 - No effect 1 - Clears BCAPS KSV list ready bit	
KSV_LIST_READY_CLR_B			SC
0x78	00000 <u>0</u> 00	This control is used to clear the BCAPS KSV list ready bit in Port B. This is a self clearing bit. 0 - No effect 1 - Clears BCAPS KSV list ready bit	
KSV_LIST_READY_CLR_A			SC
0x78	00000 <u>0</u> 00	This control is used to clear the BCAPS KSV list ready bit in Port A. This is a self clearing bit. 0 - No effect 1 - Clears BCAPS KSV list ready bit	
MAN_VGA_EDID_ENABLE			R/W
0x79	<u>1</u> 0001000	This control is used to enable I2C access to the internal EDID RAM for the VGA port when the edid_load and cksum_calc operations are finished. 0 - Manual enable not active for E-EDID on VGA port 1 - Manual enable active for E-EDID on VGA port	
AUTO_HDCP_MAP_ENABLE			R/W
0x79	1000 <u>1</u> 000	This control is used to select the port to be accessed for HDCP addresses, i.e. the HDMI active port (selected by hdcp_port_select in the HDMI Map), or the port selected in hdcp_map_select. 0 - HDCP data read from port given by hdcp_map_select 1 - HDCP data read from the active HDMI port	
HDCP_MAP_SELECT[2:0]			R/W
0x79	1000 <u>1</u> 000	This control is used to select the port to be accessed for HDCP addresses (0x00 to 0x42 in the Repeater Map). This only takes effect when auto_hdcp_man_enable is set to 0. 000 - Select Port A 001 - Select Port B 010 - Select Port C 011 - Select Port D	
DISABLE_AUTO_EDID			R/W
0x7A	0000 <u>0</u> 100	This control is used to disable all automatic enables for the internal E-EDID. 0 - Automatic enable of internal E-EDID on HDMI ports when part comes out of power-down mode 1 - Disable automatic enable of internal E-EDID on HDMI ports when part comes out of power-down mode	

Reg	Bits	Description	
VGA_EDID_SPACE_SEL			R/W
0x7A	000001 <u>00</u>	This control is used to select the SRAM memory bank for VGA EDID to be accessed via main I2C. 0 - Main I2C EDID access for HDMI EDID segment space 1 - Main I2C EDID access for VGA EDID space	
HDMI_EDID_SEGMENT_SEL			R/W
0x7A	000001 <u>00</u>	This control is used to select one of the two SRAM memory banks for HDMI EDID segments to be accessed via main I2C. 0 - Main I2C EDID access for HDMI EDID segment 0 1 - Main I2C EDID access for HDMI EDID segment 1	
SPI_CFG[5:0]			R/W
0x7C	00 <u>000000</u>	This control is used to set the SPI configuration values from the SPI EEPROM byte 0 in an EDID_LOAD operation, or to be written to the same byte during an EDID_STORE operation. Bit5 - SPA_Double_Byte Bit4 - VGA_EDID_present Bit2 - Assert HPA in power off mode Bits[1:0] - Number of 256byte blocks present in EDID	
KSV_BYTE_0[7:0]			R/W
0x80	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_1[7:0]			R/W
0x81	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_2[7:0]			R/W
0x82	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_3[7:0]			R/W
0x83	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_4[7:0]			R/W
0x84	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_5[7:0]			R/W
0x85	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_6[7:0]			R/W
0x86	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_7[7:0]			R/W
0x87	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_8[7:0]			R/W
0x88	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_9[7:0]			R/W
0x89	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_10[7:0]			R/W
0x8A	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_11[7:0]			R/W
0x8B	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_12[7:0]			R/W
0x8C	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_13[7:0]			R/W
0x8D	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	

Reg	Bits	Description	
KSV_BYTE_14[7:0]			R/W
0x8E	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_15[7:0]			R/W
0x8F	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_16[7:0]			R/W
0x90	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_17[7:0]			R/W
0x91	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_18[7:0]			R/W
0x92	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_19[7:0]			R/W
0x93	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_20[7:0]			R/W
0x94	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_21[7:0]			R/W
0x95	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_22[7:0]			R/W
0x96	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_23[7:0]			R/W
0x97	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_24[7:0]			R/W
0x98	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_25[7:0]			R/W
0x99	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_26[7:0]			R/W
0x9A	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_27[7:0]			R/W
0x9B	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_28[7:0]			R/W
0x9C	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_29[7:0]			R/W
0x9D	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_30[7:0]			R/W
0x9E	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_31[7:0]			R/W
0x9F	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_32[7:0]			R/W
0xA0	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	

Reg	Bits	Description	
KSV_BYTE_33[7:0]			R/W
0xA1	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_34[7:0]			R/W
0xA2	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_35[7:0]			R/W
0xA3	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_36[7:0]			R/W
0xA4	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_37[7:0]			R/W
0xA5	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_38[7:0]			R/W
0xA6	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_39[7:0]			R/W
0xA7	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_40[7:0]			R/W
0xA8	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_41[7:0]			R/W
0xA9	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_42[7:0]			R/W
0xAA	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_43[7:0]			R/W
0xAB	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_44[7:0]			R/W
0xAC	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_45[7:0]			R/W
0xAD	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_46[7:0]			R/W
0xAE	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_47[7:0]			R/W
0xAF	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_48[7:0]			R/W
0xB0	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_49[7:0]			R/W
0xB1	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_50[7:0]			R/W
0xB2	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_51[7:0]			R/W
0xB3	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	

Reg	Bits	Description	
KSV_BYTE_52[7:0]			R/W
0xB4	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_53[7:0]			R/W
0xB5	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_54[7:0]			R/W
0xB6	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_55[7:0]			R/W
0xB7	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_56[7:0]			R/W
0xB8	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_57[7:0]			R/W
0xB9	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_58[7:0]			R/W
0xBA	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_59[7:0]			R/W
0xBB	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_60[7:0]			R/W
0xBC	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_61[7:0]			R/W
0xBD	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_62[7:0]			R/W
0xBE	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_63[7:0]			R/W
0xBF	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_64[7:0]			R/W
0xC0	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_65[7:0]			R/W
0xC1	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_66[7:0]			R/W
0xC2	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_67[7:0]			R/W
0xC3	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_68[7:0]			R/W
0xC4	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_69[7:0]			R/W
0xC5	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_70[7:0]			R/W
0xC6	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	

Reg	Bits	Description	
KSV_BYTE_71[7:0]			R/W
0xC7	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_72[7:0]			R/W
0xC8	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_73[7:0]			R/W
0xC9	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_74[7:0]			R/W
0xCA	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_75[7:0]			R/W
0xCB	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_76[7:0]			R/W
0xCC	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_77[7:0]			R/W
0xCD	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_78[7:0]			R/W
0xCE	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_79[7:0]			R/W
0xCF	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_80[7:0]			R/W
0xD0	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_81[7:0]			R/W
0xD1	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_82[7:0]			R/W
0xD2	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_83[7:0]			R/W
0xD3	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_84[7:0]			R/W
0xD4	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_85[7:0]			R/W
0xD5	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_86[7:0]			R/W
0xD6	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_87[7:0]			R/W
0xD7	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_88[7:0]			R/W
0xD8	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_89[7:0]			R/W
0xD9	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	

Reg	Bits	Description	
KSV_BYTE_90[7:0]			R/W
0xDA	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_91[7:0]			R/W
0xDB	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_92[7:0]			R/W
0xDC	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_93[7:0]			R/W
0xDD	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_94[7:0]			R/W
0xDE	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_95[7:0]			R/W
0xDF	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_96[7:0]			R/W
0xE0	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_97[7:0]			R/W
0xE1	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_98[7:0]			R/W
0xE2	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_99[7:0]			R/W
0xE3	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_100[7:0]			R/W
0xE4	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_101[7:0]			R/W
0xE5	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_102[7:0]			R/W
0xE6	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_103[7:0]			R/W
0xE7	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_104[7:0]			R/W
0xE8	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_105[7:0]			R/W
0xE9	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_106[7:0]			R/W
0xEA	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_107[7:0]			R/W
0xEB	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_108[7:0]			R/W
0xEC	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	

Reg	Bits	Description	
KSV_BYTE_109[7:0]			R/W
0xED	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_110[7:0]			R/W
0xEE	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_111[7:0]			R/W
0xEF	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_112[7:0]			R/W
0xF0	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_113[7:0]			R/W
0xF1	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_114[7:0]			R/W
0xF2	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_115[7:0]			R/W
0xF3	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_116[7:0]			R/W
0xF4	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_117[7:0]			R/W
0xF5	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_118[7:0]			R/W
0xF6	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_119[7:0]			R/W
0xF7	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_120[7:0]			R/W
0xF8	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_121[7:0]			R/W
0xF9	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_122[7:0]			R/W
0xFA	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_123[7:0]			R/W
0xFB	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_124[7:0]			R/W
0xFC	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_125[7:0]			R/W
0xFD	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_126[7:0]			R/W
0xFE	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	
KSV_BYTE_127[7:0]			R/W
0xFF	00000000	This readback displays a byte in the KSV list used for the HDCP repeater protocol.	

2.11 ADDR 7C (INFOFRAME)

Reg	Bits	Description	
AVI_INF_PB[223:0]			R
0x00	00000000	This readback displays AVI InfoFrame data.	
0x01	00000000		
0x02	00000000		
0x03	00000000		
0x04	00000000		
0x05	00000000		
0x06	00000000		
0x07	00000000		
0x08	00000000		
0x09	00000000		
0x0A	00000000		
0x0B	00000000		
0x0C	00000000		
0x0D	00000000		
0x0E	00000000		
0x0F	00000000		
0x10	00000000		
0x11	00000000		
0x12	00000000		
0x13	00000000		
0x14	00000000		
0x15	00000000		
0x16	00000000		
0x17	00000000		
0x18	00000000		
0x19	00000000		
0x1A	00000000		
0x1B	00000000		
AUD_INF_PB[111:0]			R
0x1C	00000000	This readback displays audio InfoFrame data.	
0x1D	00000000		
0x1E	00000000		
0x1F	00000000		
0x20	00000000		
0x21	00000000		
0x22	00000000		
0x23	00000000		
0x24	00000000		
0x25	00000000		
0x26	00000000		
0x27	00000000		
0x28	00000000		
0x29	00000000		

Reg	Bits	Description	
SPD_INF_PB[223:0]			R
0x2A	00000000	This readback displays Source Product Descriptor (SPD) InfoFrame data.	
0x2B	00000000		
0x2C	00000000		
0x2D	00000000		
0x2E	00000000		
0x2F	00000000		
0x30	00000000		
0x31	00000000		
0x32	00000000		
0x33	00000000		
0x34	00000000		
0x35	00000000		
0x36	00000000		
0x37	00000000		
0x38	00000000		
0x39	00000000		
0x3A	00000000		
0x3B	00000000		
0x3C	00000000		
0x3D	00000000		
0x3E	00000000		
0x3F	00000000		
0x40	00000000		
0x41	00000000		
0x42	00000000		
0x43	00000000		
0x44	00000000		
0x45	00000000		
MS_INF_PB[111:0]			R
0x46	00000000	This readback displays the Moving Picture Expert Group (MPEG) source InfoFrame data.	
0x47	00000000		
0x48	00000000		
0x49	00000000		
0x4A	00000000		
0x4B	00000000		
0x4C	00000000		
0x4D	00000000		
0x4E	00000000		
0x4F	00000000		
0x50	00000000		
0x51	00000000		
0x52	00000000		
0x53	00000000		

Reg	Bits	Description	
VS_INF_PB[223:0]			R
0x54	00000000	This readback displays vendor specific InfoFrame data.	
0x55	00000000		
0x56	00000000		
0x57	00000000		
0x58	00000000		
0x59	00000000		
0x5A	00000000		
0x5B	00000000		
0x5C	00000000		
0x5D	00000000		
0x5E	00000000		
0x5F	00000000		
0x60	00000000		
0x61	00000000		
0x62	00000000		
0x63	00000000		
0x64	00000000		
0x65	00000000		
0x66	00000000		
0x67	00000000		
0x68	00000000		
0x69	00000000		
0x6A	00000000		
0x6B	00000000		
0x6C	00000000		
0x6D	00000000		
0x6E	00000000		
0x6F	00000000		
ACP_PB[223:0]			R
0x70	00000000	This readback displays ACP InfoFrame data.	
0x71	00000000		
0x72	00000000		
0x73	00000000		
0x74	00000000		
0x75	00000000		
0x76	00000000		
0x77	00000000		
0x78	00000000		
0x79	00000000		
0x7A	00000000		
0x7B	00000000		
0x7C	00000000		
0x7D	00000000		
0x7E	00000000		
0x7F	00000000		
0x80	00000000		
0x81	00000000		
0x82	00000000		
0x83	00000000		
0x84	00000000		
0x85	00000000		
0x86	00000000		
0x87	00000000		
0x88	00000000		
0x89	00000000		
0x8A	00000000		
0x8B	00000000		

Reg	Bits	Description	
ISRC1_PB[223:0]			R
0x8C	00000000	This readback displays ISRC 1 InfoFrame data.	
0x8D	00000000		
0x8E	00000000		
0x8F	00000000		
0x90	00000000		
0x91	00000000		
0x92	00000000		
0x93	00000000		
0x94	00000000		
0x95	00000000		
0x96	00000000		
0x97	00000000		
0x98	00000000		
0x99	00000000		
0x9A	00000000		
0x9B	00000000		
0x9C	00000000		
0x9D	00000000		
0x9E	00000000		
0x9F	00000000		
0xA0	00000000		
0xA1	00000000		
0xA2	00000000		
0xA3	00000000		
0xA4	00000000		
0xA5	00000000		
0xA6	00000000		
0xA7	00000000		
ISRC2_PB[223:0]			R
0xA8	00000000	This readback displays ISRC 2 InfoFrame data.	
0xA9	00000000		
0xAA	00000000		
0xAB	00000000		
0xAC	00000000		
0xAD	00000000		
0xAE	00000000		
0xAF	00000000		
0xB0	00000000		
0xB1	00000000		
0xB2	00000000		
0xB3	00000000		
0xB4	00000000		
0xB5	00000000		
0xB6	00000000		
0xB7	00000000		
0xB8	00000000		
0xB9	00000000		
0xBA	00000000		
0xBB	00000000		
0xBC	00000000		
0xBD	00000000		
0xBE	00000000		
0xBF	00000000		
0xC0	00000000		
0xC1	00000000		
0xC2	00000000		
0xC3	00000000		

Reg	Bits	Description	
GBD[223:0]			R
0xC4	00000000	This readback displays gamut InfoFrame data.	
0xC5	00000000		
0xC6	00000000		
0xC7	00000000		
0xC8	00000000		
0xC9	00000000		
0xCA	00000000		
0xCB	00000000		
0xCC	00000000		
0xCD	00000000		
0xCE	00000000		
0xCF	00000000		
0xD0	00000000		
0xD1	00000000		
0xD2	00000000		
0xD3	00000000		
0xD4	00000000		
0xD5	00000000		
0xD6	00000000		
0xD7	00000000		
0xD8	00000000		
0xD9	00000000		
0xDA	00000000		
0xDB	00000000		
0xDC	00000000		
0xDD	00000000		
0xDE	00000000		
0xDF	00000000		
AVI_PACKET_ID[7:0]			R/W
0xE0	1000010	This control is used to set the AVI InfoFrame ID. 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x00 to 0x1B 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x00 to 0x1B	
AVI_INF_VERS[7:0]			R
0xE1	00000000	This readback displays the AVI InfoFrame version.	
AVI_INF_LEN[7:0]			R
0xE2	00000000	This readback displays the AVI InfoFrame length.	
AUD_PACKET_ID[7:0]			R/W
0xE3	10000100	This control is used to set the audio InfoFrame ID. 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x1C to 0x29 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x1C to 0x29	
AUD_INF_VERS[7:0]			R
0xE4	00000000	This readback displays the audio InfoFrame version.	
AUD_INF_LEN[7:0]			R
0xE5	00000000	This readback displays the audio InfoFrame length.	
SPD_PACKET_ID[7:0]			R/W
0xE6	10000011	This control is used to set the Source Product Descriptor InfoFrame ID. 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x2A to 0x45 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x2A to 0x45	
SPD_INF_VERS[7:0]			R
0xE7	00000000	This readback displays the Source Product Descriptor InfoFrame version.	
SPD_INF_LEN[7:0]			R
0xE8	00000000	This readback displays the Source Product Descriptor InfoFrame length.	

Reg	Bits	Description	
MS_PACKET_ID[7:0]			R/W
0xE9	10000101	This control is used to set the MPEG source InfoFrame ID. 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x46 to 0x53 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x46 to 0x53	
MS_INF_VERS[7:0]			R
0xEA	00000000	This readback displays the MPEG source InfoFrame version.	
MS_INF_LEN[7:0]			R
0xEB	00000000	This readback displays the MPEG source InfoFrame length.	
VS_PACKET_ID[7:0]			R/W
0xEC	10000001	This control is used to set the Vendor Specific InfoFrame ID. 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x54 to 0x6F 1xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x54 to 0x6F	
VS_INF_VERS[7:0]			R
0xED	00000000	This readback displays the Vendor Specific InfoFrame version.	
VS_INF_LEN[7:0]			R
0xEE	00000000	This readback displays the Vendor Specific InfoFrame length.	
ACP_PACKET_ID[7:0]			R/W
0xEF	00000100	This control is used to set the ACP packet ID. 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x70 to 0x8B 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x70 to 0x8B	
ACP_TYPE[7:0]			R
0xF0	00000000	This readback displays the ACP type.	
ACP_HEADER2[7:0]			R
0xF1	00000000	This readback displays the ACP header 2.	
ISRC1_PACKET_ID[7:0]			R/W
0xF2	00000101	This control is used to set the ISRC1 packet ID. 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x8C to 0xA7 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x8C to 0xA7	
ISRC1_HEADER1[7:0]			R
0xF3	00000000	This readback displays the ISRC1 header 1.	
ISRC1_HEADER2[7:0]			R
0xF4	00000000	This readback displays the ISRC1 header 2.	
ISRC2_PACKET_ID[7:0]			R/W
0xF5	00000110	This control is used to set the ISRC2 packet ID. 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0xA8 to 0xC3 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0xA8 to 0xC3	
ISRC2_HEADER1[7:0]			R
0xF6	00000000	This readback displays the ISRC2 header 1.	
ISRC2_HEADER2[7:0]			R
0xF7	00000000	This readback displays the ISRC2 header 2.	
GAMUT_PACKET_ID[7:0]			R/W
0xF8	00001010	This control is used to set the gamut metadata packet ID. 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0xC4 to 0xDF 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0xC4 to 0xDF	
GAMUT_HEADER1[7:0]			R
0xF9	00000000	This readback displays the gamut metadata header 1.	

Reg	Bits	Description	
GAMUT_HEADER2[7:0]			R
0xFA	00000000	This readback displays the gamut metadata header 2.	
PKT_CNT_ID[7:0]			R/W
0xFD	10000001	This control is used to select which type of packet is going to be counted during each frame. Any packet header ID is supported to detect the count, but only collectable packets can be stored. The default is 0x81 for vendor specific InfoFrame. 10000001 - default	
EN_PKT_CNT_SEL			R/W
0xFE	00000000	This control enables the feature where the user can choose which of the multiple received packets per frame of type PKT_CNT_ID is to be collected. This feature is only relevant for packet types that can be stored in the InfoFrame Map. 0 - Disabled, collect every packet as it is received 1 - Enable selectively collecting one of multiple packets per frame of the same type	
PKT_CNT_SEL[3:0]			R/W
0xFE	00000000	This control selects which one of the multiple received packets per frame of type pkt_cnt_id is to be collected. It must be enabled with en_pkt_cnt_sel. It should be manually changed after receiving the corresponding new packet detect flag. 0000 - Select 1st packet after VSync rising edge xxxx - 1110 - Select 15th packet after VSync rising edge 1111 - Undefined	
RB_PKT_CNT[3:0]			R
0xFF	00000000	This readback displays the count of number of packets of type pkt_cnt_id per frame, as detected between VSync rising edges. The count readback is supported for any pkt_cnt_id, even those packets that cannot be stored in the InfoFrame Map, e.g. general control packets	

2.12 ADDR 4C (DPLL)

Reg	Bits	Description	
MCLK_FS_N[2:0]			R/W
0xB5	00000001	This control is used to select the multiple of 128 fs to be used for MCLK out. 000 - 128 fs 001 - 256 fs 010 - 384 fs 011 - 512 fs 100 - 640 fs 101 - 768 fs 110 - Not valid 111 - Not valid	
DLL_PHASE[5:0]			R/W
0xC8	00000000	This control is used to adjust the phase of the ADC clocks in CP modes. 000000 - Default xxxxxx - Adjust phase of clock in CP modes	
FB_PHASE_ADJUST[3:0]			R/W
0xC9	00000000	This control is used to adjust the phase of the fast blank signals in order to correct the delay the signal endures. 0000 - Default	

2.13 ADDR 5C (AUDIO_CODEC)

Reg	Bits	Description	
PLL_REF_FREQ[1:0]			R/W
0x00	00 <u>000001</u>	This control is used to select the PLL reference input frequency. 00 - 512*Fs (24.576 MHz) 01 - 256*Fs (12.288 MHz) 10 - 128*Fs (6.144 MHz) 11 - 64*Fs (3.072 MHz)	
ADC_INPUT_MUX[2:0]			R/W
0x00	0000 <u>0001</u>	This control is used to set the ADC input mux options. 000 - No source 001 - AUXIN1 010 - AUXIN2 011 - AUXIN3 100 - AUXIN4 101 - AUXIN5 Others - Reserved	
ENG_DIG_PU			R/W
0x01	0000 <u>0001</u>	This control is used to power up the digital engine. 0 - Power down digital engine 1 - Power up digital engine	
PLL_PU			R/W
0x01	0000 <u>001</u>	This control is used to power up PLL. 0 - Power down PLL 1 - Power up PLL	
REF_BUF_PU			R/W
0x01	0000 <u>001</u>	This control is used to power up the reference buffer. 0 - Power down reference buffer 1 - Power up reference buffer	
DAC_ANA_STDBY_DIS			R/W
0x01	0000 <u>001</u>	This control is used to disable DAC analog standby. 0 - DACs in standby mode 1 - DACs in normal mode	
RIGHT_DAC_1_PU			R/W
0x02	0000 <u>000</u>	This control is used to power up the DAC right channel. 0 - Power down DAC right channel 1 - Power up DAC right channel	
LEFT_DAC_1_PU			R/W
0x02	0000 <u>000</u>	This control is used to power up the DAC left channel. 0 - Power down DAC left channel 1 - Power up DAC left channel	
RIGHT_ADC_1_PU			R/W
0x03	0000 <u>000</u>	This control is used to power up the ADC right channel. 0 - Power down ADC right channel 1 - Power up ADC right channel	
LEFT_ADC_1_PU			R/W
0x03	0000 <u>000</u>	This control is used to power up the ADC left channel. 0 - Power down ADC left channel 1 - Power up ADC left channel	
HP_RIGHT_AMP_PU			R/W
0x05	00 <u>000000</u>	This control is used to power up the headphone right amplifier. 0 - Power down headphone right amplifier 1 - Power up headphone right amplifier	
HP_LEFT_AMP_PU			R/W
0x05	00 <u>00000</u>	This control is used to power up the headphone left amplifier. 0 - Power down headphone left amplifier 1 - Power up headphone left amplifier	

Reg	Bits	Description	
HP_SCP			R/W
0x05	0000 <u>0</u> 000	This control is used to enable short circuit protection. 0 - Enable short circuit protection 1 - Disable short circuit protection	
HP_MUTE			R/W
0x05	0000 <u>0</u> 00	This control is used to mute the headphone amplifier. 0 - Mute headphone amplifier 1 - Unmute headphone amplifier	
HP_LEFT_RIGHT_TRI_ENB			R/W
0x05	0000 <u>0</u> 00	This control is used to tristate the headphone left amplifier. 0 - Tristate headphone left amplifier 1 - Do not tristate headphone left amplifier	
HP_RIGHT_RIGHT_TRI_ENB			R/W
0x05	0000 <u>0</u> 00	This control is used to tristate the headphone right amplifier. 0 - Tristate headphone right amplifier 1 - Do not tristate headphone right amplifier	
HP1_ATTEN[4:0]			R/W
0x06	00 <u>0</u> 00000	This control is used to set headphone amplifier attenuation (0 dB to -46.5 dB in -1.5 dB steps). 00000 - 0dB ...	
PU_DAC_CUR_GEN			R/W
0x07	0 <u>1</u> 000100	This control is used to power up the DAC current generator. 0 - Power down DAC current generator 1 - Power up DAC current generator	
DAC_CLAMP_OP			R/W
0x07	0 <u>1</u> 000100	This control is used to clamp DAC output to AGND. 0 - Disable clamp 1 - Clamp DAC output to AGND	
IDAC_BUF_PU			R/W
0x07	0 <u>1</u> 000100	This control is used to power down the iDAC buffer. 0 - Power up iDAC buffer 1 - Power down iDAC buffer	
IDAC_EN			R/W
0x07	0 <u>1</u> 000100	This control is used to enable iDAC. 0 - Disable iDAC 1 - Enable iDAC	
PU_DAC_IBIAS_DIST			R/W
0x07	0 <u>1</u> 000100	This control is used to power up DAC ibias distribution. 0 - Power down DAC ibias distribution 1 - Power up DAC ibias distribution	
HP_CLAMP_OP			R/W
0x07	0 <u>1</u> 000100	This control is used to unclamp headphone outputs from AGND. 0 - Clamp output 1 - Disable clamp	
PU_PDN_DWHMPR_I			R/W
0x08	0000 <u>0</u> 000	This control is used to power down the reference in an S-ramp shape. 0 - Disable S-ramp 1 - Enable S-ramp on power down	
PU_PUP_DWHMPR_I			R/W
0x08	0000 <u>0</u> 000	This control is used to power up the reference in an S-ramp shape. 0 - Disable S-ramp 1 - Enable S-ramp on power up	
VREF_ENB			R/W
0x08	00000 <u>0</u> 00	This control is used to disable the voltage reference. 0 - Enable voltage reference 1 - Disable voltage reference	

Reg	Bits	Description	
RIGHT_DAC_1_ANA_STDBY			R/W
0x09	000000 <u>00</u>	This control is used to set the DAC right channel into standby mode. 0 - Full power 1 - Set DAC right channel into standby mode	
LEFT_DAC_1_ANA_STDBY			R/W
0x09	000000 <u>00</u>	This control is used to set the DAC left channel into standby mode. 0 - Full power 1 - Set DAC left channel into standby mode	
RIGHT_DAC_VOL_RAMP_PD_PU			R/W
0x0A	000000 <u>00</u>	This control is used to set DAC powerup conditions. If it is set to 0 on startup and the DAC channel performs a hard powerup, setting it to 1 ramps the volume to zero and powers down the DAC channel. Setting this bit back to 0, powers up the DAC channel again and ramps the volume back up. 0 - If set to 0 on startup, DAC channel performs a hard power up	
LEFT_DAC_VOL_RAMP_PD_PU			R/W
0x0A	000000 <u>00</u>	This control is used to set DAC powerup conditions. If it is set to 0 on startup and the DAC channel performs a hard powerup, setting it to 1 ramps the volume to zero and powers down the DAC channel. Setting this bit back to 0, powers up the DAC channel again and ramps the volume back up. 0 - If set to 0 on startup, DAC channel performs a hard powerup	
RIGHT_ADC_VOL_RAMP_PD_PU			R/W
0x0B	000000 <u>00</u>	This control is used to set ADC powerup conditions. If it is set to 0 on startup and the ADC channel performs a hard powerup, setting it to 1 ramps the volume to zero and powers down the ADC channel. Setting it back to 0, powers the ADC channel up again and ramps the volume back up. 0 - If set to 0 on startup, ADC channel performs a hard powerup. Setting to 0 after setting to 1 powers up ADC channel and ramps volume up. 1 - Ramps volume down and powers down ADC channel.	
LEFT_ADC_VOL_RAMP_PD_PU			R/W
0x0B	000000 <u>00</u>	This control is used to set ADC powerup conditions. If it is set to 0 on startup and the ADC channel performs a hard powerup, setting it to 1 ramps the volume to zero and powers down the ADC channel. Setting it back to 0, powers the ADC channel up again and ramps the volume back up. 0 - If set to 0 on startup, ADC channel performs a hard powerup. Setting to 0 after setting to 1 powers up ADC channel and ramps volume up. 1 - Ramps volume down and powers down ADC channel.	
DAC_SLAVE_SERIAL_PORT			R/W
0x0C	000000 <u>10</u>	This control is used to select master or slave mode in the DAC serial port. 0 - Select master mode 1 - Select slave mode	
ADC_SLAVE_SERIAL_PORT			R/W
0x0C	000000 <u>10</u>	This control is used to select master or slave mode in the ADC serial port. 0 - Select master mode 1 - Select slave mode	
AUDIO_PLL_LOCKED			R
0x0D	000000 <u>00</u>	This readback indicates the audio PLL locking status. 0 - Unlocked 1 - Locked	
MUX_OUT_L_SEL[3:0]			R/W
0x0E	<u>0100</u> 0011	This control is used to select the analog input to mux to the analog output right channel. 0000 - No source 0001 - AUXIN1_R 0010 - AUXIN1_L 0011 - AUXIN2_R 0100 - AUXIN2_L 0101 - AUXIN3_R 0110 - AUXIN3_L 0111 - AUXIN4_R 1000 - AUXIN4_L 1001 - AUXIN5_R 1010 - AUXIN5_L Others - Reserved	

Reg	Bits	Description	
MUX_OUT_R_SEL[3:0]			R/W
0x0E	01000011	This control is used to select the analog input to mux to the analog output left channel. 0000 - No source 0001 - AUXIN1_R 0010 - AUXIN1_L 0011 - AUXIN2_R 0100 - AUXIN2_L 0101 - AUXIN3_R 0110 - AUXIN3_L 0111 - AUXIN4_R 1000 - AUXIN4_L 1001 - AUXIN5_R 1010 - AUXIN5_L Others - Reserved	
VOL_DAC_LEFT[7:0]			R/W
0x10	00000000	This control is used to set the volume control. Volume in dB = value * -0.375 dB	
VOL_DAC_RIGHT[7:0]			R/W
0x11	00000000	This control is used to set the volume control. Volume in dB = value * -0.375 dB	
VOL_ADC_LEFT[7:0]			R/W
0x18	00000000	This control is used to set the volume control. Volume in dB = value * -0.375 dB	
VOL_ADC_RIGHT[7:0]			R/W
0x19	00000000	This control is used to set the volume control. Volume in dB = value * -0.375 dB	
MUXOUT_PDB			R/W
0x2C	00000001	This control is used to power down the amplifier. 0 - Power down amplifier 1 - Power up amplifier	
REF_CORE_PD			R/W
0x33	00000000	This control is used to power down the reference core. 0 - Power down reference core 1 - Power up reference core	
DAC_ANA_STNDBY_ADJ[1:0]			R/W
0x38	00000000	This control is used to adjust the DAC standby current. 00 - 2 uA 01 - 4 uA 10 - 6 uA 11 - 12 uA	

2.14 ADDR B8 (TX MAIN)

Reg	Bits	Description	
N_HIGH_BYTE[3:0]			R/W
0x01	00000000	This control is used to set the value of N. ($128 * F_s = \text{ftrnds_clock} * N / \text{CTS}$) 0000 - Default	
N_MID_BYTE[7:0]			R/W
0x02	00000000	This control is used to set the middle byte of N. 00000000 - Default	
N_LOW_BYTE[7:0]			R/W
0x03	00000000	This control is used to set the lower byte of N. 00000000 - Default	
SPDIF_SF[3:0]			R
0x04	00000000	This readback displays the SPDIF audio sampling frequency decoded by the hardware. 0000 - 44.1 kHz 0001 - NA 0010 - 48 kHz 0011 - 32 kHz 0100 - NA 0101 - NA 0110 - NA 0111 - NA 1000 - 88.2 kHz 1001 - NA 1010 - 96 kHz 1011 - NA 1100 - 176.4 kHz 1101 - NA 1110 - 192 kHz 1111 - NA	
INT_CTS_HIGH_BYTE[3:0]			R
0x04	00000000	This readback displays the top four bits of the measured CTS. It indicates the value of the calculated CTS.	
INT_CTS_MID_BYTE[7:0]			R
0x05	00000000	This readback displays the middle byte of the measured CTS.	
INT_CTS_LOW_BYTE[7:0]			R
0x06	00000000	This readback displays the low byte of the measured CTS.	
EXTERNAL_CTS_HIGH_BYTE[3:0]			R/W
0x07	00000000	This control is used to set the value of the top four bits of the external CTS. 0000 - Default	
EXTERNAL_CTS_MID_BYTE[7:0]			R/W
0x08	00000000	This control is used to set the middle byte of the external CTS. 00000000 - Default	
EXTERNAL_CTS_LOW_BYTE[7:0]			R/W
0x09	00000000	This control is used to set the low byte of external CTS 00000000 - Default	
CTS_SEL			R/W
0x0A	00000001	This control is used to select the CTS option; either internally generated CTS values or external user-defined CTS. 0 - Internally generated 1 - Set by user	
AUDIO_SEL[2:0]			R/W
0x0A	00000001	This control is used to select the audio input format. 000 - I2S 001 - SPDIF 010 - One bit audio (DSD) 011 - High bit rate (HBR) audio 100 - DST	

Reg	Bits	Description	
AUDIO_MODE[1:0]			R/W
0x0A	0000 <u>00</u> 1	This control is used to set the audio mode selection This is used in conjunction with audio_sel and i2sformat. 00 - DSD raw mode (DSD case), four streams with BPM encoding (HBR case) 01 - DSD raw mode (DSD case), four streams, no BPM encoding (HBR case) 10 - SPDIF mode (DSD case), one stream with BPM encoding (HBR case) 11 - SPDIF mode (DSD,case) one stream, no BPM encoding (HBR case)	
MCLK_RATIO[1:0]			R/W
0x0A	00000 <u>0</u> 1	This control is used to select the MCLK speed ratio. It is only used with external MCLK. 00 - 128 fs 01 - 256 fs 10 - 384 fs 11 - 512 fs	
SPDIF_EN			R/W
0x0B	<u>0</u> 0001110	This control is used to enable the SPDIF receiver. It is only required with an internal MCLK. 0 - Disable SPDIF receiver 1 - Enable SPDIF receiver	
MCLK_POL			R/W
0x0B	<u>0</u> 0 <u>0</u> 01110	This control is used to set the MCLK polarity. 0 - Rising edge 1 - Falling edge	
MCLK_EN			R/W
0x0B	0 <u>0</u> <u>0</u> 01110	This control is used to select the MCLK source. 0 - MCLK internally generated 1 - MCLK available	
EXT_AUDIOSF_SEL			R/W
0x0C	<u>1</u> 0111100	This control is used to select the sampling frequency for the SPDIF output. 0 - Use sampling frequency from I2S stream, for SPDIF stream 1 - Use sampling frequency from I2C registers	
CS_BIT_OVERRIDE			R/W
0x0C	<u>1</u> 0 <u>1</u> 11100	This control is used to select the source of the channel status bits when using I2S mode. 0 - Use channel status bits from I2S stream 1 - Use channel status bits from I2C registers	
I2SENABLE[3:0]			R/W
0x0C	<u>1</u> 0 <u>111</u> 100	This control is used to enable the I2S pins. 0000 - Disable all channels 1111 - Enable all channels	
I2SFORMAT[1:0]			R/W
0x0C	<u>1</u> 0111 <u>1</u> <u>00</u>	This control is used to select the I2S output format. 00 - I2S 01 - Right justified 10 - Left justified 11 - AES3 direct mode	
I2S_BIT_WIDTH[4:0]			R/W
0x0D	000 <u>1</u> 1000	This control is used to select the I2S bit width. It is for right justified audio only. 11000 - Default	
SUBPKT0_L_SRC[2:0]			R/W
0x0E	0 <u>0</u> <u>000</u> 001	This control is used to specify the source of the sub packet 0, left channel. 000 - Default	
SUBPKT0_R_SRC[2:0]			R/W
0x0E	0000 <u>0</u> 001	This control is used to specify the source of the sub packet 0, right channel. 001 - Default	
SUBPKT1_L_SRC[2:0]			R/W
0x0F	0 <u>0</u> <u>010</u> 011	This control is used to specify the source of the sub packet 1, left channel. 010 - Default	

Reg	Bits	Description	
SUBPKT1_R_SRC[2:0]			R/W
0x0F	00010011	This control is used to specify the source of the sub packet 1, right channel. 011 - Default	
SUBPKT2_L_SRC[2:0]			R/W
0x10	00100101	This control is used to specify the source of the sub packet 2, left channel. 100 - Default	
SUBPKT2_R_SRC[2:0]			R/W
0x10	00100101	This control is used to specify the source of the sub packet 2, right channel. 101 - Default	
SUBPKT3_L_SRC[2:0]			R/W
0x11	00110111	This control is used to specify the source of the sub packet 3, left channel. 110 - Default	
SUBPKT3_R_SRC[2:0]			R/W
0x11	00110111	This control is used to specify the source of the sub packet 3, right channel. 111 - Default	
CS_BIT_1_0[1:0]			R/W
0x12	00000000	This control is used to set the channel status bits[0] and [1]. Bit 0 = 0 indicates consumer use. Bit 1 = 0 indicates LPCM audio. 00 - Default	
CR_BIT			R/W
0x12	00000000	This control is used to set the copyright protection. 0 - Copyright 1 - Not copyright protected	
A_INFO[2:0]			R/W
0x12	00000000	This control is used to select the pre-emphasis on the audio output channels. Refer to IEC 60958 for more details. 000 - Two audio channels without pre-emphasis 001 - Two audio channels with 50/15 uS pre-emphasis 010 - Reserved 011 - Reserved 100 - Not described 101 - Not described 110 - Not described 111 - Not described	
CLK_ACC[1:0]			R/W
0x12	00000000	This control is used to set the clock accuracy. 00 - Level II - normal accuracy +/-1000 x 10 ⁻⁶ 01 - Level I - high accuracy +/- 50 x 10 ⁻⁶ 10 - Level III - variable pitch shifted clock 11 - Reserved	
CATEGORY_CODE[7:0]			R/W
0x13	00000000	This control is used to set the category code for the audio InfoFrame. 00000000 - Default	
SOURCE_NUMBER[3:0]			R/W
0x14	00000000	This control is used to set the source number. 0000 - Default	

Reg	Bits	Description	
WORD_LENGTH[3:0]			R/W
0x14	00000000	This control is used to set the word length. 0000 - Not specified 0001 - Not specified 0010 - 16 bits 0011 - 20 bits 0100 - 18 bits 0101 - 22 bits 0110 - Reserved 0111 - Reserved 1000 - 19 bits 1001 - 23 bits 1010 - 20 bits 1011 - 24 bits 1100 - 17 bits 1101 - 21 bits 1110 - Reserved 1111 - Reserved	
I2S_SF[3:0]			R/W
0x15	00000000	This control is used to set the sampling frequency for I2S audio. This information is used by both the audio Rx and the pixel repetition. 0000 - 44.1 kHz 0001 - Reserved 0010 - 48 kHz 0011 - 32 kHz 0100 - Reserved 0101 - Reserved 0110 - Reserved 0111 - Reserved 1000 - 88.2 kHz 1001 - Reserved 1010 - 96 kHz 1011 - Reserved 1100 - 176.4 kHz 1101 - Reserved 1110 - 192 kHz 1111 - Reserved	
VFE_INPUT_ID[3:0]			R/W
0x15	00000000	This control is used to select the input data format for the HDMI Tx. 000 - RGB 444 or YCbCr 444 001 - YCbCr 422 separate syncs 010 - YCbCr 422 embedded syncs 011 - YCbCr 422, 2x pixel clock, separated syncs 100 - YCbCr 422, 2x pixel clock, embedded syncs 101 - 12-bit RGB 444 or YCbCr (DDR separate syncs) 110 - YCbCr 422 (DDR with separate syncs) 111 - Undefined	
VFE_OUT_FMT[1:0]			R/W
0x16	00000000	This control is used to select the video output format. 00 - RGB 444 01 - YCbCr 444 10 - YCbCr 422 11 - YCbCr 422	
VFE_422_WIDTH[1:0]			R/W
0x16	00000000	This control is used to select the output bus width. 00 - 12 bits 01 - 10 bits 10 - 12 bits 11 - 8 bits	

Reg	Bits	Description	
GEN_444_EN			R/W
0x17	00000 <u>0</u> 00	This control is used to enable 422 to 444 up conversion. 0 - Disable 422 to 444 up conversion 1 - Enable 422 to 444 up conversion	
ASP_RATIO			R/W
0x17	00000 <u>0</u> 0	This control is used to set the aspect ratio of the input video. 0 - 4:3 1 - 16:9	
CSC_EN			R/W
0x18	<u>0</u> 1000110	This control is used to enable color space conversion. 0 - Disable color space conversion 1 - Enable color space conversion	
CSC_MODE[1:0]			R/W
0x18	<u>0</u> 1 <u>0</u> 00110	This control is used to set the CSC scaling factor. The default is YCbCr to RGB for SD video. 00 - +/- 1.0, -4096 to 4095 01 - +/-2.0, -8192 to 8190 10 - +/- 4.0, -16384 to 16380 11 - +/- 4.0, -16384 to 16380	
CSC_A1[12:0]			R/W
0x18 0x19	<u>0</u> 1 <u>0</u> <u>0</u> 00110 <u>0</u> 1100010	This control is used to set the color space converter coefficient A1	
CSC_A2[12:0]			R/W
0x1A 0x1B	<u>0</u> 0 <u>0</u> <u>0</u> 0100 <u>1</u> 0101000	This control is used to set the color space converter coefficient A2.	
CSC_A3[12:0]			R/W
0x1C 0x1D	<u>0</u> 0 <u>0</u> <u>0</u> 00000 <u>0</u> 0000000	This control is used to set the color space converter coefficient A3.	
CSC_A4[12:0]			R/W
0x1E 0x1F	<u>0</u> 0 <u>0</u> <u>1</u> 1100 <u>1</u> 0000100	This control is used to set the color space converter coefficient A4.	
CSC_B1[12:0]			R/W
0x20 0x21	<u>0</u> 0 <u>0</u> <u>1</u> 1100 <u>1</u> 0111111	This control is used to set the color space converter coefficient B1.	
CSC_B2[12:0]			R/W
0x22 0x23	<u>0</u> 0 <u>0</u> <u>0</u> 0100 <u>1</u> 0101011	This control is used to set the color space converter coefficient B2.	
CSC_B3[12:0]			R/W
0x24 0x25	<u>0</u> 0 <u>0</u> <u>1</u> 1110 <u>0</u> 1110000	This control is used to set the color space converter coefficient B3.	
CSC_B4[12:0]			R/W
0x26 0x27	<u>0</u> 0 <u>0</u> <u>0</u> 0010 <u>0</u> 0011110	This control is used to set the color space converter coefficient B4.	
CSC_C1[12:0]			R/W
0x28 0x29	<u>0</u> 0 <u>0</u> <u>0</u> 0000 <u>0</u> 0000000	This control is used to set the color space converter coefficient C1.	
CSC_C2[12:0]			R/W
0x2A 0x2B	<u>0</u> 0 <u>0</u> <u>0</u> 0100 <u>1</u> 0101000	This control is used to set the color space converter coefficient C2.	

Reg	Bits	Description	
CSC_C3[12:0]			R/W
0x2C 0x2D	00001000 00010010	This control is used to set the color space converter coefficient C3.	
CSC_C4[12:0]			R/W
0x2E 0x2F	00011011 10101100	This control is used to set the color space converter coefficient C4.	
PR_MODE[1:0]			R/W
0x3B	10000000	This control is used to select the pixel repetition mode. 00 - Auto mode 01 - Maximum mode 10 - Manual mode 11 - Manual mode	
EXT_PLL_PR[1:0]			R/W
0x3B	10000000	This control is used to set the value for PLL pixel repetition. 00 - x1 01 - x2 10 - x4 11 - x4	
EXT_TARGET_PR[1:0]			R/W
0x3B	10000000	This control is used to set the pixel repetition number to send to the Rx. 00 - x1 01 - x2 10 - x4 11 - x4	
EXT_VID_TO_RX[5:0]			R/W
0x3C	00000000	This control is used to set the manual VIC sent to the Rx. 000000 - Default	
PR_TO_RX[1:0]			R
0x3D	00000000	This readback indicates the actual pixel repetition sent to the Rx. 00 - x1 01 - x2 10 - x4 11 - x4	
VID_TO_RX[5:0]			R
0x3D	00000000	This readback indicates the actual VIC sent to the HDMI Rx.	
VFE_FMT_VID[5:0]			R
0x3E	00000000	This readback indicates the VIC detected by the video front end.	
VFE_AUX_VID[2:0]			R
0x3F	00000000	This readback indicates the video input formats that are not inside the 861B table. 000 - Set by vfe_fmt_vid 001 - 240p not active 010 - 576i not active 011 - 288p not active 100 - 480i active 101 - 240p active 110 - 576i active 111 - 288p active	
VFE_PROG_MODE[1:0]			R
0x3F	00000000	This readback indicates the progressive mode information about 240p and 288p 01 - 262 lines (240p),312 lines (288p) 10 - 263 lines(240p),313 lines (288p) 11 - undefined(240p),314lines (288p)	

Reg	Bits	Description	
GC_PKT_EN			R/W
0x40	00000000	This control is used to enable a general control packet. 0 - Disable general control packet 1 - Enable general control packet	
SPD_PKT_EN			R/W
0x40	00000000	This control is used to enable an SPD packet. 0 - Disable SPD packet 1 - Enable SPD packet	
MPEG_PKT_EN			R/W
0x40	00000000	This control is used to enable an MPEG packet. 0 - Disable MPEG packet 1 - Enable MPEG packet	
ACP_PKT_EN			R/W
0x40	00000000	This control is used to enable an ACP packet. 0 - Disable ACP packet 1 - Enable ACP packet	
ISRC_PKT_EN			R/W
0x40	00000000	This control is used to enable an ISRC packet. 0 - Disable ISRC packet 1 - Enable ISRC packet	
GM_PKT_EN			R/W
0x40	00000000	This control is used to enable a gamut metadata packet. 0 - Disable gamut metadata packet 1 - Enable gamut metadata packet	
SPARE_PKT1_EN			R/W
0x40	00000000	This control is used to enable spare_packet1. 0 - Disable spare_packet1 1 - Enable spare_packet1	
SPARE_PKT0_EN			R/W
0x40	00000000	This control is used to enable spare_packet0. 0 - Disable spare_packet0 1 - Enable spare_packet0	
SYSTEM_PD			R/W
0x41	01010000	This control is used to power down the HDMI Tx. 0 - Normal operation 1 - Power down ADV7850 Tx	
HPD_STATE			R
0x42	10010000	This readback displays the state of the hot plug detection. 0 - Low hot plug detect state 1 - High hot plug detect state	
MSEN_STATE			R
0x42	10010000	This readback displays the state of the clock termination. 0 - HDMI clock termination not detected 1 - HDMI clock termination detected	
I2S_32BIT_MODE			R
0x42	10010000	This readback indicates the mode of the I2S detected. 0 - 32-bit mode detected 1 - 64-bit mode detected	
EDID_ID[7:0]			R/W
0x43	01111110	This controls sets the I2C address for the EDID memory map of the HDMI Tx. 01111110 - Default	
N_CTS_PKT_EN			R/W
0x44	01111001	This control is used to enable an N_CTS packet. 0 - Disable N_CTS packet 1 - Enable N_CTS packet	

Reg	Bits	Description	
AUDIO_SAMPLE_PKT_EN			R/W
0x44	0111001	This control is used to enable an audio sample packet. 0 - Disable audio sample packet 1 - Enable audio sample packet	
AVIIF_PKT_EN			R/W
0x44	0111001	This control is used to enable an AVI InfoFrame. 0 - Disable AVI InfoFrame 1 - Enable AVI InfoFrame	
AUDIOIF_PKT_EN			R/W
0x44	0111001	This control is used to enable an audio InfoFrame. 0 - Disable audio InfoFrame 1 - Enable audio InfoFrame	
DCM_MODE			R/W
0x44	0111001	This control is used to enable a DCM. 0 - Disable DCM 1 - Enable DCM	
DSD_EN[7:0]			R/W
0x46	00000000	This control is used to enable the DSD data channel. 0 - Disable DSD data channel 1 - Enable DSD data channel	
AUTO_CHECKSUM_EN			R/W
0x4A	10000000	This control is used to enable the automatic checksum on the InfoFrame packets. 0 - Disable automatic checksum 1 - Enable automatic checksum generated by chip for all InfoFrame packets	
AVI_UPDATE			R/W
0x4A	10000000	This control is used to stop new AVI InfoFrames from being transmitted to the Rx. This control allows the InfoFrame data to be updated fully before the Rx is updated. 0 - New AVI InfoFrame data transmitted immediately to Rx 1 - New AVI InfoFrame data not transmitted to Rx	
AUDIO_UPDATE			R/W
0x4A	10000000	This control is used to stop new audio InfoFrames from being transmitted to the Rx. This control allows the InfoFrame data to be updated fully before the Rx is updated. 0 - Audio InfoFrame data transmitted immediately to Rx 1 - New Audio InfoFrame data not transmitted to Rx	
GCP_UPDATE			R/W
0x4A	10000000	This control is used to stop new GCP InfoFrames from being transmitted to the Rx. This control allows the InfoFrame data to be updated fully before the Rx is updated. 0 - GCP InfoFrame data transmitted immediately to Rx 1 - New GCP InfoFrame data not transmitted to Rx	
CLEAR_AVMUTE			R/W
0x4B	00000000	This control is used to set the clear AV mute signal. 0 - Clear the clear AV mute signal 1 - Set clear AV mute signal	
SET_AVMUTE			R/W
0x4B	00000000	This control is used to set the set AV mute signal. 0 - Clear the set AV mute signal signal 1 - Set the set AV mute signal	
GC_CD[3:0]			R/W
0x4C	00000000	This control is used to set the pixel packing phase. 4'b0000 - Color Depth not indicated 4'b0001 - Reserved 4'b0010 - Reserved 4'b0011 - Reserved 4'b0100 - 24 bits per pixel 4'b0101 - 30 bits per pixel 4'b0110 - 36 bits per pixel 4'b0111 - 48 bits per pixel	

Reg	Bits	Description	
GC_BYTE2[7:0]			R/W
0x4D	00000000	This control is reserved.	
GC_BYTE3[7:0]			R/W
0x4E	00000000	This control is reserved.	
GC_BYTE4[7:0]			R/W
0x4F	00000000	This control is reserved.	
GC_BYTE5[7:0]			R/W
0x50	00000000	This control is reserved.	
GC_BYTE6[7:0]			R/W
0x51	00000000	This control is reserved.	
AVI_VERSION[2:0]			R/W
0x52	00000010	This control is used to set the AVI InfoFrame version. 010 - Default	
AVI_LENGTH[4:0]			R/W
0x53	00001101	This control is used to set the length of the AVI InfoFrame packet body, excluding the checksum. 01101 - Default	
AVI_CHECKSUM[7:0]			R/W
0x54	00000000	This control is used to set the checksum for AVI InfoFrame. It is only used in manual mode. 00000000 - Default	
AVI_BYTE1_7			R/W
0x55	00000000	This control is reserved.	
Y1Y0[1:0]			R/W
0x55	00000000	This control is used to set the Y1Y0 value in the InfoFrame. 00 - RGB 01 - YCbCr 422 10 - YCbCr 444 11 - Reserved	
A0			R/W
0x55	00000000	This control is used to set the active information present field in the InfoFrame. 0 - No data 1 - Active format Information valid	
B1B0[1:0]			R/W
0x55	00000000	This control is used to set the bar information in the InfoFrame. 00 - Invalid 01 - Vertical 10 - Horizontal 11 - Both	
S1S0[1:0]			R/W
0x55	00000000	This control is used to set the scan information in the InfoFrame. 00 - No data 01 - TV 10 - PC 11 - Reserved	
C1C0[1:0]			R/W
0x56	00000000	This control is used to set colorimetry information in the InfoFrame. 00 - No data 01 - ITU601 10 - ITU709 11 - Reserved	

Reg	Bits	Description	
M1M0[1:0]			R/W
0x56	00 <u>000000</u>	This control is used to set the picture aspect ratio in the InfoFrame. 00 - No data 01 - 4:3 10 - 16:9 11 - Reserved	
R3210[3:0]			R/W
0x56	0000 <u>0000</u>	This control is used to set the active format aspect ratio in the InfoFrame. 1000 - Same as aspect ratio 1001 - 4:3 (center) 1010 - 16:9 (center) 1011 - 14:9 (center)	
ITC			R/W
0x57	<u>0</u> 0000000	This control is used to set the IT content in the InfoFrame. Refer to CEA-861-D, table 11 for details. 0 - None 1 - IT content	
EC210[2:0]			R/W
0x57	<u>0</u> 0000000	This control is used to set the extended colorimetry in the InfoFrame. Refer to CEA-861-D, table 11 for details. 0 - XYVCC 601 1 - XYVCC 709	
Q1Q0[1:0]			R/W
0x57	0000 <u>00</u> 00	This control is used to set the quantization range in the InfoFrame. Refer to CEA-861-D, table 11 for details. 00 - Default range 01 - Limited range 10 - Full range 11 - Reserved	
SC[1:0]			R/W
0x57	000000 <u>00</u>	This control is used to set non uniform picture scaling. Refer to CEA-861-D, table 11 for details. 00 - Unknown 01 - Scaling in horizontal direction 10 - Scaling in vertical direction 11 - Scaling in both horizontal and vertical directions	
AVI_BYTE4_7			R/W
0x58	<u>0</u> 0000000	This control is reserved.	
AVI_BYTES_7_4[3:0]			R/W
0x59	<u>0000</u> 0000	This control is reserved. 0000 - Default	
AVI_BYTE6[7:0]			R/W
0x5A	<u>00000000</u>	This control is used to set the 1st byte of bar information. 00000000 - Default	
AVI_BYTE7[7:0]			R/W
0x5B	<u>00000000</u>	This control is used to set the 2nd byte of bar information. 00000000 - Default	
AVI_BYTE8[7:0]			R/W
0x5C	<u>00000000</u>	This control is used to set the 3rd byte of bar information. 00000000 - Default	
AVI_BYTE9[7:0]			R/W
0x5D	<u>00000000</u>	This control is used to set the 4th byte of bar information. 00000000 - Default	
AVI_BYTE10[7:0]			R/W
0x5E	<u>00000000</u>	This control is used to set the 5th byte of bar information. 00000000 - Default	

Reg	Bits	Description	
AVI_BYTE11[7:0]			R/W
0x5F	00000000	This control is used to set the 6th byte of bar information. 00000000 - Default	
AVI_BYTE12[7:0]			R/W
0x60	00000000	This control is used to set the 7th byte of bar information. 00000000 - Default	
AVI_BYTE13[7:0]			R/W
0x61	00000000	This control is used to set the last byte of bar information. 00000000 - Default	
AVI_BYTE14[7:0]			R/W
0x62	00000000	This control is reserved. 00000000 - Default	
AVI_BYTE15[7:0]			R/W
0x63	00000000	This control is reserved. 00000000 - Default	
AVI_BYTE16[7:0]			R/W
0x64	00000000	This control is reserved. 00000000 - Default	
AVI_BYTE17[7:0]			R/W
0x65	00000000	This control is reserved. 00000000 - Default	
AVI_BYTE18[7:0]			R/W
0x66	00000000	This control is reserved. 00000000 - Default	
AVI_BYTE19[7:0]			R/W
0x67	00000000	This control is reserved. 00000000 - Default	
AVI_BYTE20[7:0]			R/W
0x68	00000000	This control is reserved. 00000000 - Default	
AVI_BYTE21[7:0]			R/W
0x69	00000000	This control is reserved. 00000000 - Default	
AVI_BYTE22[7:0]			R/W
0x6A	00000000	This control is reserved. 00000000 - Default	
AVI_BYTE23[7:0]			R/W
0x6B	00000000	This control is reserved. 00000000 - Default	
AVI_BYTE24[7:0]			R/W
0x6C	00000000	This control is reserved. 00000000 - Default	
AVI_BYTE26[7:0]			R/W
0x6E	00000000	This control is reserved. 00000000 - Default	
AVI_BYTE27[7:0]			R/W
0x6F	00000000	This control is reserved. 00000000 - Default	
AUDIOIF_VERSION[2:0]			R/W
0x70	00000001	This control is used to set the version of the audio InfoFrame. 001 - Default	

Reg	Bits	Description	
AUDIOIF_LENGTH[4:0]			R/W
0x71	00001010	This control is used to set the length of the audio InfoFrame packet body, excluding the checksum. 01010 - Default	
AUDIOIF_CHECKSUM[7:0]			R/W
0x72	00000000	This control is used to set the checksum for this packet. It is only used in manual checksum mode. 00000000 - Default	
AUDIOIF_BYTE1_3			R/W
0x73	00000000	This control is reserved. 0 - Default	
AUDIOIF_CC[2:0]			R/W
0x73	00000000	This control is used to select the audio InfoFrame channel count. 000 - Refer to stream header 001 - 2 channels 010 - 3 channels 011 - 4 channels 100 - 5 channels 101 - 6 channels 110 - 7 channels 111 - 8 channels	
AUDIOIF_BYTE2_7_5[2:0]			R/W
0x74	00000000	This control is reserved.	
AUDIOIF_SF[2:0]			R/W
0x74	00000000	This control is used to set the audio sampling frequency in the InfoFrame. It should be set to 0, except for SACD. 000 - Default	
AUDIOIF_SS[1:0]			R/W
0x74	00000000	This control is used to set the sample size in the InfoFrame. It should be set to 0. 00 - Default	
AUDIOIF_BYTE3[7:0]			R/W
0x75	00000000	This control is used to set the audio InfoFrame Byte3. 00000000 - Default	
AUDIOIF_CA[7:0]			R/W
0x76	00000000	This control is used to set the speaker allocation for up to eight channels. 00000000 - Default	
AUDIOIF_BYTE5_2_0[2:0]			R/W
0x77	00000000	This control is reserved. 000 - Default	
AUDIOIF_BYTE6[7:0]			R/W
0x78	00000000	This control is reserved. 00000000 - Default	
AUDIOIF_BYTE7[7:0]			R/W
0x79	00000000	This control is reserved. 00000000 - Default	
AUDIOIF_BYTE8[7:0]			R/W
0x7A	00000000	This control is reserved. 00000000 - Default	
AUDIOIF_BYTE9[7:0]			R/W
0x7B	00000000	This control is reserved. 00000000 - Default	
AUDIOIF_BYTE10[7:0]			R/W
0x7C	00000000	This control is reserved. 00000000 - Default	

Reg	Bits	Description	
HPD_INTR_MASK			R/W
0x94	11000000	This control is used to set the mask for the HPD interrupt. 1 - Default	
MSEN_INTR_MASK			R/W
0x94	11000000	This control is used to set the mask for the MSEN interrupt. 1 - Default	
VS_INTR_MASK			R/W
0x94	11000000	This control is used to set the mask for the VS interrupt. 1 - Default	
EDID_RDY_INTR_MASK			R/W
0x94	11000000	This control is used to set the mask for the EDID ready interrupt. 0 - Default	
RI_RDY_INTR_MASK			R/W
0x94	11000000	This control is used to set the mask for the Pj ready interrupt. 0 - Default	
HDCP_ERROR_INTR_MASK			R/W
0x95	00000000	This control is used to set the mask for the HDCP error interrupt. 0 - Default	
BKSV_FLAG_INTR_MASK			R/W
0x95	00000000	This control sets the mask for the Bksv flag. 0 - Default	
HPD_INTR			R/W
0x96	00000000	This readback indicates the status of the hot plug detection interrupt. 0 - No interrupt detected 1 - Interrupt detected	
MSEN_INTR			R/W
0x96	00000000	This readback indicates the status of the monitor connection interrupt. 0 - No interrupt detected 1 - Interrupt detected	
VS_INTR			R/W
0x96	00000000	This readback indicates the status of the active VS edge interrupt. 0 - No interrupt detected 1 - Interrupt detected	
EDID_RDY_INTR			R/W
0x96	00000000	This readback indicates the status of the EDID ready interrupt. 0 - No interrupt detected 1 - Interrupt detected	
RI_RDY_INTR			R/W
0x96	00000000	This readback indicates the status Ri (16th Ri is available). 0 - No interrupt detected 1 - Interrupt detected	
HDCP_ERROR_INTR			R/W
0x97	00000000	This readback indicates the status of the HDCP master interrupt. 0 - No interrupt detected 1 - Interrupt detected	
TX_READY_INTR			R/W
0x97	00000000	This readback indicates the status of the Tx ready interrupt. 0 - No interrupt detected 1 - Interrupt detected	
TX_ARBITRATION_LOST_INTR			R/W
0x97	00000000	This readback indicates the status of the Tx arbitration lost interrupt. 0 - No interrupt detected 1 - Interrupt detected	

Reg	Bits	Description	
TX_RETRY_TIMEOUT_INTR			R/W
0x97	00000000	This readback indicates the status of the retry timeout interrupt. 0 - No interrupt detected 1 - Interrupt detected	
HIGH_VSYNC[1:0]			R/W
0x9E	00000000	This control is used to set the video refresh rates. 00 - Normal refresh rates 01 - 2x refresh rates 10 - 4x refresh rates 11 - Normal refresh rates	
VIDEO_OFFSET_CTL[1:0]			R/W
0x9E	00000000	[1] is to turn on video code offset [0] is to generate black level video Default is 00. 00 - None 01 - None 10 - None 11 - None	
LOWER_VSYNC[1:0]			R/W
0x9F	00000000	This control is used to set the video VSync frequency for lower vertical frequency signals. 00 - More than 30 Hz 01 - 24 Hz 10 - 25 Hz 11 - 30 Hz	
HDCP_START_DELAY[2:0]			R/W
0xAB	00000000	This control is used to set the delay control between HDCP enable and read Bksv. 000 - No delay 001 - 1 ms 010 - 2 ms 011 - 5 ms 100 - 10 ms 101 - 20 ms 110 - 40 ms 111 - 200 ms	
AN_DELAY[2:0]			R/W
0xAD	00000000	This control is used to set the An delay selection. 000 - No delay 001 - 1 ms 010 - 2 ms 011 - 5 ms 100 - 10 ms 101 - 20 ms 110 - 40 ms 111 - 200 ms	
AKSV_DELAY[2:0]			R/W
0xAD	00000000	This control is used to set the delay control between write An to sink and write Aksv to sink. 000 - No delay 001 - 1 ms 010 - 2 ms 011 - 5 ms 100 - 10 ms 101 - 20 ms 110 - 40 ms 111 - 200 ms	
HDCP_DESIRED			R/W
0xAF	00010100	This control is used to enable input A/V content encryption. 0 - Do not encrypt A/V content 1 - Encrypt A/V content	

Reg	Bits	Description	
FRAME_ENC			R/W
0xAF	00010100	This control is used to enable encryption on the current frame. 0 - Do not encrypt current frame 1 - Encrypt current frame	
HDMI_MODE_SEL			R/W
0xAF	00010100	This control is used to set the HDMI mode. In automatic mode, audio detection will put the Tx into HDMI mode. 0 - Set automatic mode 1 - Set DVI/HDMI mode	
EXT_HDMI_MODE			R/W
0xAF	00010100	This control is used to set the output to DVI or HDMI. 0 - Set DVI output 1 - Set HDMI output	
ENC_ON			R
0xB8	00000000	This readback indicates if the A/V content is being encrypted at present. 0 - Not encrypted 1 - Encrypted	
KEYS_READ_ERROR			R
0xB8	00000000	This readback indicates if an HDCP key error occurred. 0 - Read HDCP keys correctly 1 - Encountered errors when reading the HDCP keys	
BCAPS[7:0]			R
0xBE	00000000	This readback indicates the HDCP status. [7] - Reserved [6] - Repeater [5] - Bksv FIFO ready [4] - Fast DDC bus [3:2] - Reserved [1] - HDMI 1.1 [0] - Fast re-authentication	
BKSV0[7:0]			R
0xBF	00000000	This readback indicates the Bksv read from Rx by the HDCP controller.	
BKSV1[7:0]			R
0xC0	00000000	This readback indicates the Bksv read from Rx by the HDCP controller.	
BKSV2[7:0]			R
0xC1	00000000	This readback indicates the Bksv read from Rx by the HDCP controller.	
BKSV3[7:0]			R
0xC2	00000000	This readback indicates the Bksv read from Rx by the HDCP controller.	
BKSV4[7:0]			R
0xC3	00000000	This readback indicates the Bksv read from Rx by the HDCP controller.	
EDID_SEGMENT[7:0]			R/W
0xC4	00000000	Sets the E-DDC segment used by the EDID Fetch routine.	
ERROR_FLAG			R/W
0xC5	00000000	This readback indicates if the firmware detected an error. 0 - No error 1 - Error	
AN_STOP			R
0xC5	00000000	This readback indicates if the firmware gets an An. It is set low again if authentication is restarted. 0 - No flag 1 - Flag inserted	

Reg	Bits	Description	
HDCP_ENABLED			R
0x5	00000000	This readback indicates if the firmware completed a successful HDCP authentication. 0 - No flag 1 - Flag inserted	
EDID_READY_FLAG			R
0x5	00000000	This readback indicates if the firmware successfully read the EDID. It goes low if the firmware uses data memory for HDCP repeater authentication. 0 - No flag 1 - Flag inserted	
I2C_INTERRUPT			R
0x5	00000000	This readback indicates if an access to the EDID I2C interface is detected. It is cleared by the firmware. 0 - No flag 1 - Flag inserted	
RI_FLAG			R
0x5	00000000	This readback indicates that an ri_update took place. The flag goes high on the positive edge from the HDCP engine. It is reset by the firmware. 0 - No flag 1 - Flag inserted	
PJ_FLAG			R
0x5	00000000	This readback indicates that a pj_update took place. The flag goes high on the positive edge from the HDCP engine. It is reset by the firmware. 0 - No flag 1 - Flag inserted	
HDMI_MODE			R
0x6	00000000	This readback indicates the HDMI mode selected. 0 - DVI mode 1 - HDMI mode	
HDCP_REQUESTED			R
0x6	00000000	This readback indicates the HDCP status. 0 - No HDCP requested 1 - HDCP requested	
RX_SENSE			R
0x6	00000000	This readback indicates whether or not the receiver detected a TMDS pullup on the clock signal line. 0 - TMDS clock pullup not present 1 - TMDS clock pullup present	
EEPROM_READ_OK			R
0x6	00000000	This readback indicates the HDCP engine has successfully read the EEPROM and OTP. 0 - No error detected 1 - Error detected	
BKS_V_FLAG			R/W
0x7	00000000	This readback indicates if the bksv_count was detected. 0 - bksvs_count not detected 1 - bksvs_count detected	
BKS_V_COUNT[6:0]			R
0x7	00000000	This readback indicates the Bksvs available in the sink's Bksv FIFO.	
HDCP_CONTROLLER_ERROR[3:0]			R
0x8	00000000	This readback indicates the HDCP error information. 0000 - No error 0001 - Bad receiver Bksv 0010 - Ri mismatch 0011 - Pj mismatch 0100 - I2C error (usually a no-ack) 0101 - Time out waiting for downstream repeater 0110 - Maximum cascade of repeaters exceeded 0111 - SHA-1 hash check of KSV list failed 1000 - Too many devices connected to repeater tree	

Reg	Bits	Description	
HDCP_CONTROLLER_STATE[3:0]			R
0xC8	00000000	This readback indicates the HDCP controller status. 0000 - In reset (no hot plug detected) 0001 - Reading EDID 0010 - Idle (waiting for HDCP requested) 0011 - Initializing HDCP 0100 - HDCP enable 0101 - Initializing HDCP repeater	
EDID_TRYS[3:0]			R/W
0xC9	00000011	This control is used to set the maximum number of times that the EDID read will be attempted if unsuccessful. Reading the EDID begins upon setting this register and on powerup. 0011 - Default	
PLL_LOCK_STATUS			R
0xE4	00000000	This readback displays the PLL lock status. 0 - PLL not locked 1 - PLL locked	
TERMPWRDWN_I2C			R/W
0xE6	00000000	This control is used to enable monitor sense. 0 - Enable monitor sense 1 - Disable monitor sense	
CLKDRVENABLE_I2C			R/W
0xE8	00010000	This control is used to enable the TMDS clock. 0 - Power down TMDS clock 1 - Power up TMDS clock	
TMDS_CLK_INV_I2C			R/W
0xEA	10000100	This control is used to invert the TMDS clock. 0 - Normal TMDS clock 1 - Invert TMDS clock	
VIDEO_CLOCK_DETECT			R/W
0xEF	10000100	This control is used to enable the HDMI Tx Squelch feature. This should be set to 0 in all analog input modes. 1 - Disable TMDS Clock detection (and HS activity Detect) 0 - Enable TMDS clock detection (and HS Activity Detect if enabled)	
HS_ACTIVE_DET_EN			R/W
0xFE	00000000	This control is used to enable HS activity detection for the HDMI Tx Squelch feature. This should be set to 0 in all analog input modes. 0 - Disable HS Activity Detect 1 - Enable HS activity Detect	

2.15 ADDR 70 (PACKETMEMORY)

Reg	Bits	Description	
		SPD_HEADER_BYTE_0[7:0]	R/W
0x00	00000000		
		SPD_HEADER_BYTE_1[7:0]	R/W
0x01	00000000		
		SPD_HEADER_BYTE_2[7:0]	R/W
0x02	00000000		
		SPD_PACKET_BYTE_0[7:0]	R/W
0x03	00000000		
		SPD_PACKET_BYTE_1[7:0]	R/W
0x04	00000000		
		SPD_PACKET_BYTE_2[7:0]	R/W
0x05	00000000		
		SPD_PACKET_BYTE_3[7:0]	R/W
0x06	00000000		
		SPD_PACKET_BYTE_4[7:0]	R/W
0x07	00000000		
		SPD_PACKET_BYTE_5[7:0]	R/W
0x08	00000000		
		SPD_PACKET_BYTE_6[7:0]	R/W
0x09	00000000		
		SPD_PACKET_BYTE_7[7:0]	R/W
0x0A	00000000		
		SPD_PACKET_BYTE_8[7:0]	R/W
0x0B	00000000		
		SPD_PACKET_BYTE_9[7:0]	R/W
0x0C	00000000		
		SPD_PACKET_BYTE_10[7:0]	R/W
0x0D	00000000		
		SPD_PACKET_BYTE_11[7:0]	R/W
0x0E	00000000		
		SPD_PACKET_BYTE_12[7:0]	R/W
0x0F	00000000		
		SPD_PACKET_BYTE_13[7:0]	R/W
0x10	00000000		
		SPD_PACKET_BYTE_14[7:0]	R/W
0x11	00000000		
		SPD_PACKET_BYTE_15[7:0]	R/W
0x12	00000000		

Reg	Bits	Description	
SPD_PACKET_BYTE_16[7:0]			R/W
0x13	00000000		
SPD_PACKET_BYTE_17[7:0]			R/W
0x14	00000000		
SPD_PACKET_BYTE_18[7:0]			R/W
0x15	00000000		
SPD_PACKET_BYTE_19[7:0]			R/W
0x16	00000000		
SPD_PACKET_BYTE_20[7:0]			R/W
0x17	00000000		
SPD_PACKET_BYTE_21[7:0]			R/W
0x18	00000000		
SPD_PACKET_BYTE_22[7:0]			R/W
0x19	00000000		
SPD_PACKET_BYTE_23[7:0]			R/W
0x1A	00000000		
SPD_PACKET_BYTE_24[7:0]			R/W
0x1B	00000000		
SPD_PACKET_BYTE_25[7:0]			R/W
0x1C	00000000		
SPD_PACKET_BYTE_26[7:0]			R/W
0x1D	00000000		
SPD_PACKET_BYTE_27[7:0]			R/W
0x1E	00000000		
SPD_UPDATE			R/W
0x1F	00000000		
MPEG_HEADER_BYTE_0[7:0]			R/W
0x20	00000000		
MPEG_HEADER_BYTE_1[7:0]			R/W
0x21	00000000		
MPEG_HEADER_BYTE_2[7:0]			R/W
0x22	00000000		
MPEG_PACKET_BYTE_0[7:0]			R/W
0x23	00000000		
MPEG_PACKET_BYTE_1[7:0]			R/W
0x24	00000000		
MPEG_PACKET_BYTE_2[7:0]			R/W
0x25	00000000		

Reg	Bits	Description	
MPEG_PACKET_BYTE_3[7:0]			R/W
0x26	00000000		
MPEG_PACKET_BYTE_4[7:0]			R/W
0x27	00000000		
MPEG_PACKET_BYTE_5[7:0]			R/W
0x28	00000000		
MPEG_PACKET_BYTE_6[7:0]			R/W
0x29	00000000		
MPEG_PACKET_BYTE_7[7:0]			R/W
0x2A	00000000		
MPEG_PACKET_BYTE_8[7:0]			R/W
0x2B	00000000		
MPEG_PACKET_BYTE_9[7:0]			R/W
0x2C	00000000		
MPEG_PACKET_BYTE_10[7:0]			R/W
0x2D	00000000		
MPEG_PACKET_BYTE_11[7:0]			R/W
0x2E	00000000		
MPEG_PACKET_BYTE_12[7:0]			R/W
0x2F	00000000		
MPEG_PACKET_BYTE_13[7:0]			R/W
0x30	00000000		
MPEG_PACKET_BYTE_14[7:0]			R/W
0x31	00000000		
MPEG_PACKET_BYTE_15[7:0]			R/W
0x32	00000000		
MPEG_PACKET_BYTE_16[7:0]			R/W
0x33	00000000		
MPEG_PACKET_BYTE_17[7:0]			R/W
0x34	00000000		
MPEG_PACKET_BYTE_18[7:0]			R/W
0x35	00000000		
MPEG_PACKET_BYTE_19[7:0]			R/W
0x36	00000000		
MPEG_PACKET_BYTE_20[7:0]			R/W
0x37	00000000		
MPEG_PACKET_BYTE_21[7:0]			R/W
0x38	00000000		

Reg	Bits	Description	
MPEG_PACKET_BYTE_22[7:0]			R/W
0x39	00000000		
MPEG_PACKET_BYTE_23[7:0]			R/W
0x3A	00000000		
MPEG_PACKET_BYTE_24[7:0]			R/W
0x3B	00000000		
MPEG_PACKET_BYTE_25[7:0]			R/W
0x3C	00000000		
MPEG_PACKET_BYTE_26[7:0]			R/W
0x3D	00000000		
MPEG_PACKET_BYTE_27[7:0]			R/W
0x3E	00000000		
MPEG_UPDATE			R/W
0x3F	00000000		
ACP_HEADER_BYTE_0[7:0]			R/W
0x40	00000000		
ACP_HEADER_BYTE_1[7:0]			R/W
0x41	00000000		
ACP_HEADER_BYTE_2[7:0]			R/W
0x42	00000000		
ACP_PACKET_BYTE_0[7:0]			R/W
0x43	00000000		
ACP_PACKET_BYTE_1[7:0]			R/W
0x44	00000000		
ACP_PACKET_BYTE_2[7:0]			R/W
0x45	00000000		
ACP_PACKET_BYTE_3[7:0]			R/W
0x46	00000000		
ACP_PACKET_BYTE_4[7:0]			R/W
0x47	00000000		
ACP_PACKET_BYTE_5[7:0]			R/W
0x48	00000000		
ACP_PACKET_BYTE_6[7:0]			R/W
0x49	00000000		
ACP_PACKET_BYTE_7[7:0]			R/W
0x4A	00000000		
ACP_PACKET_BYTE_8[7:0]			R/W
0x4B	00000000		

Reg	Bits	Description	
ACP_PACKET_BYTE_9[7:0]			R/W
0x4C	00000000		
ACP_PACKET_BYTE_10[7:0]			R/W
0x4D	00000000		
ACP_PACKET_BYTE_11[7:0]			R/W
0x4E	00000000		
ACP_PACKET_BYTE_12[7:0]			R/W
0x4F	00000000		
ACP_PACKET_BYTE_13[7:0]			R/W
0x50	00000000		
ACP_PACKET_BYTE_14[7:0]			R/W
0x51	00000000		
ACP_PACKET_BYTE_15[7:0]			R/W
0x52	00000000		
ACP_PACKET_BYTE_16[7:0]			R/W
0x53	00000000		
ACP_PACKET_BYTE_17[7:0]			R/W
0x54	00000000		
ACP_PACKET_BYTE_18[7:0]			R/W
0x55	00000000		
ACP_PACKET_BYTE_19[7:0]			R/W
0x56	00000000		
ACP_PACKET_BYTE_20[7:0]			R/W
0x57	00000000		
ACP_PACKET_BYTE_21[7:0]			R/W
0x58	00000000		
ACP_PACKET_BYTE_22[7:0]			R/W
0x59	00000000		
ACP_PACKET_BYTE_23[7:0]			R/W
0x5A	00000000		
ACP_PACKET_BYTE_24[7:0]			R/W
0x5B	00000000		
ACP_PACKET_BYTE_25[7:0]			R/W
0x5C	00000000		
ACP_PACKET_BYTE_26[7:0]			R/W
0x5D	00000000		
ACP_PACKET_BYTE_27[7:0]			R/W
0x5E	00000000		

Reg	Bits	Description	
ACP_UPDATE			R/W
0x5F	00000000		
ISRC1_HEADER_BYTE_0[7:0]			R/W
0x60	00000000		
ISRC1_HEADER_BYTE_1[7:0]			R/W
0x61	00000000		
ISRC1_HEADER_BYTE_2[7:0]			R/W
0x62	00000000		
ISRC1_PACKET_BYTE_0[7:0]			R/W
0x63	00000000		
ISRC1_PACKET_BYTE_1[7:0]			R/W
0x64	00000000		
ISRC1_PACKET_BYTE_2[7:0]			R/W
0x65	00000000		
ISRC1_PACKET_BYTE_3[7:0]			R/W
0x66	00000000		
ISRC1_PACKET_BYTE_4[7:0]			R/W
0x67	00000000		
ISRC1_PACKET_BYTE_5[7:0]			R/W
0x68	00000000		
ISRC1_PACKET_BYTE_6[7:0]			R/W
0x69	00000000		
ISRC1_PACKET_BYTE_7[7:0]			R/W
0x6A	00000000		
ISRC1_PACKET_BYTE_8[7:0]			R/W
0x6B	00000000		
ISRC1_PACKET_BYTE_9[7:0]			R/W
0x6C	00000000		
ISRC1_PACKET_BYTE_10[7:0]			R/W
0x6D	00000000		
ISRC1_PACKET_BYTE_11[7:0]			R/W
0x6E	00000000		
ISRC1_PACKET_BYTE_12[7:0]			R/W
0x6F	00000000		
ISRC1_PACKET_BYTE_13[7:0]			R
0x70	00000000		
ISRC1_PACKET_BYTE_14[7:0]			R
0x71	00000000		

Reg	Bits	Description	
ISRC1_PACKET_BYTE_15[7:0]			R
0x72	00000000		
ISRC1_PACKET_BYTE_16[7:0]			R
0x73	00000000		
ISRC1_PACKET_BYTE_17[7:0]			R
0x74	00000000		
ISRC1_PACKET_BYTE_18[7:0]			R/W
0x75	00000000		
ISRC1_PACKET_BYTE_19[7:0]			R/W
0x76	00000000		
ISRC1_PACKET_BYTE_20[7:0]			R/W
0x77	00000000		
ISRC1_PACKET_BYTE_21[7:0]			R/W
0x78	00000000		
ISRC1_PACKET_BYTE_22[7:0]			R/W
0x79	00000000		
ISRC1_PACKET_BYTE_23[7:0]			R/W
0x7A	00000000		
ISRC1_PACKET_BYTE_24[7:0]			R/W
0x7B	00000000		
ISRC1_PACKET_BYTE_25[7:0]			R/W
0x7C	00000000		
ISRC1_PACKET_BYTE_26[7:0]			R/W
0x7D	00000000		
ISRC1_PACKET_BYTE_27[7:0]			R/W
0x7E	00000000		
ISRC1_UPDATE			R/W
0x7F	00000000		
ISRC2_HEADER_BYTE_0[7:0]			R/W
0x80	00000000		
ISRC2_HEADER_BYTE_1[7:0]			R/W
0x81	00000000		
ISRC2_HEADER_BYTE_2[7:0]			R/W
0x82	00000000		
ISRC2_PACKET_BYTE_0[7:0]			R/W
0x83	00000000		
ISRC2_PACKET_BYTE_1[7:0]			R/W
0x84	00000000		

Reg	Bits	Description	
		ISRC2_PACKET_BYTE_2[7:0]	R/W
0x85	00000000		
		ISRC2_PACKET_BYTE_3[7:0]	R/W
0x86	00000000		
		ISRC2_PACKET_BYTE_4[7:0]	R/W
0x87	00000000		
		ISRC2_PACKET_BYTE_5[7:0]	R/W
0x88	00000000		
		ISRC2_PACKET_BYTE_6[7:0]	R/W
0x89	00000000		
		ISRC2_PACKET_BYTE_7[7:0]	R/W
0x8A	00000000		
		ISRC2_PACKET_BYTE_8[7:0]	R/W
0x8B	00000000		
		ISRC2_PACKET_BYTE_9[7:0]	R/W
0x8C	00000000		
		ISRC2_PACKET_BYTE_10[7:0]	R/W
0x8D	00000000		
		ISRC2_PACKET_BYTE_11[7:0]	R/W
0x8E	00000000		
		ISRC2_PACKET_BYTE_12[7:0]	R/W
0x8F	00000000		
		ISRC2_PACKET_BYTE_13[7:0]	R/W
0x90	00000000		
		ISRC2_PACKET_BYTE_14[7:0]	R/W
0x91	00000000		
		ISRC2_PACKET_BYTE_15[7:0]	R/W
0x92	00000000		
		ISRC2_PACKET_BYTE_16[7:0]	R/W
0x93	00000000		
		ISRC2_PACKET_BYTE_17[7:0]	R/W
0x94	00000000		
		ISRC2_PACKET_BYTE_18[7:0]	R/W
0x95	00000000		
		ISRC2_PACKET_BYTE_19[7:0]	R/W
0x96	00000000		
		ISRC2_PACKET_BYTE_20[7:0]	R/W
0x97	00000000		

Reg	Bits	Description	
ISRC2_PACKET_BYTE_21[7:0]			R/W
0x98	00000000		
ISRC2_PACKET_BYTE_22[7:0]			R/W
0x99	00000000		
ISRC2_PACKET_BYTE_23[7:0]			R/W
0x9A	00000000		
ISRC2_PACKET_BYTE_24[7:0]			R/W
0x9B	00000000		
ISRC2_PACKET_BYTE_25[7:0]			R/W
0x9C	00000000		
ISRC2_PACKET_BYTE_26[7:0]			R/W
0x9D	00000000		
ISRC2_PACKET_BYTE_27[7:0]			R/W
0x9E	00000000		
ISRC2_UPDATE			R/W
0x9F	00000000		
GM_HEADER_BYTE_0[7:0]			R/W
0xA0	00000000		
GM_HEADER_BYTE_1[7:0]			R/W
0xA1	00000000		
GM_HEADER_BYTE_2[7:0]			R/W
0xA2	00000000		
GM_PACKET_BYTE_0[7:0]			R/W
0xA3	00000000		
GM_PACKET_BYTE_1[7:0]			R/W
0xA4	00000000		
GM_PACKET_BYTE_2[7:0]			R/W
0xA5	00000000		
GM_PACKET_BYTE_3[7:0]			R/W
0xA6	00000000		
GM_PACKET_BYTE_4[7:0]			R/W
0xA7	00000000		
GM_PACKET_BYTE_5[7:0]			R/W
0xA8	00000000		
GM_PACKET_BYTE_6[7:0]			R/W
0xA9	00000000		
GM_PACKET_BYTE_7[7:0]			R/W
0xAA	00000000		

Reg	Bits	Description	
GM_PACKET_BYTE_8[7:0]			R/W
0xAB	00000000		
GM_PACKET_BYTE_9[7:0]			R/W
0xAC	00000000		
GM_PACKET_BYTE_10[7:0]			R/W
0xAD	00000000		
GM_PACKET_BYTE_11[7:0]			R/W
0xAE	00000000		
GM_PACKET_BYTE_12[7:0]			R/W
0xAF	00000000		
GM_PACKET_BYTE_13[7:0]			R/W
0xB0	00000000		
GM_PACKET_BYTE_14[7:0]			R/W
0xB1	00000000		
GM_PACKET_BYTE_15[7:0]			R/W
0xB2	00000000		
GM_PACKET_BYTE_16[7:0]			R/W
0xB3	00000000		
GM_PACKET_BYTE_17[7:0]			R/W
0xB4	00000000		
GM_PACKET_BYTE_18[7:0]			R/W
0xB5	00000000		
GM_PACKET_BYTE_19[7:0]			R/W
0xB6	00000000		
GM_PACKET_BYTE_20[7:0]			R/W
0xB7	00000000		
GM_PACKET_BYTE_21[7:0]			R/W
0xB8	00000000		
GM_PACKET_BYTE_22[7:0]			R/W
0xB9	00000000		
GM_PACKET_BYTE_23[7:0]			R/W
0xBA	00000000		
GM_PACKET_BYTE_24[7:0]			R/W
0xBB	00000000		
GM_PACKET_BYTE_25[7:0]			R/W
0xBC	00000000		
GM_PACKET_BYTE_26[7:0]			R/W
0xBD	00000000		

Reg	Bits	Description	
GM_PACKET_BYTE_27[7:0]			R/W
0xBE	00000000		
GM_UPDATE			R/W
0xBF	00000000		
SPARE_PACKET_1_HEADER_BYTE_0[7:0]			R/W
0xC0	00000000		
SPARE_PACKET_1_HEADER_BYTE_1[7:0]			R/W
0xC1	00000000		
SPARE_PACKET_1_HEADER_BYTE_2[7:0]			R/W
0xC2	00000000		
SPARE_PACKET_1_PACKET_BYTE_0[7:0]			R/W
0xC3	00000000		
SPARE_PACKET_1_PACKET_BYTE_1[7:0]			R/W
0xC4	00000000		
SPARE_PACKET_1_PACKET_BYTE_2[7:0]			R/W
0xC5	00000000		
SPARE_PACKET_1_PACKET_BYTE_3[7:0]			R/W
0xC6	00000000		
SPARE_PACKET_1_PACKET_BYTE_4[7:0]			R/W
0xC7	00000000		
SPARE_PACKET_1_PACKET_BYTE_5[7:0]			R/W
0xC8	00000000		
SPARE_PACKET_1_PACKET_BYTE_6[7:0]			R/W
0xC9	00000000		
SPARE_PACKET_1_PACKET_BYTE_7[7:0]			R/W
0xCA	00000000		
SPARE_PACKET_1_PACKET_BYTE_8[7:0]			R/W
0xCB	00000000		
SPARE_PACKET_1_PACKET_BYTE_9[7:0]			R/W
0xCC	00000000		
SPARE_PACKET_1_PACKET_BYTE_10[7:0]			R/W
0xCD	00000000		
SPARE_PACKET_1_PACKET_BYTE_11[7:0]			R/W
0xCE	00000000		
SPARE_PACKET_1_PACKET_BYTE_12[7:0]			R/W
0xCF	00000000		
SPARE_PACKET_1_PACKET_BYTE_13[7:0]			R/W
0xD0	00000000		

Reg	Bits	Description	
		SPARE_PACKET_1_PACKET_BYTE_14[7:0]	R/W
0xD1	00000000		
		SPARE_PACKET_1_PACKET_BYTE_15[7:0]	R/W
0xD2	00000000		
		SPARE_PACKET_1_PACKET_BYTE_16[7:0]	R/W
0xD3	00000000		
		SPARE_PACKET_1_PACKET_BYTE_17[7:0]	R/W
0xD4	00000000		
		SPARE_PACKET_1_PACKET_BYTE_18[7:0]	R/W
0xD5	00000000		
		SPARE_PACKET_1_PACKET_BYTE_19[7:0]	R/W
0xD6	00000000		
		SPARE_PACKET_1_PACKET_BYTE_20[7:0]	R/W
0xD7	00000000		
		SPARE_PACKET_1_PACKET_BYTE_21[7:0]	R/W
0xD8	00000000		
		SPARE_PACKET_1_PACKET_BYTE_22[7:0]	R/W
0xD9	00000000		
		SPARE_PACKET_1_PACKET_BYTE_23[7:0]	R/W
0xDA	00000000		
		SPARE_PACKET_1_PACKET_BYTE_24[7:0]	R/W
0xDB	00000000		
		SPARE_PACKET_1_PACKET_BYTE_25[7:0]	R/W
0xDC	00000000		
		SPARE_PACKET_1_PACKET_BYTE_26[7:0]	R/W
0xDD	00000000		
		SPARE_PACKET_1_PACKET_BYTE_27[7:0]	R/W
0xDE	00000000		
		SPARE1_UPDATE	R/W
0xDF	00000000		
		SPARE_PACKET_2_HEADER_BYTE_0[7:0]	R/W
0xE0	00000000		
		SPARE_PACKET_2_HEADER_BYTE_1[7:0]	R/W
0xE1	00000000		
		SPARE_PACKET_2_HEADER_BYTE_2[7:0]	R/W
0xE2	00000000		
		SPARE_PACKET_2_PACKET_BYTE_0[7:0]	R/W
0xE3	00000000		

Reg	Bits	Description	
		SPARE_PACKET_2_PACKET_BYTE_1[7:0]	R/W
0xE4	00000000		
		SPARE_PACKET_2_PACKET_BYTE_2[7:0]	R/W
0xE5	00000000		
		SPARE_PACKET_2_PACKET_BYTE_3[7:0]	R/W
0xE6	00000000		
		SPARE_PACKET_2_PACKET_BYTE_4[7:0]	R/W
0xE7	00000000		
		SPARE_PACKET_2_PACKET_BYTE_5[7:0]	R/W
0xE8	00000000		
		SPARE_PACKET_2_PACKET_BYTE_6[7:0]	R/W
0xE9	00000000		
		SPARE_PACKET_2_PACKET_BYTE_7[7:0]	R/W
0xEA	00000000		
		SPARE_PACKET_2_PACKET_BYTE_8[7:0]	R/W
0xEB	00000000		
		SPARE_PACKET_2_PACKET_BYTE_9[7:0]	R/W
0xEC	00000000		
		SPARE_PACKET_2_PACKET_BYTE_10[7:0]	R/W
0xED	00000000		
		SPARE_PACKET_2_PACKET_BYTE_11[7:0]	R/W
0xEE	00000000		
		SPARE_PACKET_2_PACKET_BYTE_12[7:0]	R/W
0xEF	00000000		
		SPARE_PACKET_2_PACKET_BYTE_13[7:0]	R/W
0xF0	00000000		
		SPARE_PACKET_2_PACKET_BYTE_14[7:0]	R/W
0xF1	00000000		
		SPARE_PACKET_2_PACKET_BYTE_15[7:0]	R/W
0xF2	00000000		
		SPARE_PACKET_2_PACKET_BYTE_16[7:0]	R/W
0xF3	00000000		
		SPARE_PACKET_2_PACKET_BYTE_17[7:0]	R/W
0xF4	00000000		
		SPARE_PACKET_2_PACKET_BYTE_18[7:0]	R/W
0xF5	00000000		
		SPARE_PACKET_2_PACKET_BYTE_19[7:0]	R/W
0xF6	00000000		

Reg	Bits	Description	
		SPARE_PACKET_2_PACKET_BYTE_20[7:0]	R/W
0xF7	00000000		
		SPARE_PACKET_2_PACKET_BYTE_21[7:0]	R/W
0xF8	00000000		
		SPARE_PACKET_2_PACKET_BYTE_22[7:0]	R/W
0xF9	00000000		
		SPARE_PACKET_2_PACKET_BYTE_23[7:0]	R/W
0xFA	00000000		
		SPARE_PACKET_2_PACKET_BYTE_24[7:0]	R/W
0xFB	00000000		
		SPARE_PACKET_2_PACKET_BYTE_25[7:0]	R/W
0xFC	00000000		
		SPARE_PACKET_2_PACKET_BYTE_26[7:0]	R/W
0xFD	00000000		
		SPARE_PACKET_2_PACKET_BYTE_27[7:0]	R/W
0xFE	00000000		
		SPARE2_UPDATE	R/W
0xFF	00000000		

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