Gain Settings in the ADV7844/ADV7842:

The purpose of this document is to give a brief top level over view of gain control in the ADV7844 and ADV7842 products. It shows in detail how gain levels are calculated and how to establish appropriate manual gain settings by test.

The gain factor in the CP core of the ADV7844/ADV7842 can be set by one of three means:

- Automatic Gain Control (AGC) block (Only when receiving embedded sync signals)
- Hardcoded RTL values
- I2C Controlled Manual settings

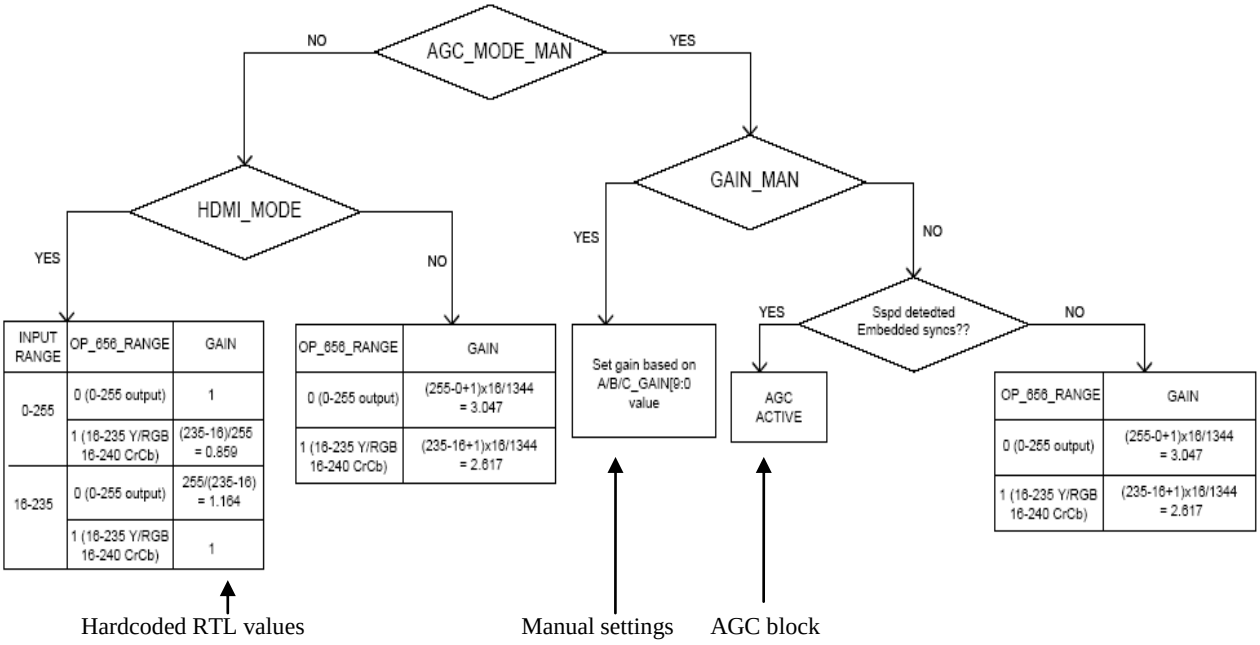

Figure 1: CP Gain Overview

Automatic Gain Control

The AGC block is only active when all of the following conditions occur:

- AGC_MODE_MAN is set to 1'b1
- GAIN_MAN is set to 1'b0
- Embedded syncs are detected on the input.

The AGC of the CP takes measurements of the signal on channel A. The AGC measures the depth of this synchronization pulse and compares it against a target value. It then determines an appropriate gain value for all three channels.

Hard Coded RTL Values

Hard coded RTL values have being calculated to apply the desired theoretical gain. They are fixed and cannot be adjusted. We need to consider two cases, HDMI and Analog Inputs.

HDMI Input

Hardcoded RTL values should always be used in HDMI mode. When processing an HDMI input this can be ensured by setting AGC_MODE_MAN to 1'b0. The gain applied is based on the desired output quantization range, as set by the bit "OP_656_RANGE" and the output colour space, as set by "RGB_OUT".

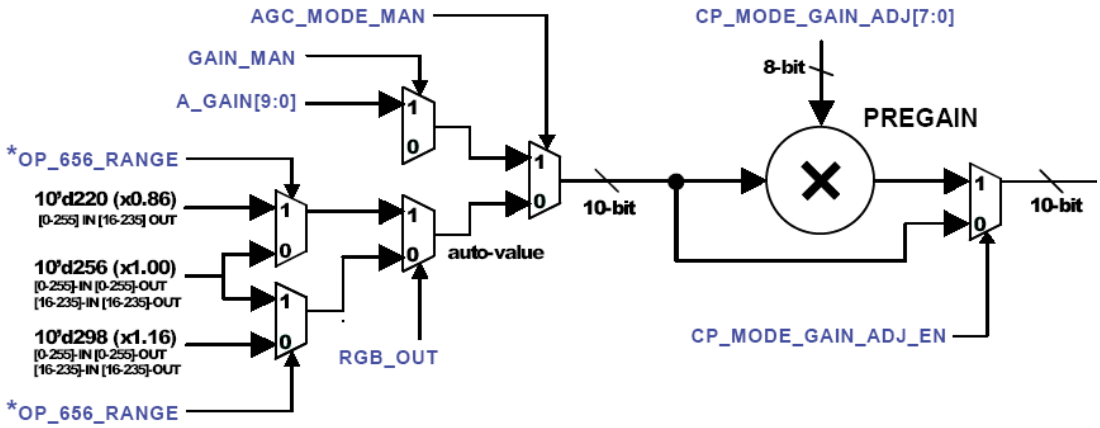

Figure 2: CP Gain Data Path for HDMI Input Mode

If the input range is the same as the output range the data is not gained and is just multiplied by unity. If the data range is being scaled from limited to full range or vice versa a gain factor of 1.16 or 0.86 will be applied as shown in Table 1. In HDMI mode the pre gain block should always be bypassed by setting GAIN_ADJ_EN to 1'b0.

Input Range	Output Range	Gain Applied
Full Range (0-255)	Full Range (0-255)	1
Full Range (0-255)	Limited Range (16-235)	(235-16)/(255) = 0.859
Limited Range (16-235)	Full Range (0-255)	(255)/ (235-16) = 1.164
Limited Range (16-235)	Limited Range (16-235)	1

Table 1: Gain Applied Automatically in HDMI mode (Based on Output Range)

Analog Input

There is no “input range equivalent” to HDMI mode since we are discussing analog input video. The active video range of the analog input video can be assumed to be 700mV.

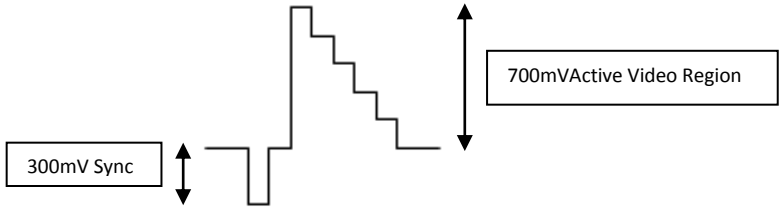

Figure 3: Nominal Analog Video Input

The active video content of the analog input will only fill a certain percentage of the total ADC range, otherwise we would lose content due to positive and/or negative clipping. We need to examine the full AFE path and CP gain path to explain the hardcoded RTL values. The objective being to take the 700mV signal at the analog input pin and map this to the entire 12 bit (4096 codes) digital range.

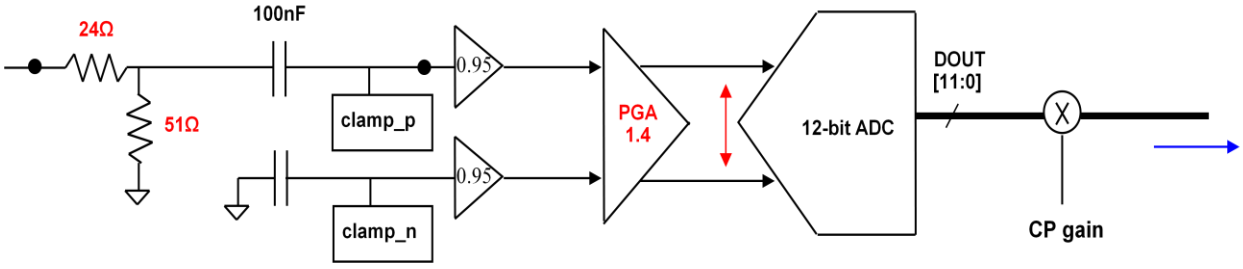

Figure 4: AFE

Resistor Divider Network: The 24/51 Ohm voltage divider passes 68% of Vin and therefore has a gain of 0.68

Input Buffer: The input buffer has a gain of 0.95

Programmable Gain Amplifier: The programmable gain amplifier has a variable gain, but in this case we will take the maximum value of 1.4

ADC: The ADC is a 12 bit, 1.4V range ADC

CP Gain: To compensate for signal attenuation/gain in the analog front end (AFE) a pregain block is provided in the CP path. (See Figure: 5). In analog mode the pregain block will enabled. Therefore the effective CP gain is the manual/hardcoded/AGC gain value multiplied by the pregain block gain.

Equation 1: *Effective CP Gain = (CP Gain Setting)(Pregain Block Gain)**

**Assuming the pregain block is enabled.*

Therefore a 700mV signal before the resistor divider will be affected as follows:

(700mV)(0.68)(0.95)(1.4) = 633mV = 45.22% of 1.4V ADC Range = 1,852 of 4096 codes.

We need to scale this digital data by gaining in order to fill the entire output range as desired.

(1852)(Gain) = 4096 => Gain = 2.21

The effective gain we want is 2.21, but since in analog modes the pregain block is enabled we need to compensate for this as in equation 1. The default value of the pregain block is 0.718. This gives a required CP gain setting of 3.07.

When outputting limited range data we need to apply a different gaining factor as we are not using the entire data output range. Unchanged we are still only using 45.22% of our 12 bit ADC. In an eight bit domain the values in limited range are from 16 to 235, or 220 possible codes. Translating to a twelve bit domain gives us a range of 3,520 codes. As before:

(1852)(Gain) = 3520 => Gain = 1.9 Again multiplying by 0.718 this gives a required CP gain setting of 2.6

Manual Gain Setting

The recommended mode of gaining is to use the manual setting via I2C registers. The manual settings are active when:

- AGC_MODE_MAN is set to 1'b1
- GAIN_MAN is set to 1'b1

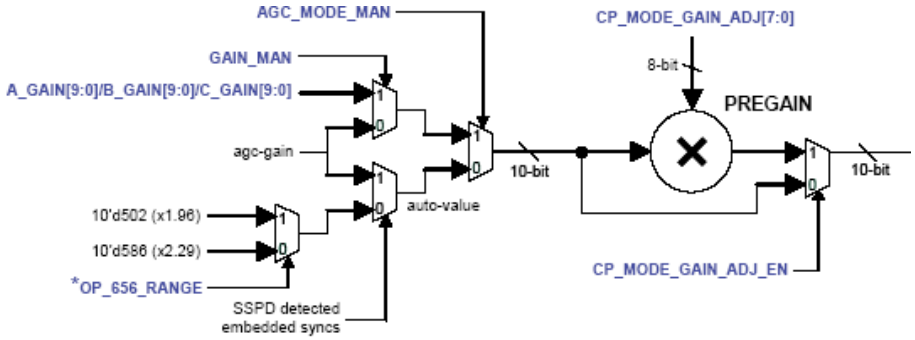

Figure 5: CP Gain Data Path for Analog Input Mode

As shown above it is important to note that the optimal manual gain settings will be dependent on the output range selected. Therefore it is advised that scripts and recommended settings documents should contain two sets of manual gain settings.

The pregain block in the CP core and PGA in the AFE are both configured in analog mode scripts to the desired setting and should not be adjusted. Similarly the recommended external hardware (voltage divider) on the analog inputs should always be used.

Experimental Measurement of Optimum Manual Gain Settings

Recommended methods & steps to measure the required manual gain based on an ADI evaluation platform are:

(1) Quantify the exact expected digital data levels from the system by connecting the source generator to the Astro VA-1809A analyser. Using the 'Colorimetry' function and suitable patterns such as 'TV Bar100' and 'Ramp', record the levels for both limited and full range HDMI inputs.

	White	Yellow	Cyan	Green	Magenta	Red	Blue	Black
R	255	255	0	0	255	255	0	0
G	255	255	255	255	0	0	0	0
B	255	0	255	0	255	0	255	0
$Y_{(709)}$	255	237	201	182	73	54	18	0
$Cb_{(709)}$	128	0	157	29	226	98	255	128
$Cr_{(709)}$	128	139	0	12	243	255	116	128
$Y_{(601)}$	255	226	179	150	105	76	29	0
$Cb_{(601)}$	128	0	171	43	212	84	255	128
$Cr_{(601)}$	128	148	0	21	234	255	107	128

(Note the above Y/Cb/Cr values may vary slightly from source to source)

Note that the 'Ramp' pattern (from the Quantum 882 generators) has a number of pixels at the start and end of a line with identical values. For the pattern below from left to right 0/16 and 235/255 repeat for approx 4% of the line width at the start and end of the line, depending on the output range.

This is important to note as it may otherwise have being interpreted as output saturation from the ADV DUT.

Once the expected output levels are known and testing is underway the following methods can be used to confirm the output levels are correct.

(1) Pass the data out through a HDMI TX and examine on the Astro VA-1809A as before.

(2) Use an analyser tool such as Xilinx Chipscope to examine the digital data entering the FPGA from the DUT.

(3) Pass the data out through a Video encoder/DAC and measure the output levels on an oscilloscope.

Methods (1) & (2) above are much more precise than method (3) and are recommended.