ANALOG DEVICES

Preliminary Recommended Settings Document

ADV7180

Preliminary Register Settings Recommendations

Revision Pr.A

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INTRODUCTION

This document describes how to configure the ADV7180 video decoder for basic and supplementary modes of operation. This document must be used in conjunction with the latest ADV7180 datasheet and the latest ADV7180 configuration script. The datasheet is available on the ADV7180 product page on the Analog Devices website. The ADV7180 product page also contains a link to the ADV7180 design support files website. The latest configuration scripts for all the ADV7180 models are available on the ADV7180 design support files website.

The document is structured as follows:

Section 1 outlines how I^2C writes are documented throughout this document.

Section 2 outlines the required writes to ensure the correct operation of the ADV7180.

Sections 3 and 4 outline the recommended writes to configure the ADV7180 for enhanced or additional modes of operation.

Section 5 and 6 contain a collection of example configuration scripts for all the 180 models.

LEGAL TERMS AND CONDITIONS

REVISION HISTORY

02/14—Revision Pr.A: Initial Version

1 DESCRIPTION OF I²C WRITES

Before proceeding please read the 'MPU Port Description' and 'Register Access' sections of the ADV7180 datasheet.

A number of script tables are provided in this document. These script tables detail the I²C register writes that are needed to configure the ADV7180. Each row of a script table details one I²C write to the ADV7180 followed by a description. Each I²C write to the ADV7180 consists of the following three groups of two hexadecimal numbers:

- The first two hexadecimal numbers state the slave address of the ADV7180 for I²C writing . This can either be 0x40 or 0x42 (see 'MPU Port Description' section of the ADV7180 datasheet for more information). Throughout this document it is assumed that the slave address of the ADV7180 for I²C writing is set to 0x42.
- The second two hexadecimal numbers state the register in the ADV7180 that is being written to.
- The last two hexadecimal numbers state what value is being written to the register.

1.1 ADI REQUIRED WRTIES

A number of I²C writes in the script tables in the document are labeled as 'ADI Required Write'. ADI required writes must be written to the ADV7180 to ensure the correct operation of the part.

1.2 EXAMPLE SCRIPT TABLE

This section provides an example of a script table followed by a description.

The writes below force the ADV7180 into free-run mode. (See Section 3.3 for more information.)

User Map	
42 0C 37	Force Free-Run Mode
42 02 XX	Force Video Standard
42 0D YY	Set Color Output

In this example:

- Each row consists of an I²C write.

  The I²C writes should be performed in the order shown in the table. The I²C write on the top row should be performed first, the I²C write on the second row should be performed next, and so on.
- **User Map** at the top of the table indicates that before the first write, the ADV7180 is in the User Map. The 'Register Access' section of the ADV7180 datasheet explains how to access the User Map and the 'Interrupt and VDP map' of the ADV7180.
- The first row indicates that the value 0x37 is being written to register 0x0C in the ADV7180.
  - The device address 0x42 indicates that the ADV7180 is being written to.
  - The register address 0x0C indicates that register 0x0C within the ADV7180 is being written to.
  - The value 0x37 indicates that the value 0x37 is being written to register 0x0C within the ADV7180.
- The comment on the right of the first row indicates that this write forces the ADV7180 into free-run mode.
- The second row shows the value XX being written to register 0x02 in the ADV7180. This write forces the video standard that is output in free-run mode.
  - Note the XX value indicates that many different values are possible. The possible values are indicated in a separate table.
- Similarly the third row shows the value of YY being written to register 0x0D in the ADV7180. This write sets the screen color that is output in free-run mode.
  - Note the YY value indicates that many different values are possible. The possible values are indicated in a separate table.

2 SETTING UP THE ADV7180

2.1 INPUT CONFIGURATION

The following two writes need to be performed at the start of every ADV7180 script.

User Map	
42 00 XX	Set VID_SEL and INSEL [1]
42 14 30	ADI Required Write; Reset Clamp Circuitry

[1] The XX value indicates that many different values are possible.

Resister 0x00 in the User Map of the ADV7180 contains two controls, the VID_SEL and the INSEL controls.

- The VID_SEL bits are available in User Map register 0x00 bits[7:4]. The VID_SEL bits are described in the 'Video Standard Selection' section of the ADV7180 datasheet.
- The INSEL bits are available in User Map register 0x00 bits[3:0]. The INSEL control is described in the 'Input Configuration' section of the ADV7180 datasheet.

After the 0x00 register is set, a write is needed to reset the clamp circuitry. This write needs to be performed directly after an INSEL write. This write resets the clamp circuitry in the ADV7180 and improves the lock time of the ADV7180.

2.2 ENABLE SFL OUTPUT (CVBS AND YC INPUTS ONLY)

This write only applies to CVBS inputs and YC inputs (i.e. this does not apply to YPbPr inputs). The following write is needed to enable the carrier frequency lock (SFL) synchronization output pin.

User Map	
42 04 57	Enable SFL Output

2.3 SELECT CHROMA SHAPING FILTER MODE (CVBS ONLY)

This write only applies to CVBS inputs (i.e. this does not apply to YC or YPbPr inputs). The following write sets the chroma shaping filter response. See the 'Chroma Filter' section of the ADV7180 datasheet for more information.

User Map	
42 17 41	Select SH1 Chroma Shaping Filter

2.4 ENABLE NEWAVMODE

The following write is needed to enable the NEWAVMODE. In NEWAVMODE the start of active video (SAV) and end of active video (EAV) are generated internally by the ADV7180. These SAV and EAV codes are optimized for Analog Devices' video encoders.

User Map	
42 31 02	Enable NEWAVMODE

2.5 WINDOWING FUNCTIONS

The following writes optimize the windowing functions that the ADV7180 uses to detect the color carrier and blank level of the incoming analog video signal. The following three writes set the color kill threshold; enable manual windowing; set the position and length of the blank level window; and set the position and length of the color bust window.

User Map	
42 3D A2	ADI Required Write (optimize windowing function Step 1)
42 3E 6A	ADI Required Write (optimize windowing function Step 2)
42 3F A0	ADI Required Write (optimize windowing function Step3)

2.6 ENABLE ADC

To enable the ADC of the ADV7180, the following three writes must be performed in the order below.

User Map	
42 0E 80	ADI Required Write (Enable ADC step 1)
42 55 81	ADI Required Write (Enable ADC step 2)
42 0E 00	ADI Required Write (Enable ADC step 3)

2.7 YC MODE MANDATORY WRITE (YC INPUTS ONLY)

The following write is needed in order for the ADV7180 to process YC inputs correctly. This write is not needed for CVBS or YPbPr inputs.

User Map	
42 58 04	ADI Required Write (YC mode mandatory write)

2.8 ANALOG FRONT END IBIAS SETTINGS FOR CVBS MODE

The following write influences the bias current for the analog front end (AFE) of the ADV7180 in CVBS mode.

This is the latest recommended write for new product designs to offer optimal performance. This write is not required for existing designs which have already been quality approved and released.

This write should not be performed for S-Video(YC) or component (YPbPr) inputs.

User Map	
42 52 0B	Original AFE I_{BIAS} Setting for CVBS mode
42 52 0D	Recommended AFE I_{BIAS} Setting for CVBS mode

3 FEATURES OF THE ADV7180

This section describes some of the supplementary modes of operation of the ADV7180.

3.1 FAST SWITCH MODE

Fast switch mode allows the ADV7180 to lock to CVBS signals more quickly. However there are some disadvantages to using fast switch mode. In fast switch mode:

- The ADV7180 will not be able to autodetect which type of CVBS source has been connected (PAL-I, NTSC-M, etc). Therefore, the user must manually program which type of CVBS source is connected to the analog input of the ADV7180. This is done by setting the VID_SEL bits. See the 'Video Standard Selection' section of the ADV7180 datasheet for more information.
- The ADV7180 will not be as robust to poor sources.
- The ADV7180 will not be able to process Rovi/Macrovision sources.

The following script is an example of how to place the ADV7180 into fast switch mode. It is assumed that an NTSC-M CVBS source has been connected to Ain1. The writes to place the ADV7180 into fast switch mode should be made in the order below.

User Map	
42 00 50	INSEL: CVBS in on Ain 1, VID_SEL: force standard to NTSC-M. Change this to suit application.[1]
42 14 30	Reset Clamping Circuitry
42 0F 40	Reacquire input signal (TRAQ)
42 01 80	Disable HSync and Vsync processor
42 19 B1	Disable Macrovision/Rovi Detection
42 2C 12	Turn Peak White Algorithm Off.
42 31 02	Enable NEWAVMODE
42 37 81	Set HS & VS polarity active high
42 51 89	FSCLE enabled (lock status set by HS & SFL), CIL (number of stable lines needed for locked status =2), COL (number of unstable lines needed for unlocked status =2
42 3A 16	Power Down Mux_1 and Mux_2
42 3D A2	ADI Required Write (optimize windowing function Step 1)
42 3E 6A	ADI Required Write (optimize windowing function Step 2)
42 3F A0	ADI Required Write (optimize windowing function Step 3)
42 51 9B	FSCLE enabled (lock status set by HS & SFL), CIL (number of stable lines needed for locked status =10), COL (number of unstable lines needed for unlocked status =10).
42 0E 80	ADI Required Write
42 B6 0C	Set manual enables for AGC & clamp loop speeds

42 BE C0	Adjust speed of digital AGC loop
42 C0 C0	Adjust speed of digital clamp loop
42 D1 B9	Disable Field output signal generator.
42 D6 6D	ADI Required Write (reduce robustness of HSYNC slicer detector)
42 D9 44	ADI Required Write (reduce robustness to non-standard field lengths)
42 0E 80	ADI Required Write (Enable ADC step 1)
42 55 81	ADI Required Write (Enable ADC step 2)
42 0E 00	ADI Required Write (Enable ADC step 3)
42 52 0D	Set AFE I_{BIAS} Setting

[1] In this example it is assumed that an NTSC-M CVBS source has been connected to Ain1. In order to receive other video formats on other Ain inputs pins, register 0x00 needs to be modified. See Sections 2.1 of this document, as well as the 'Video Standard Selection' and 'Input Configuration' sections of the ADV7180 datasheet, for more information.

3.2 OSCILLATOR CLOCK INPUT

The standard ADV7180 scripts assume that the ADV7180 is being clocked by an external 28.63636 MHz crystal. With the standard scripts the ADV7180 outputs 1.8 V between the XTAL and XTAL1 pins. However, if an oscillator is used an additional software write is needed to disable this voltage between the XTAL and XTAL1 pins.

3.2.1 Oscillator Specifications

An oscillator with an output of 1.8 Vpp must be used. The oscillator must output a 28.63636 MHz clock with a tolerance of +/- 50ppm.

3.2.2 Physical Setup

Connect the output of the oscillator to the XTAL pin of the ADV7180. Leave the XTAL1 pin of the ADV7180 floating.

3.2.3 Software Write

The following write is needed to disable the voltage output on the XTAL1 pin and allow the ADV7180 to be clocked by a 28.63636 MHz oscillator.

User Map	
42 13 04	Enable Oscillator Clock Input

3.2.4 Note on Software Write

The ADV7180 datasheet states that register 0x13 is a read only register (status register 3). Actually two registers share the register address 0x13. When a read is performed on register 0x13, Status Register 3 (which is read only) data is read. When a write command is performed on register 0x13, an internal control register (which is write only) is written to.

3.3 FREE-RUN MODE

Free-run mode is a useful function that allows the ADV7180 to output a colored screen (for example, a blue screen). A valid source must still be connected to the ADV7180 in order for free-run mode to work correctly.

The writes below force the ADV7180 into free-run mode. The writes must be made in the order shown below and should be performed after an Analog Devices' recommended script.

User Map	
42 0C 37	Force Free-Run mode
42 00 XX	Force Video Standard[1]
42 0D YY	Set Color Output[2]

[1] The 'XX' term indicates that a number of different options are available to the user. These options are discussed in Section 3.3.1.

[2] The 'YY' term indicates that a number of different options are available to the user. These options are discussed in Section 3.3.2.

3.3.1 Free-Run Video Output Standard

Under normal conditions, if the free-run mode is forced then the ADV7180 outputs in the format of video input. For example, if an NTSC source was connected to the ADV7180 before the ADV7180 was programmed into free-run mode, then the ADV7180 will output in a 480i format in free-run mode.

The writes to the VID_SEL bits (User Map register 0x00 bits[7:4]) allow the user to have control over which video format is output in free-run mode. See 'Video Standard Selection' section of the ADV7180 datasheet for more information.

The table below gives examples for two standards that can force a 576i or 480i output in free-run mode.

User Map	Output Video Standard
42 02 80	Force standard to PAL (576i output)
42 02 50	Force standard to NTSC-M (480i output)

A full list of VID_SEL standards can be found in the 'Video Standard Selection' section of the ADV7180 datasheet.

3.3.2 Free-Run Color Output

The DEF_C[7:0] bits control the color of the screen that is output in free run mode (User Map , register 0x0D, bits[7:0]).

The DEF_C[7:4] bits set the red chroma output and DEF_C[3:0] set the blue chroma output. The table below gives examples of different colors that the ADV7180 can output in free-run mode. See 'Color Controls' section of the ADV7180 datasheet for more information.

DEF_C **User Map Register 0x0D**	**Color Output in Free-Run Mode**
0x7C (default)	Dark Blue
0x00	Green
0x0F	Light Blue
0xF0	Red
0xFF	Purple

3.4 DIGITAL OUTPUT FORMAT

By default, the ADV7180 outputs digital video in an ITU-R BT656-3 standard. The user can select the ADV7180 output digital video by toggling the BT.656-4 bit (User Map, register 0x04 bit[7]).

- When the BT.656-4 bit is 0 (default), the ADV7180 outputs digital video according to the ITU-R BT.656-3 specification.
- When the BT.656-4 bit is 1, the ADV7180 outputs digital video according to the ITU-R BT.656-4 specification.

4 Example of How to Program ADV7180 to Output an Interrupt on INTRQ Pin

The INTRQ interrupt pin on the ADV7180 can be programmed to change state under a number of different conditions. This can be a useful tool to detect issues with the inputted analog video.

The INTRQ pin can be programmed to drive high or low when activated. It can drive high/low for a set period of time or can drive high/low until the interrupt is cleared. See the 'Interrupt/VDP Map Descriptions' table in the ADV7180 datasheet for more information.

The following example describes how to set the interrupt pin to go from a high state to a low state when the ADV7180 has locked or lost lock to the inputted video. The interrupt will remain low until cleared.

4.1 PROGRAMMING THE INTERRUPT

These writes should be performed in the order listed below, after an ADI recommended script has been performed.

User Map	
42 0E 20	Enter Interrupt/VDP Map
42 40 D5	Activate manual interrupts. INTRQ pin drives low when active and remains low until interrupt is cleared
42 44 03	Enable SD_LOCK and SD_UNLOCK interrupts
42 43 03	Clear SD_LOCK and SD_UNLOCK interrupts <step 1>
42 43 00	Clear SD_LOCK and SD_UNLOCK interrupts <step 2>
42 0E 00	Re-enter User Map

The ADV7180 has now been programmed to drive the INTRQ pin high under normal operation. When the ADV7180 locked to a video source or loses video lock, the INTRQ pin will drive low and remain low until the interrupt has been cleared.

4.2 CLEARING THE INTERRUPT

The writes listed below should be performed after the interrupt is triggered (i.e. INTRQ pin drives low).

User Map	
42 0E 20	Enter Interrupt/VDP Map
42 43 03	Clear SD_LOCK and SD_UNLOCK interrupts <step 1>
42 43 00	Clear SD_LOCK and SD_UNLOCK interrupts <step 2>
42 0E 00	Re-enter User Map

The interrupt is now untriggered (i.e. INTRQ pin drives high). The INTRQ will not drive low until the ADV7180 has locked or lost lock to a video source.

4.3 NOTE ON LOST_LOCK AND IN_LOCK BITS

The LOST_LOCK (User Map, register 0x10[bit 1]) and IN_LOCK bits (User Map, register 0x10[bit 0]) can be used to determine if a lock or loss of lock event has occurred.

Note: In order for the LOST_LOCK and IN_LOCK bits to work correctly the ADV7180 must be programmed with an Analog Devices recommended script.

The table below shows the operation of the LOST_LOCK and IN_LOCK bits as the active video source is connected or disconnected.

Source Connected/Disconnected	**LOST_LOCK Bit**	**IN_LOCK Bit**
When the video source is connected to the ADV7180/ ADV7180	0	1
When the video source is disconnected from the ADV7180/ ADV7180	1	0
When the video source is reconnected to the ADV7180/ ADV7180(the first read of register 0x10 after reconnection)	1	1
Second and sequent reads of register 0x10 after the video source is reconnected	0	1

See the "Global Status Register" section of the ADV7180 datasheet for more information.

5 EXAMPLE SCRIPTS FOR THE ADV7180 32 LEAD AND 40 LEAD MODELS

The following are example scripts for the ADV7180 32 lead LFCSP and 40 lead LFCSP models.

5.1 CVBS AUTODETECT SCRIPT

:Autodetect CVBS In, YPrPb Out:

42 00 00 ; INSEL = CVBS in on AIn 1

42 14 30 ; Reset Clamping Circuitry

42 04 57 ; Enable SFL

42 17 41 ; select SH1

42 31 02 ; Clears NEWAV_MODE, SAV/EAV to suit ADV video encoders

42 3D A2 ; MWE Enable Manual Window, Colour Kill Threshold to 2

42 3E 6A ; BLM optimisation

42 3F A0 ; BGB

42 0E 80 ; ADI Required Write

42 55 81 ; ADI Required Write

42 0E 00 ; ADI Required Write

42 52 0D ; ADI Required Writes [ADV7180 writes finished]

End

5.2 CVBS FAST INPUT SWITCHING (NTSC)

:NTSC-M In, Fast Switching :

42 00 50 ; INSEL = CVBS in on AIn 1, force standard to NTSC-M. Change this to suit application.

42 14 30 ; Reset Clamping Circuitry

42 0F 40 ; TRAQ

42 01 80 ; disable HSync pll, VSync processor

42 19 B1 ; Mv robustnesss bit

42 2C 12 ; Use sync based AGC

42 31 02 ; Clears NEWAV_MODE AV_MODE,SAV/EAV to suit ADV encoders

42 37 81 ; HS polarity

42 51 89 ; FSCLE enabled, CIL,COL

42 3A 16 ; Power down U and V ADC's

42 3D A2 ; MWE Enable Manual Window, Colour Kill Threshold to 2

42 3E 6A ; BLM optimisation

42 3F A0 ; BGB

42 51 9B ; ADI Required Write

42 0E 85 ; ADI Required Write

42 B6 0C ; manual enables for agc & clamp loop speeds

42 BE C0 ; speed of digital agc loop

42 C0 C0 ; speed of digital clamp loop

42 D1 B9 ; Disable always flip field ID bit, Disable VCR FIELD filtering for switching application

42 D6 6D ; ADI Required Write

42 D9 44 ; Toggle LSF set to zero

42 0E 80 ; ADI Required Write

42 55 81 ; ADI Required Write

42 0E 00 ; ADI Required Write

42 52 0D ; ADI Required Writes [ADV7180 writes finished]

End

5.3 CVBS FAST INPUT SWITCHING (PAL)

:PALM In, Fast Switching :

42 00 B0 ; INSEL = CVBS in on AIn 1, force standard to PAL-M. Change this to suit application.

42 14 30 ; Reset Clamping Circuitry

42 0F 40 ; TRAQ

42 01 80 ; disable Hsync pll, Vsync processor

42 19 B1 ; Mv robustnesss bit

42 2C 12 ; Use sync based AGC

42 31 02 ; Clears NEWAV_MODE AV_MODE,SAV/EAV to suit ADV encoders

42 37 81 ; HS polarity

42 51 89 ; FSCLE enabled, CIL,COL

42 3A 16 ; Power down U and V ADC's

42 3D A2 ; MWE Enable Manual Window, Colour Kill Threshold to 2

42 3E 6A ; BLM optimisation

42 3F A0 ; BGB

42 51 9B ; ADI Required Write

42 0E 85 ; ADI Required Write

42 B6 0C ; manual enables for agc & clamp loop speeds

42 BE C0 ; speed of digital agc loop

42 C0 C0 ; speed of digital clamp loop

42 D1 B9 ; Disable always flip field ID bit, Disable VCR FIELD filtering for switching application

42 D6 6D ; ADI Required Write

42 D9 44 ; Toggle LSF set to zero

42 0E 80 ; ADI Required Write

42 55 81 ; ADI Required Write

42 0E 00 ; ADI Required Write

42 52 0D ; ADI Required Writes [ADV7180 writes finished]

End

5.4 YC AUTODETECT

:YC In, YPrPb Out:

42 00 06 ; Insel=YC, y=Ain1, C=Ain2 [ADV7180 32 lead & 40 lead]

42 14 30 ; Reset Clamping Circuitry

42 04 57 ; Enable SFL

42 31 02 ; Clears NEWAV_MODE, SAV/EAV to suit ADV video encoders

42 3D A2 ; MWE Enable Manual Window, Colour Kill Threshold to 2

42 3E 6A ; BLM optimisation

42 3F A0 ; BGB

42 58 04 ; YC@2xOS

42 0E 80 ; ADI Required Write

42 55 81 ; ADI Required Write

42 0E 00 ; ADI Required Write [ADV7180 writes begin]

End

5.5 YPRPB AUTODETECT

:YPrPb In, YPrPb Out:

42 00 09 ; INSEL = YPrPb, Y=Ain1, Pr=Ain2, Pb=Ain3 [ADV7180 32 lead & 40 lead]

42 14 30 ; Reset Clamping Circuitry

42 31 02 ; Clears NEWAV_MODE, SAV/EAV to suit ADV video encoders

42 3D A2 ; MWE Enable Manual Window

42 3E 6A ; BLM optimisation

42 3F A0 ; ADI Required Write

42 0E 80 ; ADI Required Write

42 55 81 ; ADI Required Write

42 0E 00 ; ADI Required Write [ADV7180 writes finished]

End

6 EXAMPLE SCRIPTS FOR THE ADV7180 48 LEAD AND 64 LEAD MODELS

The following are example scripts for the ADV7180 48-lead LQFP and 64-lead LQFP.

6.1 CVBS AUTODETECT SCRIPT

:Autodetect CVBS In, YPrPb Out:

42 00 01 ; INSEL = CVBS in on Ain 2

42 14 30 ; Reset Clamping Circuitry

42 04 57 ; Enable SFL

42 17 41 ; select SH1

42 31 02 ; Clears NEWAV_MODE, SAV/EAV to suit ADV video encoders

42 3D A2 ; MWE Enable Manual Window, Colour Kill Threshold to 2

42 3E 6A ; BLM optimisation

42 3F A0 ; BGB

42 0E 80 ; ADI Required Write

42 55 81 ; ADI Required Write

42 0E 00 ; ADI Required Write

42 52 0D ; ADI Required Writes [ADV7180 writes finished]

End

6.2 CVBS FAST INPUT SWITCHING (NTSC)

:NTSC-M In, Fast Switching :

42 00 51 ; INSEL = CVBS in on AIn 2, force standard to NTSC-M. Change this to suit application.

42 14 30 ; Reset Clamping Circuitry

42 0F 40 ; TRAQ

42 01 80 ; disable HSync pll, VSync processor

42 19 B1 ; Mv robustnesss bit

42 2C 12 ; Use sync based AGC

42 31 02 ; Clears NEWAV_MODE AV_MODE,SAV/EAV to suit ADV encoders

42 37 81 ; HS polarity

42 51 89 ; FSCLE enabled, CIL,COL

42 3A 16 ; Power down U and V ADC's

42 3D A2 ; MWE Enable Manual Window, Colour Kill Threshold to 2

42 3E 6A ; BLM optimisation

42 3F A0 ; BGB

42 51 9B ; ADI Required Write

42 0E 85 ; ADI Required Write

42 B6 0C ; manual enables for agc & clamp loop speeds

42 BE C0 ; speed of digital agc loop

42 C0 C0 ; speed of digital clamp loop

42 D1 B9 ; Disable always flip field ID bit, Disable VCR FIELD filtering for switching application

42 D6 6D ; ADI Required Write

42 D9 44 ; Toggle LSF set to zero

42 0E 80 ; ADI Required Write

42 55 81 ; ADI Required Write

42 0E 00 ; ADI Required Write

42 52 0D ; ADI Required Writes [ADV7180 writes finished]

End

6.3 CVBS FAST INPUT SWITCHING (PAL)

:PALM In, Fast Switching :

42 00 B1 ; INSEL = CVBS in on AIn 2, force standard to PAL-M. Change this to suit application.

42 14 30 ; Reset Clamping Circuitry

42 0F 40 ; TRAQ

42 01 80 ; disable Hsync pll, Vsync processor

42 19 B1 ; Mv robustnesss bit

42 2C 12 ; Use sync based AGC

42 31 02 ; Clears NEWAV_MODE AV_MODE,SAV/EAV to suit ADV encoders

42 37 81 ; HS polarity

42 51 89 ; FSCLE enabled, CIL,COL

42 3A 16 ; Power down U and V ADC's

42 3D A2 ; MWE Enable Manual Window, Colour Kill Threshold to 2

42 3E 6A ; BLM optimisation

42 3F A0 ; BGB

42 51 9B ; ADI Required Write

42 0E 85 ; ADI Required Write

42 B6 0C ; manual enables for agc & clamp loop speeds

42 BE C0 ; speed of digital agc loop

42 C0 C0 ; speed of digital clamp loop

42 D1 B9 ; Disable always flip field ID bit, Disable VCR FIELD filtering for switching application

42 D6 6D ; ADI Required Write

42 D9 44 ; Toggle LSF set to zero

42 0E 80 ; ADI Required Write

42 55 81 ; ADI Required Write

42 0E 00 ; ADI Required Write

42 52 0D ; ADI Required Writes [ADV7180 writes finished]

End

6.4 YC AUTODETECT

:YC In, YPrPb Out:

42 00 08 ; Insel=YC, y=Ain3, C=Ain6 [ADV7180 48 lead & 64 lead]

42 14 30 ; Reset Clamping Circuitry

42 04 57 ; Enable SFL

42 31 02 ; Clears NEWAV_MODE, SAV/EAV to suit ADV video encoders

42 3D A2 ; MWE Enable Manual Window, Colour Kill Threshold to 2

42 3E 6A ; BLM optimisation

42 3F A0 ; BGB

42 58 04 ; YC@2xOS

42 0E 80 ; ADI Required Write

42 55 81 ; ADI Required Write

42 0E 00 ; ADI Required Write [ADV7180 writes begin]

End

6.5 YPRPB AUTODETECT

:YPrPb In, YPrPb Out:

42 00 09 ; INSEL = YPrPb, Y=Ain1, Pr=Ain4, Pb=Ain5 [ADV7180 48 lead & 64 lead]

42 14 30 ; Reset Clamping Circuitry

42 31 02 ; Clears NEWAV_MODE, SAV/EAV to suit ADV video encoders

42 3D A2 ; MWE Enable Manual Window

42 3E 6A ; BLM optimisation

42 3F A0 ; ADI Required Write

42 0E 80 ; ADI Required Write

42 55 81 ; ADI Required Write

42 0E 00 ; ADI Required Write [ADV7180 writes finished]

End

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).