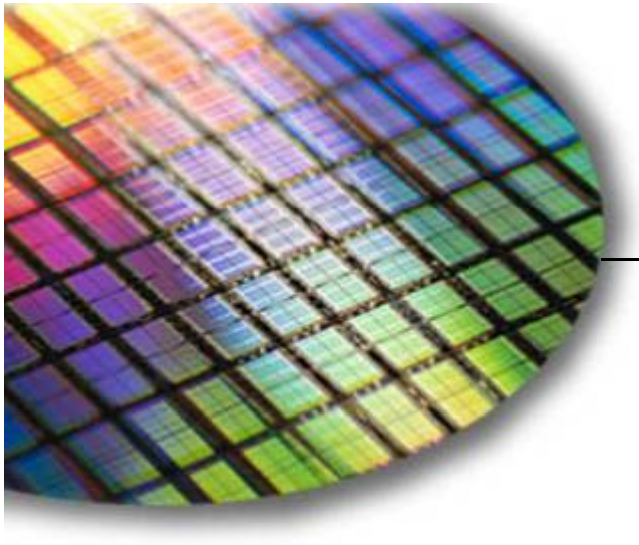

The World Leader in High Performance Signal Processing Solutions

Sync Processing

October 2005

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Sync Processing

- Why is sync processing necessary?
- Sync slicing
- Sync separation
- Coast generation
- Coast extension
- Hsync Filter
- Vsync Filter
- Bonus Features

Why Sync Processing?

- **Using Composite Sync Lowers Cable Costs**
  - A typical graphics cable will carry five signals, (red, green, blue, Hsync, Vsync)
  - One wire can be eliminated by combining Hsync and Vsync into one signal, composite sync (Csync)
  - Composite sync can be embedded onto one of the color channels to save two wires, Sync-on-Green (SOG)
- **Television Signals Include Many Embedded Signals**
  - Macrovision
  - Equalization
  - Closed Captioning
  - Tri-level composite sync
  - Color Burst

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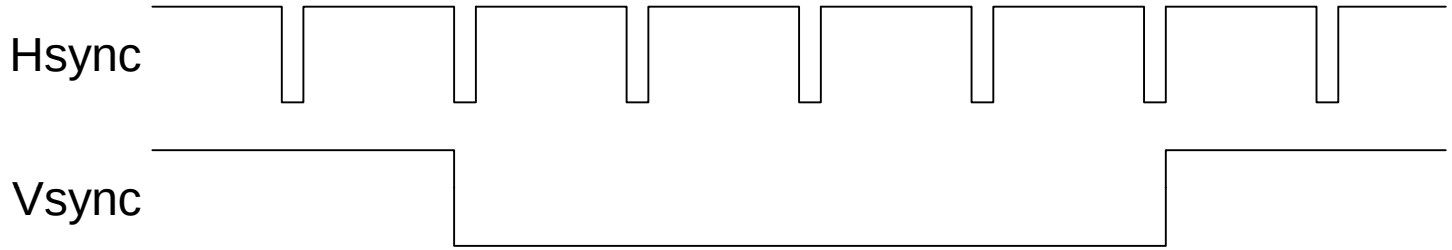
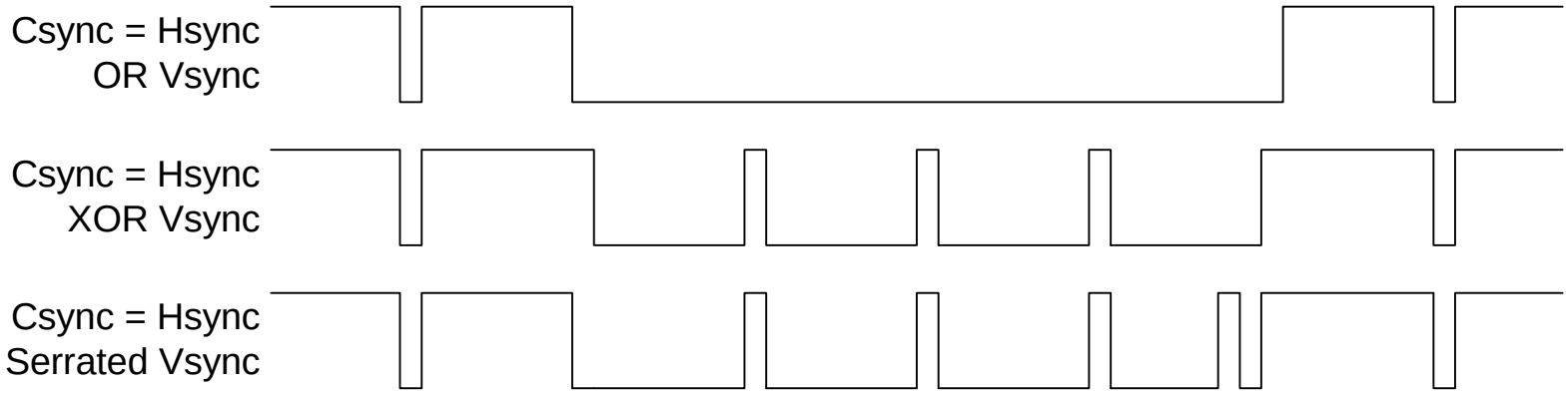
Generating Composite Sync

- **Start with Hsync and Vsync**



- **Hsync and Vsync can be combined a number of ways**



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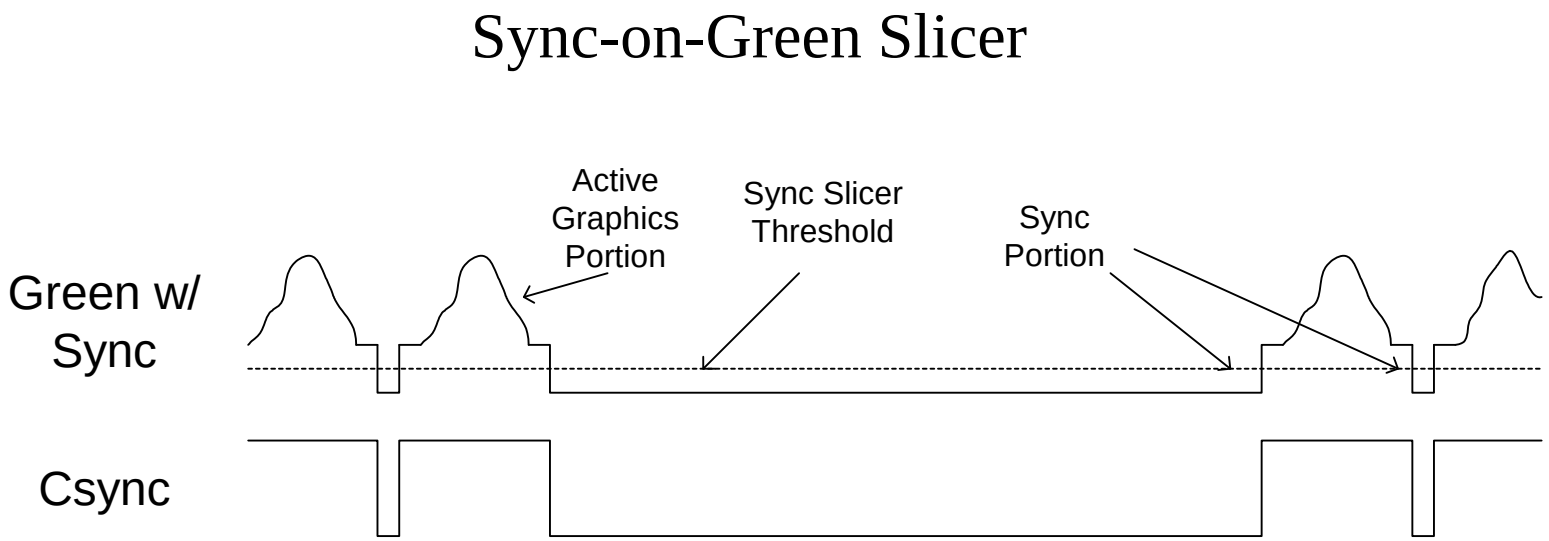
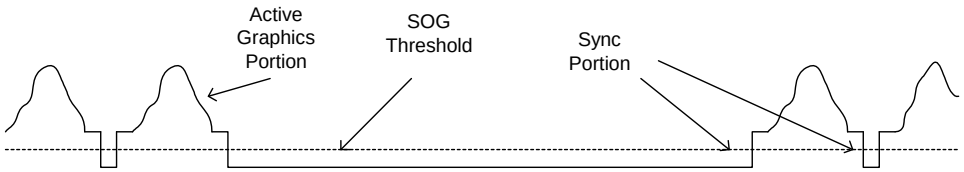
Reconstructing Hsync and Vsync

- **Step One: Sync Slicing**
  - **If Csync is imbedded onto the green channel (SOG), separate Csync from the green channel data.**



Setting the SOG Threshold

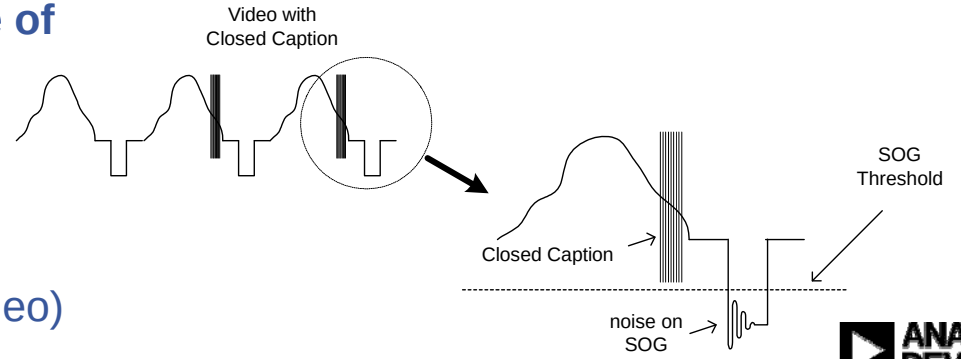
- **Many factors to consider**
  - **Sync tip amplitude**
  - **System noise**
  - **Closed Caption**
- **Clamped SOG signal is compared to the SOG Threshold**
  - **SOG Threshold must be set high enough to avoid noise and "ground bounce"**
  - **Must also be set lower than the noise (or overshoot) that could be associated with the trailing edge of the sync pulse.**
  - **Circumstances can limit the range of valid settings**
    - Low amplitude sync pulse
    - Closed-captioning (CC) with some sources
    - "color burst" signals (composite video)



Typical SOG signal

SOG Threshold Values

SOG Threshold Setting	Voltage relative to clamped SOG
0	10mV
• •	• •
15	160mV
• •	• •
31	320mV



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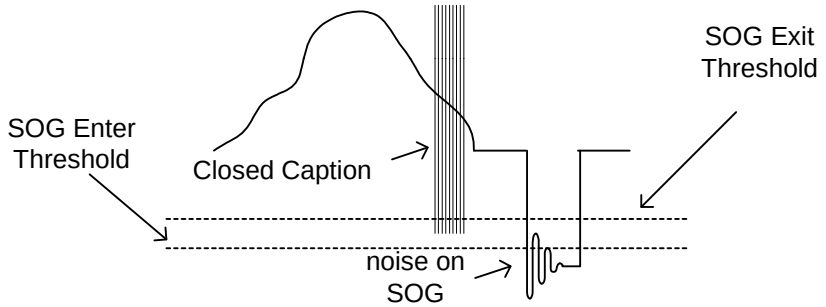
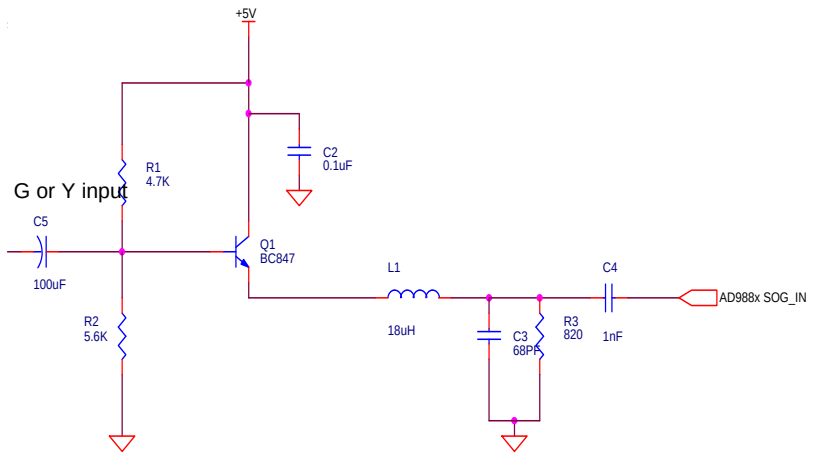
Setting the SOG Threshold

- **Using SOG Enter and Exit Thresholds**
  - **The AD9880, AD9983, and AD9984 all have separate controls for the enter and exit SOG Thresholds (optional on the AD9983/84, not available on AD9888)**
  - **Can be used to address the CC problem as shown here:**

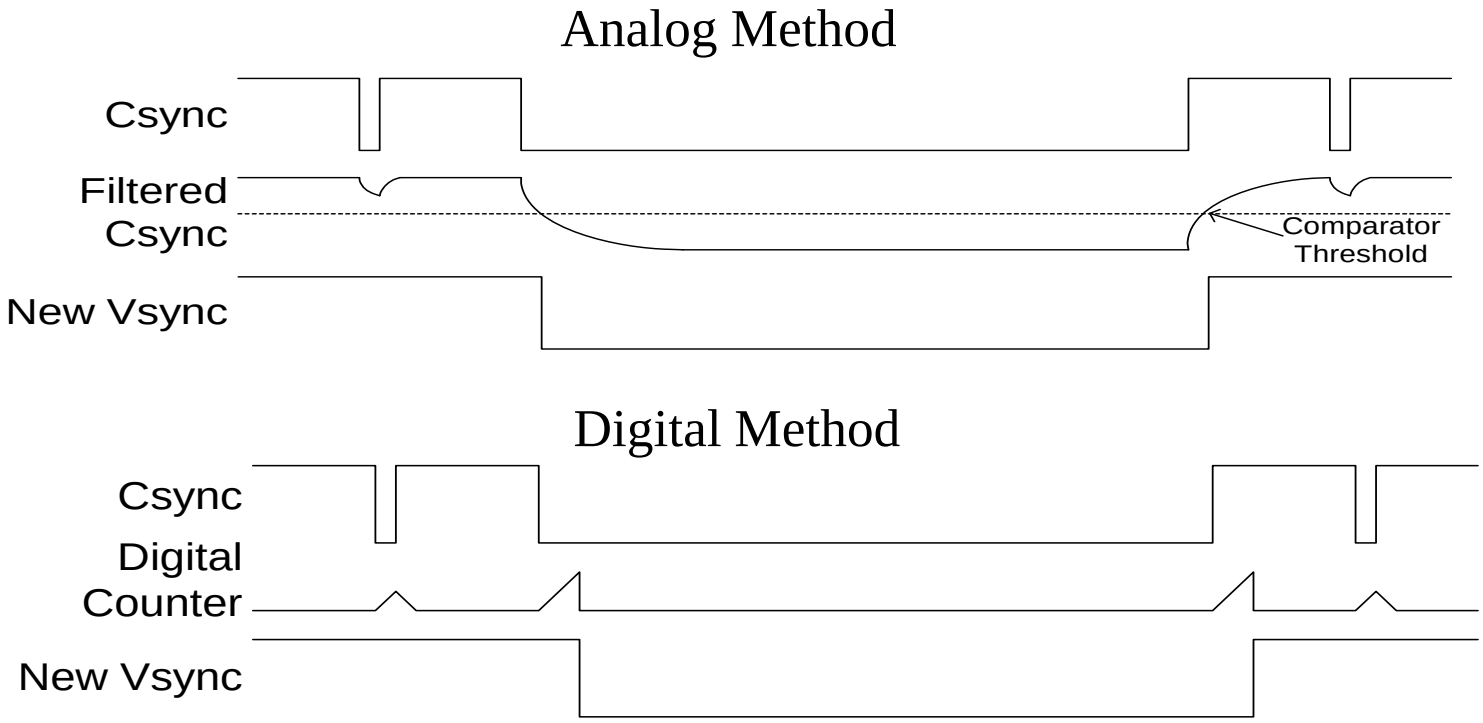


- **SOG Filter**
  - **A SOG input filter is available on the AD9983A, AD9984A, and AD9985A**
  - **The SOG filter eliminates pulses that are smaller than 60 – 120ns**
    - Makes SOG Threshold setting almost trivial
    - Some customers have implemented an external SOG filter



Reconstructing Hsync and Vsync

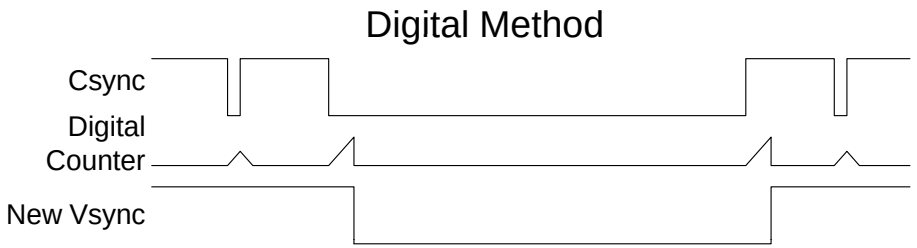
- **Step Two: Sync Separation**
  - **Separate Vsync from Csync via a low pass filter**



  - **Note that using the digital method will result in the new Vsync's leading edge always occurring after the Hsync's trailing edge**

Setting the Sync Separator Threshold

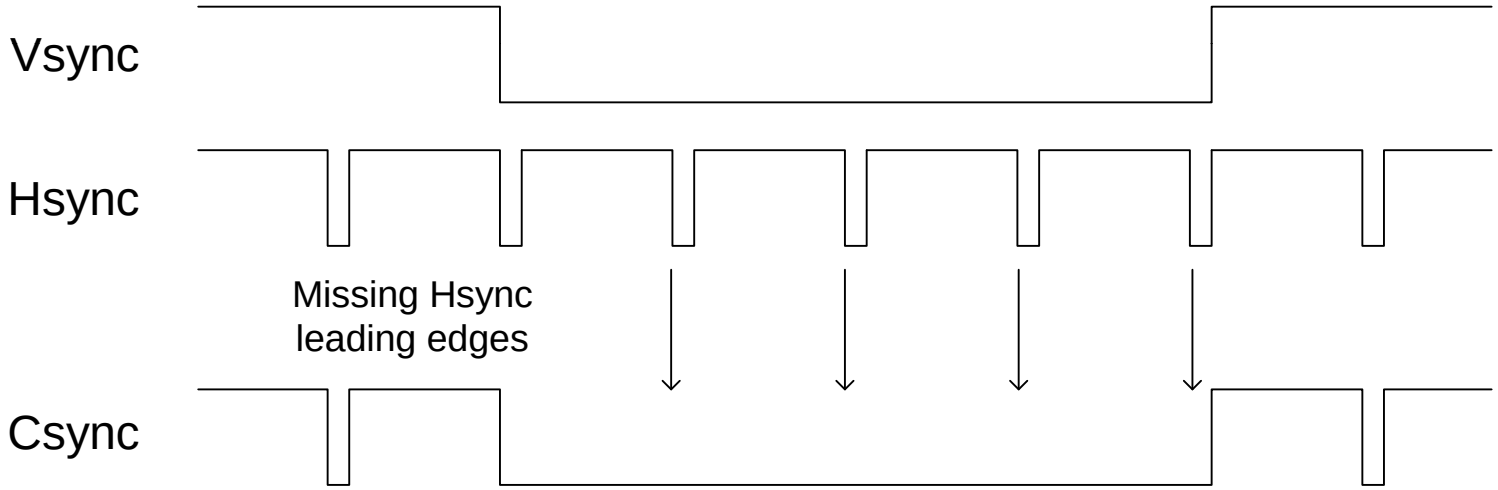
- **DEPL products use the digital method**
  - **The digital counter should be set higher than the Hsync pulse width but lower than the Vsync pulse width**



  - **Counter clock is nominally 5MHz ±20% (160 – 240ns period)**
  - **Example:**
    - To program the threshold duration, write a value (N) to Register 0x11
    - The resulting pulse width will be N × 200 nS.
    - If N = 5 the digital comparator threshold will be 1 µS.
    - Any pulses less than 1 µS are rejected, while any pulse greater than 1 µS passes through
  - **Resulting VSOUT is delayed by Nx200(±20%)nS**

Reconstructing Hsync and Vsync

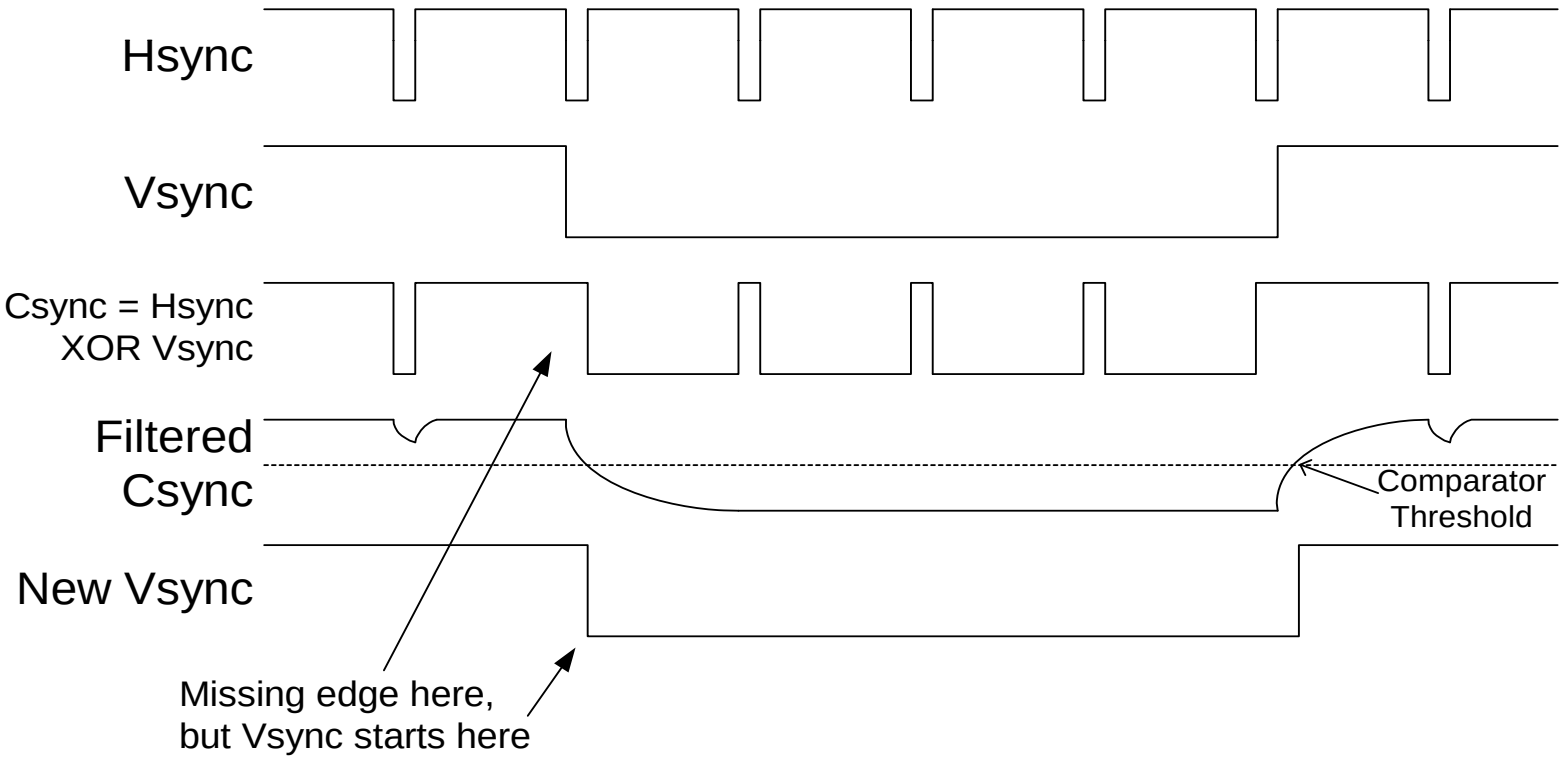
- **Step Three: Coast Generation**
  - **Coast is needed because the PLL requires an uninterrupted stream of Hsync leading edges, but Csync has missing edges.**



  - **In some cases, Vsync is sufficient to use for coasting, but in many cases, coast needs to be extended beyond Vsync.**

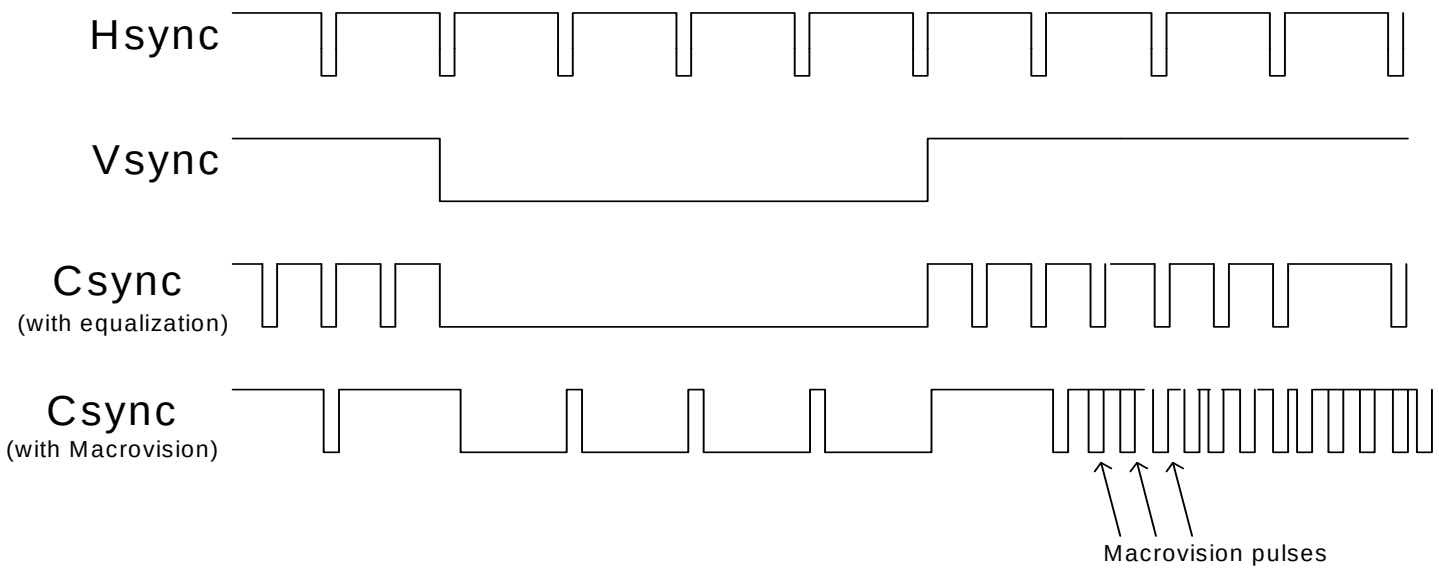
Coast Extension

- **Why does coast need to be extended?**
  - **Case 1: The XOR Csync is missing an Hsync leading edge before the new Vsync occurs**



Coast Extension

- **Why does coast need to be extended?**
  - **Case 2: If there are pre- or post- equalization pulses (NTSC video) or Macrovision**



- **On the AD9882, 83, 87, and 88, the pre- and post-Coast counter counts all pulses, not just Hsync Pulses. Therefore, the registers must be set accordingly.**

Coast Extension

- **How is coast extended?**
  - **Count Hsync (plus any “extra”) pulses between Vsyncs**
    - Newer devices (AD9880, AD9981, AD9984) and their derivatives only count Hsync pulses
  - **Assert coast any number of pulse counts before and/or after Vsync**
  - **Is programmable**

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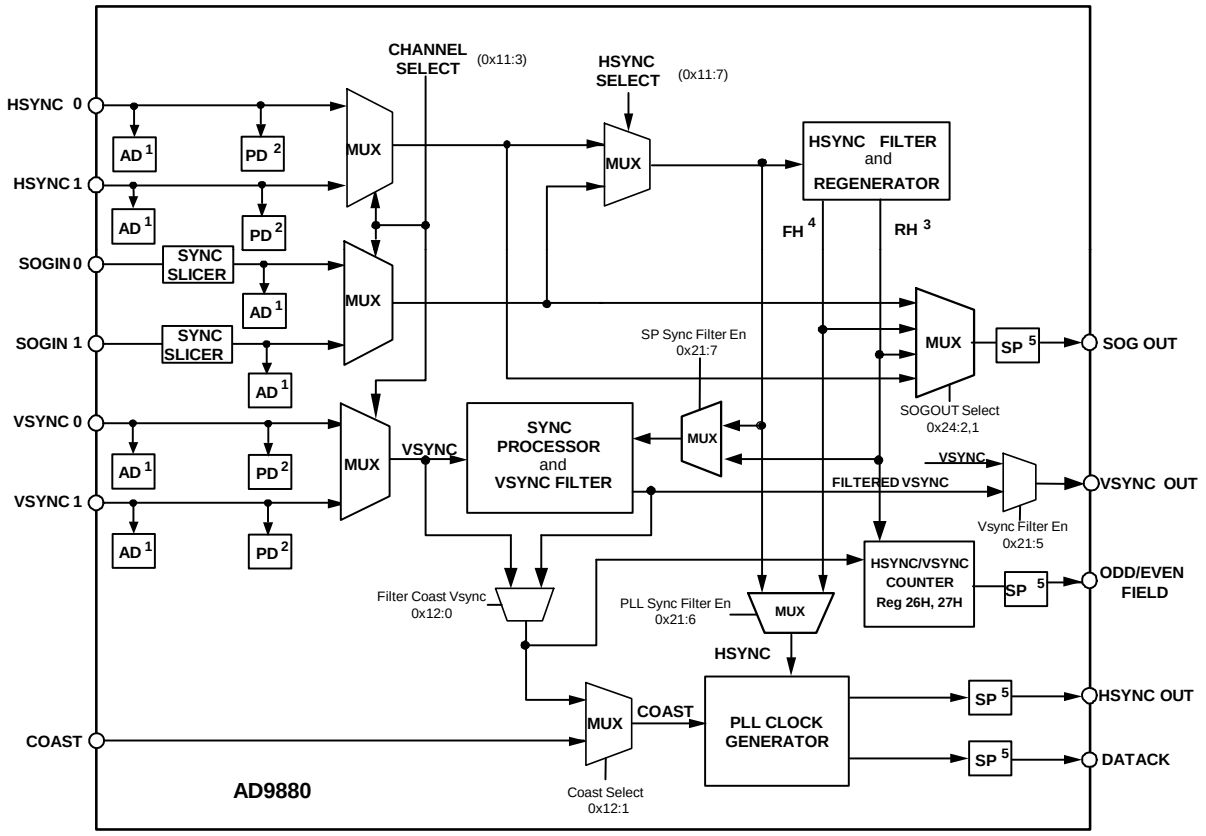
Advanced Sync Processing
(not available on AD9888)

- **Now Available on ADI's newer Analog Interfaces**
  - **Hsync Filter and Regenerator**
  - **Extraneous pulse detection and filtering**
  - **Vsync Filter**
  - **SOGOUT Mux**
  - **Hsync/Vsync Counter**
  - **Field detection**

AD9880 Sync Processing Block Diagram

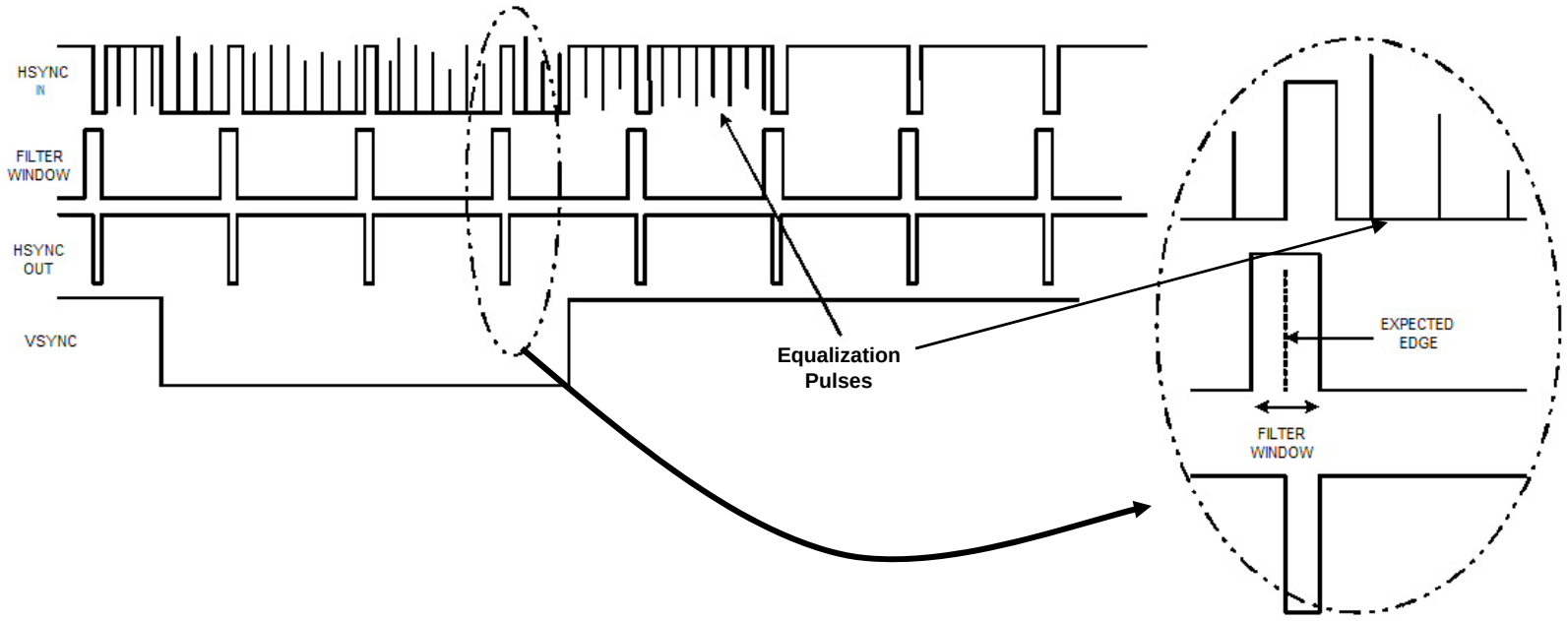


1 ACTIVITY DETECT
2 POLARITY DETECT
3 REGENERATED HSYNC
4 FILTERED HSYNC
5 SET POLARITY

Return

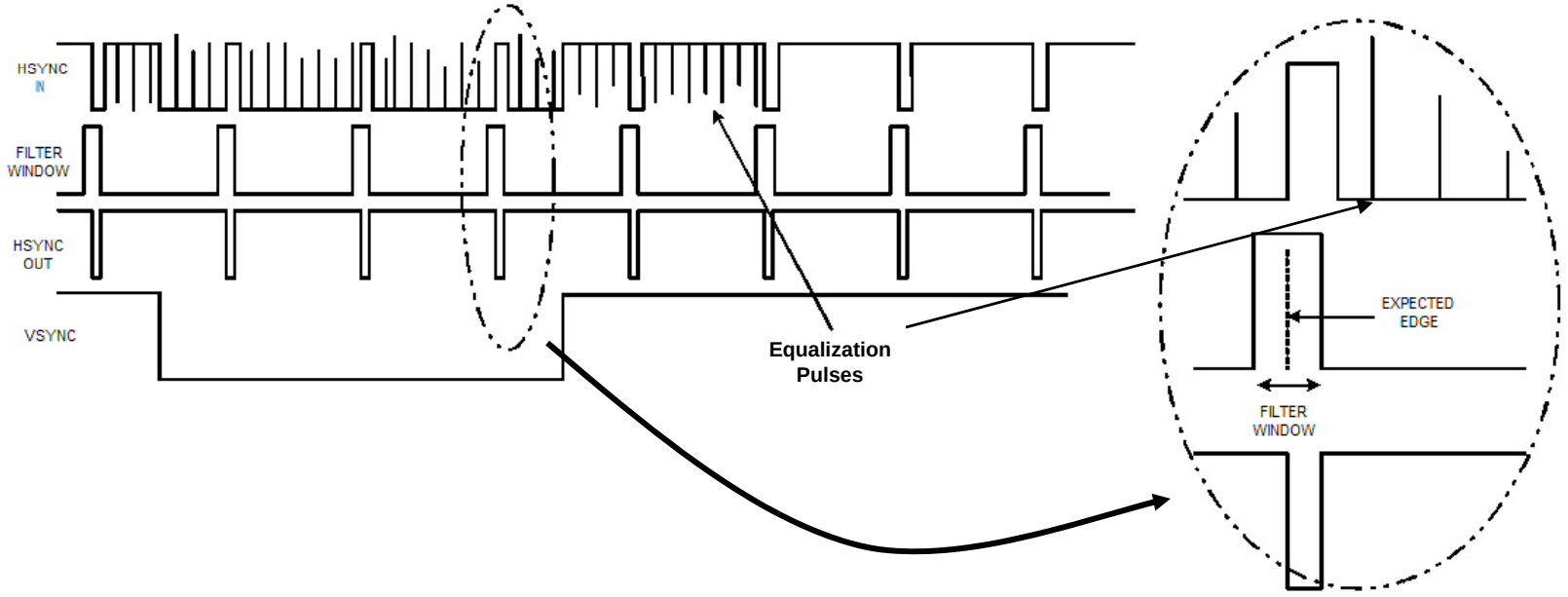
Hsync Filter and Regenerator

- **Hsync Filter**
  - **Eliminates extraneous pulses from Hsync or SOG inputs (equalization, macrovision, closed captioning, etc.)**
  - **A PLL-based filter window is generated to “gate” the input signal**
    - The Filter Window Width is programmable and should be set just narrow enough to gate all of the expected types of disruptions on the Hsync signal



Hsync Filter and Regenerator

- **Hsync Filter (continued)**
  - **Output has the same qualities as raw Hsync but without the extra activity**
    - Depending on the Sync Filter Window Width setting, the pulse width may be narrower than that of the raw Hsync
    - Because of this, this signal is not used to derive the Clamp timing
  - **This signal is used to drive the PLL for pixel clock regeneration**
  - **Sync Filter Lock and Unlock Threshold registers**
    - Sets the number of consecutive “valid” or “invalid” Hsync pulses required to “lock” or “unlock” the Filter Window PLL

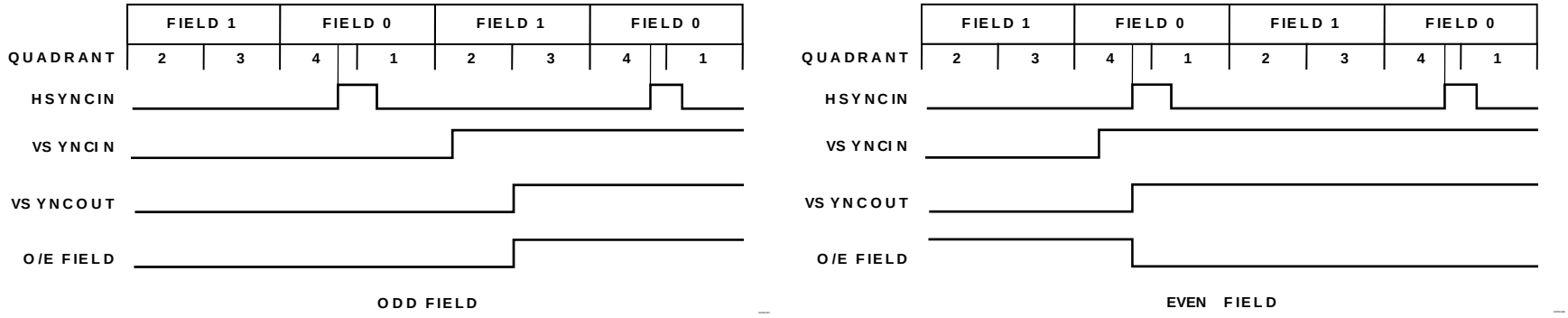


Hsync Filter and Regenerator

- **Hsync Regenerator**
  - **Regenerates an Hsync that is free of extraneous pulses**
  - **Generated by the same circuit as the Sync Filter Window**
  - **Higher jitter than raw Hsync**
    - Not appropriate for use by the PLL
    - Used for mode detection and Hsync per Vsync count
  - **Produces a continuous Hsync signal**
    - Hsync pulses are present even during vertical blanking

Vsync Filter

- **Eliminates spurious Vsync pulses**
- **Provides Odd/Even field detection**
  - **If the leading edge of Vsync occurs within ± ¼ Hsync period of the Hsync pulse it is considered an Even field. Otherwise, it is an Odd field.**
  - **The polarity of this result is programmable via the Field Output Polarity bit**



- **Maintains consistent timing relationship between the VSOUT and HSOUT**
  - **Prevents the HSOUT and VSOUT edges from switching at the same time**
  - **If Field polarity is determined downstream using VSOUT and HSOUT, the pulse width of HSOUT may need to be extended using the Hsync Duration register**

Bonus Features

- **SOGOUT Mux**
  - **Allows user to select which signal is observable on the SOGOUT pin**
    - Sync Slicer output (from SOG)
    - Raw Hsync (from Hsync pin)
    - Regenerated (constant) Hsync
    - Filtered Hsync
- **Hsync/Vsync Counter**
  - **Can be used to determine video mode**

Go To Block Diagram

Sync Processing Summary

- **Embedded television synchronization and many computer graphics signals require processing to extract syncs and accurately re-produce system timing**
- **For computer graphics, integrated Hsync and Vsync = lower end-user cost**
  - **Sync slicing (for SOG)**
  - **Sync separation**
  - **Coast generation**
  - **Coast extension**
- **Television Signals add more complexity**
  - **Macrovision**
  - **Equalization**
  - **Closed Captioning**
  - **Tri-level composite sync**
  - **Color Burst**

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