Compact PMU with Six DC-to-DC Channels, Two LDOs, Load Switch, and RTC

ADI Confidential

ADP50460008

FEATURES

- Wide input voltage range: 2.1 V to 5.5 V
- 2.5 MHz switching frequency
- Current mode architecture for best transient performance
- Internal compensation and soft start
- I²C-programmable output levels and power sequencing
- PSM mode on Channel 1
- Power
  - Channel 1: synchronous boost regulator, 1.2 A maximum
  - Channel 2: H-bridge buck-boost regulator, 0.9 A maximum
  - Channel 3: synchronous buck regulator, 1.8 A maximum
  - Channel 4: synchronous buck regulator, 0.9 A maximum
  - Channel 5: 45 mΩ load switch, 0.8 A
  - Channel 6: synchronous buck regulator, 0.9 A maximum
  - Channel 7: HV boost regulator for backlight LED, up to 23.75 V (typical)
  - Channel 8: LDO regulator, 100 mA maximum
  - Channel 9: low quiescent current LDO, 50 mA maximum
- Auxiliary
  - Real-time clock (RTC) with backup battery charger
  - Flexible power sequence control
  - Reset for external microprocessor
- Package
  - 4 mm × 4 mm, 64-ball WLCSP

APPLICATIONS

- Digital still cameras
- Digital video cameras
- Multimedia devices
- Space-constrained portable equipment

GENERAL DESCRIPTION

The ADP5046 is a compact, multi-output power management unit (PMU) designed for space-constrained applications that require high efficiency power regulation. The device includes a boost, a buck-boost, and three buck regulators; two LDOs; a backlight driver; a load switch; and an RTC/backup battery manager. The total solution size is minimized through a combination of chip scale packaging; high frequency switches; and the integration of power FETs, external compensation, and feedback resistors. To ensure maximum flexibility, the voltage outputs, power sequencing, and soft start time can be programmed via the I²C interface or set by factory programming.

FUNCTIONAL BLOCK DIAGRAM

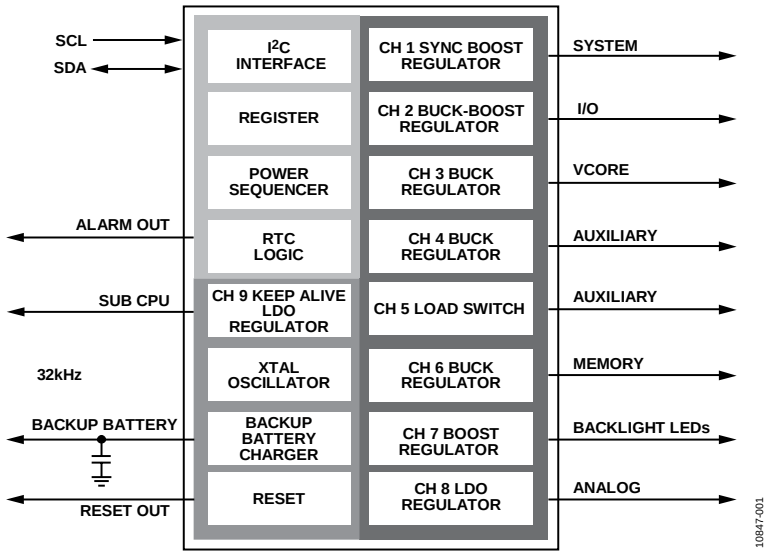


Figure 1.

Rev. Sp0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

9/12— Revision Sp0: Initial Version

SPECIFICATIONS

T_J = 25°C, V_{VBATT} = V_{VDD} = 3.6 V, V_{VDDIO} = 3.3 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT SUPPLY VOLTAGE RANGE	V_{IN}	2.1	3.6	5.5	V	Includes VBATT, PVIN2, PVIN3, PVIN4, PVIN6, VIN8, and VDDIO
Minimum Power-Up V_{VBATT} Voltage	$V_{POWER-UP\ MIN}$	2.3			V	
QUIESCENT CURRENT						
Operating Quiescent Current						
VBATT	$I_{Q(VBATT\_OP1)}$		13		µA	No switching, EN = high
	$I_{Q(VBATT\_OP2)}$		20	40	µA	No switching, EN = high, V_{VBATT} = 5.5 V
VDD	$I_{Q(VDD\_OP1)}$		3.9		mA	No switching, EN = high
	$I_{Q(VDD\_OP2)}$		4.75	7	mA	No switching, EN = high, V_{VDD} = 5.5 V
Channel 1 Power Save Mode (PSM), I_{VBATT} + I_{VDD}	$I_{Q(PSM\_OP)}$		60		µA	No switching, EN = low, V_{VBATT} = 3.0 V, 4.2 V, 5.5 V
VDDIO	$I_{Q(VDDIO)}$		0.25		µA	V_{VDDIO} = V_{SCL} = V_{SDA} = 3.3 V
PVIN2	$I_{Q(PVIN2)}$		1		µA	No switching, V_{VBATT} = V_{VDD} = V_{PVIN2} = 3.6 V, EN = high
PVIN3	$I_{Q(PVIN3)}$		1		µA	No switching, V_{VBATT} = V_{VDD} = 3.6 V, EN = high
PVIN4	$I_{Q(PVIN45)}$		1		µA	No switching, V_{VBATT} = V_{VDD} = 3.6 V, EN = high
VIN5	$I_{Q(VIN5)}$		1		µA	V_{VBATT} = V_{VDD} = 3.6 V
PVIN6	$I_{Q(PVIN6)}$		1		µA	No switching, V_{VBATT} = V_{VDD} = 3.6 V, EN = high
VIN8	$I_{Q(VIN8)}$		32		µA	No load, V_{IN8} = V_{OUT8} + 0.5 V, V_{OUT8} = 3.3 V
System Lockout Current, I_{VBATT} + I_{VDD}	$I_{Q(LOCKOUT)}$		2		µA	V_{VBATT} = V_{VDD} = 1.8 V, EN = low
BACKUP BATTERY MODE						
BU3INT Operating Quiescent Current (Backup Battery Mode)	$I_{Q(STNBYBACKUP)}$		1.5		µA	Includes RTCOSC, RTC logic, and UVLO_RTC;[1] V_{VBATT} = V_{VDD} = 0 V; V_{BU3INT} = 2.0 V
Lockout Current (Backup Battery Mode)	$I_{Q(LOCKBACKUP)}$		0.1		µA	Battery voltage disconnected from VBATT node; V_{BU3INT} = 1.0 V
UVLO						
System Undervoltage Lockout Threshold (Rising)	V_{UVLO_SYS1}	2.522	2.6	2.75	V	See Table 74, Register OPT_UVLO_SYS_R, Bit 7 (SEL_VTH_R) = 0b
		2.2	2.3	2.43	V	See Table 74, Register OPT_UVLO_SYS_R, Bit 7 (SEL_VTH_R) = 1b
Hysteresis	$V_{HSY\_UVLO\_SYS}$		0.2		V	
VDD Undervoltage Lockout Threshold (Rising)	V_{UVLO_VDD}		2.19		V	
Hysteresis	$V_{HYS(UVLO\_VDD)}$		0.1		V	
OSCILLATOR CIRCUIT						
Switching Frequency 1	f_{SW1}	2.125	2.5	2.875	MHz	
		2	2.5	3	MHz	−10°C ≤ T_J ≤ +85°C
Switching Frequency 2	f_{SW2}	1.12	1.25	1.38	MHz	
		1.0625	1.25	1.4275	MHz	−10°C ≤ T_J ≤ +85°C
LOGIC INPUTS						
EN Pin						
Low Level Threshold	$V_{IL(EN)}$			0.3 × V_{VREGO}	V	V_{VREGO} = 3.2 V, −10°C ≤ T_J ≤ +85°C
High Level Threshold	$V_{IH(EN)}$	0.7 × V_{VREGO}			V	V_{VREGO} = 3.2 V, −10°C ≤ T_J ≤ +85°C
SCL and SDA Pins						
Low Level Threshold	$V_{IL(I2C)}$			0.3 × V_{VDDIO}	V	V_{VDDIO} = 3.3 V, −10°C ≤ T_J ≤ +85°C
High Level Threshold	$V_{IH(I2C)}$	0.7 × V_{VDDIO}			V	V_{VDDIO} = 3.3 V, −10°C ≤ T_J ≤ +85°C

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS						
SDA Pin						
Low Level Output Voltage	$V_{OL(SDA)}$			0.4	V	3.0 mA sink current, −10°C ≤ T_J ≤ +85°C
Leakage Current	$I_{LEAK(SDA)}$		10		nA	V_{SDA} = 3.3 V
CLKO Pin						
Low Level Output Voltage	$V_{OL(CLKO)}$			0.4	V	3.0 mA sink current, −10°C ≤ T_J ≤ +85°C
High Level Output Voltage	$V_{OH(CLKO)}$	V_{VREGO} − 0.4			V	3.0 mA source current, −10°C ≤ T_J ≤ +85°C
ALMO Pin						
Low Level Output Voltage	$V_{OL(ALMO)}$			0.4	V	3.0 mA sink current, −10°C ≤ T_J ≤ +85°C
High Level Output Voltage	$V_{OH(ALMO)}$	V_{VREGO} − 0.4			V	3.0 mA source current, −10°C ≤ T_J ≤ +85°C
POCO Pin						
Low Level Output Voltage	$V_{OL(POCO)}$			0.4	V	3.0 mA sink current, −10°C ≤ T_J ≤ +85°C
High Level Output Voltage	$V_{OH(POCO)}$	V_{VREGO} − 0.4			V	3.0 mA source current, −10°C ≤ T_J ≤ +85°C

[1] RTCOSC refers to the XTAL oscillator; RTC logic refers to the alarm function and RTC registers.

DC-TO-DC CONVERTER BLOCK SPECIFICATIONS

T_J = 25°C, V_{VBATT} = V_{VDD} = 3.6 V, V_{VDDIO} = 3.3 V, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL 1 BOOST REGULATOR						
Channel 1 Output Voltage (V_{OUT1})						
Adjustable Range, 3 Bits	V_{OUT1}	3.8		5.3	V	
Voltage Accuracy	$V_{OUT1(DEFAULT)}$	−1.5		+1.5	%	Default VID code
		−2.5		+2.5	%	−10°C ≤ T_J ≤ +85°C
Load Regulation	$\Delta V_{OUT1}/I_{LOAD}$		−0.2		%/A	I_{VOUT1} = 100 mA to 600 mA
Line Regulation	$\Delta V_{OUT1}/V_{VBATT}$		0.1		%/V	V_{VBATT} = 2.1 V to 4.5 V
Switching Node (SW1 Pins)						
High-Side Power FET, $R_{DS(ON)}$	$R_{DS(ON)1H}$		100		mΩ	I_D = 100 mA
Low-Side Power FET, $R_{DS(ON)}$	$R_{DS(ON)1L}$		115		mΩ	I_D = 100 mA
Low-Side Switch Current Limit	I_{CL1}	3	3.4		A	−10°C ≤ T_J ≤ +85°C
Minimum Off Time	$t_{OFF1(MIN)}$		100		ns	
Soft Start Time	t_{SS1}		4		ms	Default SFTTIM code
Power Save Mode (PSM)						
Output Voltage on PSM	$V_{OUT1PSM}$		3.6		V	EN = low
PSM SW1 Low-Side Power FET, $R_{DS(ON)}$	$R_{DS(ON)2L}$		1		Ω	I_D = 30 mA, EN = low
PSM On Time	t_{ONPSM1}		450		ns	V_{VBATT} = 3.0 V
CHANNEL 2 BUCK-BOOST REGULATOR						
Channel 2 Output Voltage (V_{OUT2})						
Adjustable Range, 3 Bits	V_{OUT2}	3.3		3.65	V	
Voltage Accuracy	$V_{OUT2(DEFAULT)}$	−1.5		+1.5	%	Default VID code
		−2.5		+2.5	%	−10°C ≤ T_J ≤ +85°C
Load Regulation	$\Delta V_{OUT2}/I_{LOAD}$		−0.4		%/A	I_{VOUT2} = 100 mA to 600 mA
Line Regulation	$\Delta V_{OUT2}/V_{PVIN2}$		0.1		%/V	V_{PVIN2} = 2.1 V to 4.5 V
Switching Node (SWA2 Pins)						
High-Side Power FET, $R_{DS(ON)}$	$R_{DS(ON)PRI2H}$		95		mΩ	I_D = 100 mA, V_{PVIN2} = 3.6 V
Low-Side Power FET, $R_{DS(ON)}$	$R_{DS(ON)PRI2L}$		120		mΩ	I_D = 100 mA, V_{PVIN2} = 3.6 V
High-Side Switch Current Limit	I_{CL2}	2	2.5		A	−10°C ≤ T_J ≤ +85°C
Switching Node (SWB2 Pins)						
High-Side Power FET, $R_{DS(ON)}$	$R_{DS(ON)SEC2H}$		100		mΩ	I_D = 100 mA, V_{OUT2} = 2.8 V
Low-Side Power FET, $R_{DS(ON)}$	$R_{DS(ON)SEC2L}$		130		mΩ	I_D = 100 mA, V_{OUT2} = 2.8 V
Minimum Off Time	$t_{OFF2(MIN)}$		100		ns	
Soft Start Time	t_{SS2}		4.5		ms	Default SFTTIM code
C_{OUT} Discharge Switch On Resistance	R_{DIS2}		100		Ω	
CHANNEL 3 BUCK REGULATOR						
Channel 3 Output Voltage (FB3 Pin)						
Adjustable Range, 4 Bits	V_{FB3}	0.96		1.26	V	
Feedback Voltage Accuracy at Default VID Code	$V_{FB3(DEFAULT)}$	−1		+1	%	Default VID code
		−2.5		+2.5	%	−10°C ≤ T_J ≤ +85°C
Load Regulation	$\Delta V_{OUT3}/I_{LOAD}$		0.3		%/A	I_{VOUT3} = 100 mA to 1.4 A
Line Regulation	$\Delta V_{OUT3}/V_{PVIN3}$		0.1		%/V	V_{PVIN3} = 2.1 V to 4.5 V
Switching Node (SW3 Pins)						
High-Side Power FET, $R_{DS(ON)}$	$R_{DS(ON)3H}$		65		mΩ	I_D = 100 mA
Low-Side Power FET, $R_{DS(ON)}$	$R_{DS(ON)3L}$		50		mΩ	I_D = 100 mA
Switch Current Limit	I_{CL3}	2.3	3		A	−10°C ≤ T_J ≤ +85°C
Soft Start Time	t_{SS3}		4		ms	Default SFTTIM code
C_{OUT} Discharge Switch On Resistance	R_{DIS3}		1		kΩ	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL 4 BUCK REGULATOR						
Channel 4 Output Voltage (FB4 Pin)						
Adjustable Range, 2 Bits	V_{FB4}	1.60		2.70	V	
Feedback Voltage Accuracy at Default VID Code	$V_{FB4(DEFAULT)}$	−1		+1	%	Default VID code
		−2		+2	%	$-10°C \le T_J \le +85°C$
FB4 Load Regulation	$\Delta V_{OUT4}/I_{LOAD}$		0.2		%/A	I_{VOUT4} = 100 mA to 600 mA
FB4 Line Regulation	$\Delta V_{OUT4}/V_{PVIN4}$		0.1		%/V	V_{PVIN4} = 2.1 V to 4.5 V
Switching Node (SW4 Pin)						
High-Side Power FET, $R_{DS(ON)}$	$R_{DS(ON)4H}$		160		mΩ	I_D = 100 mA
Low-Side Power FET, $R_{DS(ON)}$	$R_{DS(ON)4L}$		130		mΩ	I_D = 100 mA
Switch Current Limit	I_{CL4}	1.2	1.5		A	$-10°C \le T_J \le +85°C$
Soft Start Time	t_{SS4}		4		ms	Default SFTTIM code
C_{OUT} Discharge Switch On Resistance	R_{DIS4}		1		kΩ	
CHANNEL 6 BUCK REGULATOR						
Channel 6 Output Voltage (FB6 Pin)						
Adjustable Range, 3 Bits	V_{FB6}	1.46		2.50	V	
Feedback Voltage Accuracy at Default VID Code	$V_{FB6(DEFAULT)}$	−1		+1	%	Default VID code
		−2		+2	%	$-10°C \le T_J \le +85°C$
Load Regulation	$\Delta V_{OUT6}/I_{LOAD}$		0.4		%/A	I_{VOUT6} = 100 mA to 600 mA
Line Regulation	$\Delta V_{OUT6}/V_{PVIN6}$		0.1		%/V	V_{PVIN6} = 2.1 V to 4.5 V
Switching Node (SW6 Pin)						
High-Side Power FET, $R_{DS(ON)}$	$R_{DS(ON)6H}$		180		mΩ	I_D = 100 mA
Low-Side Power FET, $R_{DS(ON)}$	$R_{DS(ON)6L}$		120		mΩ	I_D = 100 mA
Switch Current Limit	I_{CL6}	1.2	1.5		A	$-10°C \le T_J \le +85°C$
Soft Start Time	t_{SS6}		4		ms	Default code
C_{OUT} Discharge Switch On Resistance	R_{DIS6}		1		kΩ	
CHANNEL 7 BOOST REGULATOR AND LED DRIVER						
LSTR7 Pin Sink Current	I_{LSTR7}		33.3		mA	IID7[4:0] = 00000b, R_{SET7} = 15 kΩ
OVP7 Threshold Voltage	V_{OVP7}	22	23.7	25	V	$-10°C \le T_J \le +85°C$
SW7 Low-Side Power FET, $R_{DS(ON)}$	$R_{DS(ON)7}$		450		mΩ	I_D = 50 mA, $-10°C \le T_J \le +85°C$
SW7 Switch Current Limit	I_{CL7}	0.45	0.65		A	$-10°C \le T_J \le +85°C$
SW7 Minimum Off Time	$t_{OFF7(MIN)}$		60		ns	
Channel 7 Soft Start Time from 0 mA to Full Current Limit[1]	t_{SS7}		8		ms	Default code
Channel 7 ISET7 Voltage	V_{ISET}	487.5	500	512.5	mV	R_{SET7} = 15 kΩ

[1] Soft start time for Channel 7 depends on the forward voltage of the LED used.

LINEAR REGULATOR BLOCK SPECIFICATIONS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL 8 LDO						
Output Voltage Adjustable Range, 3 Bits	V_{OUT8}	1.5		3.5	V	$V_{VIN8} = V_{OUT8} + 0.5$ V
Voltage Accuracy at Default VID Code	$V_{OUT8(DEFAULT)}$	−1.5		+1.5	%	$V_{VIN8} = V_{OUT8} + 0.5$ V
		−2.5		+2.5	%	$V_{VIN8} = V_{OUT8} + 0.5$ V, −10°C ≤ T_J ≤ +85°C
Load Regulation	$\Delta V_{OUT8}/I_{LOAD}$		0.002		%/mA	I_{VOUT8} = 1 mA to 100 mA, $V_{VIN8} = V_{OUT8} + 0.5$ V
Line Regulation	$\Delta V_{OUT8}/V_{VIN8}$		0.02		%/V	V_{VIN8} = (V_{OUT8} + 0.5 V) to 5.5 V, I_{VOUT8} = 1 mA
Power Supply Reject Ratio	PSRR		50		dB	f = 1 kHz, V_{OUT8} = 3.40 V, $V_{VIN8} = V_{OUT8} + 0.5$ V
Output Noise	OUT_{NOISE}		300		µV rms	10 Hz to 100 kHz, V_{OUT8} = 3.40 V
Dropout Voltage at 100 mA[1]	V_{DROP}		110		mV	V_{OUT8} programmed to 3.40 V
Output Current Limit	I_{CL8}		200		mA	V_{OUT8} drops 5% from nominal voltage

[1] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage.

LOAD SWITCH SPECIFICATIONS

T_J = 25°C, $V_{VBATT} = V_{VDD}$ = 3.6 V, V_{VDDIO} = 3.3 V, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Comments
CHANNEL 5 LOAD SWITCH						
Load Switch, $R_{DS(ON)}$	$R_{DS(ON)5}$		45		mΩ	I_D = 100 mA, V_{VIN5} = 1.8 V
C_{OUT} Discharge Switch On Resistance	R_{DIS5}		1		kΩ	

HOUSEKEEPING BLOCK SPECIFICATIONS

T_J = 25°C, V_{VBATT} = V_{VDD} = 3.6 V, V_{VDDIO} = 3.3 V, unless otherwise noted.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Comments
CHANNEL 9 LDO						
Keep Alive LDO Operating Quiescent Current	$I_{Q(VDD)}$		4.3		µA	No load, V_{VDD} = 3.6 V
Keep Alive LDO Output Voltage	V_{VREGO1}	3.135	3.2	3.265	V	I_{VREGO} = 1 mA, V_{IN} = V_{OUT} + 0.5 V, −10°C ≤ T_J ≤ +85°C
	V_{VREGO2}	2.94	3.0	3.06	V	I_{VREGO} = 1 mA, −10°C ≤ T_J ≤ +85°C, V_{VDD} = V_{VREGO} + 0.5 V
Current Limit Threshold	$I_{REGO\ LIM}$	75	115	155	mA	−10°C ≤ T_J ≤ +85°C
Keep Alive LDO Load Regulation	$\Delta V_{VREGO}/I_{LOAD}$		0.04		%/mA	10 µA < I_{VREGO} < 50 mA, V_{VDD} = 5.0 V
Keep Alive LDO Line Regulation	$\Delta V_{VREGO}/V_{VDD}$		0.01		%/V	V_{VDD} = (V_{VREGO} + 0.5 V) to 5.5 V, I_{VREGO} = 1 mA
Keep Alive LDO PSRR	V_{VREGO}PSRR		40		dB	f = 1 kHz
KEEP ALIVE LDO RESET (POCO)						
Keep Alive LDO RESET Voltage Threshold (Rising)[1]	$V_{TH(POCO)}$		2.8		V	
Hysteresis[1]	$V_{HYS(POCO)}$		0.2		V	
End of RESET Delay Time	$t_{DLY(POCO)}$		4		ms	
BACKUP BATTERY CHARGER						
Backup Battery Charger Output Voltage	V_{BU3INT}		3.0		V	I_{BU3INT} = 1 µA
Backup Battery Connect Switch On Resistance, M1	$R_{CONREGO}$		110		Ω	
REAL-TIME CLOCK (RTC)						
RTC Operating Voltage Range	V_{BU3INT}	1.6		3.3	V	
RTC Oscillator Start-Up Time	t_{START}		0.4		sec	
RTC CLK Frequency Error		−5		+5	ppm	
SEQUENCER AND SUPERVISORY CIRCUIT						
Undervoltage Protection Threshold	V_{UVP}		67		%	
Overvoltage Protection Threshold	V_{OVP}		125		%	
Undervoltage Protection Latch Delay	$t_{DLY(UV)}$		200		ms	
Overvoltage Protection Latch Delay	$t_{DLY(OVP)}$		1.2		ms	
Programmable Enable Delay Range, 4 Bits	t_{DLY}	0		30	ms	
Default Enable Delay Time from EN to Channel 1 On	$t_{DLY1(DEFAULT)}$		0		ms	
Default Enable Delay Time from EN to Channel 3 On	$t_{DLY3(DEFAULT)}$		12		ms	
Default Enable Delay Time from EN to Channel 2 On	$t_{DLY2(DEFAULT)}$		16		ms	
Default Enable Delay Time from EN to Channel 8 On	$t_{DLY8(DEFAULT)}$		16		ms	
Default Enable Delay Time from EN to Channel 6 On	$t_{DLY6(DEFAULT)}$		22		ms	
Default Off Delay Time from Channel 2 Shutdown to Channel 3 Shutdown	$t_{OFFDLY(2)}$, $t_{OFFDLY(3)}$		30		ms	

[1] Detected at the VREGO pin.

I²C INTERFACE TIMING SPECIFICATIONS

T_J = 25°C, V_{VBATT} = V_{VDD} = 3.6 V, V_{VDDIO} = 3.3 V, unless otherwise noted.

Table 6.

Parameter	Min	Typ	Max	Unit	Description
f_{SCL}			400	kHz	SCL clock frequency
t_{HIGH}	0.6			µs	SCL high time
t_{LOW}	1.3			µs	SCL low time
$t_{SU,DAT}$	100			ns	Data setup time
$t_{HD,DAT}$	0		0.9	µs	Data hold time[1]
$t_{SU,STA}$	0.6			µs	Setup time for repeated start
$t_{HD,STA}$	0.6			µs	Hold time for start or repeated start
t_{BUF}	1.3			µs	Bus-free time between a stop condition and a start condition
$t_{SU,STO}$	0.6			µs	Setup time of a stop condition
t_R	$20 + 0.1C_B$[2]		300	ns	Rise time of SCL and SDA
t_F	$20 + 0.1C_B$[2]		300	ns	Fall time of SCL and SDA
t_{SP}	0		50	ns	Pulse width of suppressed spike
C_B[2]			400	pF	Capacitive load for each bus line

[1] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the VIH minimum of the SCL signal) to bridge the undefined region of the SCL falling edge.
[2] B of C_B is the total capacitance of one bus line in picofarads (pF).

Timing Diagram

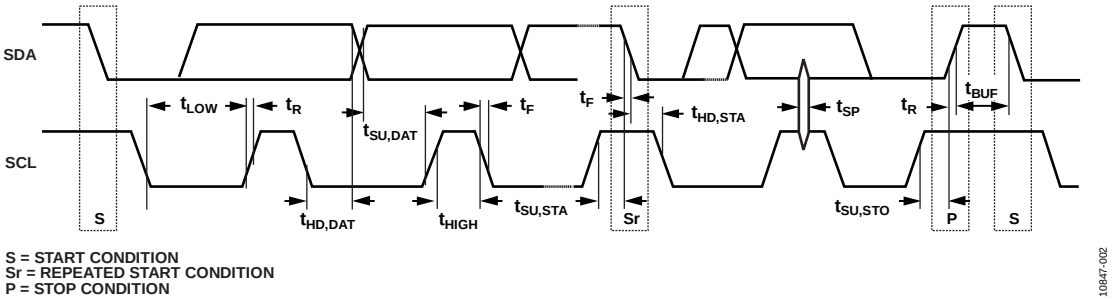


Figure 2. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
VBATT to GND	−0.3 V to +6.5 V
VREGO to GND	−0.3 V to +6.5 V
VDD to GND	−0.3 V to +6.5 V
VDDIO to GND	−0.3 V to +6.5 V
PVIN2 to PGND2	−0.3 V to +6.5 V
PVIN3 to PGND3	−0.3 V to +6.5 V
PVIN4 to PGND4	−0.3 V to +6.5 V
PVIN6 to PGND6	−0.3 V to +6.5 V
PVIN7 to PGND7	−0.3 V to +6.5 V
VIN5 to GND	−0.3 V to +3.6 V
VIN8 to GND	−0.3 V to +6.5 V
VOUT1 to PGND1	−0.3 V to +6.5 V
VOUT2 to PGND2	−0.3 V to +6.5 V
VOUT5 to GND	−0.3V to VIN5 + 0.3 V
PGNDx to GND	−0.3 V to +0.3 V
SW1 to PGND1	−0.5 V to +6.5 V
SWA2 to PGND2	−2.0 V to +6.5 V
SWB2 to PGND2	−0.5 V to +6.5 V
SW3 to PGND3	−2.0 V to +6.5 V
SW4 to PGND4	−2.0 V to +6.5 V
SW6 to PGND6	−2.0 V to +6.5 V
SW7 to PGND7	−0.5 V to +27 V
OVP7 to GND	−0.3 V to +27 V
LSTR7 to BLGND7	−0.3 V to +6.5 V
ISET7 to GND	−0.3 V to VDD + 0.3 V
BLGND7 to GND	−0.3 V to +0.3 V
EN to GND	−0.3 V to +6.5 V
I_{VIN5} to I_{VOUT5}	1 A
FB3 to GND	−0.3 V to +6.5 V
FB4 to GND	−0.3 V to +6.5 V
FB6 to GND	−0.3 V to +6.5 V
BU3INT to RTCGND	−0.3 V to +3.6 V
XIN and XOUT to RTCGND	−0.3 V to BU3INT + 0.3 V
CLKO to GND	−0.3 V to VREGO + 0.3 V
SCL and SDA to GND	−0.3 V to VDDIO + 0.3 V
POCO to GND	−0.3 V to VREGO + 0.3 V
ALMO to GND	−0.3 V to VREGO + 0.3 V
TEST1 to GND	−0.3 V to VDD + 0.3 V
TEST2 to GND	−0.3 V to VDD + 0.3 V
TEST3 to GND	−0.3 V to VDD + 0.3 V
TEST4 to GND	−0.3 V to VDD + 0.3 V
Storage Temperature Range	−65°C to +150°C
Operating Ambient Temerature Range	−25°C to +85°C
Operating Junction Temperature Range[1]	−25°C to +125°C

[1] To guarantee reliability, it is recommended that the ADP5046 not be operated with an average T_J of >90°C for an extended period of time.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for worst-case conditions; that is, a device soldered in a circuit board for surface-mount packages. Note that actual θ_{JA} depends on the application environment.

Table 8. Thermal Resistance

PCB Type[1]	θ_{JA}[2]	Unit
1S0P	60.6	°C/W
2S2P	26.9	°C/W

[1] PCB type conforms to JEDEC51-9.
[2] 1.25 W power dissipation.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

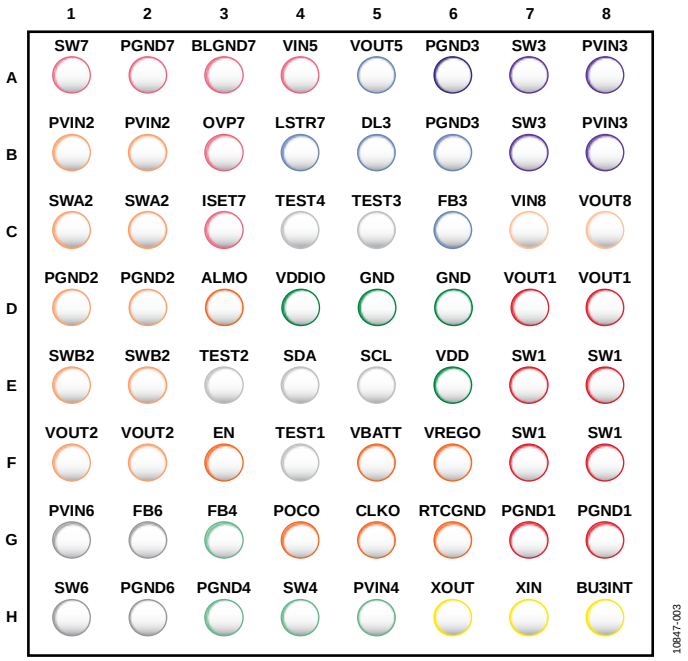


Figure 3. Pin Configuration (Top View)

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1A	SW7	Switching Node for Channel 7 (Boost Regulator and LED Driver). Leave this pin open if Channel 7 is not used.
1B	PVIN2	Input Power Supply for Channel 2 (Buck-Boost Regulator).
1C	SWA2	Primary-Side Switching Node for Channel 2 (Buck-Boost Regulator).
1D	PGND2	Power Ground for Channel 2 (Buck-Boost Regulator).
1E	SWB2	Secondary-Side Switching Node for Channel 2 (Buck-Boost Regulator).
1F	VOUT2	Output Voltage for Channel 2 (Buck-Boost Regulator).
1G	PVIN6	Input Power Supply for Channel 6 (Buck Regulator).
1H	SW6	Switching Node for Channel 6 (Buck Regulator).
2A	PGND7	Power Ground for Channel 7 (Boost Regulator and LED Driver). Connect this pin to ground if Channel 7 is not used.
2B	PVIN2	Input Power Supply for Channel 2 (Buck-Boost Regulator).
2C	SWA2	Primary-Side Switching Node for Channel 2 (Buck-Boost Regulator).
2D	PGND2	Power Ground for Channel 2 (Buck-Boost Regulator).
2E	SWB2	Secondary-Side Switching Node for Channel 2 (Buck-Boost Regulator).
2F	VOUT2	Output Voltage for Channel 2 (Buck-Boost Regulator).
2G	FB6	Feedback for Channel 6 (Buck Regulator).
2H	PGND6	Power Ground for Channel 6 (Buck Regulator).
3A	BLGND7	Analog Ground for Channel 7 (Boost Regulator and LED Driver). Connect this pin to ground if Channel 7 is not used.
3B	OVP7	Overvoltage Sensing for Channel 7 (Boost Regulator and LED Driver). Connect this pin to ground if Channel 7 is not used.
3C	ISET7	LED Current Reference for Channel 7 (Boost Regulator and LED Driver). Leave this pin open if Channel 7 is not used.
3D	ALMO	Alarm Output. This pin can be connected to an external processor. This pin is also a VREGO domain CMOS output. Leave this pin open if ALMO is not used.
3E	TEST2	Test Pin. Connect to ground.
3F	EN	Enable. Logic high turns on the PMU.
3G	FB4	Feedback for Channel 4 (Buck Regulator).
3H	PGND4	Power Ground for Channel 4 (Buck Regulator).

Pin No.	Mnemonic	Description
4A	VIN5	Input Power Supply for Channel 5 (Load Switch).
4B	LSTR7	LED String Sink for Channel 7 (Boost Regulator and LED Driver). This pin connects to the cathode side of the LED string. Connect this pin to ground if Channel 7 is not used.
4C	TEST4	Test Pin. Connect to ground.
4D	VDDIO	Supply Voltage for the I^2C Interface. This pin is typically connected externally to the Channel 2 output.
4E	SDA	Data Input/Output for the I^2C Interface.
4F	TEST1	Test Pin. Connect to ground.
4G	POCO	RESET Output for Sub-CPU. Leave this pin open if POCO is not used. This pin is also a VREGO domain CMOS output.
4H	SW4	Switching Node for Channel 4 (Buck Regulator).
5A	VOUT5	Output Voltage for Channel 5 (Load Switch).
5B	DL3	Channel 3 External FET Gate Driver. Leave this pin open if the external NFET is not used.
5C	TEST3	Test Pin. Connect to ground.
5D	GND	Ground.
5E	SCL	Clock Input for the I^2C Interface.
5F	VBATT	Power Supply Input for the Internal Circuits.
5G	CLKO	32 kHz Clock Buffered Output. Leave this pin open if the 32 kHz output is not used. This pin is also a VREGO domain CMOS output.
5H	PVIN4	Input Power Supply for Channel 4 (Buck Regulator).
6A	PGND3	Power Ground for Channel 3 (Buck Regulator).
6B	PGND3	Power Ground for Channel 3 (Buck Regulator).
6C	FB3	Feedback for Channel 3 (Buck Regulator).
6D	GND	Ground.
6E	VDD	Power Supply. Connect to Channel 1 output through a 0.1 Ω/10 µF RC filter.
6F	VREGO	Keep Alive LDO Output.
6G	RTCGND	Ground for RTC. This pin is internally connected to GND. Do not connect this pin to the power ground plane of the PCB.
6H	XOUT	Real-Time Clock Crystal Driver Output. Bypass with a compensation capacitor to RTCGND. Connect this pin to ground if the 32 kHz oscillator is not used.
7A	SW3	Switching Node for Channel 3 (Buck Regulator).
7B	SW3	Switching Node for Channel 3 (Buck Regulator).
7C	VIN8	Power Supply Input for Channel 8 (LDO Regulator). Connect this pin to ground if Channel 8 is not used.
7D	VOUT1	Output Voltage for Channel 1 (Boost Regulator).
7E	SW1	Switching Node for Channel 1 (Boost Regulator).
7F	SW1	Switching Node for Channel 1 (Boost Regulator).
7G	PGND1	Power Ground for Channel 1 (Boost Regulator).
7H	XIN	Real-Time Clock Crystal Driver Input. Bypass with a compensation capacitor to RTCGND. Connect this pin to ground if the 32 kHz oscillator is not used.
8A	PVIN3	Input Power Supply for Channel 3 (Buck Regulator).
8B	PVIN3	Input Power Supply for Channel 3 (Buck Regulator).
8C	VOUT8	Output Voltage for Channel 8 (LDO Regulator). Leave this pin open if Channel 8 is not used.
8D	VOUT1	Output Voltage for Channel 1 (Boost Regulator).
8E	SW1	Switching Node for Channel 1 (Boost Regulator).
8F	SW1	Switching Node for Channel 1 (Boost Regulator).
8G	PGND1	Power Ground for Channel 1 (Boost Regulator).
8H	BU3INT	Power Supply for the Real-Time Clock XTAL Oscillator and Associated Logic. Connect a capacitor of 1 µF minimum to RTCGND. If the 32 kHz oscillator is not used, leave this pin open with only the capacitor connected.

TYPICAL PERFORMANCE CHARACTERISTICS

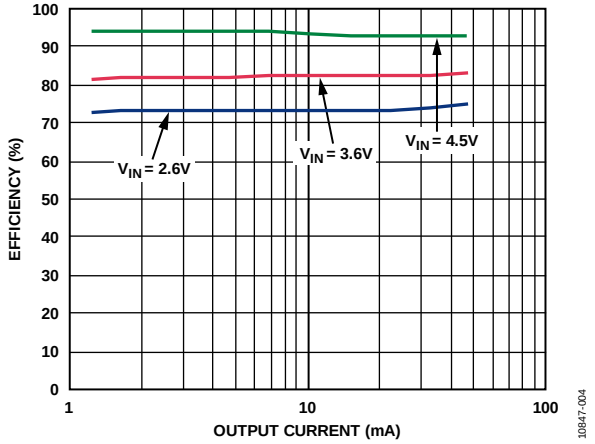


Figure 4. Efficiency, Channel 1 (PSM), V_{OUT1} = 3.6 V

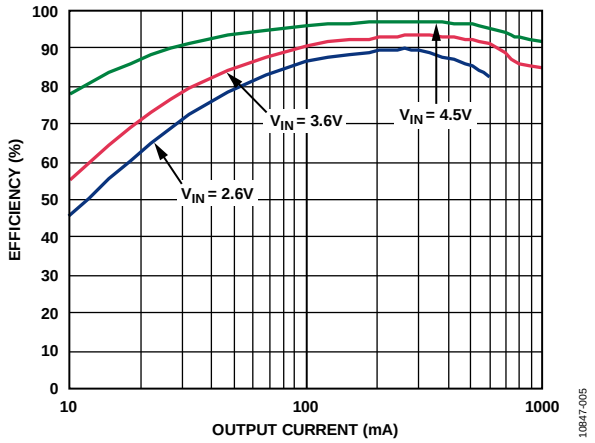


Figure 5. Efficiency, Channel 1 (PWM), V_{OUT1} = 5.0 V

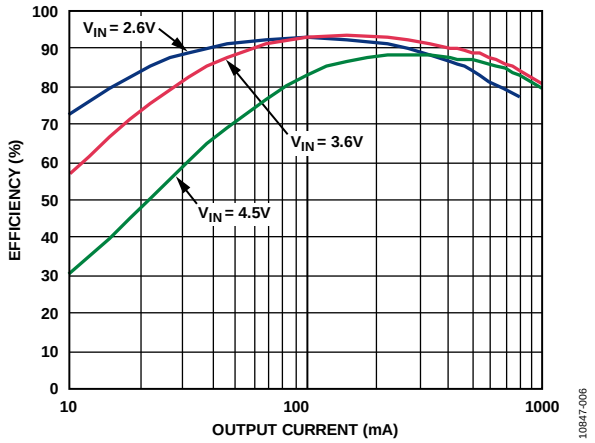


Figure 6. Efficiency, Channel 2, V_{OUT2} = 3.3 V

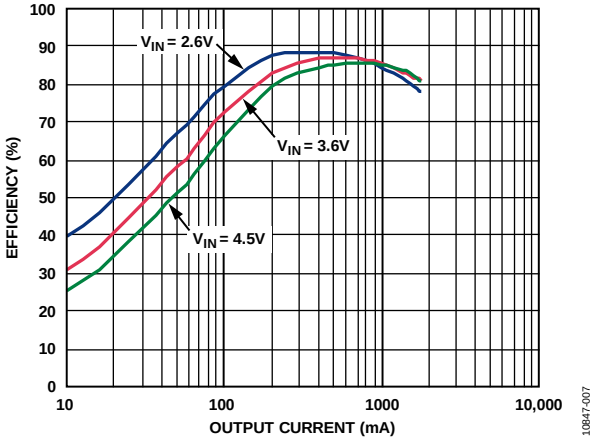


Figure 7. Efficiency, Channel 3, V_{OUT3} = 1.1 V

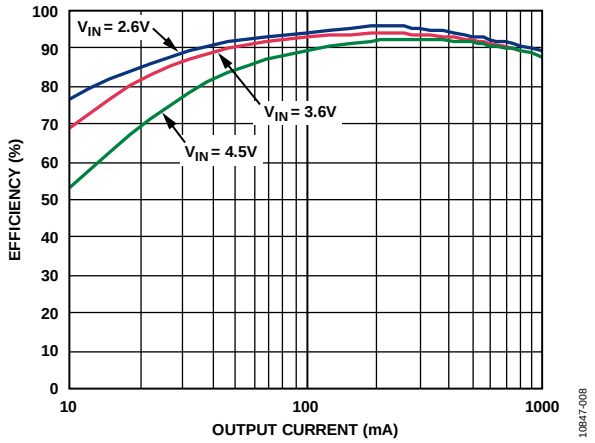


Figure 8. Efficiency, Channel 4, V_{OUT4} = 2.7 V

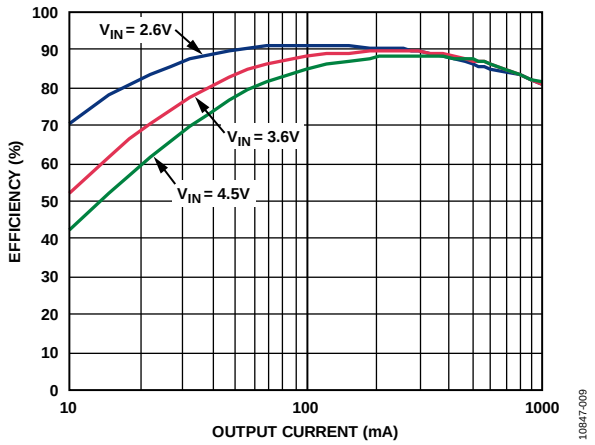


Figure 9. Efficiency, Channel 6, V_{OUT6} = 1.8 V

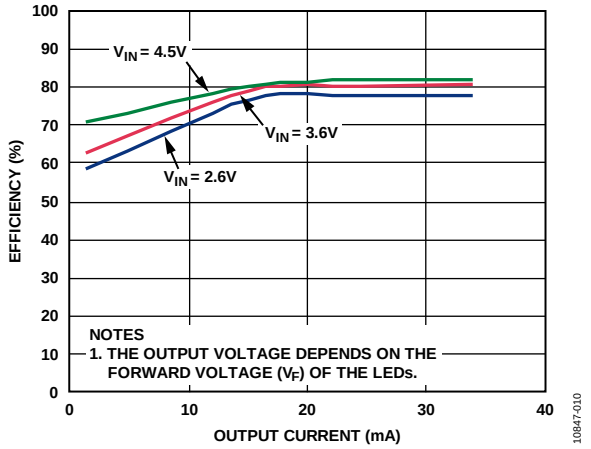


Figure 10. Efficiency, Channel 7 with Four White LEDs Connected in Series (Output Voltage Depends on the Forward Voltage (V_F) of the LEDs)

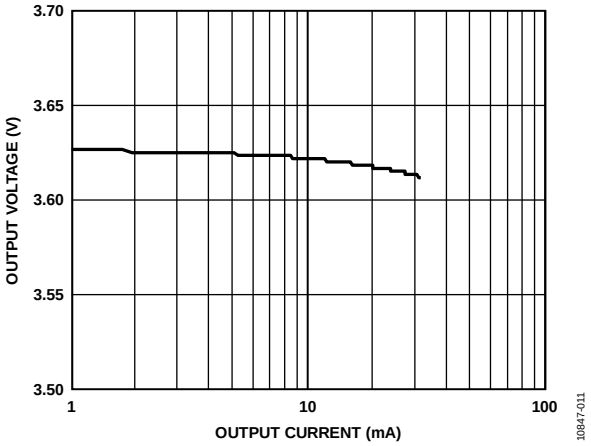


Figure 11. Load Regulation, Channel 1 (PSM), V_{OUT1} = 3.6 V

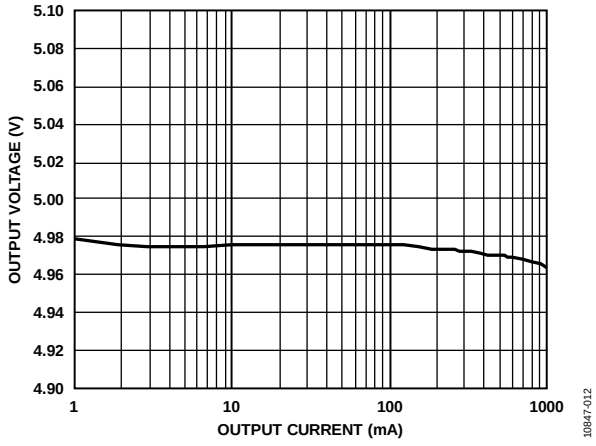


Figure 12. Load Regulation, Channel 1 (PWM), V_{OUT1} = 5.0 V

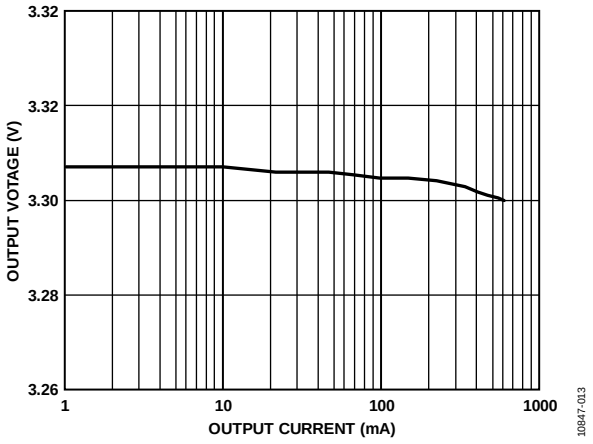


Figure 13. Load Regulation, Channel 2, V_{OUT2} = 3.3 V

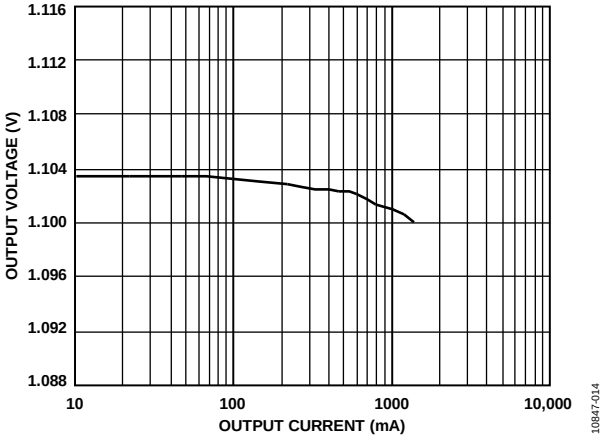


Figure 14. Load Regulation, Channel 3, V_{OUT3} = 1.1 V

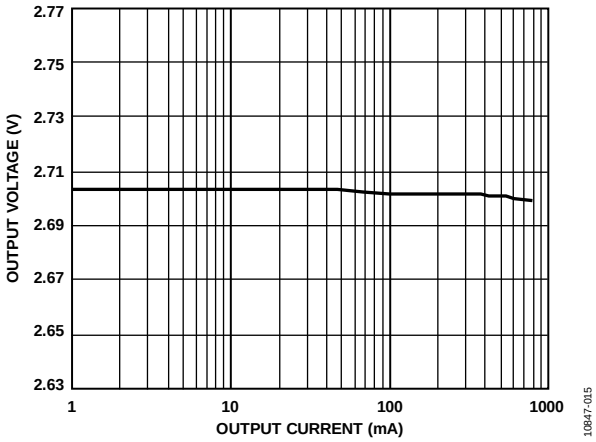


Figure 15. Load Regulation, Channel 4, V_{OUT4} = 2.70 V

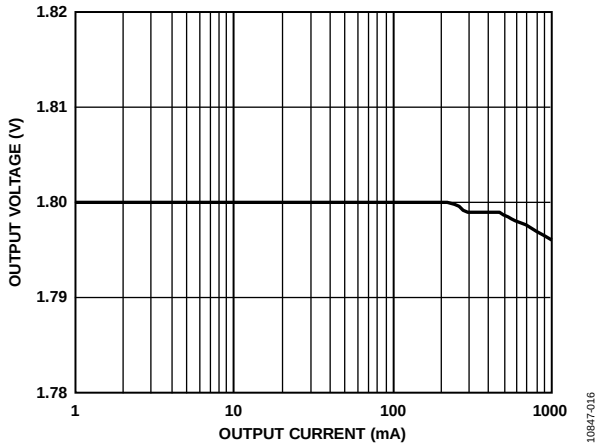


Figure 16. Load Regulation, Channel 6, V_{OUT6} = 1.8 V

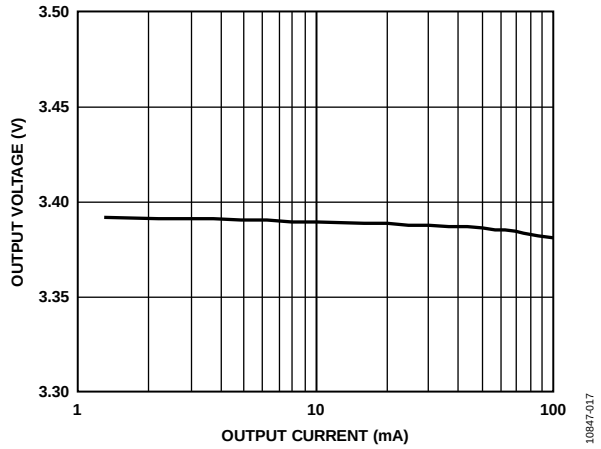


Figure 17. Load Regulation, Channel 8, V_{OUT8} = 3.4 V

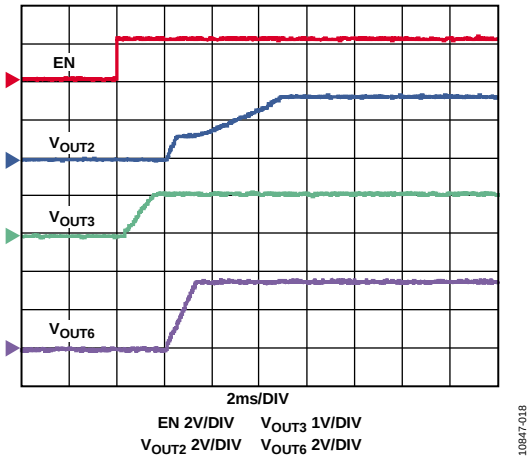


Figure 18. Soft Start, V_{OUT2}, V_{OUT3}, and V_{OUT6}

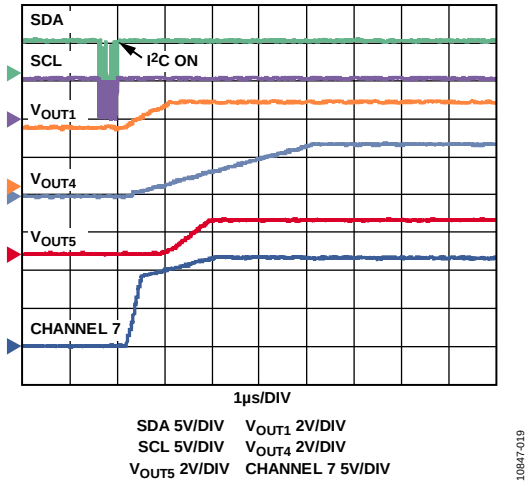


Figure 19. Soft Start, V_{OUT1}, V_{OUT4}, V_{OUT5}, and Channel 7 Output

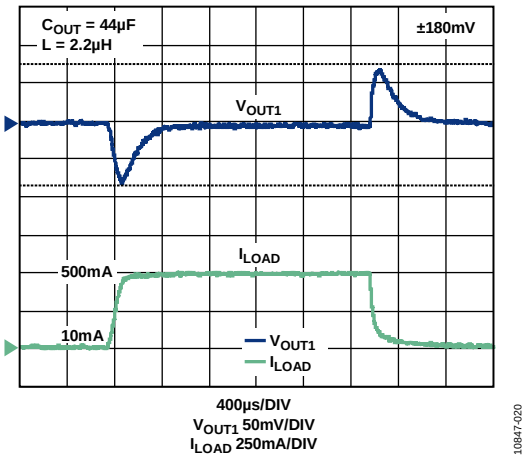


Figure 20. Load Transient Channel 1 (PWM), V_{OUT1} = 5.0 V, 10 mA to 500 mA

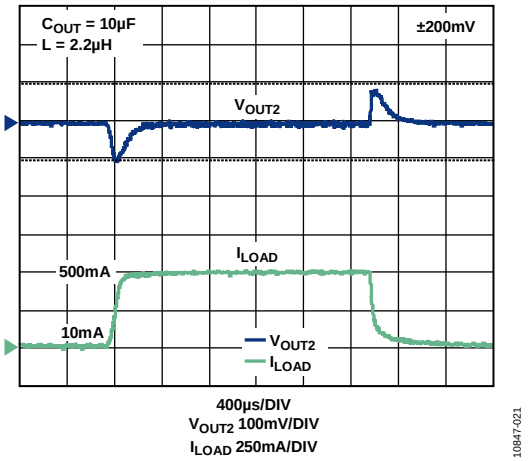


Figure 21. Load Transient Channel 2, V_{OUT2} = 3.3 V, 10 mA to 500 mA

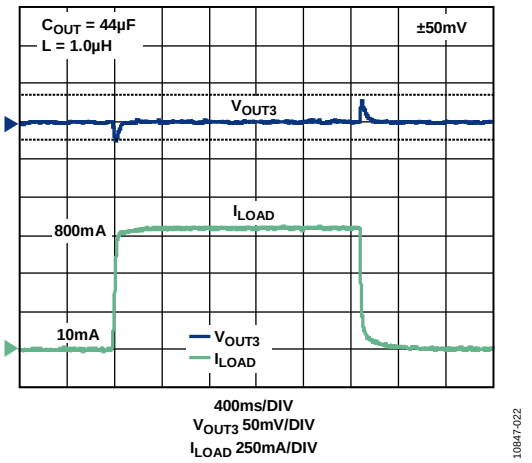


Figure 22. Load Transient Channel 3, V_{OUT3} = 1.1 V, 10 mA to 800 mA

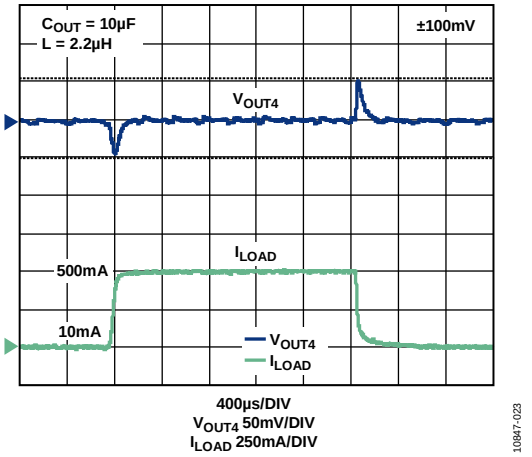


Figure 23. Load Transient Channel 4, V_{OUT4} = 2.7 V, 10 mA to 500 mA

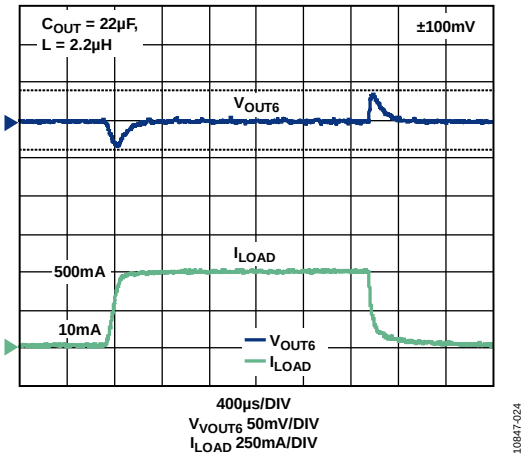


Figure 24. Load Transient Channel 6, V_{OUT6} = 1.8 V, 10 mA to 500 mA

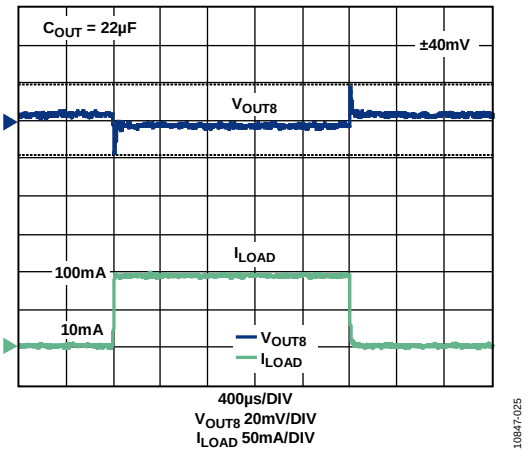


Figure 25. Load Transient Channel 8, V_{OUT8} = 3.4 V, 10 mA to 100 mA

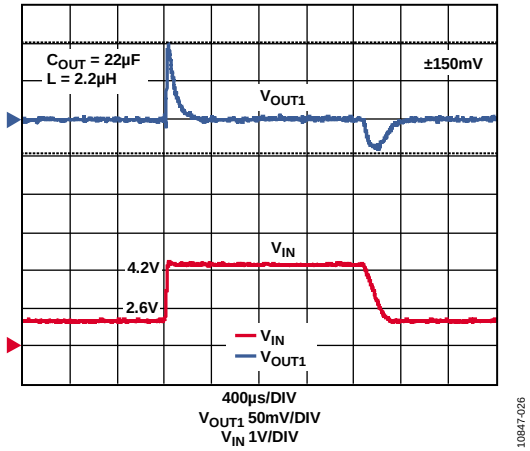


Figure 26. Line Transient, Channel 1 (PWM), V_{OUT1} = 5.0 V, 10 mA

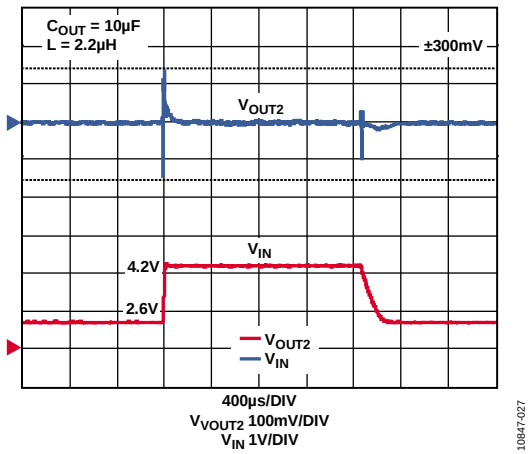


Figure 27. Line Transient, Channel 2, V_{OUT2} = 3.3 V, 10 mA

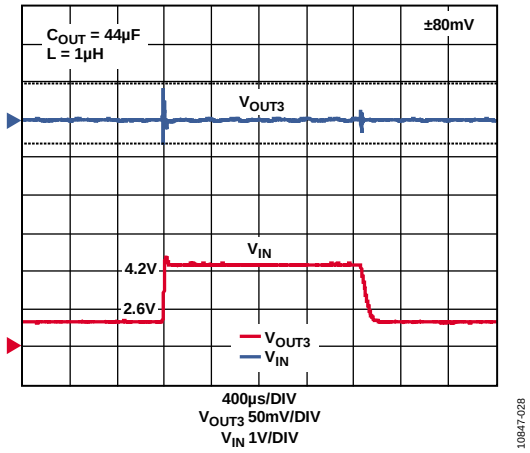


Figure 28. Line Transient, Channel 3, V_{OUT3} = 1.1 V, 10 mA

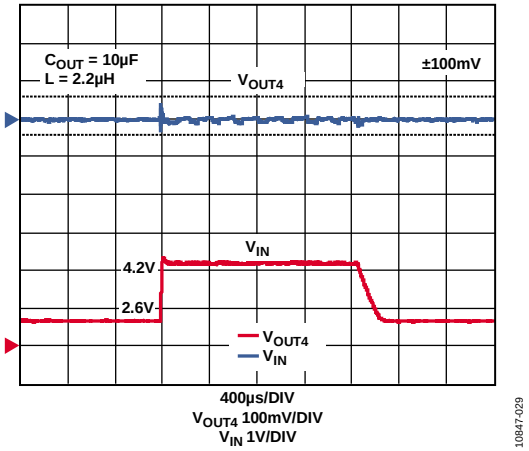


Figure 29. Line Transient, Channel 4, V_{OUT4} = 2.7 V, 10 mA

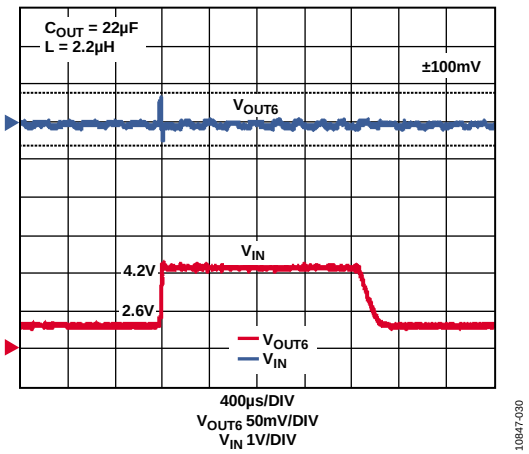


Figure 30. Line Transient, Channel 6, V_{OUT6} = 1.8 V, 10 mA

THEORY OF OPERATION

INTRODUCTION

The ADP5046 is a highly integrated power management unit (PMU) that features six switching regulators, two LDOs, a load switch, a backup battery charger, a real-time clock, and a 32 kHz oscillator. The PMU can be activated by a logic level high on the EN pin or following an alarm event that is generated by the countdown timer.

The ADP5046 also includes a slave-only I^2C interface for communication with an external processor. Through the I^2C interface, it is possible to change parameters, such as the output voltage, soft start, and sequencing of the regulators, and to set the RTC registers and the countdown alarm. Some parameters are factory defined to address different system requirements that must be available before the system powers up and programs the PMU registers. Contact an Analog Devices, Inc., representative for information about the factory programming options that are available.

ENABLE

The enable pin (EN) controls the on and off states of the ADP5046. A high logic level on the EN pin turns the device on, whereas a low logic level turns the device off.

A low-to-high transition on the EN pin starts the activation circuit by enabling the reference block after three 32 kHz clock cycles. Then the activation circuit checks for fault conditions, such as the V_{VDD} voltage being below the threshold, the temperature being too high, the oscillator not running, and the reference voltage being below the nominal level. If no fault is detected, the power-up sequence is generated after the turn-on delay time, which is factory programmed for each regulator channel.

The default power-up sequence of the regulators is Channel 2 first, Channel 3 second, Channel 6 third, and Channel 8 fourth, while Channel 1 stays in PSM mode. No regulator sequence is generated when the device is turned off (EN = low) except the Channel 1 PSM mode. All the active regulators, except Channel 3, are turned off simultaneously. Channel 3 is turned off after the disable delay time (default = 30 ms), upon a high-to-low transition at the EN pin.

The ADP5046 can also turn on after the countdown timer decrements to 0 and an alarm is generated. Then Bit 6 (TIMEOUT) in Register RTCAL_HR (Address 35) is set to 1.

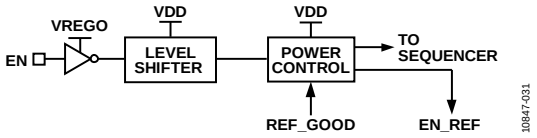


Figure 31. Enable Circuit

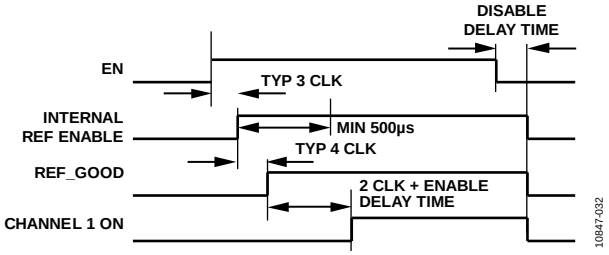


Figure 32. Enable Timings

WAKE-UP SEQUENCE

The ADP5046 wake-up sequence is shown in Figure 33. Wake-up starts when the main battery voltage rises above the system undervoltage level (UVLO_SYS). The ADP5046 remains in standby mode as long as the EN pin is set to a logic level low. In this mode, the PSM boost regulator and the low quiescent current regulator keep alive LDO are active.

A high logic level at the EN pin initiates the turn-on sequence, which starts by checking that there are no fault conditions and that the internal biasing circuits have reached the nominal operating conditions.

If the state machine does not detect a fault condition, the regulator turn-on sequence begins after the enable turn-on delay has elapsed.

The regulators (except Channel 4, Channel 5, and Channel 7) turn on according to the predefined timing sequence. The ADP5046 remains in the wake-up state as long as the EN pin is at logic level high and no undervoltage condition is detected. An undervoltage condition triggers the power-down sequence (instant shutoff system), where the active regulators are turned off and the ADP5046 waits for a new activation from the EN pin.

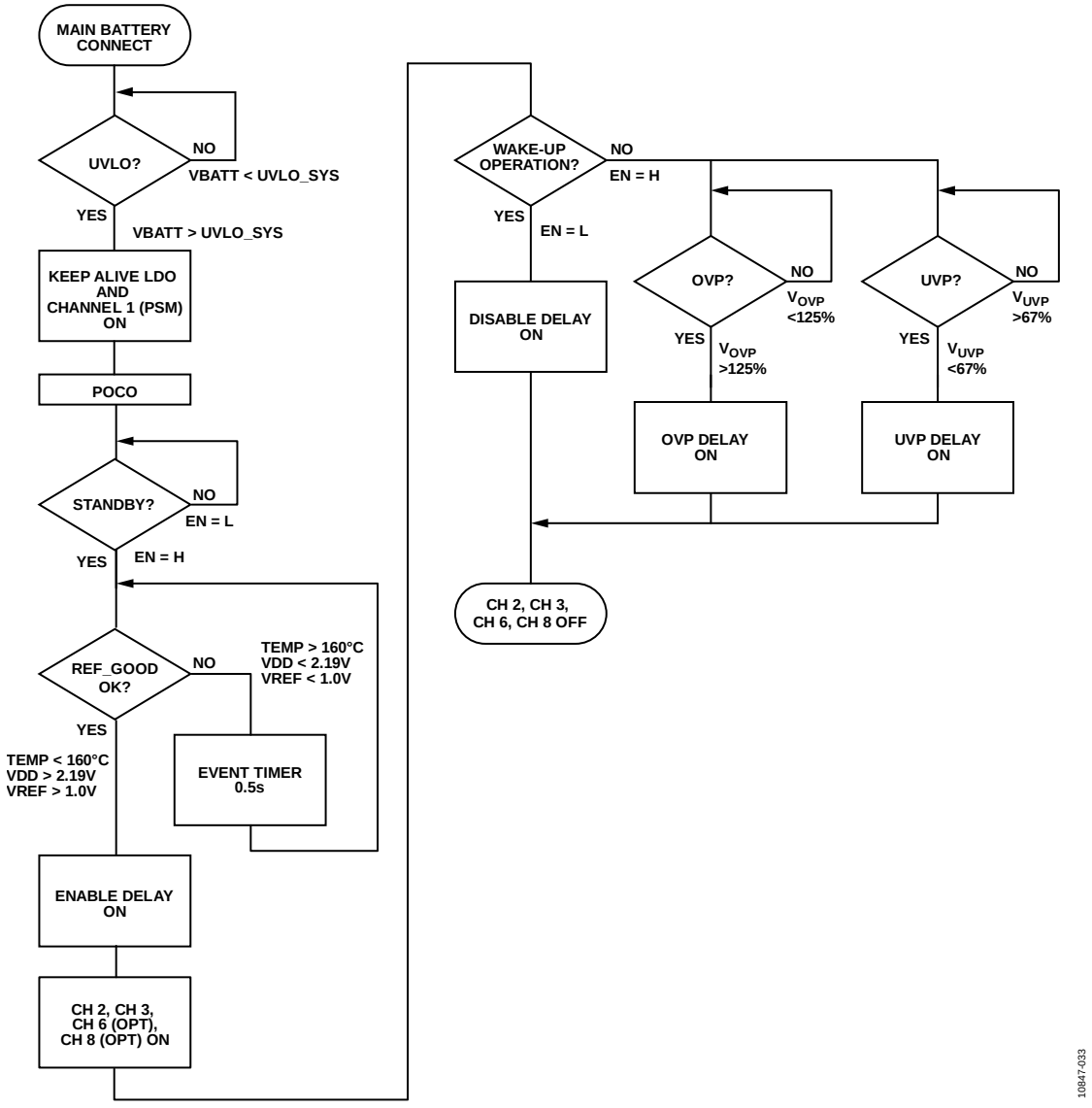


Figure 33. Wake-Up Sequence

REFERENCE BLOCK

The reference block contains the voltage reference circuit. It also monitors the overtemperature, the switching oscillation, the power supply, and the reference voltage; and it is activated by a logic high at the EN pin or by a countdown timer alarm event. The REF_GOOD signal enables the sequencer.

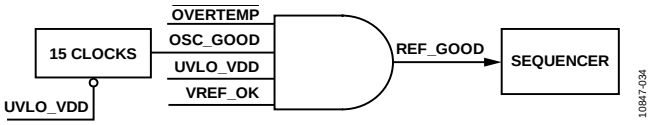


Figure 34. Internal Reference Control

Table 10. Conditions for REF_GOOD Generation

Status Signal	Conditions
OVERTEMP	Overtemperature. High: temperature < 140°C. Low: temperature > 160°C.
OSC_GOOD	Switching oscillation. High: 15 clocks after the V_{VDD} voltage is above the threshold. Low: the oscillator did not start.
UVLO_VDD	Power supply. High: 2.19 V rising. Low: 2.06 V falling.
VREF_OK	Reference voltage. High: reference voltage > 1.00 V.

32 kHz OSCILLATOR

The oscillator circuit uses an external 32.768 kHz crystal and two small capacitors to generate the clock signal that is used as a time base for the RTC block. The buffered 32 kHz clock signal is available at a dedicated pin (CLKO), and it is used as a reference signal for external circuits. The CLKO logic level high is defined by the voltage of the VREGO pin. Note that the ground connection for the two capacitors should be directly to the RTCGND pin and not to any other ground plane on the PCB.

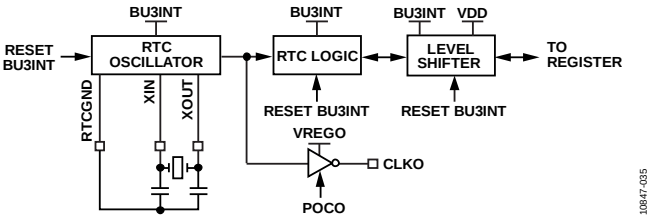


Figure 35. 32 kHz Generation and Distribution

The 32 kHz oscillator has a dedicated calibration register (Register RTCADJ, Address 40) to fine-tune the frequency (see Table 54). The value that is written in Register RTCADJ, Bits[5:0], is the correction amount in parts per million (ppm). The calibration range is ±61 ppm. Bit 6 (ADJS) in Register RTCADJ sets the correction sign (0 = frequency decrease, 1 = frequency increase).

REAL-TIME CLOCK (RTC)

The RTC block keeps track of the elapsed time, and it operates as long as either the main battery voltage (V_{VBATT}) or the backup battery voltage (V_{BU3INT}) is above the respective UVLO level. When the voltage supplying the RTC block is below the under-voltage threshold (UVLO_RTC), all registers are cleared to 0.

The RTC block has 33 bits that are capable of counting up to 100 years. The following registers support the RTC date and time:

- RTCT_SEC for seconds, from 0 to 59
- RTCT_MIN for minutes, from 0 to 59
- RTCT_HR for hours, from 0 to 23
- RTCT_DAY for days, from 0 to 30
- RTCT_MO for months, from 0 to 11
- RTCT_YR for years, from 0 to 127
- RTCT_WK for day of the week, from 0 to 6

The year register (Register RTCT_YR, Address 38) contains the offset value, starting from the Year 2000 (RTCT_YR = 0).

All RTC registers are both read and write. After the first power-up, all RTC registers are set to 0. The RTC block includes leap year adjustments.

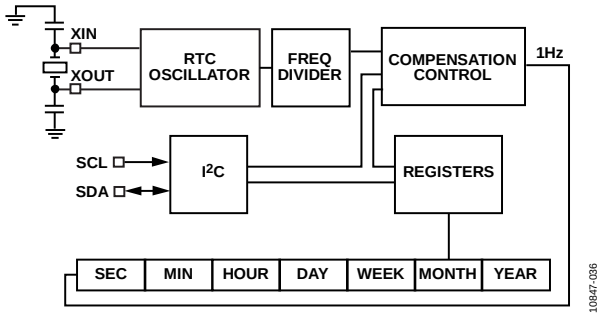


Figure 36. Real-Time Clock Block Diagram

POWER-UP SEQUENCER

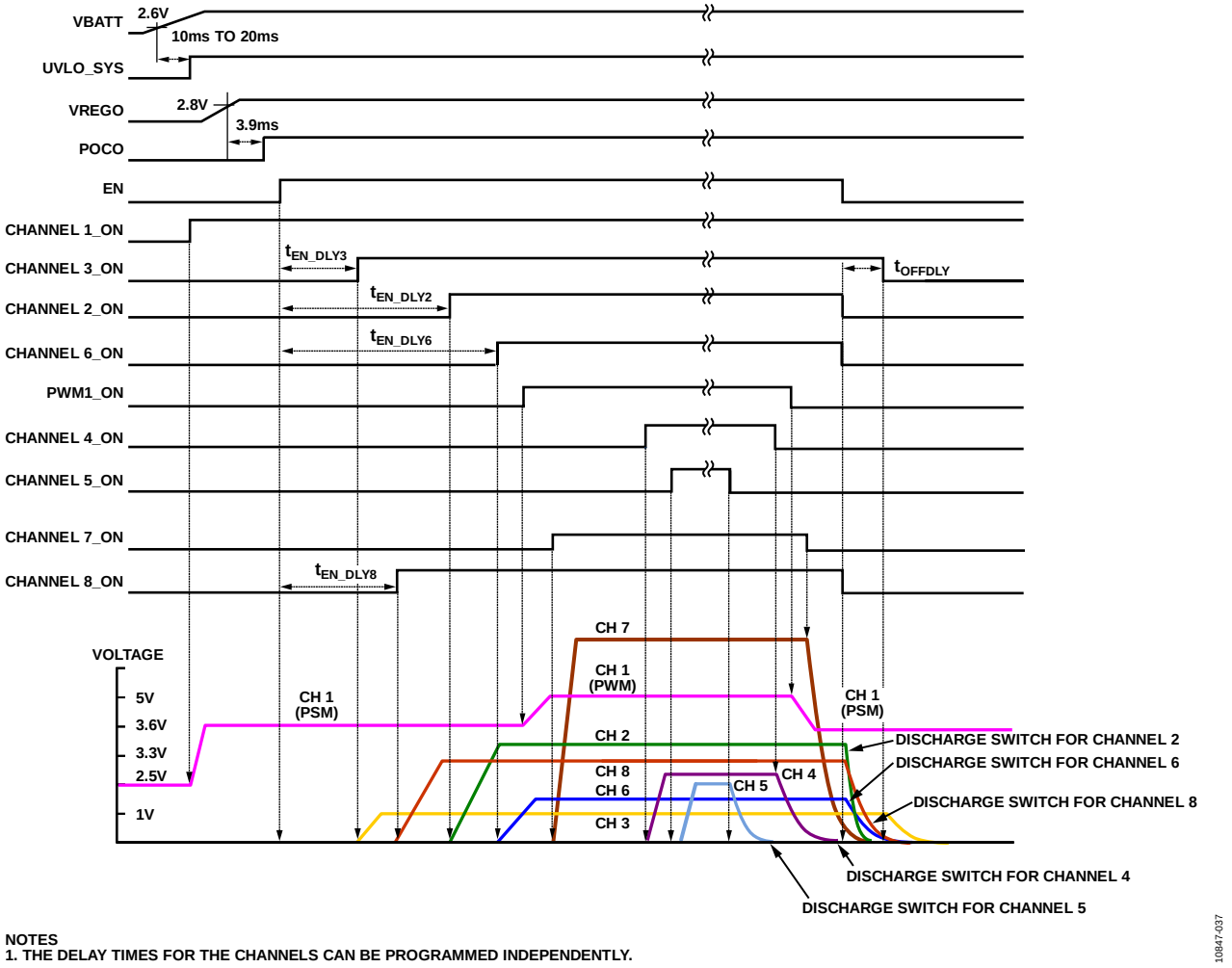
The sequencer block controls the activation and turn-on order of the regulators (see the timing diagram in Figure 37, but note that this timing diagram is just an example).

The activation delays of the regulators are programmable via the following: Register EN_DLY12 (Address 4), Bits[7:4] for Channel 1 and Bits[3:0] for Channel 2; Register EN_DLY36 (Address 5), Bits[7:4] for Channel 3 and Bits[3:0] for Channel 6; and Register EN_DLY8 (Address 6), Bits[7:4] for Channel 8. The delay time ranges from 0 ms to 30 ms in 2 ms steps. When the internal oscillator is used, either the Channel 3 enable delay (EN_DLY3) or the disable delay function must be set to 0 ms.

Each regulator has a programmable soft start; Register SFTTIM (Address 2) controls the soft start for Channel 1 to Channel 7.

The soft start of each regulator can be programmed to two levels (see Table 17 to Table 21). The soft start circuit limits the inrush current when a regulator turns on and the output capacitors are charged. Excessive inrush current can create too much stress on the main battery and decrease the input or battery voltage. The activation for Channel 1 pulse-width modulation (PWM) mode, Channel 4, Channel 5, Channel 6, Channel 7, and Channel 8 is software controlled.

Register PWMCONT (Address 14), Bit 0 (PWM1) is the mode select for Channel 1 PWM/PSM. The on/off controls for Channel 4 to Channel 8 are found in Register PCTRL (Address 32): Bit 4 (CH6_ON) is for Channel 6, Bit 3 (CH8_ON) is for Channel 8, Bit 2 (CH7_ON) is for Channel 7, Bit 1 (CH4_ON) is for Channel 4, and Bit 0 (CH5_ON) is for Channel 5.



NOTES
1. THE DELAY TIMES FOR THE CHANNELS CAN BE PROGRAMMED INDEPENDENTLY.

Figure 37. Power-Up/Power-Down Sequence

COUNTDOWN ALARM TIMER

The countdown timer can be used to periodically enable the system as shown in Figure 38 and Figure 39. Two types of countdown timers are available using the countdown mode register options. Bit 4 (ALMMD) in Register RTCALRMD (Address 62) is set to 1 for the one-shot mode countdown timer, and it is set to 0 for the repeat mode countdown timer. In one-shot mode, the timer counts down once; whereas in repeat mode, the countdown sequence is repeated. The one-shot countdown interval is programmable via the I²C interface in 0.5 sec intervals, up to 31 hours. The repeat countdown interval is programmable via the I²C interface in 0.5 sec intervals, up to 63 minutes.

The one shot countdown alarm timer features three read/write registers that count hours (Register RTCAL_HR, Address 43), minutes (Register RTCAL_MIN, Address 42), and seconds (Register RTCAL_SEC, Address 41).

The values programmed in these three registers are decremented at a rate of 0.5 sec. The repeat countdown alarm timer features two read/write registers that set the repeat period of minutes (Register RTCALR_MIN, Address 61) and seconds (Register RTCALR_SEC, Address 60). The values programmed in these two registers are copied to the RTCAL_MIN and RTCAL_SEC registers Then these two registers are both decremented to 0, and Register RTCAL_HR is set to 0.

The autoenable feature wakes up the ADP5046 without EN being set to logic level high. A factory-set trim option controls the autoenable feature: Option 1 uses the autoenable feature; Option2 does not. The autoenable feature can also be controlled via the I²C interface (see Table 67 and Table 68).

When the autoenable feature is used (Option 1), the timer begins to count down when Bit 0 (ALMST) in the RTCALRMD register is set to 1. Bit 6 (TIMEOUT) in the RTCAL_HR register is set to 1 when the three countdown alarm timers reach 0, and the setting remains unchanged until 0 is overwritten by I²C.

When the autoenable feature is not used (Option2), the timer begins to count down when Bit 0 (ALMST) in the RTCALRMD register is set to 1. When the three countdown alarm timers reach 0, Bit 6 (TIMEOUT) in the RTCAL_HR register is set to 1 for 125 ms to ~250 ms. A read operation of the countdown register reports the current state of the countdown timer.

The status of the timeout bit is replicated as an alarm signal at the ALMO pin (see Figure 38 and Figure 39).

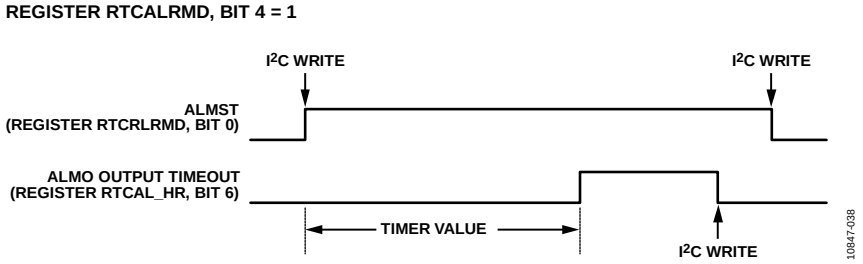


Figure 38. One-Shot Mode Alarm Generation

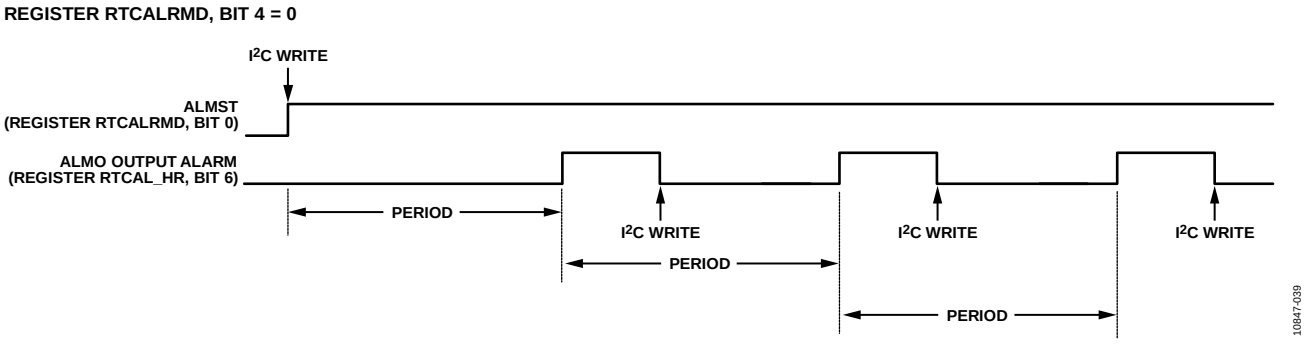


Figure 39. Repeat Mode Alarm Generation

UNDERVOLTAGE PROTECTION (UVP) AND OVERVOLTAGE PROTECTION (OVP)

Channel 2, Channel 3, Channel 6, and Channel 8 have individual undervoltage detection and status flags in Register UVPST at Address 12 (Bit 7, Bit 5, Bit 2, and Bit 1). In addition, Channel 2, Channel 3, Channel 6, and Channel 7 have individual overvoltage detection and status flags in Register OVPST at Address 13 (Bits[2:1] for Channel 3 and Channel 2, respectively; and Bits[6:5] for Channel 7 and Channel 6, respectively). Channel 4 has a fault status flag (Bit 3 in the UVPST register) that can indicate both UVP and OVP status.

An undervoltage condition occurs when a regulator output voltage falls below the regulation value for a time that is longer than the undervoltage detection delay.

The UVP thresholds for Channel 2, Channel 3, Channel 4, Channel 6, and Channel 8 are 67% of their respective nominal output voltage. The undervoltage detection delay is factory programmed, and it can be set to 0 ms (no delay), 78 ms, 200 ms, or disabled (no undervoltage detection).

If an undervoltage event is detected on Channel 2, Channel 3, Channel 6, or Channel 8, all the enabled channels are turned off and the affected channel status flag in the UVPST register (Bit 1 for Channel 2, Bit 2 for Channel 3, Bit 5 for Channel 6, and Bit 7 for Channel 8) is reset. The UVPST register is cleared after its content is read once, and then the state machine waits for the enable input pin (EN) to be set low.

If either an undervoltage or overvoltage event is detected on Channel 4, both Channel 4 and Channel 5 are turned off.

Channel 2, Channel 3, Channel 6, and Channel 7 have individual overvoltage detection and status flags in the OVPST register (Bits[2:1] for Channel 3 and Channel 2, respectively; and Bits[6:5] for Channel 7 and Channel 6, respectively). An overvoltage condition occurs when a regulator output voltage is greater than the regulation threshold for a time longer than the overvoltage detection delay.

Channel 7 is turned off and the status flag (Register OVPST, Bit 6) is set if an overvoltage event is detected at its output. The OVPST register is cleared after its content is read once. OVP can be triggered regardless of the status register content.

If an overvoltage event is detected on Channel 2, Channel 3, or Channel 6, all of the enabled channels are turned off and the affected channel status flag in Register OVPST (Bit 1 for Channel 2, Bit 2 for Channel 3, and Bit 5 for Channel 6) is set. The OVPST register is cleared after its content is read once, and then the state machine waits for the enable input pin (EN) to be set low.

The overvoltage detection delay is factory programmed and can be set to 0 ms (no delay), 1.2 ms, 3.3 ms, or disabled (no overvoltage detection). The overvoltage detection delay setting is also valid for the undervoltage detection delay for Channel 4. In other words, the setting of undervoltage detection delay is not applied to Channel 4.

The OVP thresholds for Channel 2, Channel 3, Channel 4, and Channel 6 are 125% of their nominal output voltage. The OVP for Channel 7 is monitored at the OVP7 pin, and the threshold is 24.3 V typical.

Table 11. UVP and OVP Mapping for Each Channel[1]

	CH 1	CH 2	CH 3	CH 4	CH 5	CH 6	CH 7	CH 8
UVP	No	Yes	Yes	Yes	No	Yes	No	Yes
OVP	No	Yes	Yes	Yes	No	Yes	Yes	No

[1] A yes means that this feature is available; a no means that it is not available.

VREGO KEEP ALIVE LDO CIRCUIT

The voltage of the VREGO pin is regulated by the keep alive LDO to have a fixed output voltage of 3.2 V, which is used for powering up the internal RTC. It can also be used for supplying power to external components, such as a microcontroller.

The maximum current that can be derived from VREGO is 50 mA.

The keep alive LDO stays on even when the ADP5046 is disabled. Only the UVLO_SYS circuit can disable this regulator. When the keep alive LDO regulator is disabled and the VREGO is at the off state, the discharge switch is turned on.

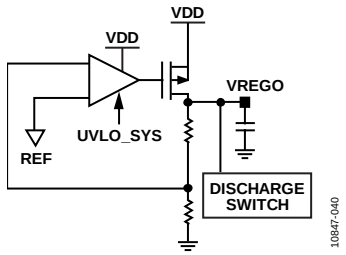


Figure 40. Keep Alive LDO Circuit

UVLO_SYS CIRCUIT

The UVLO_SYS circuit detects a low supply voltage from the main battery. The output signal from this circuit enables the VREGO keep alive LDO circuit and the Channel 1 PSM boost regulator.

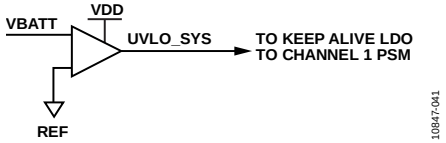


Figure 41. UVLO_SYS Circuit

UVLO_RTC CIRCUIT

The UVLO_RTC circuit detects a low supply voltage of the RTC block and the backup registers. When the voltage at the BU3INT pin falls below the UVLO_RTC threshold, the RTC and the backup registers are reset.

SYSTEM RESET FOR EXTERNAL PROCESSOR (POCO)

The ADP5046 has a low quiescent current power save mode (PSM) boost regulator to maintain the voltage of the VDD pin above 3.6 V. Therefore, the keep alive LDO output (VREGO) can consistently supply a stable 3.2 V to external circuits that are always on, such as a microprocessor. The POCO signal can be used as a reset signal to these circuits. The internal POCO comparator monitors the voltage of the VREGO pin. If V_{VREGO} rises above 2.8 V, the POCO output is set to high after a 4 ms delay. When the V_{VREGO} voltage falls below 2.6 V, the POCO output immediately goes low.

BACKUP BATTERY CHARGER

The backup battery charger is included to charge the external backup battery (either a PAS614 from Shoei Co., Ltd. or an MS614SE from Seiko Instruments Inc. is recommended) or a super capacitor. The 3 V LDO, located between VREGO and BU3INT (see Figure 42), regulates the V_{BU3INT} voltage to 3 V. The 3 V LDO output is connected to the BU3INT pin through the PMOS switch, M1. After the V_{VREGO} voltage rises above the POCO threshold, the 3 V LDO and the M1 switch are turned on sequentially with a delay of 4 ms.

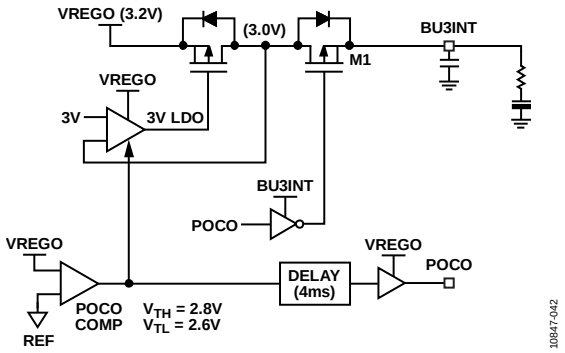


Figure 42. Backup Battery Block Circuit

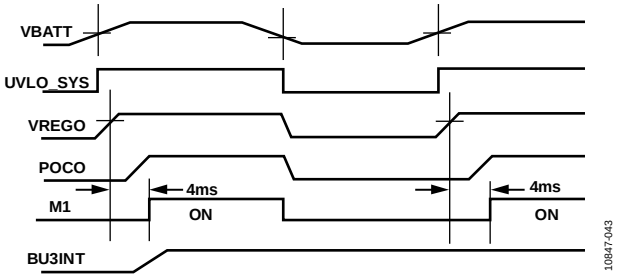


Figure 43. Backup Battery Charger Timing

When the V_{VBATT} voltage falls below 2.4 V, the 3 V LDO and the M1 switch are immediately turned off to prevent any discharge from the backup battery.

BACKUP MEMORY

The ADP5046 includes a 64-bit backup memory that is accessible via the I²C interface. The power source for these registers is the same as the power source for the RTC. As long as the backup battery is alive or there is a main power supply, the data in the backup memory is retained. All data in the backup registers is cleared when the UVLO_RTC signal goes low.

I²C INTERFACE

Access to the internal registers is available using the I²C interface. This serial interface has two dedicated pins: SDA, an open-drain line for receiving and transmitting data; and SCL, an input line for receiving the clock signal. Both lines must be terminated with pull-up resistors to the VDDIO supply. Serial data is transferred at the SCL rising edge. The read data is generated at the SDA pin in read mode.

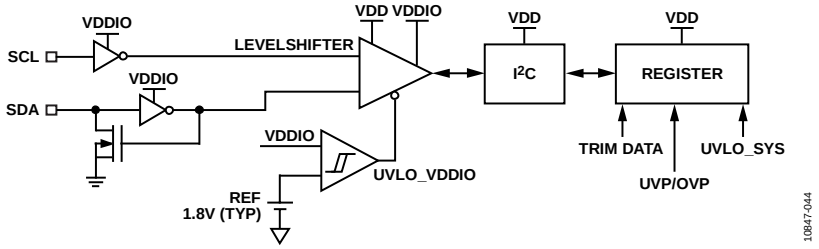


Figure 44. I²C Interface Block Diagram

I²C Interface Timing

The ADP5046 includes an I²C-compatible serial interface for control of the power management blocks and for reading back the RTC registers and system status. The I²C chip address is 0x30 (0011 0000 (binary) in write mode), and the subaddress is used to select any of the user registers that are implemented. The ADP5046 sends the data from the register denoted by the subaddress. Note that the ADP5046 does not respond to general calls. The ADP5046 accepts multiple masters, but if the device is in read mode, this access is limited to one master until the data transmission is complete. Table 12 shows a complete map of the available registers. See Figure 45 for a write mode timing diagram; Figure 46 and Figure 47 show diagrams of read mode timing. The I²C interface operates at clock frequencies of up to 400 kHz.

The registers from Address 32 to Address 62 have a special status flag (Bit 7) that can be read to determine if valid data is present in the register. If the status bit is 0, the data is not yet valid; therefore, the read operation must be repeated until the status bit changes to 1, indicating that the data is valid. Before the status bit changes to 1, a minimum of two read operations is required. The required number of reads depends on the relationship between the RTC clock frequency and the SCL frequency. For example, when the SCL frequency is 400 kHz, the minimum number of reads is approximately 6.

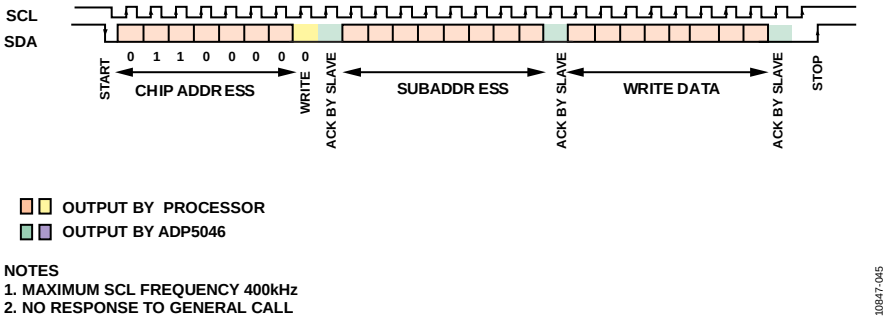


Figure 45. I²C Write to Registers

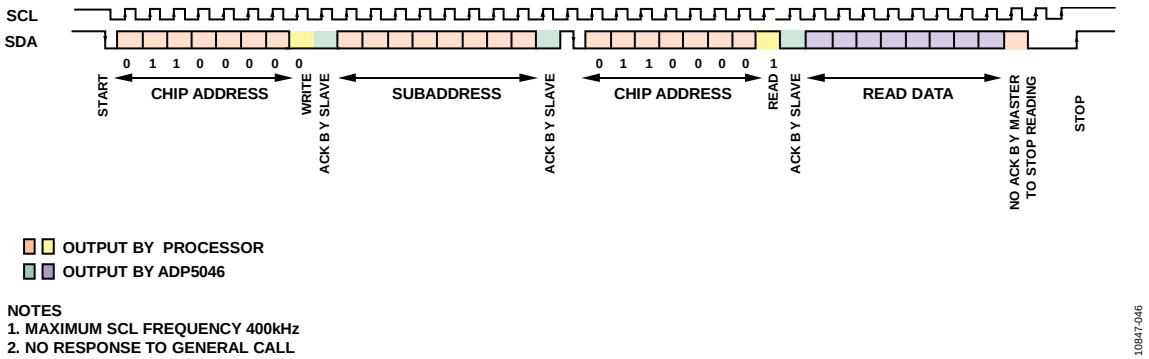


Figure 46. I²C Read from Registers with No Read Status Bits

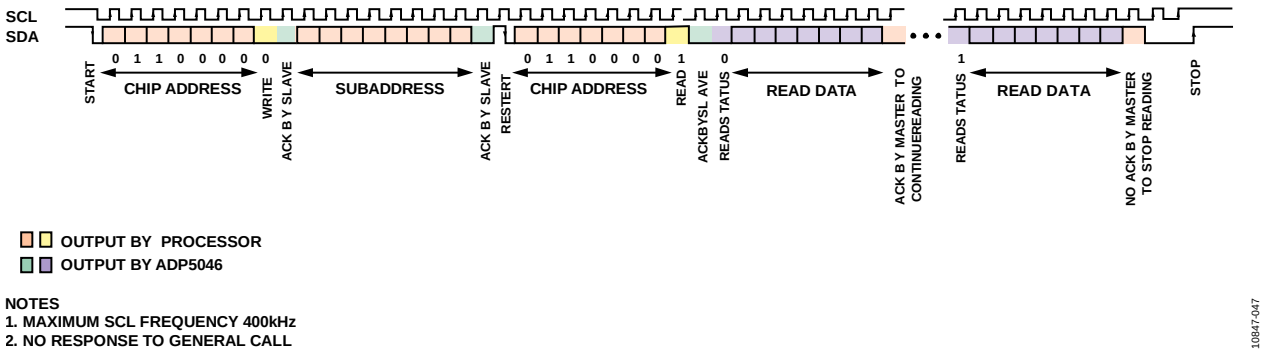


Figure 47. I²C Read from Registers with Read Status Bits

VOLTAGE REGULATOR BLOCK

Channel 1 Boost Regulator

The Channel 1 boost regulator provides a regulated output voltage (higher than the input voltage) that is applied to one side of the inductor. Channel 1 features adaptive on-time gated-oscillator control in PSM mode and Flex-Mode™ current mode control in PWM mode. The default output voltage in PSM mode is 3.6 V, and the default output voltage in PWM mode is factory programmed from 3.8 V to 5.3 V. PSM mode can deliver up to 30 mA at a 2.4 V V_{VBATT} voltage condition. PWM mode can deliver up to a 1.2 A output current at a typical V_{VBATT} voltage condition of 3.6 V. It is recommended that the voltage supply for the VDD pin be applied from the Channel 1 output.

The adaptive on-time gated-oscillator control provides high efficiency at light load conditions and a coarsely regulated 3.6 V to the keep alive LDO regulator through the VDD pin. Therefore, the control is suitable for a system that requires constant voltage on the VREGO pin even in an EN = low condition. To ensure the 30 mA maximum output current, the on time is controlled by monitoring the V_{VBATT} voltage. The Flex-Mode current mode control provides synchronous boost architecture with integrated FETs for optimal efficiency and fast response to load changes. The boost operates at a 2.5 MHz or 1.25 MHz switching frequency in forced PWM mode.

Register PWMCONT, Bit 0 (PWM1) at Address 14 defines the control mode. When Bit 0 is set to 0, Channel 1 operates in PSM mode. When Bit 0 is set to 1, Channel 1 operates in PWM mode. A high-to-low transition on the EN pin does not clear the data in Bit 0 in Register PWMCONT unless a 0 is written into this register through the I^2C interface. Channel 1 stays in PWM mode when the EN pin is set to logic level high. The host processor can override the default values for the output voltage, the internal soft start time, and the factory-programmed start-up delay time by sending I^2C commands.

Channel 1 soft start is affected by the voltage that precharges the output capacitor connected to VOUT1. This occurs because the synchronous PFET body diode is forwardbiased, connecting the battery voltage to VOUT1. Therefore, the actual soft start time is shorter when the battery voltage is high.

The Channel 1 regulator soft start ramp is controlled by Bit 7 in Register SFTTIM at Address 2 (see Table 16, Table 17, and Table 18). The Channel 1 regulator turn-on delay is controlled by Bits[7:4] in Register EN_DLY12 at Address 4 (see Table 22, Table 23, and Table 24). The output voltage level for Channel 1 is controlled by Bits[6:4] in Register VID12 at Address 8 (see Table 34 and Table 35).

The boost regulator requires only one small external inductor and the input and output ceramic capacitors for bypassing and filtering purposes. The output voltage is sensed directly on the two VOUT1 pins, and an internal voltage divider is used to set the output voltage and to close the regulation loop. The current mode regulation circuit derives the inductor current from the internal FET, adding a compensation ramp from the oscillator circuit. The resultant signal controls the regulation loop in a cycle-by-cycle fashion. Channel 1 is protected against overcurrent and overtemperature.

However, a path from VBATT to VOUT1 still exists through the inductor and the synchronous PFET body diode. Therefore, it is recommended that an input fuse be used to protect the ADP5046 from damage due to a short to ground. The soft start circuit ensures that the input and output currents increase gradually when the regulator is turned on, avoiding stress on the battery. The soft start is programmable to two values.

When the input voltage is approximately equal to or below the output voltage level, the PFET is always on and the circuit cannot regulate the output voltage. In this situation, the output voltage equals the input voltage minus the resistive drop on the PFET and the inductor.

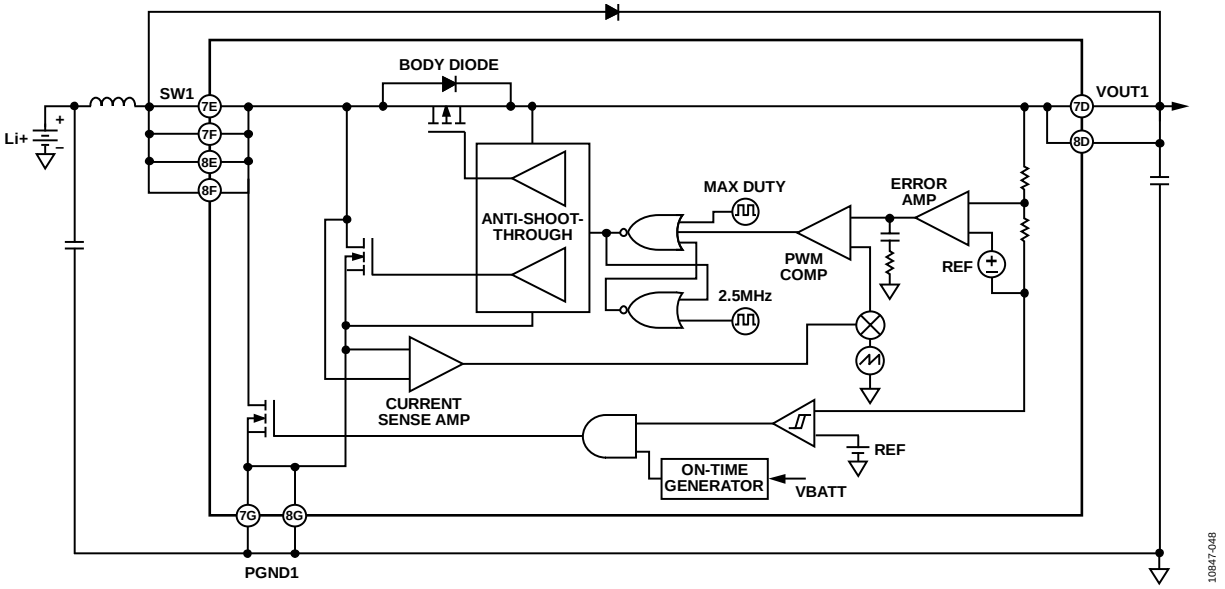


Figure 48. Channel 1 Boost Regulator Block Diagram

Channel 2 Buck-Boost Regulator

The Channel 2 buck-boost regulator provides a regulated output voltage that is higher or lower than the input voltage (PVIN2). The default output voltage is 3.3 V, but the output voltage can be programmed via the I²C interface (see Table 34 and Table 36). Channel 2 can deliver up to 0.9 A of current at a typical VBATT condition of 3.6 V

When PVIN2 voltage is significantly lower than VOUT2, Channel 2 is in boost mode. In boost mode, PMOS1 is always enabled and NMOS1 is always disabled. The inductor is charged when NMOS2 is enabled and PMOS2 is disabled, and it is discharged to the load and output capacitor when PMOS2 is enabled and NMOS2 is disabled. The duty cycle of NMOS2 determines the boost ratio and, therefore, the output voltage.

When PVIN2 is approximately equal to VOUT2, Channel 2 is in buck-boost mode. In this mode, the two operations—buck (PMOS1 and NMOS1 switching in antiphase) and boost (NMOS2 and PMOS2 switching in antiphase)—take place at each period of the clock. This process maintains the regulation and keeps a minimal current ripple in the inductor to guarantee good transient performance. Regarding the external components that are used on Channel 2, it is recommended that the inductor value be less than or equal to 2.2 µH with small DCR and that the output capacitor value be larger than 20 µF.

The buck-boost regulator operates at a 2.5 MHz switching frequency in forced PWM mode. The host processor can override the default values for the output voltage, the internal soft start time, and the factory-programmed start-up delay time by sending I²C commands. An internal discharge resistor, if enabled, guarantees full discharge of the output capacitor when the regulator is turned off.

The regulator discharge switch for Channel 2 is controlled by Bit 3 in Register DSCG at Address 1 (see Table 14 and Table 15). The regulator soft start ramp for Channel 2 is controlled by Bit 6 in Register SFTTIM at Address 2 (see Table 16, Table 17, and Table 20). The regulator turn-on delay for Channel 2 is controlled by Bits[3:0] in Register EN_DLY12 at Address 4 (see Table 22, Table 23, and Table 24). The output voltage level for Channel 2 is controlled by Bits[2:0] in Register VID12 at Address 8 (see Table 34 and Table 36). The undervoltage protection status for Channel 2 can be tested by reading Bit 1 in Register UVPST at Address 12 (see Table 45 and Table 46). The overvoltage protection status for Channel 2 can be tested by reading Bit 1 in Register OVPST at Address 13 (see Table 47 and Table 48).

The buck-boost regulator requires only a small external inductor and input and output ceramic capacitors for bypassing and filtering purposes. The output voltage is sensed directly at the VOUT2 pins, and an internal voltage divider is used to set the output voltage and to close the regulation loop. The current mode regulation circuit derives the inductor current from the internal FET (that is, the boost side), adding a compensation ramp from the oscillator circuit. The resultant signal controls the regulation loop in a cycle-by-cycle fashion. Channel 2 is protected against overload, overtemperature, undervoltage, and overvoltage, with an overvoltage and/or undervoltage fault bit that puts the ADP5046 into the shutdown state.

The soft start circuit ensures that the input and output currents increase gradually when the regulator is turned on, avoiding stress on the battery. The soft start is programmable to two values.

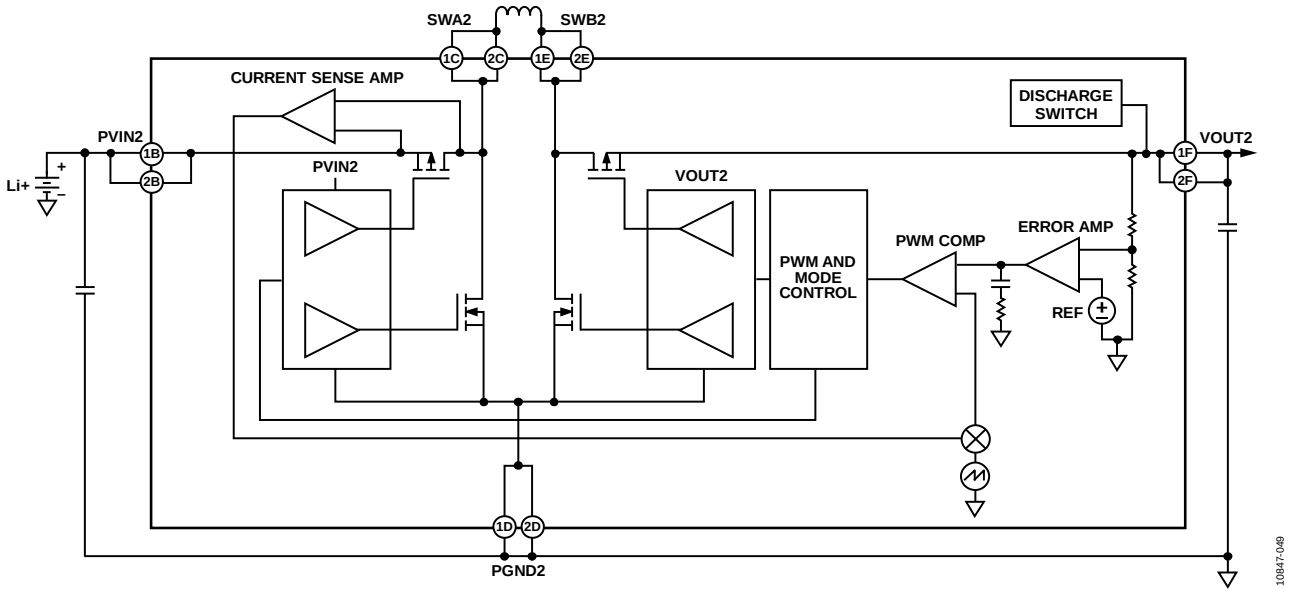


Figure 49. Channel 2 Buck-Boost Regulator Block Diagram

Channel 3 Buck Regulator

The Channel 3 buck regulator is a highly efficient, step-down dc-to-dc converter that utilizes a high speed, fixed-frequency current mode architecture. No external compensation is needed. Channel 3 maintains a constant output voltage, regardless of load, by adjusting the peak inductor current threshold and the duty cycle of the power switches. At the start of each oscillator cycle, the PFET switch is turned on, sending a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current threshold, which turns off the PFET switch and turns on the NFET synchronous rectifier. This sends a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle.

Channel 3 has protection circuitry to limit the amount of positive current flowing through the PFET switch and the synchronous rectifier. The current limit on the power switch limits the amount of current that can flow from the input to the output. The output voltage of Channel 3 is programmable via the I²C interface (see Table 37 and Table 38).

Channel 3 includes an internal soft start function that ramps the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This prevents possible input voltage drops when a battery is connected to the input of the converters. The soft start time can be programmed through the I²C interface and selected from 1.3 ms or 4 ms (see Table 16, Table 17, and Table 18).

The overvoltage or undervoltage status of each channel can be read back through the I²C interface.

The regulator turn-on delay for Channel 3 is controlled by Bits[7:4] in Register EN_DLY36 at Address 5 (see Table 25, Table 26, and Table 27). The regulator turn-off delay for Channel 3 is controlled by Bits[2:0] in Register DIS_DLY3 at Address 7 (see Table 31, Table 32, and Table 33). The output voltage level for Channel 3 is controlled by Bits[7:4] in Register VID34 at Address 9 (see Table 37 and Table 38). The undervoltage protection status for Channel 3 is confirmed by Bit 2 in Register UVPST at Address 12 (see Table 45 and Table 46). The overvoltage protection status for Channel 3 can be tested by reading Bit 2 in Register OVPST at Address 13 (see Table 47 and Table 48).

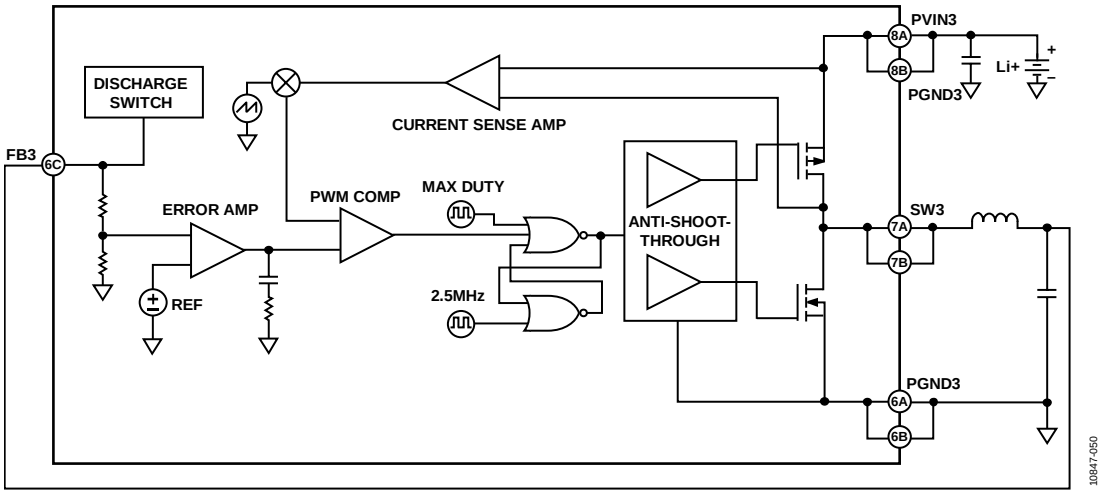


Figure 50. Channel 3 Buck Regulator Block Diagram

Channel 4 Buck Regulator

The Channel 4 buck regulator is a highly efficient step-down dc-to-dc converter that utilizes a high speed, fixed-frequency current mode architecture. No external compensation is needed. The regulator maintains a constant output voltage regardless of load by adjusting the peak inductor current threshold and the duty cycle of the power switches. At the start of each oscillator cycle, the PFET switch is turned on, sending a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current threshold, which turns off the PFET switch and turns on the NFET synchronous rectifier. This sends a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle.

Channel 4 has protection circuitry to limit the amount of positive current flowing through the PFET switch and the synchronous rectifier. The positive current limit on the power switch limits the amount of current that can flow from the input to the output.

The output voltage of Channel 4 is programmable through the I^2C interface (see Table 37 and Table 39). The Channel 4 block has an adjustable mode, as well, that can be programmed externally through a resistor divider to a value between 0.5 V and $V_{IN} \times 0.95$. Note that an output voltage setting that is too low (for example, 0.5 V) may go out of regulation at high V_{IN} conditions due to the minimum time limitation of Channel 4.

Channel 4 includes an internal soft start function that ramps the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This prevents possible input voltage drops when a battery is connected to the input of the converter. The soft start time can be programmed through the I^2C interface and set to 1.3 ms or 4 ms.

Channel 4 can start up from any voltage between 0 V and the final target output voltage without discharging output capacitor charge at the beginning of the soft start.

When Channel 4 is disabled, there is an option to automatically discharge the converter output capacitor though a discharge switch. This discharge function can be enabled through the I^2C interface.

The overvoltage or the undervoltage status of each channel can be read back through the I^2C interface.

The regulator discharge switch for Channel 4 is controlled by Bit 4 in Register DSCG at Address 1 (see Table 14 and Table 15). The regulator soft start ramp for Channel 4 is controlled by Bit 4 in Register SFTTIM at Address 2 (see Table 16, Table 17, and Table 18).

The output voltage level of Channel 4 is controlled by Bits[1:0] in Register VID34 at Address 9 (see Table 37 and Table 39). The undervoltage and the overvoltage protection status for Channel 4 is confirmed by Bit 3 in Register UVPST at Address 12 (see Table 45 and Table 46).

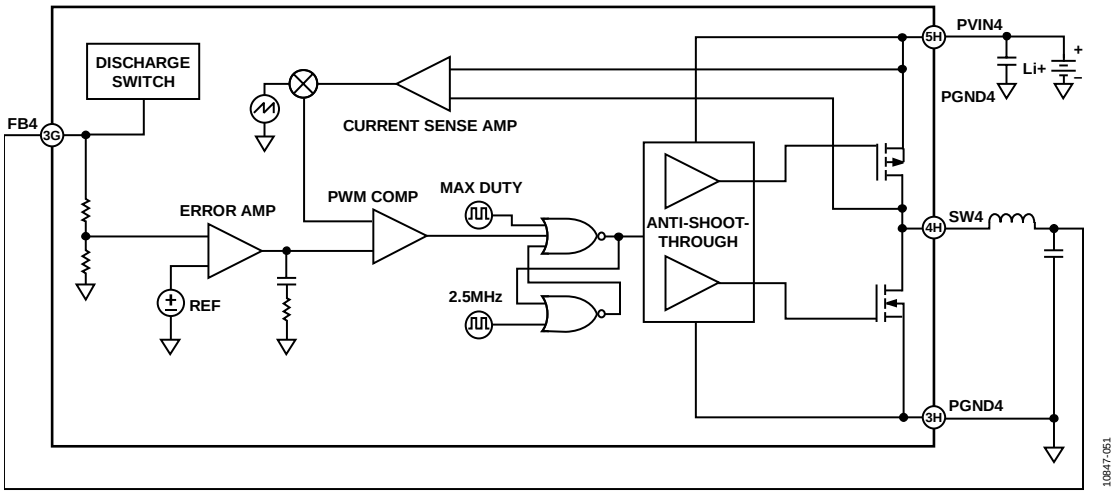


Figure 51. Channel 4 Buck Regulator Block Diagram

Channel 5 Load Switch

Channel 5 is a low R_{ON} switch featuring an internal soft start function that ramps the output voltage in a controlled manner upon startup, thereby limiting the inrush current.

The load switch on/off activation is controlled by Register PCTRL, Bit 0, at Address 32 (see Table 51 and Table 52).

When Channel 5 is disabled, there is an option to automatically discharge the output capacitor though a discharge switch. The discharge switch is controlled by Bit 1 in Register DSCG at Address 1 (see Table 14 and Table 15).

The soft start uses two regions to reach the desired voltage: the soft start delay region (t_{SS_DLY}) and the soft start ramp-up region (t_{SS_RAMP}), as shown in Figure 52.

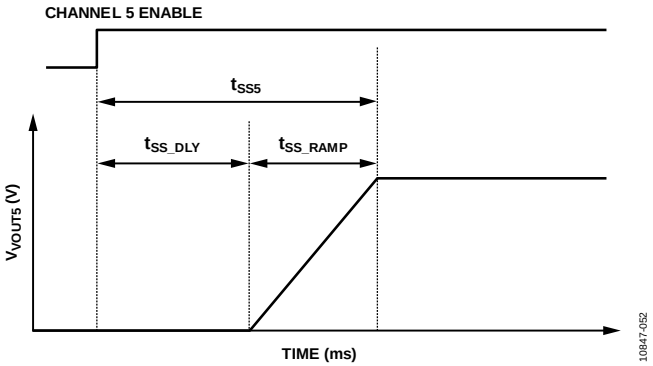


Figure 52. Load Switch Soft Start Timing

The total start-up time (t_{SS5}) is defined by Equation 1, as follows:

$$t_{SS5}\,(\text{ms}) = t_{SS\_DLY} + t_{SS\_RAMP} \quad (1)$$

Soft start is controlled by Bit 3 in Register SFTTIM at Address 2 (see Table 16, Table 17, and Table 19).

An external capacitor can be used at the output node for noise filtering purposes in noise-sensitive applications (see Figure 53). To guarantee low on resistance at the switch, the voltage at the VIN5 pin must be at least 0.9 V lower than the voltage at the VDD pin. Note that the absolute maximum rating of VIN5 is 3.6 V.

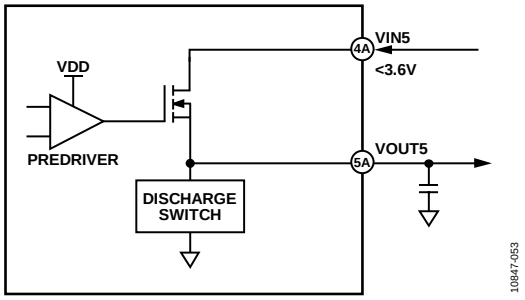


Figure 53. Channel 5 Load Switch Block Diagram

Channel 6 Buck Regulator

The Channel 6 buck regulator is a highly efficient, step-down dc-to-dc converter that uses a high speed, fixed-frequency current mode architecture. No external compensation is required. The regulator maintains a constant output voltage, regardless of load, by adjusting the peak inductor current threshold and the duty cycle of the power switches. At the start of each oscillator cycle, the PFET switch is turned on, sending a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current threshold, which turns off the PFET switch and turns on the NFET synchronous rectifier. This sends a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle.

Channel 6 has protection circuitry to limit the amount of positive current that flows through the PFET switch and the synchronous rectifier. The positive current limit on the power switch limits the amount of current that can flow from the input to the output.

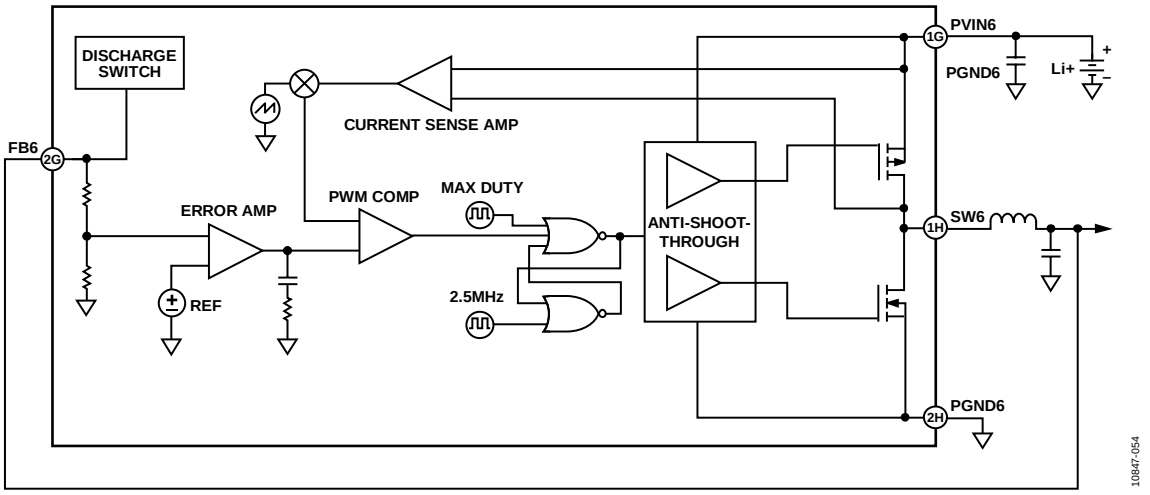


Figure 54. Channel 6 Buck Regulator Block Diagram

The output of Channel 6 is programmable through the I²C interface in the range of 1.46 V to 2.5 V. The Channel 6 block has an adjustable mode option, as well, that can be programmed externally through a resistor divider to a value between 0.5 V and $V_{IN} \times 0.95$. Note that an output voltage setting that is too low (for example, 0.5 V) may go out of regulation at high V_{IN} conditions due to the minimum on time limitation of Channel 6.

Channel 6 includes an internal soft start function (see Figure 55) that ramps the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This prevents possible input voltage drops when a battery is connected to the input of the converter. The soft start time can be programmed through the I²C interface and set to 1.3 ms or 4 ms.

Channel 6 can start up from any voltage between 0 volts and the final target output voltage without discharging the output capacitor charge at the beginning of the soft start. This makes it possible to connect an external LDO. If an external LDO is used, the voltage setting for Channel 6 must be greater than the output voltage of the external LDO.

Channel 6 enable mode can be selected from either sequencer mode or the factory-programmed I²C mode. When sequencer mode is selected, Channel 6 on/off activation is controlled by the EN pin and the factory-programmed enable delay time.

When I²C mode is selected, Channel 6 on/off activation is controlled by Bit 4 in Register PCTRL at Address 32 (see Table 51 and Table 52).

When Channel 6 is disabled, there is an option to automatically discharge the converter output capacitor though a discharge switch. This discharge function can be enabled through the I²C interface.

The overvoltage or undervoltage status of each channel can be read back through the I²C interface.

The regulator discharge switch for Channel 6 is controlled by Bit 0 in Register DSCG at Address 1 (see Table 14 and Table 15). The regulator soft start ramp for Channel 6 is controlled by Bit 2 in Register SFTTIM at Address 2 (see Table 16, Table 17, and Table 18).

The regulator turn-on delay for Channel 6 is controlled by Bits[3:0] in Register EN_DLY36 at Address 5 (see Table 25, Table 26, and Table 27). The output voltage level for Channel 6 is controlled by Bits[2:0] in Register VID6 at Address 10 (see Table 40 and Table 41). The undervoltage protection status for Channel 6 is confirmed by Bit 5 in Register UVPST at Address 12 (see Table 45 and Table 46). The overvoltage protection status for Channel 6 can be tested by reading Bit 5 in Register OVPST at Address 13 (see Table 47 and Table 48).

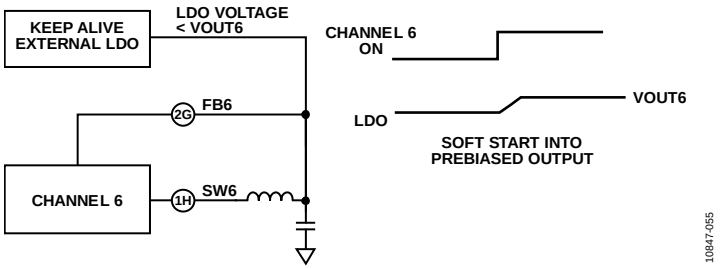


Figure 55. Soft Start into Prebiased Output

Channel 7 Backlight Boost Regulator and LED Driver

The Channel 7 boost regulator has a constant-current sink LED driver. An external resistor connected to ISET7 defines the reference current for the LED driver. The LED current is programmable through the I²C interface in 32 steps. An external PWM interface circuit, connected to ISET7, can be used in applications where the LED brightness must be controlled with fine adjustments. The PWM interface circuit is based on an RC filter producing a dc level that is proportional to the duty cycle of the PWM signal supplied from an external microprocessor.

Channel 7 is an asynchronous, current mode regulator that supports up to four LEDs connected in series. The operating switching frequency of this boost regulator can be 1.25 MHz or 2.5 MHz. The frequency selection is a factory-programming option with a default value of 2.5 MHz. Channel 7 includes an overvoltage detection circuit that protects the regulator in case of an LED failure or string disconnection. The overvoltage protection is a latched event with a delay to avoid false triggering.

Channel 7 has a programmable soft start ramp that is controlled by Bit 1 in Register SFTTIM at Address 2 (see Table 16, Table 17, and Table 21). The LED current for Channel 7 is controlled by Bits[7:3] in Register VID78 at Address 11 (see Table 42 and Table 43). The overvoltage protection status for Channel 7 can be tested by reading Bit 6 in Register OVPST at Address 13 (see Table 47 and Table 48). The forward voltage of the LEDs used in the application affects the selected soft start time. The regulator on/off activation for Channel 7 is controlled by Bit 2 in Register PCTRL at Address 32 (see Table 51 and Table 52).

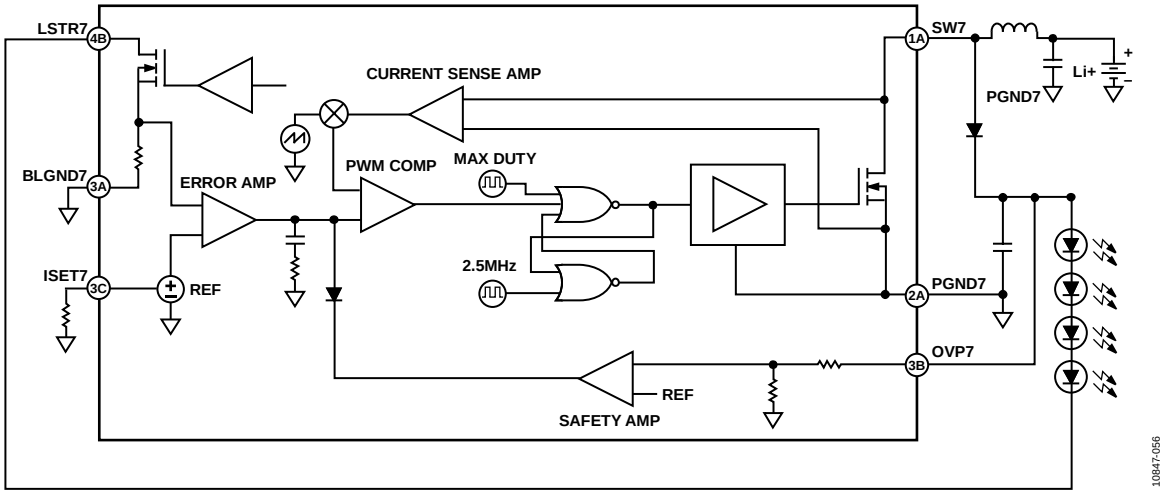


Figure 56. Channel 7 Backlight Boost Regulator Block Diagram

Channel 8 Auxiliary LDO

Channel 8 is an auxiliary LDO that is programmable in fixed voltage steps between 1.5 V and 3.5 V. It is stable with a 1 µF, low ESR ceramic capacitor and has a 200 mA output current limit. The LDO circuit includes short-circuit protection with a latched timer delay. The channel is enabled and disabled via the I^2C interface. When the LDO is disabled, the discharge switch is activated. In addition, the status of the undervoltage protection circuit can be monitored via the I^2C interface.

Channel 8 enable mode can be selected from either sequencer mode or the factory-programmed I^2C mode. When sequencer mode is selected, Channel 8 on/off activation is controlled by the EN pin and the factory-programmed enable delay time. When I^2C mode is selected, Channel 8 on/off activation is controlled by Bit 3 in Register PCTRL at Address 32 (see Table 51 and Table 52).

The regulator soft start ramp for Channel 8 is controlled by Bit 0 in Register SFTTIM at Address 2 (see Table 16 to Table 18). The regulator turn-on delay for Channel 8 is controlled by Bits[7:4] in Register EN_DLY8 at Address 6 (see Table 28 and Table 29). The output voltage level for Channel 8 is controlled by Bits[2:0] in Register VID78 at Address 11 (see Table 42 and Table 44).

The undervoltage protection status for Channel 8 can be tested by reading Bit 7 in Register UVPST at Address 12 (see Table 45 and Table 46). The regulator power-on for Channel 8 is controlled by Bit 3 in Register PCTRL at Address 32 (see Table 51 and Table 52).

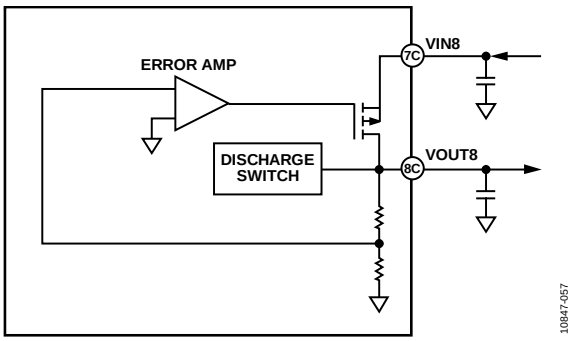


Figure 57. Channel 8 Auxiliary LDO Block Diagram

HOUSEKEEPING BLOCK

Channel 9 Keep Alive LDO

The low quiescent current keep alive LDO provides a fixed output voltage for the backup battery and RTC. As long as the main battery voltage is greater than the UVLO_SYS threshold, the LDO remains on. The VREGO pin can be used to power external circuits that are kept alive when the system is off. The LDO can provide up to 50 mA of output current, and it includes an integrated C_{OUT} discharge switch that is turned on when the LDO is disabled by the UVLO_SYS circuit.

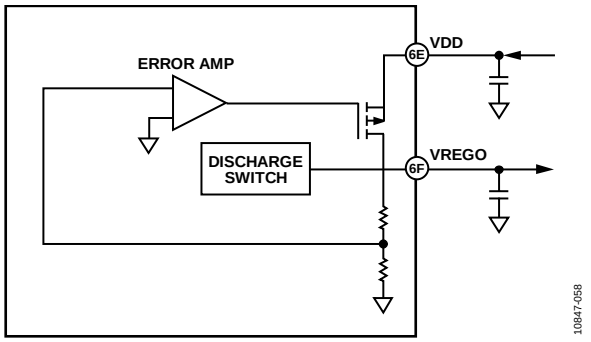


Figure 58. Channel 9 Keep Alive LDO Block Diagram

CONTROL REGISTER MAP

Table 12. Control Register Map[1]

Addr. (Dec)[2]	Register	B7	B6	B5	B4	B3	B2	B1	B0
0	Reserved[3]	0	0	0	0	0	0	0	0
1	DSCG	0	0	0	DSCG4_ON	DSCG2_ON	DSCG3_ON	DSCG5_ON	DSCG6_ON
2	SFTTIM	SS1	SS2	SS3	SS4	SS5	SS6	SS7	SS8
3	Reserved[3]	0	0	0	0	0	0	0	0
4	EN_DLY12	EN_DLY1_3	EN_DLY1_2	EN_DLY1_1	EN_DLY1_0	EN_DLY2_3	EN_DLY2_2	EN_DLY2_1	EN_DLY2_0
5	EN_DLY36	EN_DLY3_3[4]	EN_DLY3_2[4]	EN_DLY3_1[4]	EN_DLY3_0[4]	EN_DLY6_3	EN_DLY6_2	EN_DLY6_1	EN_DLY6_0
6	EN_DLY8	EN_DLY8_3	EN_DLY8_2	EN_DLY8_1	EN_DLY8_0	0	0	0	0
7	DIS_DLY3	0	0	0	0	0	DIS_DLY_2[4]	DIS_DLY_1[4]	DIS_DLY_0[4]
8	VID12	0	VID1_2	VID1_1	VID1_0	0	VID2_2	VID2_1	VID2_0
9	VID34	VID3_3	VID3_2	VID3_1	VID3_0	0	0	VID4_1	VID4_0
10	VID6	0	0	0	0	0	VID6_2	VID6_1	VID6_0
11	VID78	IID7_4	IID7_3	IID7_2	IID7_1	IID7_0	VID8_2	VID8_1	VID8_0
12	UVPST	UV8	0	UV6	0	FAULT4	UV3	UV2	0
13	OVPST	0	OV7	OV6	0	0	OV3	OV2	0
14	PWMCONT	0	0	0	0	0	0	0	PWM1
15 to 31	Reserved	0	0	0	0	0	0	0	0
32	PCTRL	RDST_PCTRL	0	0	CH6_ON	CH8_ON	CH7_ON	CH4_ON	CH5_ON
33	RTCT_SEC	RDST_TSEC	0	SEC_5	SEC_4	SEC_3	SEC_2	SEC_1	SEC_0
34	RTCT_MIN	RDST_TMIN	0	MIN_5	MIN_4	MIN_3	MIN_2	MIN_1	MIN_0
35	RTCT_HR	RDST_THR	0	0	HR_4	HR_3	HR_2	HR_1	HR_0
36	RTCT_DAY	RDST_TDAY	0	0	DAY_4	DAY_3	DAY_2	DAY_1	DAY_0
37	RTCT_MO	RDST_TMON	0	0	0	MO_3	MO_2	MO_1	MO_0
38	RTCT_YR	RDST_TYAR	YR_6	YR_5	YR_4	YR_3	YR_2	YR_1	YR_0
39	RTCT_WK	RDST_TWEK	0	0	0	0	WK_2	WK_1	WK_0
40	RTCADJ	RDST_ADJ	ADJS	ADJ_5	ADJ_4	ADJ_3	ADJ_2	ADJ_1	ADJ_0
41	RTCAL_SEC	RDST_ASEC	ASEC_6	ASEC_5	ASEC_4	ASEC_3	ASEC_2	ASEC_1	ASEC_0
42	RTCAL_MIN	RDST_AMIN	0	AMIN_5	AMIN_4	AMIN_3	AMIN_2	AMIN_1	AMIN_0
43	RTCAL_HR	RDST_AHR	TIMEOUT	0	AHR_4	AHR_3	AHR_2	AHR_1	AHR_0
44	REG0	RDST_REG0	0	0	0	RG0_3	RG0_2	RG0_1	RG0_0
45	REG1	RDST_REG1	0	0	0	RG1_3	RG1_2	RG1_1	RG1_0
46	REG2	RDST_REG2	0	0	0	RG2_3	RG2_2	RG2_1	RG2_0
47	REG3	RDST_REG3	0	0	0	RG3_3	RG3_2	RG3_1	RG3_0
48	REG4	RDST_REG4	0	0	0	RG4_3	RG4_2	RG4_1	RG4_0
49	REG5	RDST_REG5	0	0	0	RG5_3	RG5_2	RG5_1	RG5_0
50	REG6	RDST_REG6	0	0	0	RG6_3	RG6_2	RG6_1	RG6_0
51	REG7	RDST_REG7	0	0	0	RG7_3	RG7_2	RG7_1	RG7_0
52	REG8	RDST_REG8	0	0	0	RG8_3	RG8_2	RG8_1	RG8_0
53	REG9	RDST_REG9	0	0	0	RG9_3	RG9_2	RG9_1	RG9_0
54	REG10	RDST_REG10	0	0	0	RG10_3	RG10_2	RG10_1	RG10_0
55	REG11	RDST_REG11	0	0	0	RG11_3	RG11_2	RG11_1	RG11_0
56	REG12	RDST_REG12	0	0	0	RG12_3	RG12_2	RG12_1	RG12_0
57	REG13	RDST_REG13	0	0	0	RG13_3	RG13_2	RG13_1	RG13_0
58	REG14	RDST_REG14	0	0	0	RG14_3	RG14_2	RG14_1	RG14_0
59	REG15	RDST_REG15	0	0	0	RG15_3	RG15_2	RG15_1	RG15_0
60	RTCALR_SEC	RDST_RSEC	RSEC_6	RSEC_5	RSEC_4	RSEC_3	RSEC_2	RSEC_1	RSEC_0
61	RTCALR_MIN	RDST_RMIN	0	RMIN_5	RMIN_4	RMIN_3	RMIN_2	RMIN_1	RMIN_0
62	RTCALRMD	RDST_ALRM	0	0	ALMMD	0	0	0	ALMST
97	SEL_FSW	0	SEL_FREQ7	1	SEL_FREQ4	SEL_FREQ3_1	SEL_FREQ3_0	SEL_FREQ2	SEL_FREQ1
98	VID_REGO	0	0	0	0	0	0	0	VID_REGO
100	SEQ_MODE	0	0	0	0	0	0	OPT_MODE_EN6	OPT_MODE_EN8
101	PROT_DLY	0	0	OPT_UV_DLY_1	OPT_UV_DLY_0	0	0	OPT_OV_DLY_1	OPT_OV_DLY_0
102	OPT_ALMO	0	0	0	0	0	0	0	OPT_ALMO

[1] The 0s and the 1 are all factory reserved bit settings and should not be changed via the I²C interface.
[2] For Address 32 to Address 62, the register status can be read from Bit 7 (see Figure 47 in the I²C Interface section).
[3] Address 0 and Address 15 return 0. Address 16 to Address 31 are shadows of Address 0 to Address 15.
[4] When the internal oscillator is used, either the Channel 3 enable delay (EN_DLY3) or the disable delay function must be set to 0 ms.

CONTROL REGISTER READ/WRITE AND RESET

Table 13. Operations and Reset Condition of Registers

Address (Dec)	Register	Read/Write	Read Only	Write Only	Reset Conditions
0	Reserved				
1	DSCG	B4 to B0			UVLO_SYS
2	SFTTIM	B7 to B0			UVLO_SYS
3	Reserved				
4	EN_DLY12	B7 to B0			UVLO_SYS
5	EN_DLY36	B7 to B0			UVLO_SYS
6	EN_DLY8	B7 to B4			UVLO_SYS
7	DIS_DLY3	B2 to B0			UVLO_SYS
8	VID12	B6 to B4, B2 to B0			UVLO_SYS
9	VID34	B7 to B4, B1 to B0			UVLO_SYS
10	VID6	B2 to B0			UVLO_SYS
11	VID78	B7 to B0			UVLO_SYS
12	UVPST		B7, B5, B3 to B1		UVLO_SYS
13	OVPST		B6 to B5, B2 to B1		UVLO_SYS
14	PWMCONT	B0			UVLO_SYS
15 to 31	Reserved				
32	PCTRL	B4 to B0	B7		UVLO_SYS, EN = low or REF_GOOD = falling
33	RTCT_SEC	B5 to B0	B7		UVLO_RTC
34	RTCT_MIN	B5 to B0	B7		UVLO_RTC
35	RTCT_HR	B4 to B0	B7		UVLO_RTC
36	RTCT_DAY	B4 to B0	B7		UVLO_RTC
37	RTCT_ MO	B3 to B0	B7		UVLO_RTC
38	RTCT_YR	B6 to B0	B7		UVLO_RTC
39	RTCT_WK	B2 to B0	B7		UVLO_RTC
40	RTCADJ	B6 to B0	B7		UVLO_RTC
41	RTCAL_SEC	B6 to B0	B7		UVLO_SYS
42	RTCAL_MIN	B5 to B0	B7		UVLO_SYS
43	RTCAL_HR	B6, B4 to B0	B7		UVLO_SYS
44 to 59	REG0 to REG15	B3 to B0	B7		UVLO_RTC
60	RTCALR_SEC	B6 to B0	B7		UVLO_SYS
61	RTCALR_MIN	B5 to B0	B7		UVLO_SYS
62	RTCALRMD	B4, B0	B7		UVLO_SYS
97	SEL_FSW	B6 to B0			UVLO_SYS
98	VID_REGO	B0			UVLO_SYS
100	SEQ_MODE	B1, B0			UVLO_SYS
101	PROT_DLY	B5, B4, B1, B0			UVLO_SYS
102	OPT_ALMO	B0			UVLO_SYS

CONTROL REGISTER DETAILS

Address 1—DSCG (Discharge Switch Register)

Table 14. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
0	0	0	DSCG4_ON	DSCG2_ON	DSCG3_ON	DSCG5_ON	DSCG6_ON

Table 15. Discharge Switch Register Bit Definitions

Bit	Description
DSCG4_ON	Channel 4 discharge switch at disable. 1: discharge switch on; 0: discharge switch off (default).
DSCG2_ON	Channel 2 discharge switch at disable. 1: discharge switch on; 0: discharge switch off (default).
DSCG3_ON	Channel 3 discharge switch at disable. 1: discharge switch on; 0: discharge switch off (default).
DSCG5_ON	Channel 5 discharge switch at disable. 1: discharge switch on; 0: discharge switch off (default).
DSCG6_ON	Channel 6 discharge switch at disable. 1: discharge switch on; 0: discharge switch off (default).

Address 2—SFTTIM (Channel 1 to Channel 7 Soft Start Timer Register)

Table 16. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
SS1	SS2	SS3	SS4	SS5	SS6	SS7	SS8

Table 17. Soft Start Control Bits for Channel 1 to Channel 7

Bit	Description
SS1	Channel 1 soft start time
SS2	Channel 2 soft start time
SS3	Channel 3 soft start time
SS4	Channel 4 soft start time
SS5	Channel 5 soft start time
SS6	Channel 6 soft start time
SS7	Channel 7 soft start time
SS8	Channel 8 soft start time

Table 18. Channel 1, Channel 3, Channel 4, Channel 6, and Channel 8 Soft Start Settings

Setting	
Bx	Soft Start Time (ms)
0	4
1	1.3

Table 19. Channel 5 Soft Start Settings

Setting	
B3	Soft Start Time (ms)
0	Long
1	Short

Table 20. Channel 2 Soft Start Settings

Setting	
B6	Soft Start Time (ms)
0	4.5
1	1.5

Table 21. Channel 7 Soft Start Settings[1]

Setting	
B1	Soft Start Time (ms)
0	8
1	2.7

[1] The soft start time for Channel 7 depends on the forward voltage of LED.

Address 4—EN_DLY12 (Channel 1 and Channel 2 Enable Delay Time Register)

Table 22. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
EN_DLY1_3	EN_DLY1_2	EN_DLY1_1	EN_DLY1_0	EN_DLY2_3	EN_DLY2_2	EN_DLY2_1	EN_DLY2_0

Table 23. Enable Delay for Channel 1 and Channel 2

Bits	Description
EN_DLY1_3	Channel 1 enable delay time, 16 ms
EN_DLY1_2	Channel 1 enable delay time, 8 ms
EN_DLY1_1	Channel 1 enable delay time, 4 ms
EN_DLY1_0	Channel 1 enable delay time, 2 ms
EN_DLY2_3	Channel 2 enable delay time, 16 ms
EN_DLY2_2	Channel 2 enable delay time, 8 ms
EN_DLY2_1	Channel 2 enable delay time, 4 ms
EN_DLY2_0	Channel 2 enable delay time, 2 ms

Table 24. Channel 1 and Channel 2 Enable Delay Time Settings

Setting				
B7, B3	B6, B2	B5, B1	B4, B0	Enable Delay Time (ms)
0	0	0	0	0
0	0	0	1	2
0	0	1	0	4
0	0	1	1	6
0	1	0	0	8
0	1	0	1	10
0	1	1	0	12
0	1	1	1	14
1	0	0	0	16
1	0	0	1	18
1	0	1	0	20
1	0	1	1	22
1	1	0	0	24
1	1	0	1	26
1	1	1	0	28
1	1	1	1	30

Address 5—EN_DLY36 (Channel 3 and Channel 6 Enable Delay Time Register)

Table 25. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
EN_DLY3_3	EN_DLY3_2	EN_DLY3_1	EN_DLY3_0	EN_DLY6_3	EN_DLY6_2	EN_DLY6_1	EN_DLY6_0

Table 26. Enable Delay for Channel 3 and Channel 6

Bits	Description
EN_DLY3_3	Channel 3 enable delay time, 16 ms
EN_DLY3_2	Channel 3 enable delay time, 8 ms
EN_DLY3_1	Channel 3 enable delay time, 4 ms
EN_DLY3_0	Channel 3 enable delay time, 2 ms
EN_DLY6_3	Channel 6 enable delay time, 16 ms
EN_DLY6_2	Channel 6 enable delay time, 8 ms
EN_DLY6_1	Channel 6 enable delay time, 4 ms
EN_DLY6_0	Channel 6 enable delay time, 2 ms

Table 27. Channel 3 and Channel 6 Enable Delay Time Settings

Setting				
B7, B3	B6, B2	B5, B1	B4, B0	Enable Delay Time (ms)
0	0	0	0	0
0	0	0	1	2
0	0	1	0	4
0	0	1	1	6
0	1	0	0	8
0	1	0	1	10
0	1	1	0	12
0	1	1	1	14
1	0	0	0	16
1	0	0	1	18
1	0	1	0	20
1	0	1	1	22
1	1	0	0	24
1	1	0	1	26
1	1	1	0	28
1	1	1	1	30

Address 6—EN_DLY8 (Channel 8 Enable Delay Time Register)

Table 28. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
EN_DLY8_3	EN_DLY8_2	EN_DLY8_1	EN_DLY8_0	0	0	0	0

Table 29. Enable Delay for Channel 8

Bits	Description
EN_DLY8_3	Channel 8 enable delay time, 16 ms
EN_DLY8_2	Channel 8 enable delay time, 8 ms
EN_DLY8_1	Channel 8 enable delay time, 4 ms
EN_DLY8_0	Channel 8 enable delay time, 2 ms

Table 30. Channel 8 Enable Delay Time Setting

Setting				
B7	B6	B5	B4	Enable Delay Time (ms)
0	0	0	0	0
0	0	0	1	2
0	0	1	0	4
0	0	1	1	6
0	1	0	0	8
0	1	0	1	10
0	1	1	0	12
0	1	1	1	14
1	0	0	0	16
1	0	0	1	18
1	0	1	0	20
1	0	1	1	22
1	1	0	0	24
1	1	0	1	26
1	1	1	0	28
1	1	1	1	30

Address 7—DIS_DLY3 (Channel 3 Disable Delay Time Register)

Table 31. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
0	0	0	0	0	DIS_DLY_2	DIS_DLY_1	DIS_DLY_0

Table 32. Channel 3 Disable Delay time

Bits	Description
DIS_DLY_2	Channel 3 disable delay time, 120 ms
DIS_DLY_1	Channel 3 disable delay time, 60 ms
DIS_DLY_0	Channel 3 disable delay time, 30 ms

Table 33. Channel 3 Disable Delay Time Settings

Setting			
B2	B1	B0	Disable Delay Time (ms)
0	0	0	0
0	0	1	30
0	1	0	60
0	1	1	90
1	0	0	120
1	0	1	150
1	1	0	180
1	1	1	210

Address 8—VID12 (Channel 1 and Channel 2 VID Setting Register)

Table 34. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
0	VID1_2	VID1_1	VID1_0	0	VID2_2	VID2_1	VID2_0

Table 35. Channel 1 VID Settings

Setting			
B6	B5	B4	V_{OUT1} (V)
0	0	0	5.3
0	0	1	5.2
0	1	0	5.0
0	1	1	4.8
1	0	0	4.6
1	0	1	4.4
1	1	0	4.2
1	1	1	3.8

Table 36. Channel 2 VID Settings

Setting			
B2	B1	B0	V_{OUT2} (V)
0	0	0	3.65
0	0	1	3.6
0	1	0	3.55
0	1	1	3.5
1	0	0	3.45
1	0	1	3.4
1	1	0	3.35
1	1	1	3.3

Address 9—VID34 (Channel 3 and Channel 4 VID Setting Register)

Table 37. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
VID3_3	VID3_2	VID3_1	VID3_0	0	0	VID4_1	VID4_0

Table 38. Channel 3 VID Settings

Setting				
B7	B6	B5	B4	V_{OUT3} (V)
0	0	0	0	1.26
0	0	0	1	1.24
0	0	1	0	1.22
0	0	1	1	1.20
0	1	0	0	1.18
0	1	0	1	1.16
0	1	1	0	1.14
0	1	1	1	1.12
1	0	0	0	1.10
1	0	0	1	1.08
1	0	1	0	1.06
1	0	1	1	1.04
1	1	0	0	1.02
1	1	0	1	1.00
1	1	1	0	0.98
1	1	1	1	0.96

Table 39. Channel 4 VID Settings

Setting		
B1	B0	V_{OUT4} (V)
0	0	Adjust
0	1	2.7
1	0	1.80
1	1	1.60

Address 10—VID6 (Channel 6 VID Setting Register)

Table 40. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
0	0	0	0	0	VID6_2	VID6_1	VID6_0

Table 41. Channel 6 VID Settings

Setting			
B2	B1	B0	V_{OUT6} (V)
0	0	0	Adjust
0	0	1	2.50
0	1	0	1.87
0	1	1	1.80
1	0	0	1.76
1	0	1	1.55
1	1	0	1.50
1	1	1	1.46

Address 11—VID78 (Channel 7 IID and Channel 8 VID Setting Register)

Table 42. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
IID7_4	IID7_3	IID7_2	IID7_1	IID7_0	VID8_2	VID8_1	VID8_0

Table 43. Channel 7 IID Settings

B7	B6	B5	B4	B3	IID	B7	B6	B5	B4	B3	IID
0	0	0	0	0	0	1	0	0	0	0	16
0	0	0	0	1	1	1	0	0	0	1	17
0	0	0	1	0	2	1	0	0	1	0	18
0	0	0	1	1	3	1	0	0	1	1	19
0	0	1	0	0	4	1	0	1	0	0	20
0	0	1	0	1	5	1	0	1	0	1	21
0	0	1	1	0	6	1	0	1	1	0	22
0	0	1	1	1	7	1	0	1	1	1	23
0	1	0	0	0	8	1	1	0	0	0	24
0	1	0	0	1	9	1	1	0	0	1	25
0	1	0	1	0	10	1	1	0	1	0	26
0	1	0	1	1	11	1	1	0	1	1	27
0	1	1	0	0	12	1	1	1	0	0	28
0	1	1	0	1	13	1	1	1	0	1	29
0	1	1	1	0	14	1	1	1	1	0	30
0	1	1	1	1	15	1	1	1	1	1	31

Table 44. Channel 8 VID Settings

Setting			
B2	B1	B0	V_{OUT8} (V)
0	0	0	3.5
0	0	1	3.4
0	1	0	3.3
0	1	1	3.0
1	0	0	2.8
1	0	1	2.5
1	1	0	1.8
1	1	1	1.5

Address 12—UVPST (UVP Status Register)

Table 45. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
UV8	0	UV6	0	FAULT4	UV3	UV2	0

Table 46. Undervoltage Status for Channel 2 to Channel 6 and Channel 8

Bits	Description
UV8	Channel 8 undervoltage status. 1: the channel is in undervoltage condition.
UV6	Channel 6 undervoltage status. 1: the channel is in undervoltage condition.
FAULT4	Channel 4 undervoltage or overvoltage status. 1: the channel is in undervoltage or overvoltage condition.
UV3	Channel 3 undervoltage status. 1: the channel is in undervoltage condition.
UV2	Channel 2 undervoltage status. 1: the channel is in undervoltage condition.

Address 13—OVPST (OVP Status Register)

Table 47. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
0	OV7	OV6	0	0	OV3	OV2	0

Table 48. Overvoltage Status for Channel 2, Channel 3, Channel 6, and Channel 7

Bits	Description
OV7	Channel 7 overvoltage status. 1: the channel is in overvoltage condition.
OV6	Channel 6 overvoltage status. 1: the channel is in overvoltage condition.
OV3	Channel 3 overvoltage status. 1: the channel is in overvoltage condition.
OV2	Channel 2 overvoltage status. 1: the channel is in overvoltage condition.

Address 14—PWMCONT (Enable PWM Mode for Channel 1)

Table 49. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
0	0	0	0	0	0	0	PWM1

Table 50. Regulator Mode Control for Channel 1

Bit	Description
PWM1	Channel 1 switching mode. 0: PSM mode (default); 1: PWM mode.

Address 32—PCTRL (Power-On/Power-Off Sequence Register)

Table 51. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
RDST_PCTRL	0	0	CH6_ON	CH8_ON	CH7_ON	CH4_ON	CH5_ON

Table 52. Regulator Activation

Bits	Description
CH6_ON	Channel 6 Buck regulator on. When enabled by sequencer (EN pin is high). 1: enable delay is active. 0: Channel 6 is off. When enabled by I^2C command, 1: Channel 6 is on. 0: Channel 6 is off.
CH8_ON	Channel 8 LDO on. When enabled by sequencer (EN pin is high). 1: enable delay is active. 0: Channel 8 is off. When enabled by I^2C command, 1: Channel 8 is on. 0: Channel 8 is off.
CH7_ON	Channel 7 backlight regulator on. 1: Channel 7 is on. 0: Channel 7 is off (default).
CH4_ON	Channel 4 buck regulator on. 1: Channel 4 is on. 0: Channel 4 is off (default).
CH5_ON	Channel 5 load switch. 1: Channel 5 is on. 0: Channel 5 is off (default).

Address 33 to Address 39—RTCT (Set for Time Registers)

Table 53. Bus Assignment Bit Map for the RTCT Registers[1, 2]

Register	Data Range	B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
RTCT_SEC	0 to 59	RDST_TSEC	0	SEC_5	SEC_4	SEC_3	SEC_2	SEC_1	SEC_0
RTCT_MIN	0 to 59	RDST_TMIN	0	MIN_5	MIN_4	MIN_3	MIN_2	MIN_1	MIN_0
RTCT_HR	0 to 23	RDST_THR	0	0	HR_4	HR_3	HR_2	HR_1	HR_0
RTCT_DAY	0 to 30	RDST_TDAY	0	0	DAY_4	DAY_3	DAY_2	DAY_1	DAY_0
RTCT_MO	0 to 11	RDST_TMON	0	0	0	MO_3	MO_2	MO_1	MO_0
RTCT_YR	0 to 127	RDST_TYAR	YR_6	YR_5	YR_4	YR_3	YR_2	YR_1	YR_0
RTCT_WK	0 to 6	RDST_TWEK	0	0	0	0	WK_2	WK_1	WK_0

[1] Default value is 01/01/2000 00:00.
[2] These registers are backed up with a backup battery. In case of undervoltage lockout of the BU3INT pin, all data is cleared to 0. The read status is assigned to Bit 7 (see the I²C Interface section).

Address 40—RTCADJ (RTC Adjust Data Register)

Table 54. Bus Assignment Bit Map[1, 2]

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
RDST_ADJ	ADJS[3] ±	ADJ_5 (32 ppm)	ADJ_4 (16 ppm)	ADJ_3 (8 ppm)	ADJ_2 (4 ppm)	ADJ_1 (2 ppm)	ADJ_0 (1 ppm)

[1] The total minimum adjustment value is −61 ppm, and the total maximum adjustment value is +61 ppm.
[2] This register is backed up by a backup battery. If an undervoltage lockout of the BU3INT pin occurs, all data is cleared to 0. The read status is assigned to Bit 7 (see the I²C Interface section).
[3] The ADJS bit determines if the set adjustment values (shown in parentheses) of Bits[5:0] are added or subtracted to increase or decrease the correction. If Bit 6 is set to 1, the values of Bits[5:0] that are set to 1 are added; if Bit 6 is set to 0, the values of Bits[5:0] that are set to 1 are subtracted.

Address 41 to Address 43—RTCAL (RTC Countdown Alarm Timer One-Shot Data Registers)

Table 55. Bus Assignment Bit Map

Register	Data Range	B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
RTCAL_SEC	0 to 119	RDST_ASEC	ASEC_6	ASEC_5	ASEC_4	ASEC_3	ASEC_2	ASEC_1	ASEC_0
RTCAL_MIN	0 to 59	RDST_AMIN	0	AMIN_5	AMIN_4	AMIN_3	AMIN_2	AMIN_1	AMIN_0
RTCAL_HR	0 to 31	RDST_AHR	TIMEOUT	0	AHR_4	AHR_3	AHR_2	AHR_1	AHR_0

Address 44 to Address 59—REG0 to REG15 (Configuration Registers)

Table 56. Bus Assignment Bit Map for the Configuration Registers[1]

Register	B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
REG0	RDST_REG0	0	0	0	RG0_3	RG0_2	RG0_1	RG0_0
REG1	RDST_REG1	0	0	0	RG1_3	RG1_2	RG1_1	RG1_0
REG2	RDST_REG2	0	0	0	RG2_3	RG2_2	RG2_1	RG2_0
REG3	RDST_REG3	0	0	0	RG3_3	RG3_2	RG3_1	RG3_0
REG4	RDST_REG4	0	0	0	RG4_3	RG4_2	RG4_1	RG4_0
REG5	RDST_REG5	0	0	0	RG5_3	RG5_2	RG5_1	RG5_0
REG6	RDST_REG6	0	0	0	RG6_3	RG6_2	RG6_1	RG6_0
REG7	RDST_REG7	0	0	0	RG7_3	RG7_2	RG7_1	RG7_0
REG8	RDST_REG8	0	0	0	RG8_3	RG8_2	RG8_1	RG8_0
REG9	RDST_REG9	0	0	0	RG9_3	RG9_2	RG9_1	RG9_0
REG10	RDST_REG10	0	0	0	RG10_3	RG10_2	RG10_1	RG10_0
REG11	RDST_REG11	0	0	0	RG11_3	RG11_2	RG11_1	RG11_0
REG12	RDST_REG12	0	0	0	RG12_3	RG12_2	RG12_1	RG12_0
REG13	RDST_REG13	0	0	0	RG13_3	RG13_2	RG13_1	RG13_0
REG14	RDST_REG14	0	0	0	RG14_3	RG14_2	RG14_1	RG14_0
REG15	RDST_REG15	0	0	0	RG15_3	RG15_2	RG15_1	RG15_0

[1] These registers are backed up with a backup battery. In case of undervoltage lockout of the BU3INT pin, all data is cleared to 0. The read status is assigned to Bit 7 (see the I²C Interface section).

Address 60 and Address 61—RTCALR (RTC Countdown Alarm Timer Repeat Data Registers)

Table 57. Bus Assignment Bit Map for the RTCALR Registers[1]

Register	Data Range	B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
RTCALR_SEC	0 to 119	RDST_RSEC	RSEC_6	RSEC_5	RSEC_4	RSEC_3	RSEC_2	RSEC_1	RSEC_0
RTCALR_MIN	0 to 59	RDST_RMIN	0	RMIN_5	RMIN_4	RMIN_3	RMIN_2	RMIN_1	RMIN_0

[1] The read status is assigned to Bit 7 (see the I²C Interface section).

Address 62—RTCALRMD (RTC Countdown Time Alarm Mode Register)

Table 58. Bus Assignment Bit Map for the RTCALRMD Registers

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
RDST_ALRM	0	0	ALMMD	0	0	0	ALMST

Address 97—SEL_FSW (Switcher Frequency Select Register)

Table 59. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
0	SEL_FREQ7	1	SEL_FREQ4	SEL_FREQ3_1	SEL_FREQ3_0	SEL_FREQ2	SEL_FREQ1

Table 60. SEL_FSW Programming Bits

Bits	Description
SEL_FREQ7	Channel 7 switching frequency. 0: 1.25 MHz. 1: 2.5 MHz.
SEL_FREQ4	Channel 4 switching frequency. 0: 1.25 MHz. 1: 2.5 MHz.
SEL_FREQ3[1:0]	Channel 3 switching frequency. 00: 1.25 MHz. 01: 625 kHz. 10: 312 kHz. 11: 2.5 MHz.
SEL_FREQ2	Channel 2 switching frequency. 0: 1.25 MHz. 1: 2.5 MHz.
SEL_FREQ1	Channel 1 switching frequency. 0: 1.25 MHz. 1: 2.5 MHz.

Address 98—VID_REGO (VID for VREGO Output Voltage)

Table 61. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
0	0	0	0	0	0	0	VID_REGO

Table 62. VID_REGO Programming Bits

Bits	Description
VID_REGO	VREGO output voltage selection. 0: 3.2 V. 1: 3.0 V.

Address 100—SEQ_MODE (Sequencer Mode Setting Register for Channel 6 and Channel 8)

Table 63. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
0	0	0	0	0	0	OPT_MODE_EN6	OPT_MODE_EN8

Table 64. SEQ_Mode Programming Bits

Bits	Description
OPT_MODE_EN6	Mode for Channel 6 turning on. 1: sequencer. 0: I^2C.
OPT_MODE_EN8	Mode for CH8 turning on. 1: sequencer. 0: I^2C.

Address 101—PROT_DLY (Undervoltage/Overvoltage Protection Delay Register)

Table 65. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
0	0	OPT_UV_DLY_1	OPT_UV_DLY_0	0	0	OPT_OV_DLY_1	OPT_OV_DLY_0

Table 66. PROT_DLY Programming Bits

Bits	Description
OPT_UV_DLY[1:0]	Undervoltage protection delay. 00: 0 ms (no delay). 01: 78 ms. 10: 200 ms. 11: disabled (no undervoltage detection).
OPT_OV_DLY[1:0]	Overvoltage protection delay. 00: 0 ms (no delay). 01: 1.2 ms. 10: 3.3 ms. 11: disabled (no overvoltage detection).

Address 102—OPT_ALMO (Option Setting Register for Alarm Function)

Table 67. Bus Assignment Bit Map

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0 (LSB)
0	0	0	0	0	0	0	OPT_ALMO

Table 68. OPT_ALMO Programming Bits

Bits	Description
OPT_ALMO	Select autoenable option for the alarm function. 1: autoenable used. 0: autoenable not used.

APPLICATIONS INFORMATION

EXTERNAL COMPONENT SELECTION FOR BUCK REGULATORS

Trade-offs between performance parameters such as efficiency and transient response can be made by varying the choice of external components in the applications circuit, as shown in Figure 62.

Inductor

The high switching frequency of Channel 3 and Channel 6 allows for the selection of small chip inductors. For best performance, use inductor values between 0.7 µH and 3 µH for 2.5 MHz switching. Recommended inductors are shown in Figure 62.

The peak-to-peak inductor current ripple is calculated using Equation 2.

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \quad (2)$$

where:
f_{SW} is the switching frequency.
L is the inductor value.

The minimum dc current rating of the inductor must be greater than the inductor peak current. The inductor peak current is calculated using Equation 3.

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{I_{RIPPLE}}{2} \quad (3)$$

Inductor conduction loss is caused by the flow of current through the inductor, which has an associated internal dc resistance (DCR). Larger sized inductors have smaller DCR, which may decrease inductor conduction loss. Inductor core loss is related to the magnetic permeability of the core material.

Output Capacitor

Higher output capacitor values reduce the output voltage ripple and improve load transient response. When choosing an output capacitor value, it is also important to account for the loss of capacitance due to output voltage dc bias.

Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric that is adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. The X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. The Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converters because of their poor temperature and dc bias characteristics.

The peak-to-peak output voltage ripple for the selected output capacitor and inductor values is calculated using Equation 4.

$$V_{RIPPLE} = \frac{V_{IN}}{(2\pi \times f_{SW}) \times 2 \times L \times C_{OUT}} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}} \quad (4)$$

Capacitors with lower equivalent series resistance (ESR) are preferred to guarantee low output voltage ripple, as shown in Equation 5.

$$ESR_{COUT} \leq \frac{V_{RIPPLE}}{I_{RIPPLE}} \quad (5)$$

The minimum capacitance needed for stability, which includes temperature and dc bias effects, is 10 µF for Channel 3 and 10 µF for Channel 6 when the switching frequency is 2.5 MHz.

Channel 4 and Channel 6 Adjustable Output Voltage Setting

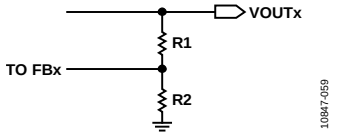


Figure 59. Channel 4 and Channel 6 Output Voltage (V_{OUTx}) Setting

In the case of the external VID setting ([VID4_1, VID4_0] = 00b for Channel 4 at Address 9 or [VID6_2, VID6_1, VID6_0] = 000b for Channel 6 at Address 10), the output voltages of these channels are programmed externally through resistor dividers to a value that is between 0.5 V and $V_{IN} \times 0.95$. Note that output voltage settings that are too low (for example, 0.5 V) may go out of regulation at high V_{IN} conditions due to the minimum on time limitation of Channel 6.

It is recommended that a current level of at least 300 µA lead to the FB node for Channel 6. In contrast, a current level in the 10s of microamps (µA) should be used for Channel 4. The output voltage is regulated around the reference voltage of the internal sense amplifier, which is set to 0.5 V (V_{FB4}, V_{FB6}). The relationship between the output voltage and the resistor divider network is provided by Equation 6.

$$V_{VOUTx} = V_{FBx} \times \left(1 + \frac{R1}{R2}\right) \quad (6)$$

Note that it could be required to change the output capacitor value when the output voltage level is extremely out of range from the VID option table. If the adjustable mode is used in the applications, it is recommended to contact an Analog Devices representative.

EXTERNAL COMPONENT SELECTION FOR THE BUCK-BOOST REGULATOR (CHANNEL 2)

Inductor Selection

The high 2.5 MHz switching frequency of Channel 2 allows for minimal output voltage ripple while minimizing inductor size and cost. Careful inductor selection also optimizes efficiency and reduces electromagnetic interference (EMI). The selection of the inductor value determines the inductor current ripple and loop dynamics.

$$\Delta I_{L,peak}\ (Boost) = \frac{(V_{OUT} - V_{IN})}{V_{OUT}} \times \frac{V_{IN}}{f_{OSC} \times L} \quad (7)$$

where:
f_{OSC} is the switching frequency (typically 2.5 MHz).
L is the inductor value in henrys (H).

A larger inductor value reduces the current ripple (and, therefore, the peak inductor current) but is physically larger in size with increased dc resistance. For increased efficiency, use a 2.2 µH inductor.

The inductor peak current is at its maximum in boost mode. To determine the actual maximum inductor current in boost mode, the input dc current should be estimated as follows:

$$I_{IN(MAX)} = I_{LOAD(MAX)} \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \frac{1}{\eta} \quad (8)$$

where η is efficiency (assume $\eta \approx 0.85$ to 0.90).

The saturation current rating of the inductor must be at least

$$I_{IN(MAX)} + \Delta I_{LOAD}/2 \quad (9)$$

Ceramic multilayer inductors can be used in low current designs for a reduced overall solution size and DCR. Such inductors are available in low profile packages. Care must be taken because these inductors derate quickly as the inductance value is increased, especially at higher operating temperatures.

Ferrite core inductors have good core loss characteristics as well as reasonable dc resistance. A shielded ferrite inductor reduces the EMI generated by the inductor.

Output Capacitor Selection

The output capacitor selection determines the output voltage ripple, the transient response, and the loop dynamics of the buck-boost regulator. The output voltage ripple for a given output capacitor is given by Equation 10.

$$\Delta V_{OUT,peak}(Boost) = \frac{I_{LOAD} \times (V_{OUT} - V_{IN})}{C_{OUT} \times V_{OUT} \times f_{OSC}} \quad (10)$$

If Channel 2 is operating in boost mode, the worst-case voltage ripple occurs for the lowest input voltage, V_{IN}.

The maximum voltage overshoot or undershoot is inversely proportional to the value of the output capacitor. To ensure stability and excellent transient response, it is recommended that a minimum of one 10 µF, X5R capacitor with a voltage rating of 6.3 V be used.

Input Capacitor Selection

Channel 2 requires an input capacitor to filter noise on the PVIN2 pins and to provide the transient current while maintaining constant input and output voltage. A 10 µF, X5R or X7R ceramic capacitor rated for 6.3 V is the minimum recommended input capacitor. Increased input capacitance reduces the amplitude of the switching frequency ripple on the battery. Because of the dc bias characteristics of ceramic capacitors, using a 0603, 10 µF, X5R or X7R ceramic capacitor with a voltage rating of 6.3 V is preferred.

Table 69. Suggested Output Capacitors for Channel 1, Channel 3, Channel 4, Channel 5, Channel 6, Channel 7, and Channel 8

Channel	Vendor	Working Voltage (V)	Capacitor (µF)	Model	Dimensions L × W × H (mm)
1, 3, 4	Murata	6.3	22	GRM21BR60J226ME39L	2.0 × 1.25 × 1.25
	Taiyo Yuden	6.3	22	JMK212BJ226MG-T	2.0 × 1.25 × 1.25
	Murata	10	10	GRM188R60J106ME47J	1.6 × 0.8 × 0.8
	Taiyo Yuden	6.3	10	JMK107BJ106MA-T	1.6 × 0.8 × 0.8
6	Murata	6.3	22	GRM21BR60J226ME39L	2.0 × 1.25 × 1.25
	Taiyo Yuden	6.3	22	JMK212BJ226MG-T	2.0 × 1.25 × 1.25
7	Murata	25	1	GRM188R61E105KA12D	1.6 × 0.8 × 0.8
	Taiyo Yuden	6.3	1	JMK107BJ105MA-T	1.6 × 0.8 × 0.8
5, 8	Murata	6.3	1	GRM155R60J105KE19D	1.0 × 0.5 × 0.5
	Taiyo Yuden	6.3	1	JMK105BJ105MV-T	1.0 × 0.5 × 0.5

Table 70. Suggested Output Capacitors for Channel 2

Vendor	Working Voltage (V)	Capacitor (µF)	Model	Dimensions L × W × H (mm)
Murata	6.3	10	GRM188R60J106ME47J	1.6 × 0.8 × 0.8
TDK	6.3	10	C1608JB0J106K	1.6 × 0.8 × 0.8
Taiyo Yuden	6.3	10	JMK107BJ106MA-T	1.6 × 0.8 × 0.8
Murata	6.3	10	GRM21BR71A106KE51L	2 × 1.25 × 1.25
Taiyo Yuden	6.3	10	JMK212BJ106MG-T	2 × 1.25 × 1.25

Table 71. Suggested Input Capacitors for Channel 1 to Channel 7

Vendor	Working Voltage (V)	Capacitor (µF)	Model	Dimensions L × W × H (mm)
Murata	6.3	10	GRM188R60J106ME47J	1.6 × 0.8 × 0.8
TDK	6.3	10	C1608JB0J106K	1.6 × 0.8 × 0.8

Table 72. Suggested Inductors

Channel	Vendor	Value (µH)	Rated Current (mA)	DCR (Ω)	Model	Dimensions L × W × H (mm)
1, 2, 4, 6	Murata	2.2	1300	0.08	LQM2HPN2R2MG0	2.5 × 2.0 × 0.9
	TDK	2.2	1300	0.08	MLP2520S2R2L	2.5 × 2.0 × 1.0
2, 4, 6[1]	TDK	4.7	1005	0.13	VLS3012ET-4R7M	3.1 × 3.1 × 1.2
7	TDK	4.7	1200	0.13	VLS3012T4R7N1RQ	3.1 × 3.1 × 1.2
	Murata	4.7	925	0.26	LQH3NPN4R7NG0	3.0 × 2.7 × 0.9
	TDK	4.7	1200	0.34	VLS3012T-4R7M1R0	2.6 × 2.1 × 1.2
3	Murata	1.0	2450	0.03	LQH44PN1R0NP0	4.0 × 4.0 × 1.8
	TDK	1.3	2560	0.019	VLCF5028T-1R3N2R5-2	5.0 × 5.0 × 2.8

[1] Using a switching frequency of 1.25 MHz.

EXTERNAL COMPONENT SELECTION FOR BOOST REGULATORS

Inductor

The high switching frequency of Channel 4 (1.25 MHz), Channel 1, and Channel 7 (2.5 MHz) allows for minimal output voltage ripple while minimizing inductor size and cost. Careful inductor selection also optimizes efficiency and reduces electromagnetic interference (EMI). The selection of the inductor value determines the inductor current ripple and loop dynamics.

For determining the inductor ripple current in continuous operation, the input (V_{IN}) and output (V_{OUT}) voltages determine the switch duty cycle (D) as shown in Equation 11.

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (11)$$

Using the duty cycle and switching frequency (f_{SW}), users can determine the on time as shown in Equation 12.

$$t_{ON} = \frac{D}{f_{SW}} \quad (12)$$

The inductor ripple current (ΔI_L) in steady state is

$$\Delta I_L = \frac{V_{IN} \times t_{ON}}{L} \quad (13)$$

Solve for the inductance value (L) as follows:

$$L = \frac{V_{IN} \times t_{ON}}{\Delta I_L} \quad (14)$$

Make sure that the peak inductor current (that is, the maximum input current plus half the inductor ripple current) is below the rated saturation current of the inductor. Likewise, make sure that the maximum rated rms current of the inductor is greater than the maximum dc input current to the regulator.

The current mode architecture of the boost regulator includes a slope compensation circuit necessary for duty cycles greater than 50% that occur with input voltages greater than one-half the output voltage.

Choosing the Input and Output Capacitors

Boost regulators require input and output bypass capacitors to supply transient currents while maintaining constant input and output voltages. Use a low ESR input capacitor of 10 µF or greater to prevent noise at the regulator input. Place the capacitor between VIN and GND as close to the regulator as possible. Ceramic capacitors are preferred because of their low ESR characteristics. Alternatively, use a high value, medium ESR capacitor in parallel with a 0.1 µF, low ESR capacitor as close to the regulator as possible.

The output capacitor maintains the output voltage and supplies current to the load while the regulator switch is on. The value and characteristics of the output capacitor significantly affect the output voltage ripple and stability of the regulator. Use a low ESR output capacitor; ceramic dielectric capacitors are preferable.

For Channel 7, the soft start time is affected by the output capacitor value. A larger output capacitor increases the soft start time. For Channel 1 and Channel 4, the soft start time is not affected by the output capacitor value unless the device reaches the current limit during soft start. Increasing the output capacitor value for Channel 4 may significantly increase inrush current because of the high boosting ratio. For very low ESR capacitors, such as ceramic capacitors, the ripple current due to the capacitance is calculated as follows. In continuous mode, because the capacitor discharges during the on time (t_{ON}), the charge removed from the capacitor (Q_C) is the load current multiplied by the on time.

Therefore, the output voltage ripple (ΔV_{OUT}) is

$$\Delta V_{OUT} = \frac{Q_C}{C_{OUT}} = \frac{I_L \times t_{ON}}{C_{OUT}} \quad (15)$$

where:
C_{OUT} is the output capacitance.
I_L is the average inductor current.

Using the duty cycle and switching frequency (f_{SW}), the user can determine the on time by using Equation 16.

$$t_{ON} = \frac{D}{f_{SW}} \quad (16)$$

The input (V_{IN}) and output (V_{OUT}) voltages determine the switch duty cycle (D), using Equation 17.

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (17)$$

Choose the output capacitor based on Equation 18.

$$C_{OUT} \geq \frac{I_L \times (V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times \Delta V_{OUT}} \quad (18)$$

The minimum output capacitor required for Channel 1 is a 10 µF, X5R capacitor; however, to maintain stability across the entire operating range and with component variations, it is recommended that one 22 µF, X5R capacitor with a voltage rating of 6.3 V be used. For Channel 4, a minimum of one 4.7 µF, X5R capacitor with a voltage rating of 25 V is needed. For Channel 7, a minimum of one 1 µF, X5R capacitor with a voltage rating of 25 V is required.

Diode Selection

The output rectifier conducts the inductor current to the output capacitor and to the load while the switch is off. For high efficiency, minimize the forward voltage drop of the diode. To achieve this, Schottky rectifiers are recommended. Be sure that the diode is rated to handle the average output load current. Many diode manufacturers derate the current capability of diodes as a function of the duty cycle. Verify that the output diode is rated to handle the average output load current with the minimum duty cycle.

The minimum duty cycle of the boost regulator is

$$D_{MIN} = \frac{V_{OUT} - V_{IN(MAX)}}{V_{OUT}} \quad (19)$$

where $V_{IN(MAX)}$ is the maximum input voltage.

Channel 7 LED Current Setting

Channel 7 is a boost regulator with a constant current control. This regulator is used to drive a string of LEDs in series with a constant current. The output voltage is automatically adjusted to the level needed to guarantee the desired LED current. This implementation offers the greatest efficiency and compensates for LED forward voltage variations.

Channel 7 can provide two options to determine the LED current: it can be programmed through the I^2C interface (IID setting) or controlled by an external PWM signal or a DAC (dimming setting), as shown in Figure 56.

An external resistor (R_{SET7}) connected between ISET7 and GND allows adjustment of the LED current. The relationship between R_{SET7} and the maximum LED current is given by Equation 20.

$$I_{LED} = \left(\frac{0.5}{R_{SET7}} + \frac{0.5 - V_{EXT}}{R_{DIM}} \right) \times \frac{32 - IID}{32} \times 1000000 \quad (20)$$

In the case of the IID setting, all of the components except R_{SET7} can be removed (see Figure 60). Therefore, in IID setting mode, Equation 21 is simplified as follows:

$$I_{LED} = \frac{0.5}{R_{SET7}} \times \frac{32 - IID}{32} \times 1000000 \quad (21)$$

Using this equation, when R_{SET7} = 15 kΩ, for example, the maximum current is 33 mA; and it can be programmed via Register VID78, Bits[7:3] (see Table 43), as shown in Table 73.

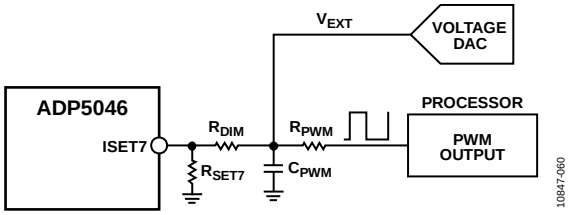


Figure 60. LED Current Setting with an External PWM Signal or DAC

Figure 62 shows an applications circuit allowing an external processor to fade the LED brightness with a PWM signal or a DAC. The relationship between the analog control signal, V_{EXT}, and the LED current, I_{LED} (mA), is given by Equation 21.

If a PWM signal is used to control the LED current, add a filter composed of R_{PWM} and C_{PWM} to transform the digital on/off signal to an analog voltage, proportional to the duty cycle of the PWM signal. The time constant of the RC filter depends on the PWM signal frequency, but it should be large enough to minimize the LED current ripple. R_{PWM} should be able to load R_{DIM}; for example, $R_{PWM} < R_{DIM}/10$.

Table 73. LED Current Programming (R_{SET7} = 15 kΩ)

IID (Decimal)	I_{LED} (mA)
0	33.3
1	32.3
2	31.3
3	30.2
4	29.2
5	28.1
6	27.1
7	26.0
8	25.0
9	24.0
10	22.9
11	21.9
12	20.8
13	19.8
14	18.8
15	17.7
16	16.7
17	15.6
18	14.6
19	13.5
20	12.5
21	11.5
22	10.4
23	9.4
24	8.3
25	7.3
26	6.3
27	5.2
28	4.2
29	3.1
30	2.1
31	1.0

TYPICAL POWER SUPPLY FOR DIGITAL STILL CAMERAS (DSC)

Figure 61 shows the system block diagram of the ADP5046 when it is used to power a digital still camera (DSC) system. An external microcontroller supplied from VREGO controls the power management activation.

The microcontroller controls the EN pin of the ADP5046 to turn the regulator rails on or off. Channel 1 (boost) is used to supply the camera motors and can provide a stable input voltage for other regulators that have an output voltage that is higher than the Li-Ion operating range. It is also recommended that the VDD voltage supply be applied from Channel 1. Channel 2 (buck-boost) provides the supply voltage for the I/O rail. Channel 3 and Channel 6 (buck) are used to supply the main processor core and memory, respectively. Channel 4 (buck) is dedicated to the supply rail of the CMOS sensor. Channel 7 provides the output voltage with constant current control for the LCD backlight and can support from two to five LEDs in series. The ADP5046 autonomously controls the backup battery charging and switchover in case the main battery is removed. The ADP5046 also contains a very low quiescent current real-time clock circuit that can operate independently of the main processor and can help to increase the backup time of the system in the absence of the main battery.

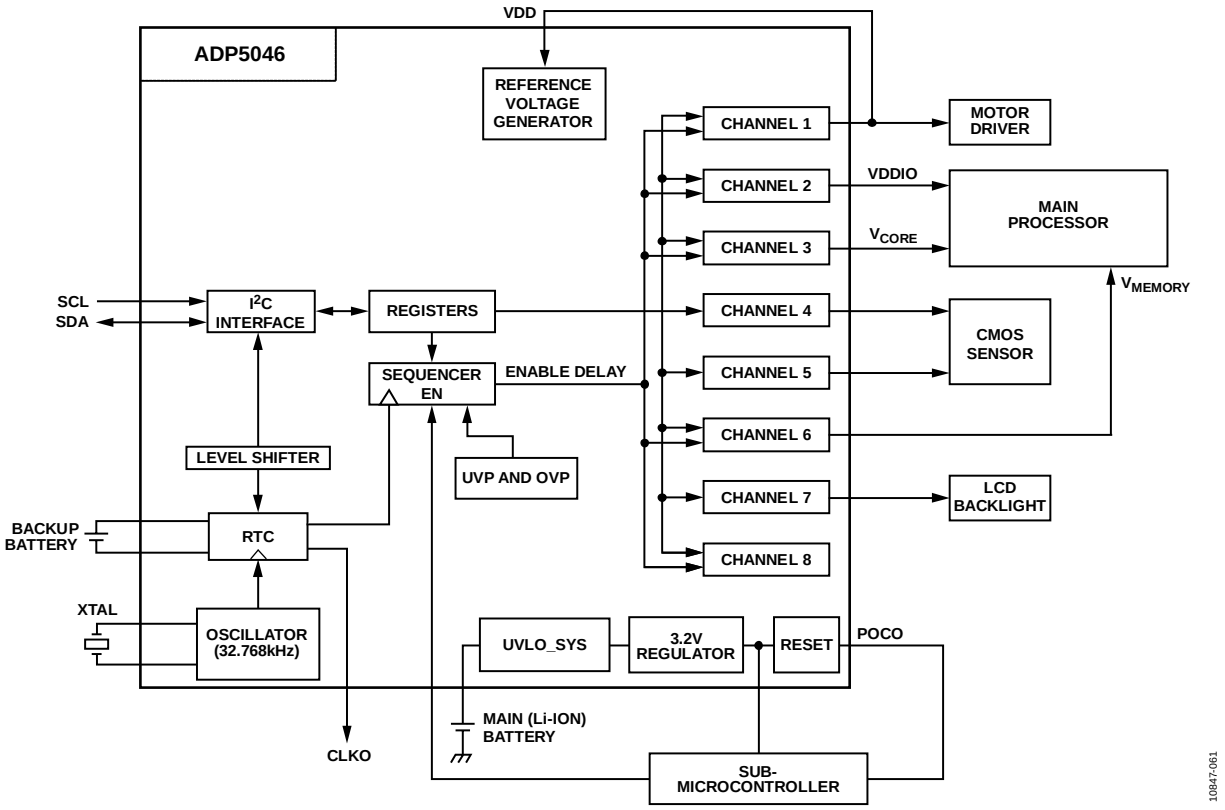


Figure 61. Top-Level Diagram in DSC Application

LAYOUT AND DESIGN RECOMMENDATIONS

For effective results, use at least a 6-layer printed circuit board (PCB) to provide the needed flexibility for routing to sensitive parts of the circuit and to allow optimal placement of the passive components. This also simplifies the distribution of the power planes for the ground and the input and output power rails.

For best EMI containment, use a solid power ground plane as one of the inner layers and extend it fully under all the power components.

As a general recommendation, avoid running sensitive lines beneath the ADP5046 or the inductors. Each switching regulator feedback trace should be routed from the output capacitor pad to the respective feedback input. In addition, these traces should be as short as possible and should not be placed in close proximity to noisy or switching signals. If needed, remove the vias and use a layer containing a ground plane to shield the feedback trace from the output capacitor to the feedback pin.

The majority of the switching regulator signals are located at the outer bumps of the device, providing direct connections for external components. Do not use vias to connect these signals to external components, such as inductors, diodes, and capacitors.

When designing the layout, it is important to know the specific layout requirements for each switching regulator topology because the current shape in each node of the circuit is different and can adversely affect the functionality and/or noise of the system.

A buck regulator has a discontinuous current flowing from the input capacitor to the PFET switch and then to either the load (during the on time) or the NFET switch (during the off time) before returning from the ground. The input capacitor, together with the input source, provides current to the load and output capacitor during the on time and is recharged during the off time. To minimize noise, keep this loop as short as possible. Therefore, the input capacitor must be placed in close proximity to the PVINx pin with a direct connection and without vias, and the return side of the input capacitor must be connected directly (with no vias) to the dedicated power ground pin (PGNDx). The switching node (SWx) connection to the inductor must be as short as possible with no vias. The output capacitor must be connected to the inductor with a short trace, and the return side must be connected directly to the dedicated power ground pin (PGNDx).

A boost regulator has discontinuous current flowing in the output node. The output capacitor provides current to the load during the on time, and it is recharged by the energy stored in the inductor during the off time. To minimize noise, keep the current loop in the output node as short as possible. Therefore, the output capacitor must be connected to the VOUTx pin and the dedicated power ground (PGNDx) with short traces and no vias. In addition, the input capacitor must be placed as close as possible to the inductor and be connected to one side of the inductor with a short connection. However, this is not as critical as the length of the output capacitor traces because the input current in a boost regulator has continuous shape. The other side of the inductor must be connected to the switching node (SWx) and the external diode (if needed) with a short trace to minimize the irradiative noise that can perturb other circuits. In particular, Channel 1 has the highest output power. Therefore, it is important to place the output capacitor with the shortest trace.

The buck-boost input and output current shape depends on the mode of operation of the regulator. When designing the layout, use the considerations presented for buck and boost regulators and be sure to keep the input and output capacitors as close as possible to the pins of the ADP5046. In addition, keep the inductor connection as short as possible.

Regardless of the regulator in use, keep noisy signals (such as switching nodes) away from the XIN, XOUT, FB3, FB4, FB6 and ISET7 pins. These signals connect to sensitive analog circuits inside the ADP5046 and may affect device functionality.

Place the RTC compensation capacitors and crystal as close as possible to the ADP5046. Furthermore, the crystal and compensation capacitors should be tied to RTCGND without sharing the node to any other ground. The traces connecting the crystal to the ADP5046 should be routed as a differential pair and have a ground guarding in between to prevent noise issues. The oscillator circuit must be laid out carefully because its performance can easily be affected by the errors due to the parasitic impedance of the PCB board, crystal, and compensation capacitors. The XIN and XOUT pins each have a 3 pF internal capacitor.

THERMAL CONSIDERATIONS

The ADP5046 provides high efficiency performance. However, in applications with maximum loads at high ambient temperature (T_A), low supply voltage, and high duty cycle, the heat dissipated on die may exceed the maximum junction temperature of 125°C. If the junction temperature (T_J) exceeds 160°C, the ADP5046 goes into thermal shutdown. It recovers when the junction temperature falls below 140°C. The junction temperature can be calculated by the following equation:

$$T_J = T_A + T_R \quad (22)$$

where:
T_R is the rise in temperature of the package due to power dissipation.

The rise in temperature of the package is directly proportional to the power dissipation in the package, as shown in the following equation:

$$T_R = PD_{LOSS} \times \theta_{JA} \quad (23)$$

where:
PD_{LOSS} is the power dissipation in the package.
θ_{JA} is the junction-to-ambient thermal resistance of the package.

To investigate the junction temperature in the package, it is recommended, instead, that the case temperature of the package be measured under worst-case conditions. The case temperature (T_C) can be calculated by the following equation:

$$T_C = T_A + PD_{LOSS} \times (\theta_{JA} - \theta_{JC}) \quad (24)$$

where:
θ_{JC} is the junction-to-case thermal resistance of the package, which is 0.2°C/W.

The power dissipation in the package is extracted from Equation 24. T_J can be estimated by the following equation, which is derived from a combination of Equation 22, Equation 23, and Equation 24:

$$T_J = T_A + (T_C - T_A)/(\theta_{JA} - \theta_{JC}) \times \theta_{JA}$$

The estimated junction temperature should be less than the maximum junction temperature of 125°C.

APPLICATIONS CIRCUIT

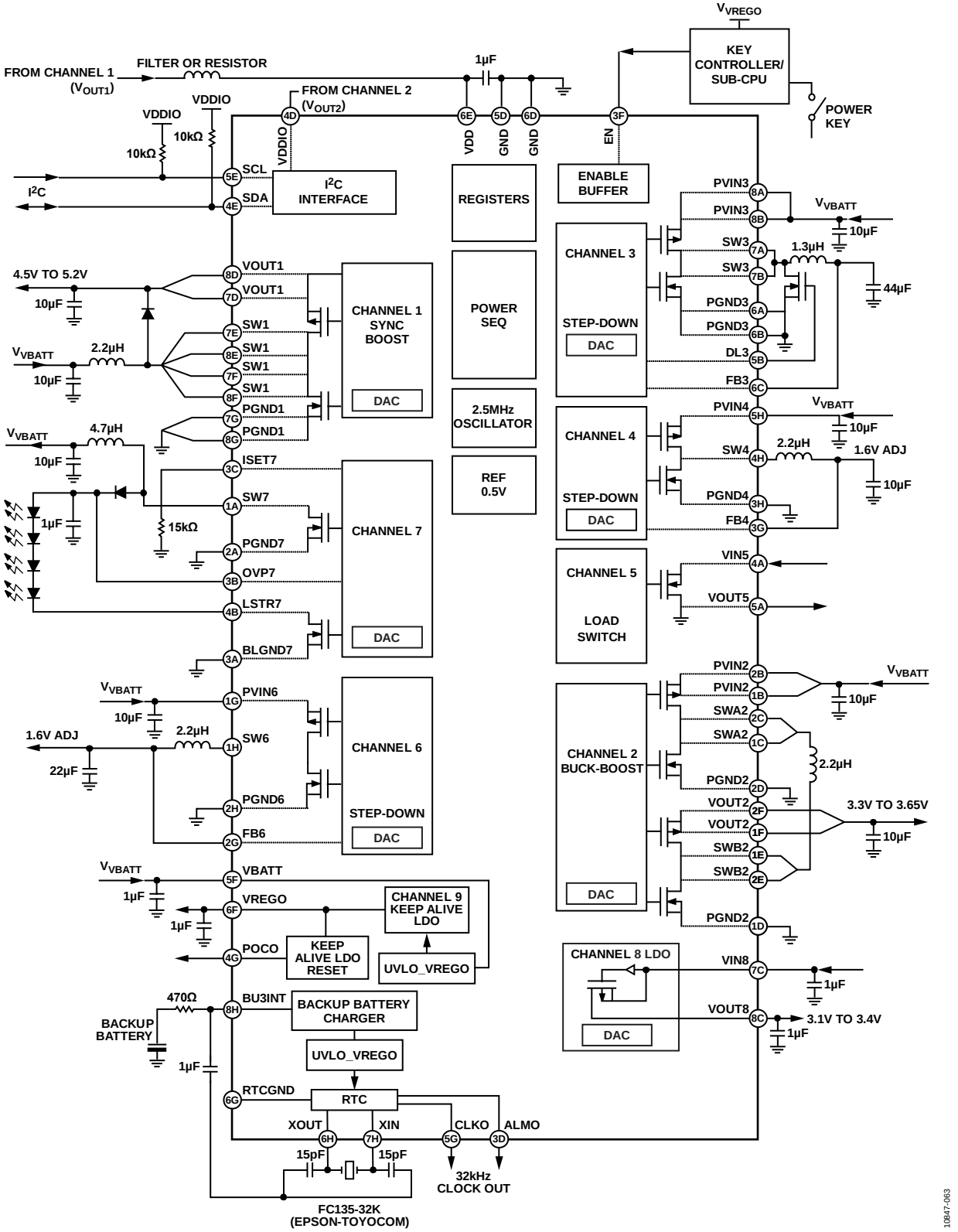


Figure 62. Typical Applications Circuit

TRIM SETTINGS FOR THE ADP50460008

FACTORY PROGRAMMING DEFAULTS

For more information about the available factory programming options, contact an Analog Devices representative.

Table 74. Factory Programming Default Settings

Address (Dec)	Bit Numbers	Bit Name	Setting	Binary Code	Decimal Code
N/A	N/A	OPT_UVLO_SYS_F	2.4 V (falling)	0	0
N/A	N/A	OPT_UVLO_SYS_R	2.6 V (rising)	0	0
102	0	OPT_ALMO	Autoenable not used	0	0
101	[5:4]	OPT_UV_DLY	78 ms	01	1
101	[1:0]	OPT_OV_DLY	1.2 ms	01	1
100	1	OPT_MODE_EN6	Sequencer	1	1
100	0	OPT_MODE_EN8	Sequencer	1	1
N/A	N/A	I2C_CHIP_ADDRESS[1:0]	0x30	00	0
98	0	VID_REGO	3.2 V	0	0
97	6	SEL_FREQ7	1.25 MHz	0	0
97	4	SEL_FREQ4	2.5 MHz	1	1
97	[3:2]	SEL_FREQ3	1.25 MHz	00	0
97	1	SEL_FREQ2	1.25 MHz	0	0
97	0	SEL_FREQ1	2.5 MHz	1	1
N/A	N/A	SEL_EXT_CLK	RTC function not used	1	1
N/A	N/A	SEL_EXT_OSC	Internal RC oscillator	1	1
11	[2:0]	VID8	2.5 V	101	5
10	[2:0]	VID6	Adjustable	000	0
9	[7:4]	VID3	1.10 V	1000	8
9	[1:0]	VID4	1.80 V	10	2
8	[6:4]	VID1	5.3 V	000	0
8	[2:0]	VID2	3.3 V	111	7
7	[2:0]	DIS_DLY	0 ms	000	0
6	[7:4]	EN_DLY8	6 ms	0011	3
5	[7:4]	EN_DLY3	4 ms	0010	2
5	[3:0]	EN_DLY6	2 ms	0001	1
4	[7:4]	EN_DLY1	0 ms	0000	0
4	[3:0]	EN_DLY2	8 ms	0010	4
2	7	SS1	4 ms	0	0
2	6	SS2	4.5 ms	0	0
2	5	SS3	1.3 ms	1	1
2	4	SS4	4 ms	0	0
2	3	SS5	Long	0	0
2	2	SS6	1.3 ms	1	1
2	1	SS7	8 ms	0	0
2	0	SS8	1.3 ms	1	1
1	4	DSCG4_ON	On	1	1
1	3	DSCG2_ON	On	1	1
1	2	DSCG3_ON	On	1	1
1	1	DSCG5_ON	On	1	1
1	0	DSCG6_ON	On	1	1

OUTLINE DIMENSIONS

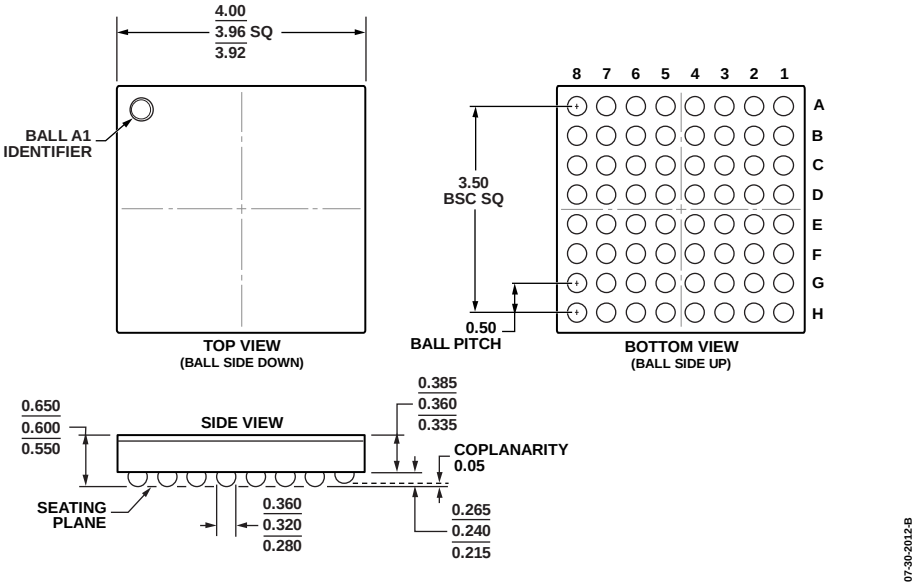


Figure 63. 64-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-64-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP50460008CBZR	−25°C to +85°C	64-Ball Wafer Level Chip Scale Package [WLCSP], 0.5 mm Pitch	CB-64-4

[1] Z = RoHS Compliant Part.

NOTES

NOTES

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).