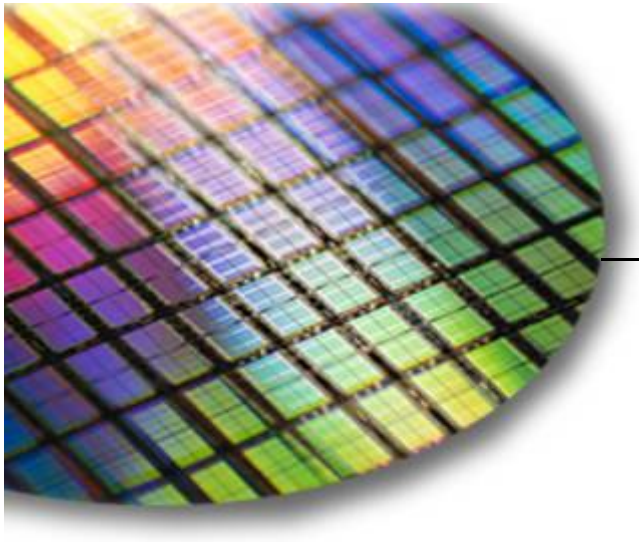


The World Leader in High Performance Signal Processing Solutions

ADP1046 Improvements

ANALOG DEVICES

ADP1046 Design Changes
Key issues resolved from ADP1043A

- **Improved architecture for control loop**
  - **Improve transient response**
  - **Reduce residual ripple noise**
  - **Allows current sharing**
  - **Increased HF ADC range**
- **Soft Start issues**
  - **Dedicated Type 3 Soft Start filter**

ANALOG DEVICES

ADP1046 Design Changes
Additional improvements

- **Fast ORFET comparator improvements**
- **Programmable smooth filter transitioning**
- **Improved Volt-sec balance (supports phase shifted mode)**
- **Adaptive dead time timing, fully programmable**
- **SR Turn off speed (3 new speed options)**
- **Light Load mode hysteresis (programmable hysteresis)**
- **Voltage Feed Forward, to improve transient response**
- **Improved and more flexible Flag response**
- **Improved CS1 current sensing and measuring**
- **Improved high side current sensing**
- **Dedicated fast OVP comparator**
- **Voltage Slew rate control**
- **Improved Droop-sharing control**
- **Improved constant current sharing function**
- **Programmable PGOOD1/2 functions**

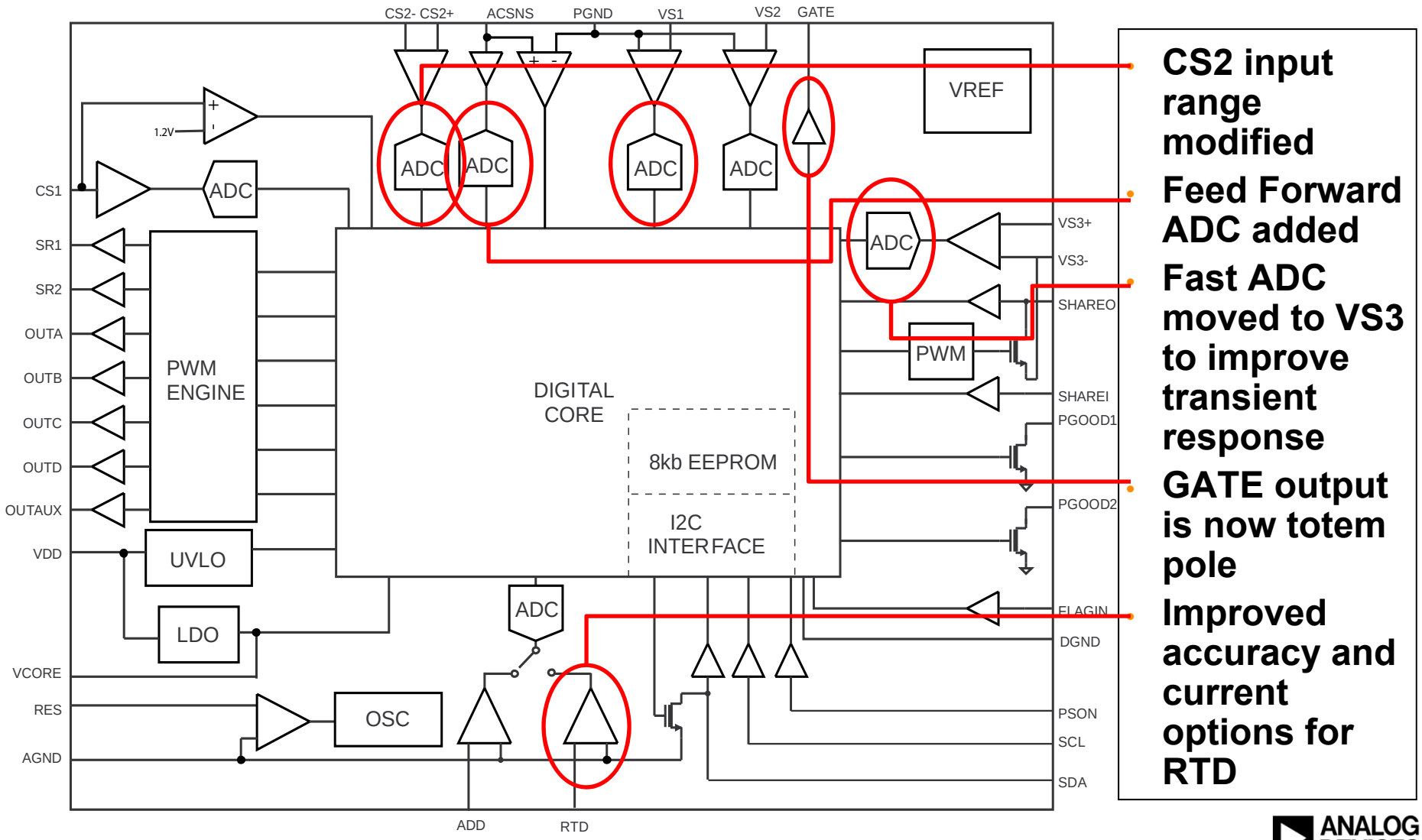
ANALOG DEVICES

ADP1046 → ADP1043A compatibility

- **Same Pinout – no layout changes**
- **Minimized component change**
- **95% register setting backward compatibility**
- **New GUI with same look and feel, plus new features**

ANALOG DEVICES

ADP1046 Affected Analog blocks



- **CS2 input range modified**
- **Feed Forward ADC added**
- **Fast ADC moved to VS3 to improve transient response**
- **GATE output is now totem pole**
- **Improved accuracy and current options for RTD**

ANALOG DEVICES

External Components Changes
Same Pinout/PCB Layout as ADP1043A/B

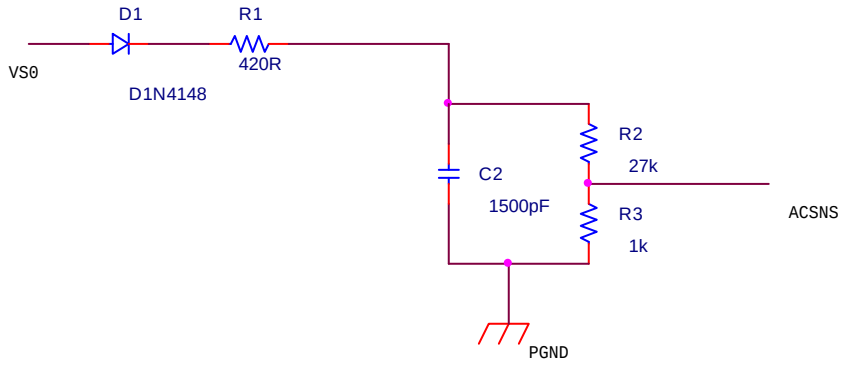
Change Reason	Pin affected	ADP1043A/B	ADP1046
RES pin current increased to improve noise immunity	RES (30)	50kΩ	10kΩ
CS2 level shifter current increased to improve noise immunity (low side)	CS+ (5)	10kΩ	5kΩ
CS2 level shifter current increased to improve noise immunity (low side)	CS- (4)	10kΩ	5kΩ
RTD : more options added, still backward compatible w/ ADP1043A	RTD(28)	100kΩ	16.5k||(100 kΩ NTC)
Feed forward ADC added on ACSNS, needs RC filtering	ACSNS		See next slide
GATE is now totem pole	GATE	Needs pull-up	No pull-up
Bypass cap	VCORE	100nF	330nF

ANALOG DEVICES

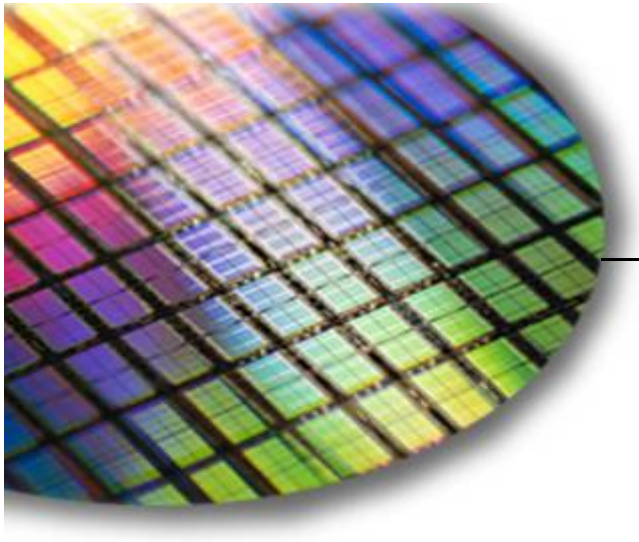
External Components Changes
Same Pinout/PCB Layout as ADP1043A/B

1. R1 limits charging of C2 during initial spike.
2. R1C1 chosen to be higher than spike duration.
3. R2-R3 should give about 1V at Vin_max and should not be greater than Ts

Alternately we can use a diode (D1) that has very slow turn on time >200ns which is the approximate duration of the spike.

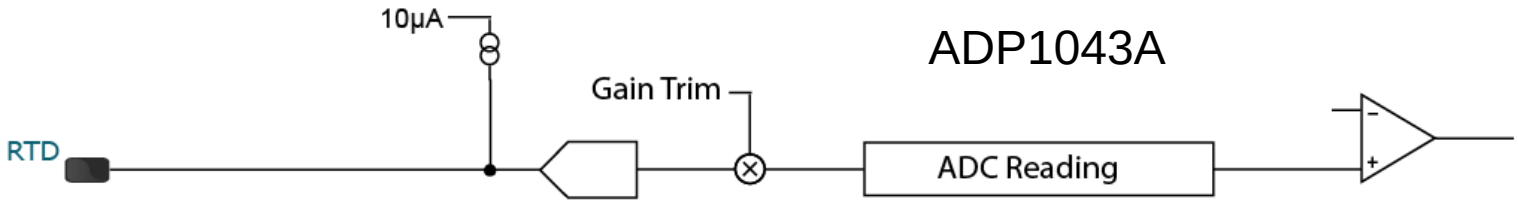


Typical application circuit for line voltage feedforward

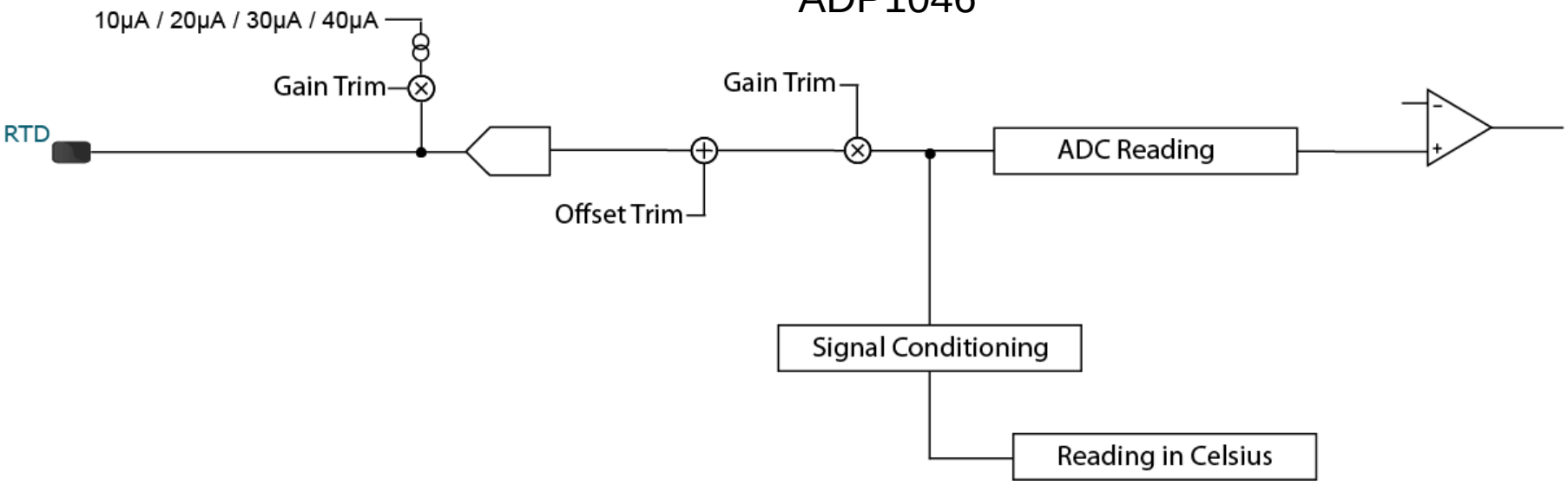


Other Improvements/Changes

RTD Changes

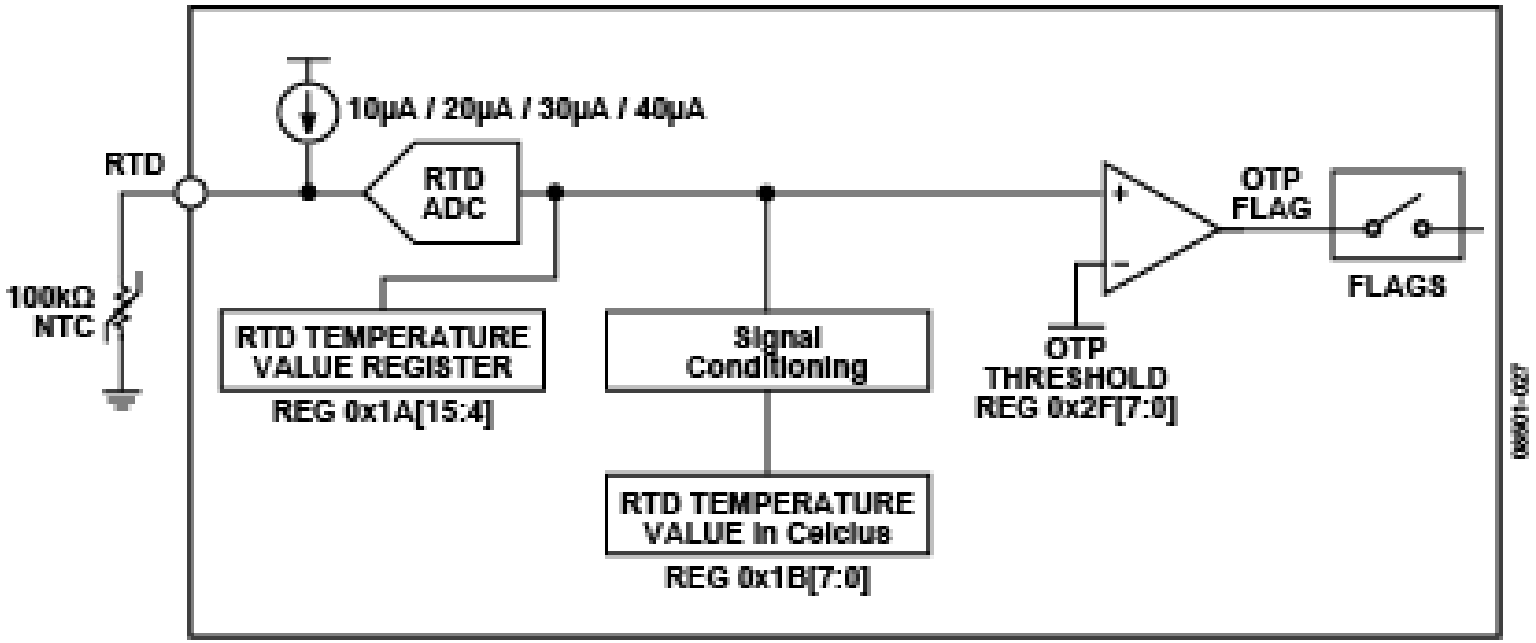


ADP1043A



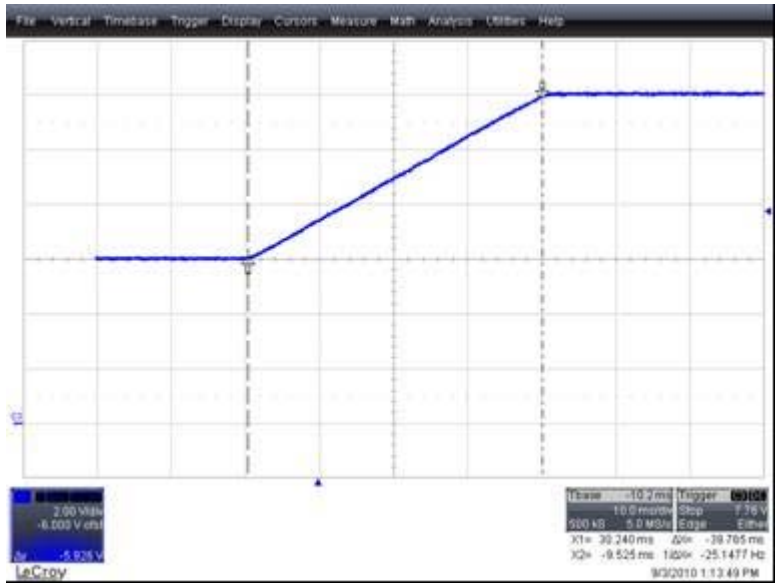
ADP1046

ADP1046 RTD structure

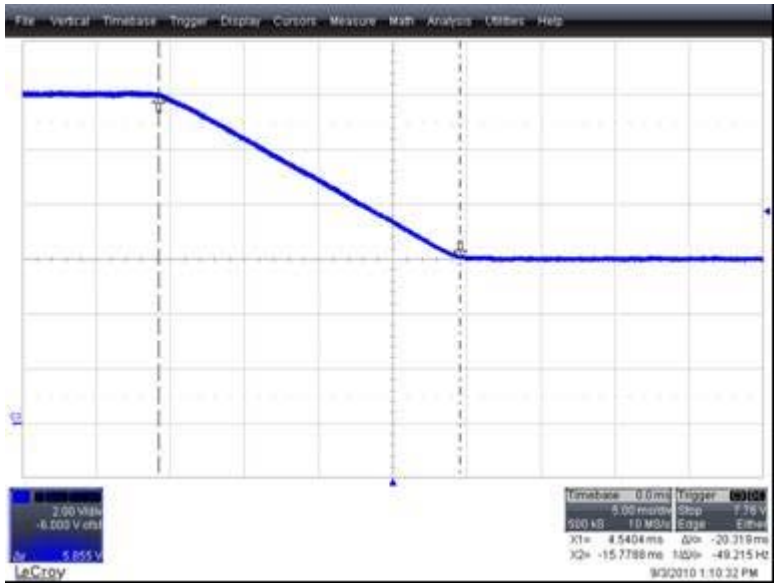


VOUT slew rate control

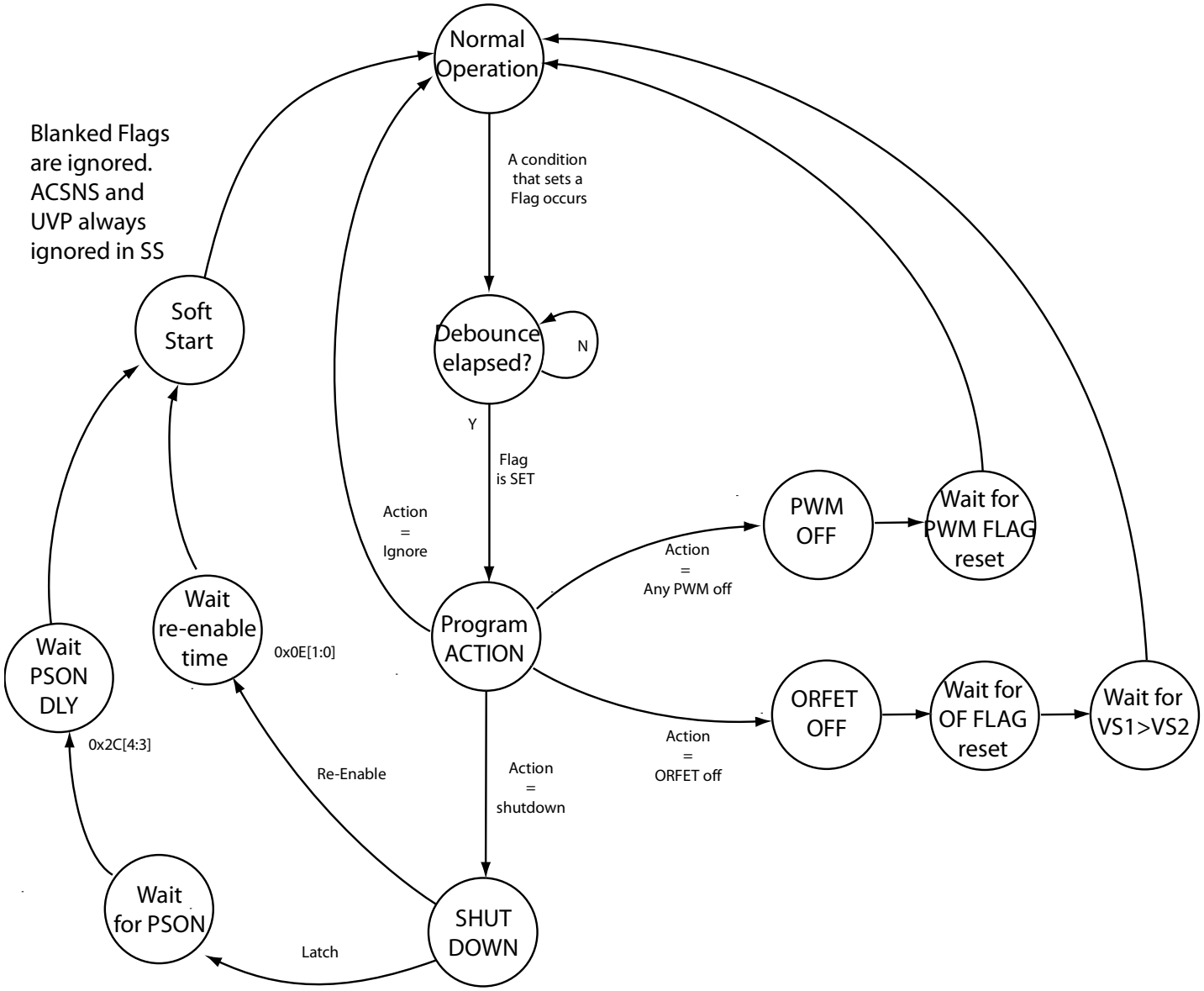
6V to 12V with 12.5mV/V slew rate
Time scale 10mV/div



12V to 6V with -25mV/V slew rate
Time scale 5ms/div



Flags State Diagram

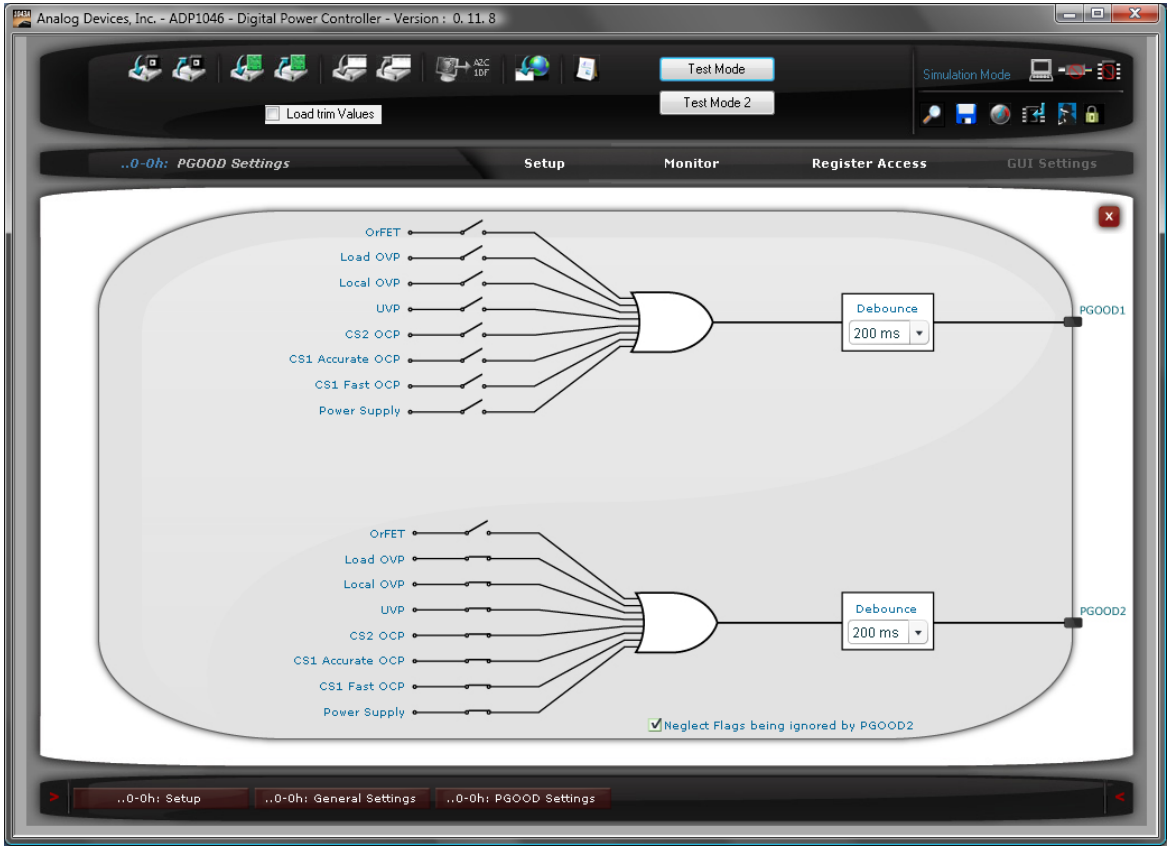


ADP1046 fault responses

Table 1. Register 0x08 to Register 0x0D—Fault Configuration Register Bit Descriptions

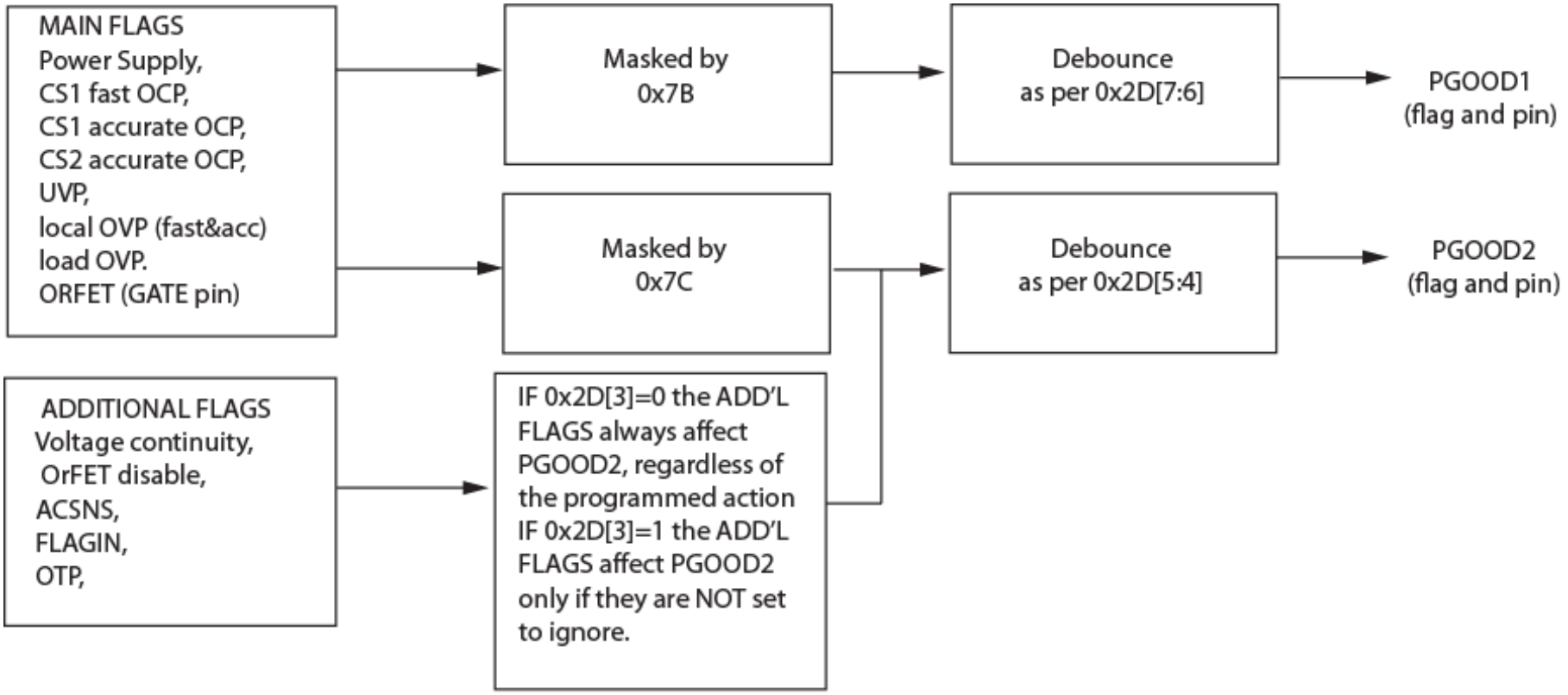
Bits	Name	R/W	Description			
7	Timing	R/W	This bit specifies when the flag is set. 0 = after debounce. 1 = immediately.			
[6:4]	Action	R/W	These bits specify the action that the part takes in response to the flag.			
			Bit 6	**Bit 5**	**Bit 4**	**Action**
			0	0	0	Ignore flag completely
			0	0	1	Disable SR1 and SR2
			0	1	0	Disable OrFET
			0	1	1	Disable power supply and reenable after the power supply reenable time set in Register 0x0E[1:0].
			1	0	0	Disable OUTAUX
			1	0	1	Disable all PWMs except OUTAUX
			1	1	0	Disable SR1, SR2 and ORFET
			1	1	1	Disable power supply and remain disabled; PSON signal necessary to restart

3. PGOOD masking function.

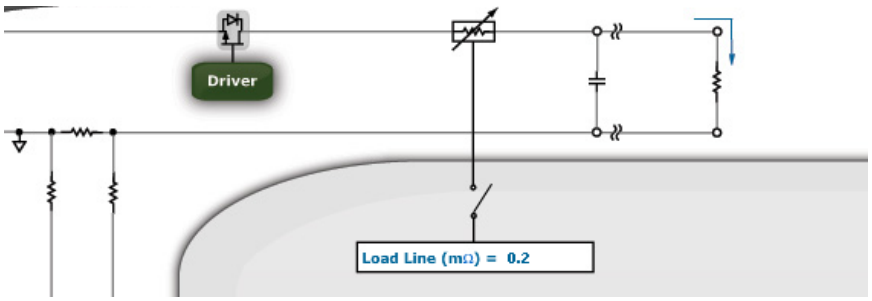


- **In ADP1043A PGOOD1 and 2 are set by a fixed list of flags.**
- **In ADP1046 the user can select which flags set PGOOD1/2 independently.**
- **Also separate debounce times are used for the two flags.**

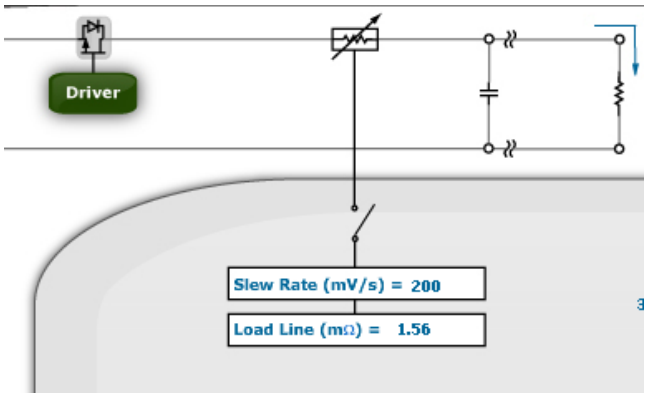
PGOOD1/2 Operation



2. Droop sharing control.

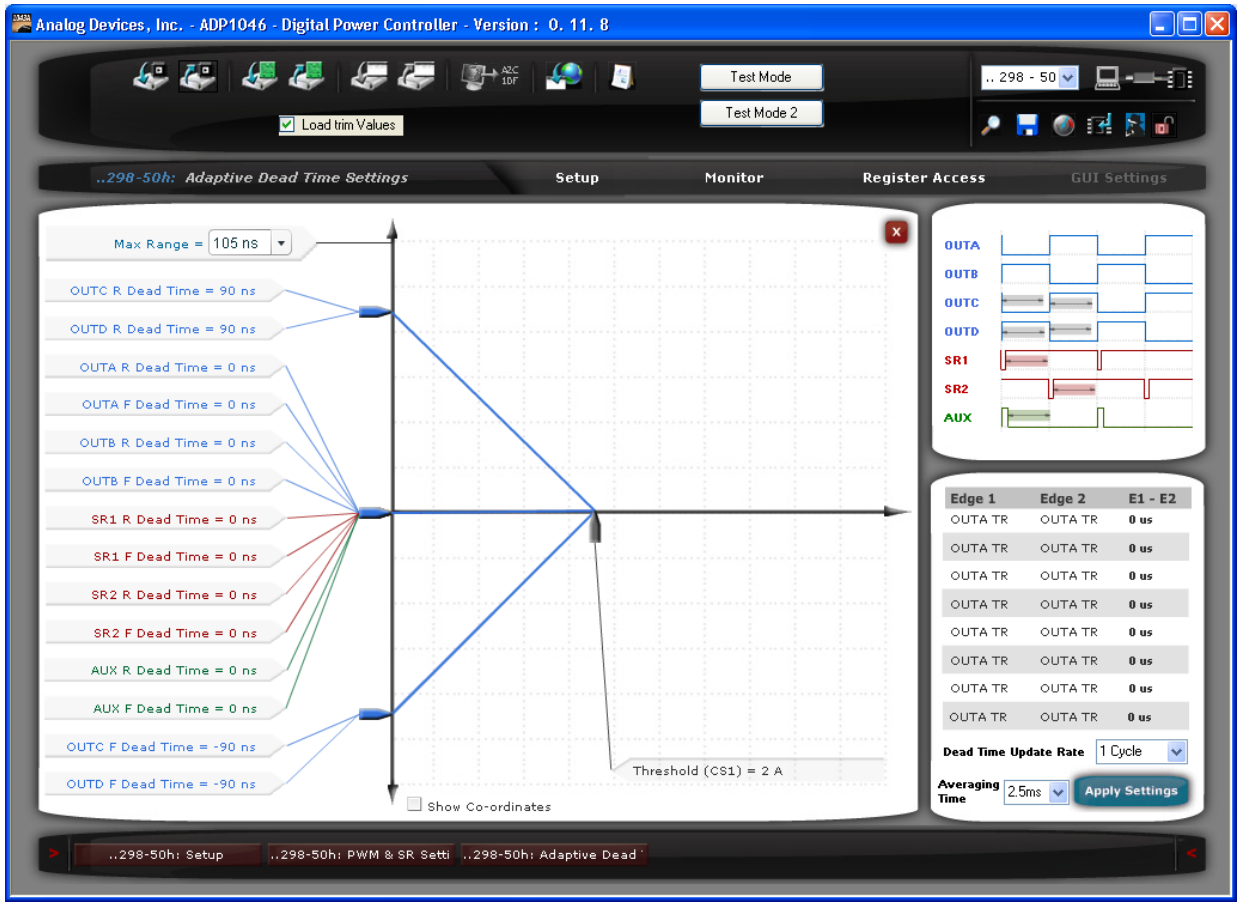


ADP1043A: load line updated every 10ms, abrupt transition, no slew rate control. This caused step change in the voltage reference and impossible to droop share.



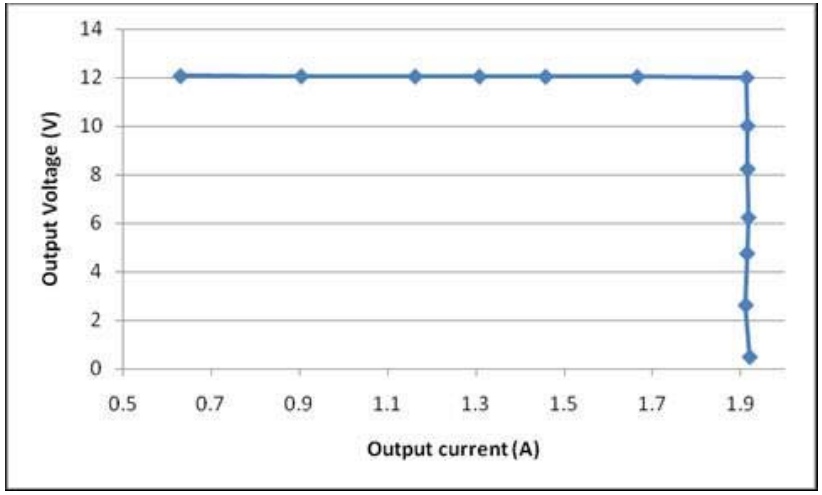
ADP1046: load line is updated continuously and the slew rate for the change of the reference is limited and programmable.

GUI set up window example for ADT



In this example, only rising/falling edge of OUTC and OUTD is implemented for ADT with a offset change of 90ns (step change of 15 ns with a multiplier of 6), the current threshold level is 2A.
The edge change rate is 5ns per switching cycle. CS1 update rate is 2.5ms

Constant Current Mode



- **Test: CC current set at 1.9A. A resistive load was used to decrease the load resistance from 19Ω to 0Ω.**
- **Output voltage was measured at VS3+ and VS3-.**

ANALOG DEVICES