24-Bit Stereo DAC Evaluation Board

EVAL-AD1853EB

OVERVIEW

The AD1853 (EVAL-AD1853-EB) evaluation board permits testing and demonstration of the high performance AD1853 24-bit Stereo DAC. An input signal is required in either optical or coaxial SPDIF format or alternatively directly via a 10-pin header in I^2S, left justified, right justified or DSP modes. A second 10-pin header allows control of the internal registers from an external controller.

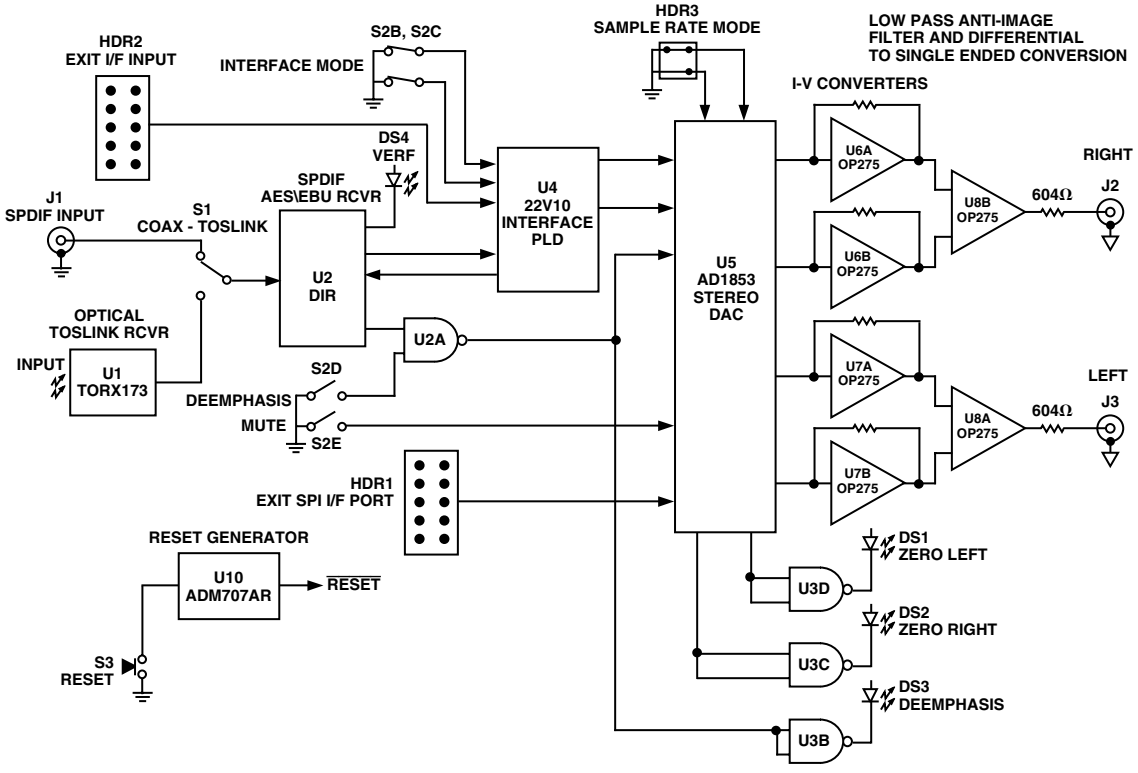
Power requirements are a +12 V to +15 V dc source for the digital section and ±15 V dc for the analog section. On board regulators derive separate "clean" 5 V dc supplies for the digital and analog sections. Audio output is provided from two RCA phone jacks.

AD1853 OVERVIEW

The AD1853 is a complete high performance single-chip stereo digital audio playback system. It is comprised of a multibit sigma-delta modulator with dither, continuous time analog filters, and analog output drive circuitry. Other features include an on-chip stereo attenuator and mute, programmed through an SPI-compatible serial control port. The AD1853 is fully compatible with all known DVD formats including 192 kHz as well as 96 kHz sample frequency and 24 bits. It also is backwards compatible by supporting 50 µs/15 µs digital de-emphasis intended for "redbook" compact discs, as well as de-emphasis at 32 kHz and 48 kHz sample frequencies.

The AD1853 has a very simple but very flexible serial data input port that allows for glueless interconnection to a variety of ADCs, DSP chips, AES/EBU receivers and sample rate converters. The AD1853 can be configured in left justified, I^2S, right justified, or DSP serial port compatible modes. It can support 16/20 and 24 bits in all modes. The AD1853 accepts serial audio data in MSB first, twos-complement format. The AD1853 operates from a single +5 V power supply. It is fabricated on a single monolithic integrated circuit and is housed in a 28-lead SSOP packages for operation over the temperature range 0°C to +70°C.

FUNCTIONAL BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

The AD1853 evaluation board presents a reference design that can be used as a suggested layout and circuit implementation, which will deliver optimal performance from the audio DAC. As far as is possible, on an evaluation board, current assembly methods and components are used. Most components are surface mount devices and a four-layer printed circuit board is used with full internal power and ground planes for superior noise performance. A schematic, bill of materials, PLD source code and PCB plots are included for guidance.

POWER SUPPLIES

The board is divided into analog and digital sections, each with separate power supplies.

The digital power supply input is via binding post terminals J4 and J5. The recommended digital supply is +15 V dc at 120 mA ± 25 mA. An on-board voltage regulator (U9) provides +5 V dc, ±5% to the digital circuitry.

The analog power supply inputs are binding posts J6, J7 and J8. Recommended analog supply is +15 V dc at 40 mA ± 10 mA and –15 V dc at –20 ± 5 mA. An on-board, low noise voltage regulator (U11) provides +5 V dc, ±5% to the analog power pins of the AD1853 DAC.

DIGITAL SIGNAL INPUTS

RCA phone Jack J1 and optical TOS Link input U1 may be used for standard consumer mode SPDIF input signals. J1 is terminated with a 75 Ω resistor. Switch S1 selects between J1 and U1 inputs and feeds the selected signal to the digital interface receiver (U2). Switch S2A chooses between the SPDIF input and the direct input via the 10-pin header, HDR2 "EXT I/F IN."

The "EXT I/F IN" input permits buffered (U4, 22V10) access to the BCLK, LRCLK, SDATA and MCLK inputs of the AD1853 DAC. This permits testing with left justified, I^2S or right justified, serial input modes. Note that with right justified input data, the AD1853 control register must be programmed for the correct number of data bits, i.e., 16, 20 or 24 bits. When using the direct input header, it is necessary to provide all four signals, MCLK, BCLK, LRCLK and SDATA. A termination network consisting of a series connected 100 Ω resistor and a 47 pF capacitor is shunted across each signal line to reduce line reflections.

EXTERNAL SPI CONTROL PORT

An external, pseudo SPI control port, HDR1 "EXT µC I/F", is provided via a 10-pin header, so that the AD1853 internal volume control and control registers can be programmed from an external host or microcontroller. This port accepts serial data to independently set the left/right volume or the operating mode of the AD1853 by programming the contents of three internal 16-bit registers. Details of the signal format and timing are discussed in the AD1853 data sheet.

AUDIO SIGNAL OUTPUTS

RCA Jacks J2 and J3 provide left and right audio output. The output is low-pass filtered with an anti-image filter and converted from a differential current output to a single ended voltage output by op amps, U6, U7 and U8. The filter –3 dB cutoff frequency is 75 kHz and has an approximate 4th order linear phase Bessel response. The output impedance is 600 Ω. The full-scale output signal is 4.2 V rms (12 V p-p).

SWITCH AND JUMPER FUNCTIONS

Slide switch S1, DIP switch S2 and push button S3 are used to control the operation of the evaluation board. An additional header, HDR3 is provided to permit control of the AD1853 internal interpolation filter to optimize performance for different sample rates.

S1 is used to select between the RCA "SPDIF INPUT" and the "TOSLINK" optical input, U1.

DIP switch S2 provides four functions:

- S2A switches between the "SPDIF" inputs and the "EXT I/F IN", via the 10-pin header, HDR2.
- S2B "IDPM0" and S2C "IDPM1" are used to select the AD1853 "INTERFACE MODE." Table I shows the available interface modes.

Table I.

Serial Interface Format	IDPM1 (S2C)	IDPM0 (S2B)
Right Justified—16-Bit Only	0	0
I^2S	0	1
Left Justified	1	0
DSP Mode	1	1

- S2D is used to switch on the AD1853 "DEEMPHASIS" filter which is confirmed by illumination of the "DEEMPH" LED, DS3.
- S2E is used to activate the AD1853 "MUTE" function.

The default S2 switch positions are shown in Figure 1.

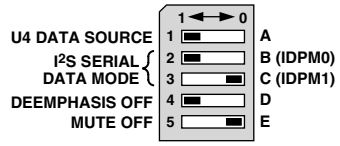

Figure 1.

Push button S3 provides a "RESET" function via reset generator U10 (ADM707) and a "clean" 200 ms delay after release. U10 also provides a 200 ms reset pulse at power-up.

Header HDR3 jumpers are selected according to Table II. The default is 8× interpolation, i.e., both jumpers are installed.

Table II.

Interpolation Ratio	INT2× (HDR3-1)	INT4× (HDR3-2)
8× (44.1 kHz or 48 kHz)	0	0
4× (88.2 kHz or 96 kHz)	0	1
2× (176.4 kHz or 192 kHz)	1	0
Not Allowed	1	1

INDICATOR DISPLAY LEDS

Five red LED indicators are provided for status indication.

- Display LEDs DS1, "ZL" and DS2, "ZR" are provided to show that the AD1853 is detecting a zero signal in either the left or right channel respectively.
- Display LED DS3, "DEEMPH" indicates that either switch S2D has been selected or that the incoming signal has the "EMPHASIS" status bit set. In either case, illumination of DS3 indicates that the DEEMPHASIS filter function of the AD1853 is active.
- Display LED DS4, "VERF" indicates that the SPDIF digital interface receiver has detected an error condition in the received signal.
- Display LED DS5, "POWER", is showing the presence of +5 V dc on the analog +5 V power supply.

INTEGRATED CIRCUIT FUNCTIONS

There are 11 active devices on the AD1853 evaluation board. Following is a brief description of the function of each part.

- U1 (TORX173) is the Toshiba digital audio optical receiver. This part accepts the visible red SPDIF modulated signal and converts it to a standard TTL digital signal suitable for input to the digital audio receiver (U2).
- U2 (CS8414-CS) receives and decodes the serial SPDIF, digital audio encoded signal and decodes the audio information. Four digital audio signals are decoded by the CS8414. The serial data SDATA, the master clock at 256 F_S, MCLK, the left/right frame clock LRCLK and the serial bit clock at 64 F_S, BCLK. The output interface mode of U2 must be compatible with the input to the AD1853 (U5) and this is selected at the same time as the mode for the AD1853 is selected via switches S2B (IDPM0) and S2C (IDMP1).
- U3 (74HC00D) is a quad, two input NAND gate and provides miscellaneous buffering and interface functions.
- U4 (22V10) provides decoding, buffering and selection functions between the different modes of operation.
- U5 (AD1853JRS) is the high performance stereo DAC. Depending upon selected modes of operation, sample rates up to 192 kHz and 24 bits may be tested.
- U6, U7, U8 (OP275) is a low noise and distortion, audio op-amp. U6 and U7 provide current to voltage conversion and a single low-pass real pole for the output of the AD1853 while U8 provides differential to single ended conversion and a low pass complex pole pair. An overall third order low pass Bessel filter is implemented, followed by a single RC filter low pass filter pole. The over all response is approximately linear phase with a –3 dB corner frequency of 75 kHz and an 80 dB/decade roll-off.
- U9 (LM317) provides +5 V dc low voltage regulation for the digital section of the evaluation board.
- U10 (ADM707AR) is a RESET generator that provides a debounced reset signal from the push button (S3) or a 200 ms reset pulse on power up.
- U11 (AD3303-5.0) is a low noise +5 V dc regulator for the analog section of the AD1853.

PERFORMANCE SPECIFICATIONS

The typical evaluation board performance is tabulated below.

1. SNR	–113 dBFS ±1 dB
2. DR, A-Weighted	–115 dBFS ±1 dB
3. THD+N	–103 dBFS ±2 dB
4. Frequency Response	±0.25 dB, 10 Hz to 20 kHz
5. Noise Floor	–145 dBFS
6. Full Scale Audio Output	4.2 V rms

AD1853 INTERFACE GLUE LOGIC (U4)

This chip handles the logic interface for selecting between external and internal signal sources for the DAC. It also handles the decoding of the mode control switch to set the operating mode for the CS8414 and the AD1853.

```
INPUT EX_SDATA, EX_MCLK, EX_BCLK, EX_LRCLK;
INPUT L_SDATA, MCK, SCK, FSYNC;
INPUT EXT;
INPUT IDPM0_IN, IDPM1_IN;

OUTPUT LRCLK, BCLK, SDATA, MCLK, C_MCLK;
OUTPUT IDPM1, IDPM0;
OUTPUT M2, M1, M0;

IDPM0 = IDPM0_IN;
IDPM1 = IDPM1_IN;

M0 = /IDPM1 * /IDPM0;
M1 = /IDPM1 * IDPM0;
M2 = /IDPM1*/IDPM0 + IDPM1*IDPM0;

LRCLK =  /EXT*EX_LRCLK + EXT*FSYNC;
BCLK  =  /EXT*EX_BCLK  + EXT*(IDPM1*/IDPM0*/SCK
  +SCK*(/IDPM1 + IDPM0));
SDATA =  /EXT*EX_SDATA + EXT*L_SDATA;
MCLK  =  /EXT*EX_MCLK  + EXT*MCK;
C_MCLK = /EXT*EX_MCLK  + EXT*MCK;
```

ATTACHMENTS

The following is included for your convenience.

- Digital receiver, mux and AD1853 DAC schematics are shown in Figure 2.
- DAC output LP filter, power and reset schematics are shown in Figure 3.
- Bill of materials (Table I).
- PCB plots showing: silkscreen layers in Figure 4, top layer in Figure 5, ground planes in Figure 6, power planes in Figure 7, and the bottom layer in Figure 8.

FURTHER INFORMATION

Ordering information: order number is EVAL-AD1853EB.

For application questions, please contact our Central Applications Department at 1-781-937-1428 for assistance.

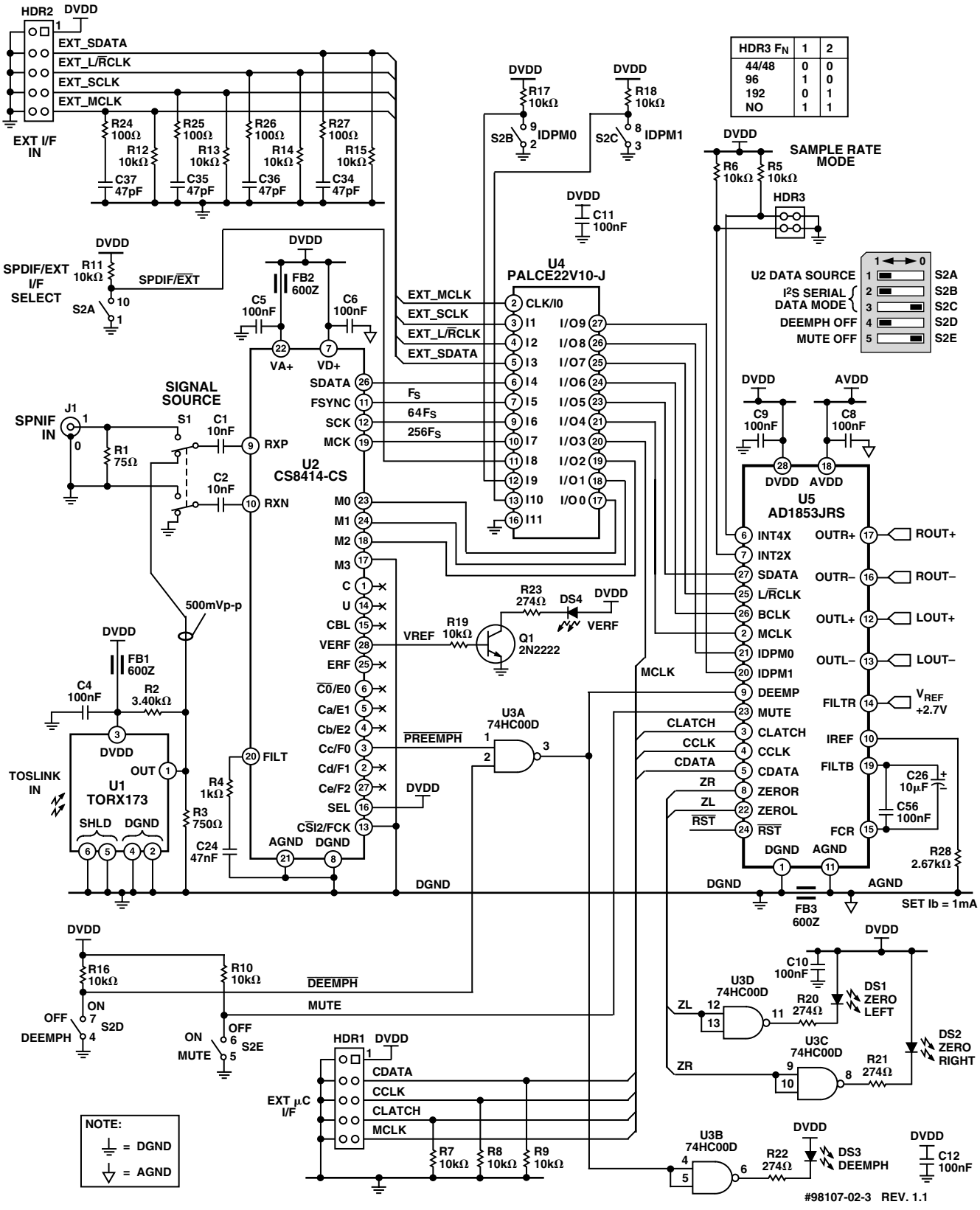

Figure 2. Digital Receiver, MUX and AD1853 DAC

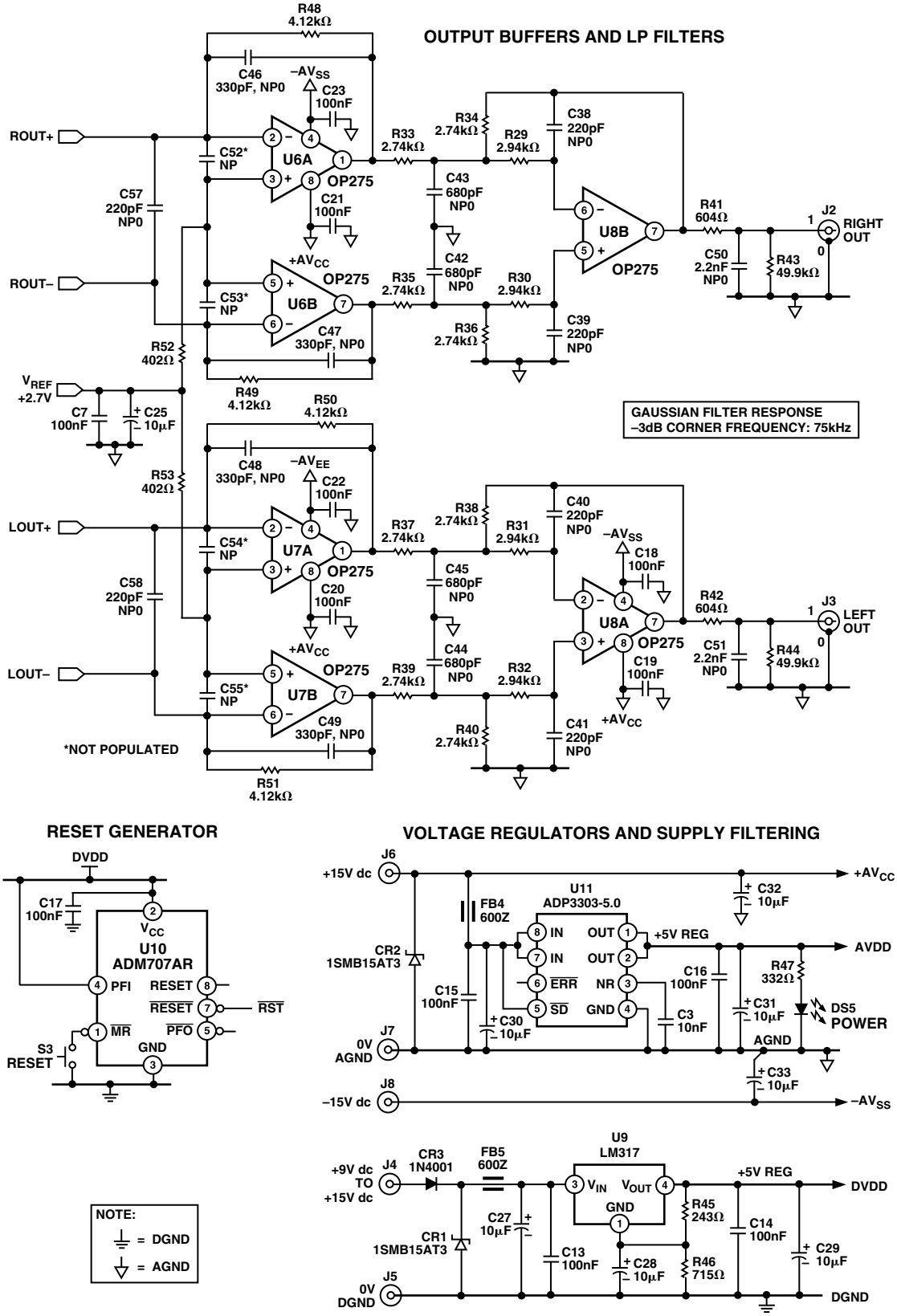

Figure 3. DAC Output Filters, Power and Reset

Table III. EVAL-AD1853EB Bill of Materials

Qty. Used	Part Type	Designator	Footprint	Description
2	10-PIN HEADER	HDR1 HDR2	10-PIN HDR	10-Pin Vertical Thru Hole, Shrouded Header
4	100Ω	R24 R25 R26 R27	SMD 0805	±1%, 100 mW, ±100 ppm/°C MF Chip Resistor
21	100nF	C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C4 C5 C56 C6 C7 C8 C9	SMD 0805	±10%, 50 V dc, X7R Ceramic Chip Capacitor
15	10kΩ	R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R5 R6 R7 R8 R9	SMD 0805	±1%, 100 mW, ±100 ppm/°C MF Chip Resistor
3	10nF	C1 C2 C3	SMD 0805	±10%, 50 V dc, X7R Ceramic Chip Capacitor
9	10µF	C25 C26 C27 C28 C29 C30 C31 C32 C33	SMD 6032, C-CASE	±10%, 16 V dc SMD Tantalum Capacitor
1	1kΩ	R4	SMD 0805	±1%, 100 mW, ±100 ppm/°C MF Chip Resistor
1	1N4001	CR3	SOD80	Power Diode/Rectifier
2	1SMB15AT3	CR1 CR2	SMD 403A	Transient Protection Zener Diode
6	220pF NP0	C38 C39 C40 C41 C57 C58	SMD 0805	±5%, 50 V dc, NP0 Ceramic Chip Capacitor
1	243Ω	R45	SMD 0805	±1%, 100 mW, ±100 ppm/°C MF Chip Resistor
4	274Ω	R20 R21 R22 R23	SMD 0805	±1%, 100 mW, ±100 ppm/°C MF Chip Resistor
2	402Ω	R52 R53	SMD 0805	±1%, 100 mW, ±100 ppm/°C MF Chip Resistor
1	2.67kΩ	R28	SMD 0805	±1%, 100 mW, ±100 ppm/°C MF Chip Resistor
8	2.74kΩ	R33 R34 R35 R36 R37 R38 R39 R40	SMD 0805	±1%, 100 mW, ±100 ppm/°C MF Chip Resistor
4	2.94kΩ	R29 R30 R31 R32	SMD 0805	±1%, 100 mW, ±100 ppm/°C MF Chip Resistor
2	2n2 NP0	C50 C51	SMD 1206	±5%, 50 V dc, NP0 Ceramic Chip Capacitor
1	2N2222	Q1	SOT 23	NPN Bipolar Transistor
4	330pF NP0	C46 C47 C48 C49	SMD 0805	±5%, 50 V dc, NP0 Ceramic Chip Capacitor
1	332Ω	R47	SMD 0805	±1%, 100 mW, ±100 ppm/°C MF Chip Resistor
1	3.40kΩ	R2	SMD 0805	±1%, 100 mW, ±100 ppm/°C MF Chip Resistor
1	47nF	C24	SMD 0805	±10%, 50 V dc, X7R Ceramic Chip Capacitor
4	47pF	C34 C35 C36 C37	SMD 0805	±5%, 50 V dc, NP0 Ceramic Chip Capacitor
2	49.9kΩ	R43 R44	SMD 0805	±1%, 100 mW, ±100 ppm/°C MF Chip Resistor
4	4.12kΩ	R48 R49 R50 R51	SMD 0805	±1%, 100 mW, ±100 ppm/°C MF Chip Resistor
5	600Z	FB1 FB2 FB3 FB4 FB5	SMD 0805	Ferrite Bead, 600 Ohm @ 100 MHz, <2 Ohm dc
2	604Ω	R41 R42	SMD 0805	±1%, 100 mW, ±100 ppm/°C MF Chip Resistor
4	680pF NP0	C42 C43 C44 C45	SMD 0805	±5%, 50 V dc, NP0 Ceramic Chip Capacitor
1	715Ω	R46	SMD 0805	±1%, 100 mW, ±100 ppm/°C MF Chip Resistor
1	74HC00D	U3	14-LEAD SOIC	Quad 2-Input Positive N and Gate
1	75.0Ω	R1	SMD 0805	±1%, 100 mW, ±100 ppm/°C MF Chip Resistor
1	750Ω	R3	SMD 0805	±1%, 100 mW, ±100 ppm/°C MF Chip Resistor
1	AD1853JRS	U5	28-LEAD SSOP	24-Bit, 192 kS/s STEREO DAC
1	ADM707AR	U10	SO-8	200 ms Reset Generator
1	ADP3303-5.0	U11	SO-8	Low Noise, Low Dropout Adjustable Voltage Regulator
1	BINDING POST, BLK	J5	BNDNG PST 1	Screw Terminal/Banana Binding Post
1	BINDING POST, BLU	J8	BNDNG PST 1	Screw Terminal/Banana Binding Post
1	BINDING POST, GRN	J7	BNDNG PST 1	Screw Terminal/Banana Binding Post
1	BINDING POST, ORG	J6	BNDNG PST 1	Screw Terminal/Banana Binding Post
1	BINDING POST, RED	J4	BNDNG PST 1	Screw Terminal/Banana Binding Post
1	CS8414-CS	U2	28-LEAD SOIC	AES/EBU Digital Audio Interface Receiver
1	DPDT SWITCH	S1	EG-2215	PCB Mount DPDT Slide Switch
1	LM317	U9	DPAK	3-Terminal, Adjustable Voltage Regulator
4	NP	C52 C53 C54 C55	SMD 0805	±5%, 50 V dc, NP0 Ceramic Chip Capacitor
3	OP275	U6 U7 U8	8-LEAD SOIC	Dual Bipolar/JFET Lo Noise, Lo Dist, Hi Slew Rate, Audio Op-Amp
1	PALCE22V10-J	U4	28-LEAD PLCC	EE CMOS PLD
3	RCA JACK	J1 J2 J3	CTP-021	Right Angle PCB Mount, RCA JACK
5	RED LED	DS1 DS2 DS3 DS4 DS5	LED 1206	PCB SMD Light Emitting Diode
1	SAMPLE RATE MODE	HDR3	4-PIN Header	4-Pin Vertical Mount PCB Header
1	SW DIP-5	S2	10-PIN DIP	Five Way, SPST, DIP Switch
1	SW-PB	S3	FSM4JSMA	Normally Open, Tactile Push Button
1	TORX173	U1	TORX173	TOSLink Digital Audio Fibre Optic Receiver

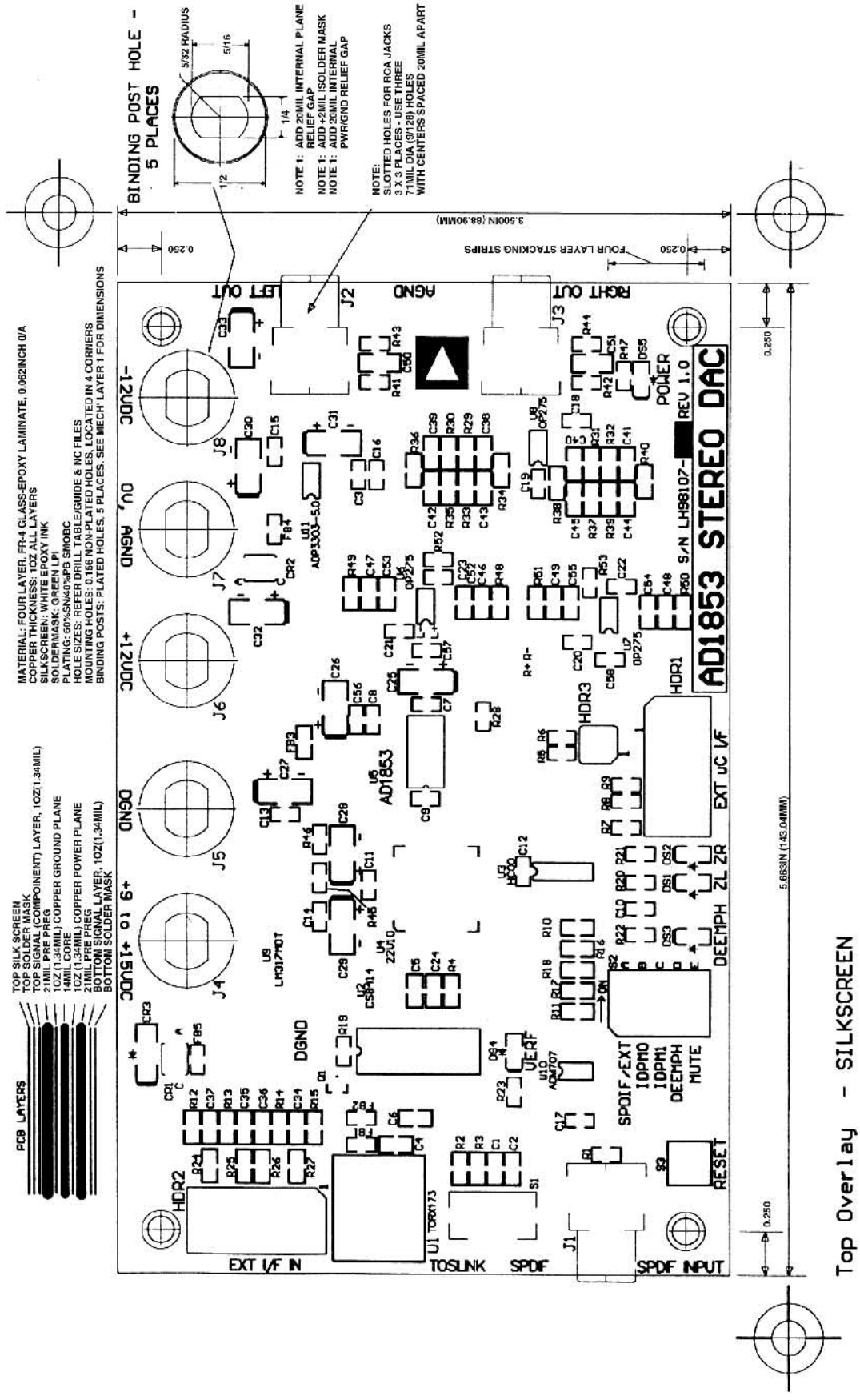

Figure 4. Silkscreen—Top Overlay

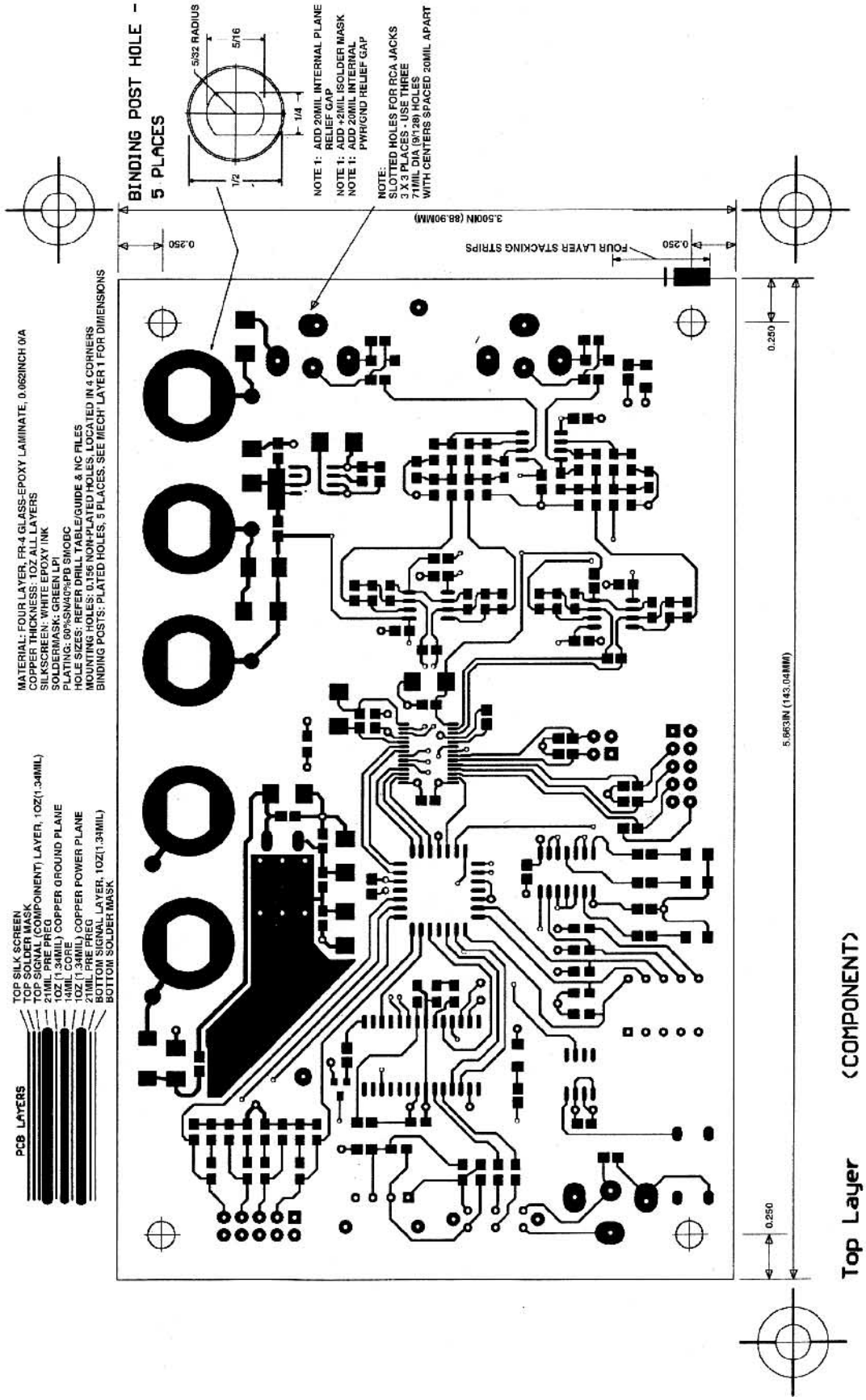

Figure 5. Component—Top Layer

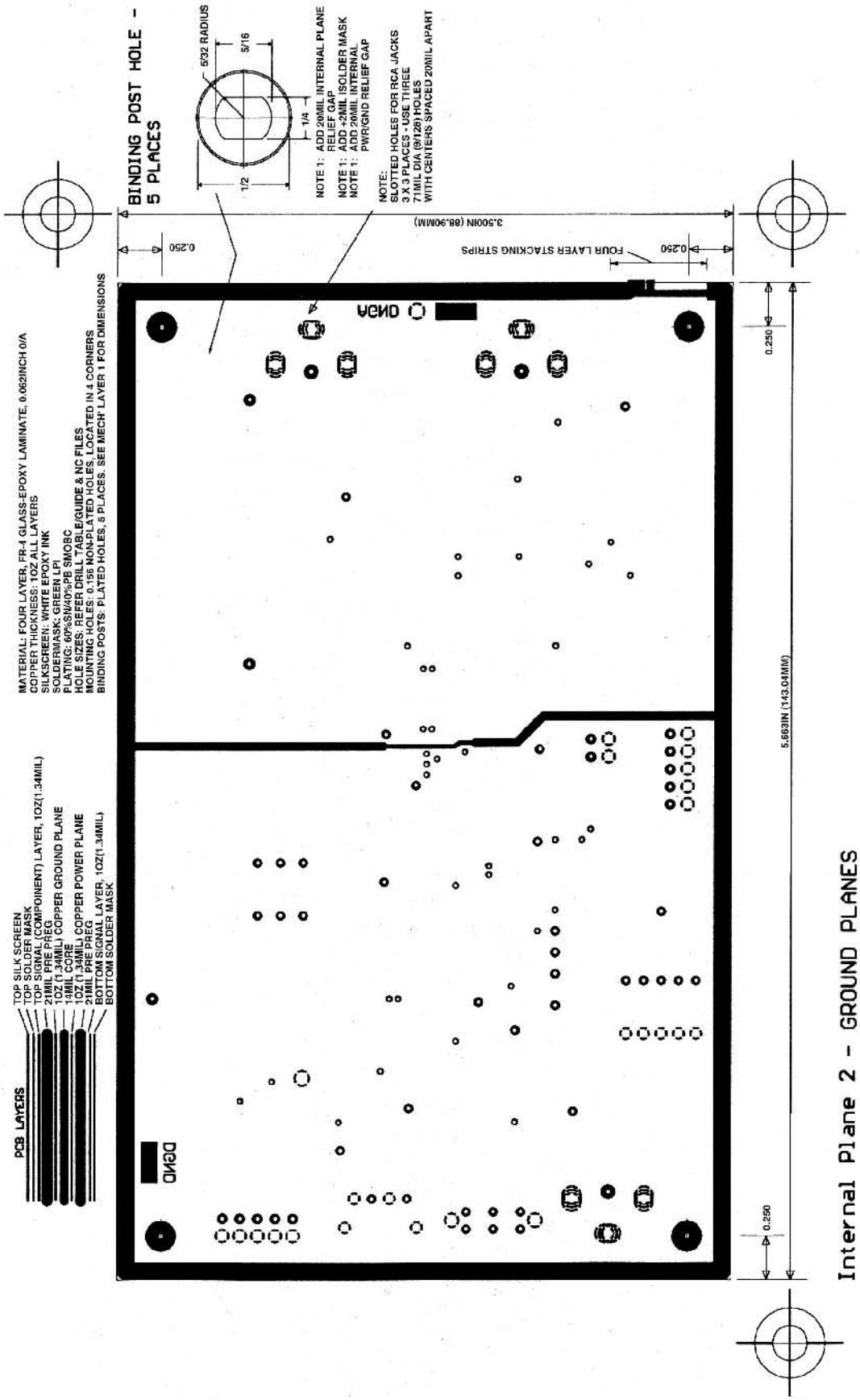

Figure 6. Internal Plane 2—Ground Planes

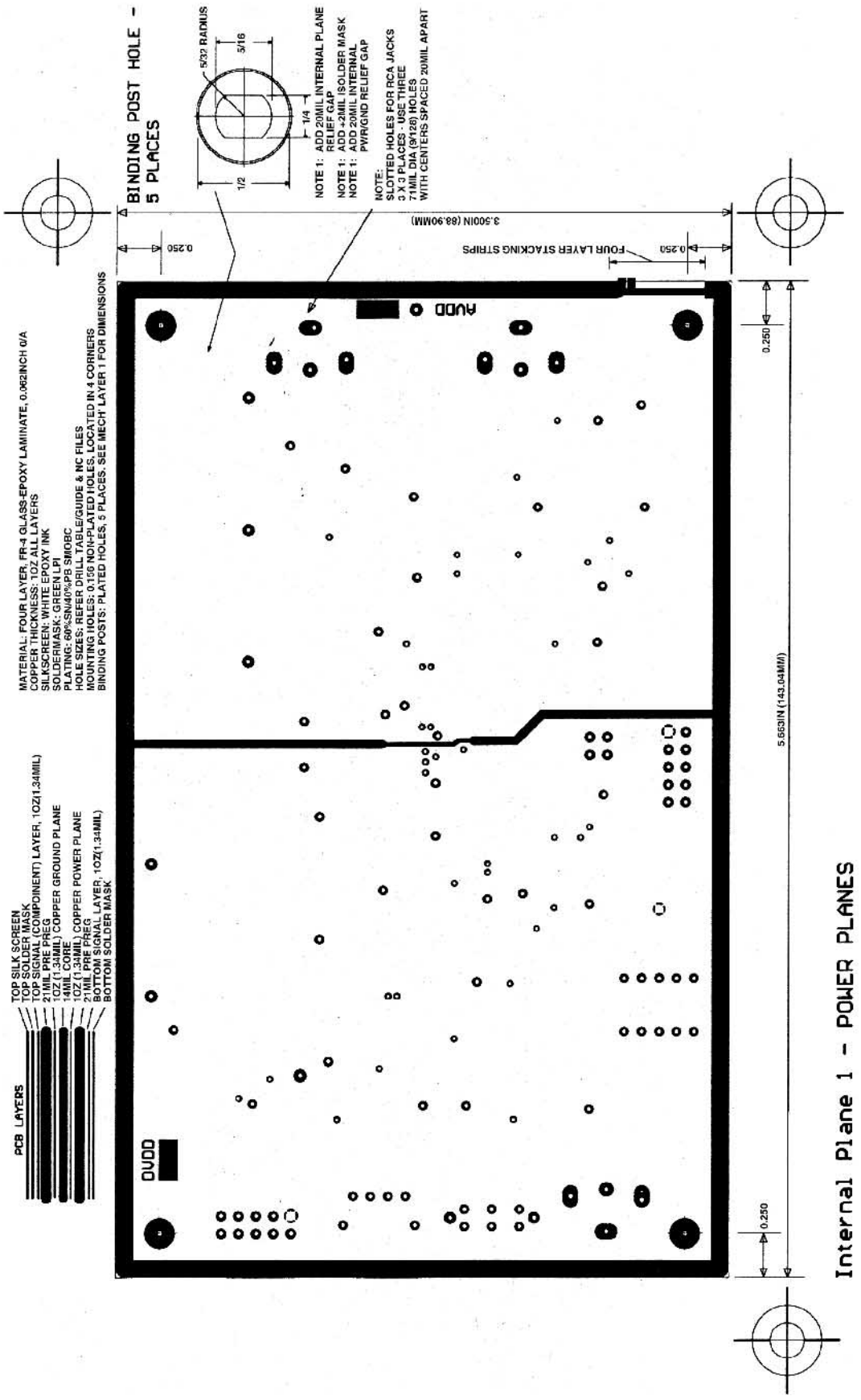

Figure 7. Internal Plane 1—Power Planes

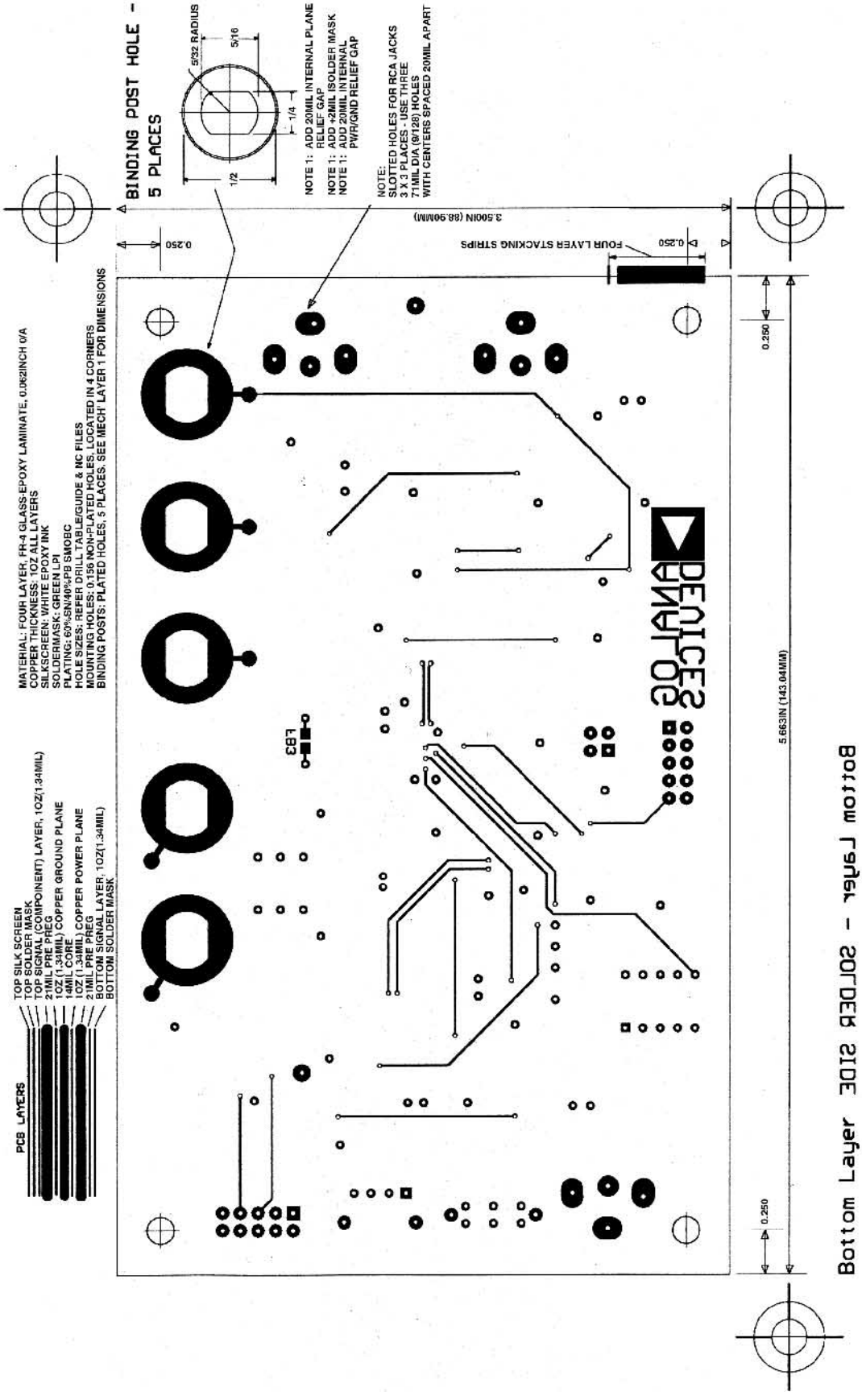

Figure 8. Bottom Layer—Solder Side

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