



ADAU1381, ADAU1382, ADAU1781, ADAU1361,
 ADAU1761, ADAU1442, ADAU1445, ADAU1446

Anomaly Sheet for All Revisions

This anomaly list represents the known bugs, anomalies, and workarounds for the ADAU1381, ADAU1382, ADAU1781, ADAU1361, ADAU1761, ADAU1442, ADAU1445, and ADAU1446 products. The anomalies listed apply to all material branded as follows:

First Line ADAU1381, ADAU1382, ADAU1781,
 ADAU1361, ADAU1761, ADAU1442,
 ADAU1445, or ADAU1446

Analog Devices, Inc. is committed, through future silicon revisions, to continuously improving silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems implementing the recommended workarounds outlined here.

ADAU1381/ADAU1382/ADAU1781/ADAU1361/ADAU1761/ADAU1442/ADAU1445/ADAU1446 SILICON REVISION HISTORY

Silicon Revision Identifier	Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
		All silicon branded ADAU1381BCPZ ADAU1382BCPZ ADAU1781BCPZ ADAU1361BCPZ ADAU1761BCPZ ADAU1442YSVZ-3A ADAU1445YSVZ-3A ADAU1446YSTZ-3A	Release	Rev. 0	1

Rev. 0

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**ADAU1381, ADAU1382, ADAU1781,
ADAU1361, ADAU1761, ADAU1442,
ADAU1445, ADAU1446**

Anomaly Sheet for All Revisions

ANOMALIES

1. De-Jitter Circuits Fail to Output Data [er001]

Background:	The global de-jitter control register allows all de-jitter circuits in the device to be activated or bypassed, and allows the size of the de-jitter window to be set. De-jitter circuits protect against duplicate samples or skipped samples due to jitter from the serial ports in slave mode.
Issue:	Disabling and re-enabling certain subsystems in the device – the ADCs, serial ports, sound engine / DSP core, or DACs – during operation can cause associated de-jitter circuits to fail. As a result, audio data fails to be output to the following subsystem in the device.
Workarounds:	<ol style="list-style-type: none"> 1. When the serial ports are in master mode, the de-jitter circuit can be bypassed by setting the De-Jitter Control Register Address listed in the second column of Table 1 to the Bypass/Reset Setting listed in the fifth column of Table 1. This may be done as the last step in system initialization. This workaround results in no degradation of audio performance. 2. When the serial ports are in slave mode, the de-jitter circuit can be bypassed by setting the De-Jitter Control Register Address listed in the second column of Table 1 to the Bypass/Reset Setting listed in the fifth column of Table 1. This may be done as the last step in system initialization. Because the serial ports are in slave mode and there may be jitter in the incoming clock signal, samples may be duplicated or skipped, depending on the severity of the jitter. This can result in duplicated or skipped samples, which will manifest itself as a slight increase in distortion on the audio output from the device, but will guarantee that the audio output will not fail. 3. When the serial ports are in slave mode, the de-jitter circuit can be re-initialized prior to outputting audio from the device, guaranteeing that audio will be output to the following subsystem in the device. Any time audio needs to pass through the ADCs, serial port, sound engine / DSP core, or DACs, the de-jitter circuit can be bypassed and reset by setting the De-Jitter Control Register Address listed in the second column of Table 1 to the Bypass/Reset Setting listed in the fifth column of Table 1. Then, the de-jitter circuit can be activated once again by setting the De-Jitter Control Register Address listed in the second column of Table 1 to the Default Active Setting listed in the sixth column of Table 1. No wait is required between the two register writes required in this workaround.
Related Issues:	None.

Table 1. De-Jitter Register Address and Settings

Device	De-Jitter Control Register Address (Hex)	De-Jitter Control Register Address (Decimal)	Number of Bytes	Bypass/Reset Setting	Default Active Setting
ADAU1381	0x4032	16434	1	0x00	0x05
ADAU1382	0x4032	16434	1	0x00	0x05
ADAU1781	0x4032	16434	1	0x00	0x05
ADAU1361	0x4036	16430	1	0x00	0x03
ADAU1761	0x4036	16430	1	0x00	0x03
ADAU1442	0xE221	57889	2	0x00, 0x00	0x00, 0x05
ADAU1445	0xE221	57889	2	0x00, 0x00	0x00, 0x05
ADAU1446	0xE221	57889	2	0x00, 0x00	0x00, 0x05

ADAU1381/ADAU1382/ADAU1781/ADAU1361/ADAU1761/ADAU1442/ADAU1445/ADAU1446 SILICON ANOMALIES

Anomaly No.	Description	Status
er001	De-Jitter Circuits Fail to Output Data	Pending

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ADAU1381, ADAU1382, ADAU1781,
ADAU1361, ADAU1761, ADAU1442,
ADAU1445, ADAU1446

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