ADC interface conditions high-level signals

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Designers who build equipment for the industrial market share a widespread problem. At one extreme, they must build equipment that supports ±10V bipolar voltages, often riding on a high common-mode level, a requirement enforced by 30 years of legacy industrial equipment. At the other extreme, the analog signal needs conditioning to match the full-scale range of a low-voltage, single-supply ADC. Designers need to scale and level-shift signal levels throughout their system to accommodate the high voltage levels that sensor manufacturers dictate and the low voltage levels that the ADC dictates. Operating from a single 5V supply, the circuit in this Design Idea provides an interface of large bipolar inputs to a single-supply, low-voltage, differential-input ADC. The circuit in **Figure 1** comprises two difference amplifiers, connected in antiphase. The differential output, V_1-V_2, is an attenuated version of the input signal: $V_1-V_2=(V_A-V_B)/5$.

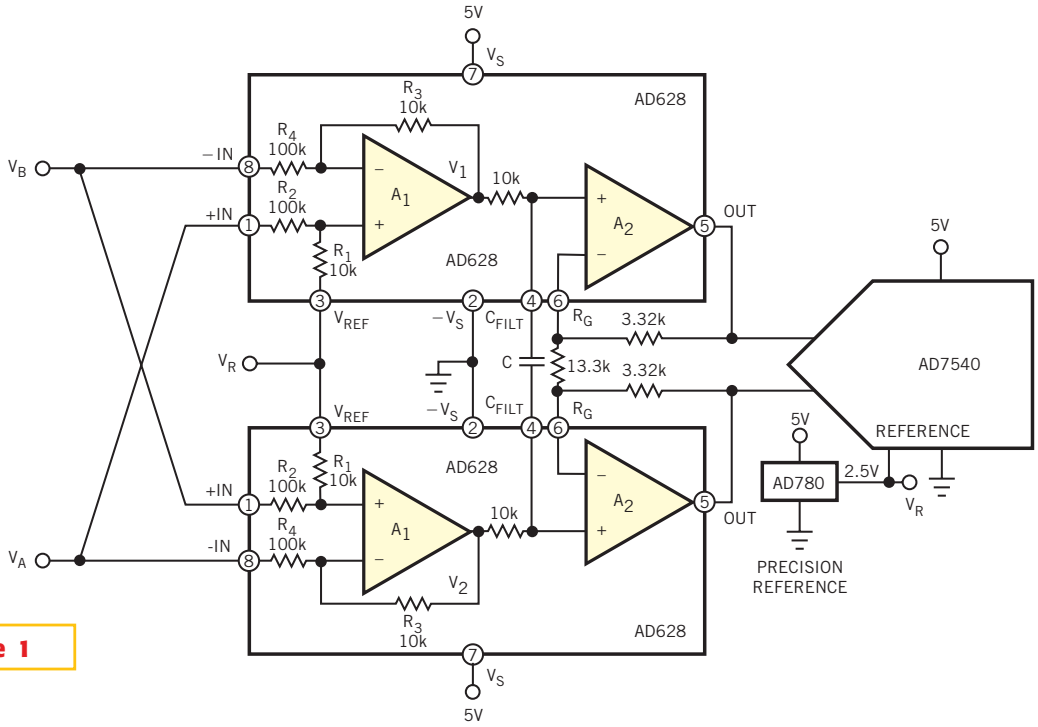

Figure 1 This circuit attenuates and level-shifts a ±10V differential signal while operating from a single 5V supply.

The difference amplifiers reject the common-mode voltage on inputs V_A and V_B. The reference voltage, V_R, which the AD780 develops and the ADC and the amplifier share, sets the output common-mode voltage. A single capacitor, C, placed arcros the C_{FILT} pins, lowpass-filters the difference signal, V_1-V_2. The −3-dB pole frequency is: $f_P=1/(40{,}000\times\pi\times C)$. A_2 amplifies the difference signal by 1.5. Thus, the total gain of this circuit is $^3/_{10}$. **Figure 2** shows a 10V input signal (top), the signals at the output of each AD628 (middle), and the differential output (bottom). The benefits of this configuration go beyond simply interfacing with the ADC. The circuit improves specifications such as common-mode-rejection ratio, offset voltage, drift, and noise by a factor of $\sqrt{2}$ because the errors of each AD628 are not correlated.

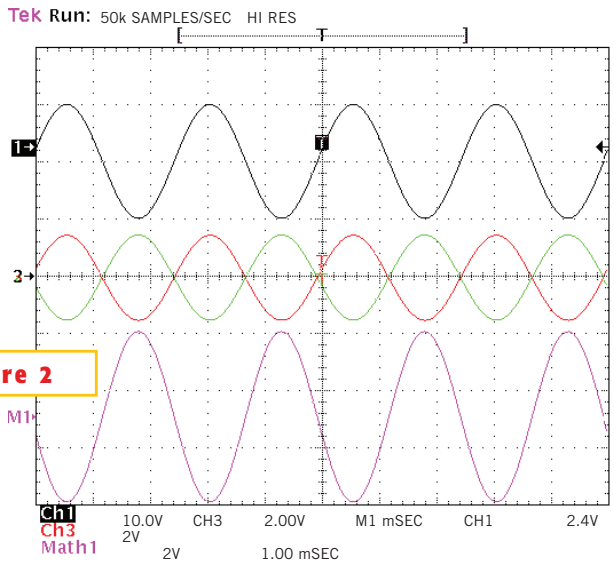

Figure 2 The waveforms show a 10V input signal (top), the signals at the output of each AD628 (middle), and the differential output (bottom).

The output demonstrates 85-dB SNR (**Figure 3**). The two AD628s interface with an AD7450 12-bit, differential-input ADC. The AD7450 easily rejects residual common-mode signals at the output of the difference amplifiers. **Figure 4** shows the common-mode error at the output of the AD628.

The topmost waveform is a 10V, common-mode input signal. The middle waveform, measuring 150 µV, is the common-mode error measured, differentially, from the output of the two AD628s. The bottom waveform, measuring 80 µV, is the resultant common-mode error.□

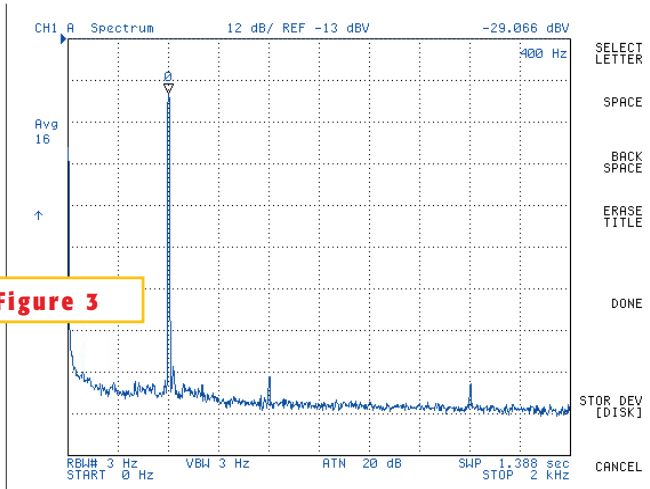

Figure 3

The circuit in Figure 1 has an 85-dBV SNR.

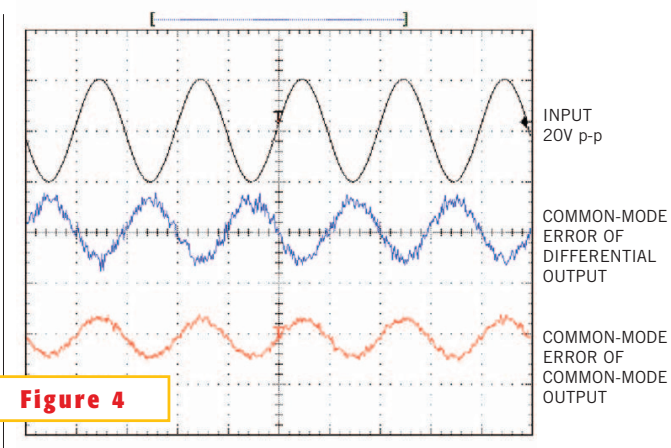

Figure 4

The common mode input (top) measures 20V p-p. The common-mode error of the differential output (middle) is 200 µV p-p. The error of the common-mode output (bottom) is 80 µV p-p.

Two op amps provide averaged absolute value

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THE CIRCUIT in **Figure 1** is useful when you need amplitude demodulation or an averaged absolute-value conversion. The circuit comprises two stages, the first of which, IC_{1A}, is a differential-output absolute-value converter. The second stage, IC_{1B}, is a traditional differential amplifier. The combination of the two stages performs single-ended absolute-value conversion but only if $R_3 >> R_2$. The C_1 capacitors integrate the current flow and yield averaged voltages V_A and V_B. In addition, the capacitors ensure low ac-impedance points at nodes V_A and V_B when the output diodes are reverse-biased. The additional C_2 capacitors in parallel with R_4 resistors impart a second-order-lowpass-filter characteristic to the circuit and remove the remaining ac signal. From a practical point of view, you can choose R_3 to be five to 10 times higher than R_2. The gain of the circuit is $(R_2||R_3/R_1)(R_4/R_3)$. In most applications, you would choose the filter time constants $\tau_1 = R_2||R_3C_1$ and $\tau_2 = R_4C_2$ to be equal. The circuit in **Figure 1** is simple, symmetrical, and cost-effective. It also makes it easy to calculate and adjust the gain using one resistor, R_1. Other advantages are that the circuit has equal delay for positive- and negative-going signals and that it doesn't need matched diodes.□

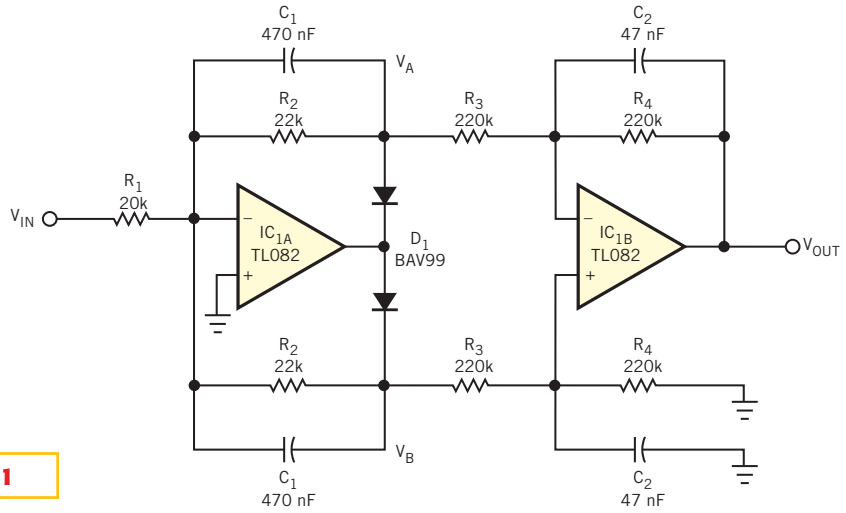

Figure 1

This single-ended, averaged absolute-value converter is useful for amplitude demodulation.