JESD204B High-Speed ADC-to-FPGA and FPGA-to-DAC Connectivity

AD9250 Dual 14-bit, 250-Mspl ADC
Seminar Overview

- Background and discussion of JESD204 standard development and revision notes
- AD9250 Key specifications (JESD204B SC1 ADC)
- Demo with Analog Devices AD9250 + Xilinx Kintex-7 KC705
- ADI’s product offerings with JESD204
- Discussion of practical layout considerations for high speed ADC interfaces
Why the need for a high-speed converter-to-FPGA serial interface?

- **Simplification** of overall system design
  - Smaller/lower number of trace routes, easier to route board designs

- **Reduction** in pin count – Both the Tx and Rx side
  - Move from *high pin count low speed* parallel interfaces to *low pin count high speed* serial interfaces
  - *Embedded clock* incorporated to even further reduce pin count

- Reduction in system **costs**
  - Smaller IC packages and board designs lead to lower cost

- Easily **scalable** to meet future bandwidth requirements
  - As geometries shrink and speed increases, the standard adapts
What is JESD204?

◆ “SERDES” is often used instead of JESD204. SERDES is simply a generic name for any serial interface.

◆ JESD204 is a high speed, point to point, serial interface used to interconnect 2 (or more) devices.
  ● ADC to digital receiver
  ● Digital source to DAC
  ● ADC and DAC to Digital engine
  ● Digital source to digital receiver

◆ How is it different than previous data converter interfaces?
  ● A single primary interface can be used to pass all data, clocking and framing information.
    ◆ The clock and frame information are embedded in the data stream.
    ◆ No need to worry about set up and hold time between data and clock.
    ◆ One PCB trace (differential) can route all bits.
What is the JEDEC Standard 204 (JESD204)

- **JESD204** is a standard defining a multi-gigabit serial data link between converters and a receiver (commonly FPGA or ASIC)

- **JESD204 (April 2006)** – original standard defining 1 lane, 1 link
  - Defined transmission of samples across a *single* serial lane for *multiple* converters at speeds up to **3.125 Gbps**

![Diagram of JESD204](image-url)
What is the JEDEC Standard 204 (JESD204A)

- JESD204A (April 2008) – 1st revision expanding standard to multiple links and multiple lanes
  - Revision adds capability for \textit{multiple} aligned serial lanes for \textit{multiple} converters at speeds up to 3.125 Gbps
What is the JEDEC Standard 204 (JESD204B)

- JESD204B (August 2011) – 2nd revision utilizes a device clock and adds measures to ensure deterministic latency
  - Supports *multiple* aligned serial lanes for *multiple* converters at speeds up to 12.5 Gbps
JESD204 Simplified System View

Simplified View of Data Flow in a JESD204 System
Key Aspects of JESD204x Standards

- **8b/10b Embedded Clock**
  - DC balanced encoding which guarantees significant transition frequency for use with Clock and Data Recovery (CDR) designs
  - Encoding allows both data and control characters - Control characters can be used to specify link alignment, maintenance, monitoring, etc.
  - Detection of single bit error events on the link

- **Serial Lane Alignment**
  - Using special training patterns with control characters, lanes can be aligned across a “link”
  - Trace to trace tolerance may be relaxed relative to synchronous sampling parallel LVDS designs

- **Serial Lane Maintenance/Monitoring**
  - Alignment maintained through super-frame structure and use of specific “characters” to guarantee alignment.
  - Link quality monitored at receiver on lane by lane basis.
  - Link established and dropped by receiver based on error thresholds.
Deterministic Latency in JESD204x

- Latency can be defined as deterministic when the time from the input of the JESD204x transmitter to the output of the JESD204x receiver is consistently the same number of clock cycles.
- In parallel implementations, deterministic latency is rather simple – clocks are carried with the data.
- In serial implementations, multiple clock domains exist which can cause non-determinism.
- JESD204 and JESD204A do not contain provisions for guaranteeing deterministic latency.
- JESD204B looks to address this issue by specifying three device sub-classes:
  - Device Sub-class 0 – No support for deterministic latency
  - Device Sub-class 1 – Deterministic latency using SYSREF (above 500 MSPS)
  - Device Sub-class 2 – Deterministic latency using SYNC~ (up to 500 MSPS)
Key Signals in JESD204A Systems

- **frame clock**
  - A clock signal in the system equal to the frame rate of the data on the link. This is the master timing reference

- **SYNC~**
  - A system synchronous, active low signal from the receiver to the transmitter which denotes the state of synchronization
    - Synchronous to the frame clock in JESD204A
    - When SYNC~ is low, the receiver and transmitter are synchronizing
    - SYNC~ and frame clock should have similar compliance in order to ensure proper capture/transmission timing (i.e. LVDS, CMOS, CML)
    - SYNC~ signals may be combined if multiple DACs/ADCs are involved

- **Lane 0, … ,L-1**
  - Differential lanes on the link. (Typically high speed CML)
    - 8B/10B code groups are transmitted MSB first/LSB last
Key Signals in JESD204B Systems

- **Device clock**
  - A clock signal in the system which is a harmonic of the frame rate of the data on the link. In JESD204B systems the frame clock is no longer the master system reference.

- **SYNC~**
  - Same as JESD204A except synchronous to Local Multi-Frame Clock (LMFC) instead of the frame clock.

- **Lane 0, … ,L-1**
  - Same as JESD204A

- **SYSREF (optional)**
  - An optional source-synchronous, high slew rate timing resolution signal responsible for resetting device clock dividers (including LMFC) to ensure deterministic latency.
    - One-shot, “gapped periodic” or periodic
    - Distributed to both ADCs/DACs and ASIC/FPGA logic devices in the system.
    - When available, SYSREF is the master timing reference in JESD204B systems since it is responsible for resetting the LMFC references.
Example: JESD204B in Ultrasound

- High-end Ultrasound System
  - ADC Fs = 40Msps
  - Data resolution = 14bits
  - System channels = 192
  - 24 Octal AFES
  - Total data to beam-former = 14bits*40Msps*192ch = 108Gbps

LVDS Implementation
10 LVDS pairs per octal AFE
Total 240 LVDS pairs

JESD204B Implementation
2 CML pairs per octal AFE
Total 48 CML pairs
80% Reduction!
Typical Data Rates and Cable Drive Strength

- CML drivers offer the advantage of increased speed over LVDS drivers.
- Increased speed can take advantage of smaller PCB design and migration of the FPGA/ASIC to the ADCs/DACs that is typical in most designs.
**LVDS vs. CML**

<table>
<thead>
<tr>
<th>Industry Standard</th>
<th>Maximum Data Rate</th>
<th>Output Swing ((V_{OD}))</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVDS</td>
<td>TIA/EIA-644</td>
<td>3.125 Gbps</td>
<td>±350 mV</td>
</tr>
<tr>
<td>LVPECL</td>
<td>N/A</td>
<td>10+ Gbps</td>
<td>±800 mV</td>
</tr>
<tr>
<td>CML</td>
<td>N/A</td>
<td>10+ Gbps</td>
<td>±800 mV</td>
</tr>
<tr>
<td>M-LVDS</td>
<td>TIA/EIA-899</td>
<td>250 Mbps</td>
<td>±550 mV</td>
</tr>
<tr>
<td>B-LVDS</td>
<td>N/A</td>
<td>800 Mbps</td>
<td>±550 mV</td>
</tr>
</tbody>
</table>

- The increased speed of the CML driver leads to a reduction in the number of drivers by enabling more channels per lane.
- With JESD204 providing an up to 80% lane reduction, the power increase of JESD204 CML is comparable to an LVDS implementation.
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The World Leader in High Performance Signal Processing Solutions

JESD204B-Compatible Dual 14-Bit/250 MSPS A/D Converter

- Subclass 1 Deterministic Latency
- 711 mW Total Power Dissipation
- SFDR: 88 dBc @ 185 MHz A_IN

ANALOG DEVICES
Innovative JESD204B Subclass 1 ADC
High performance, high speed ADC supports JESD204B-SC1

Supports Growing Trends in Multiple markets

- **Wireless Infrastructure**
  - Simplified board design, fewer traces to digital ASIC

- **CMTS & Cable Access**
  - More compact layout to SOC chip

- **Electronic Test & Measurement**
  - JESD204B simplifies FPGA interfacing

- **Medical Imaging systems**
  - Reduced data I/O to FPGAs & data processors

- **High End Imaging (Industrial and Military/Aerospace)**
  - Fewer high speed data traces enables more ADC channels per system
AD9250-250 typical performance characteristics

- **f_{IN}:** 90.1MHz
  - **f_{S}:** 250MSPS
  - **SNR:** 71.8dBFS
  - **SFDR:** 85dBc

- **f_{IN}:** 185.1MHz
  - **f_{S}:** 250MSPS
  - **SNR:** 70.7dBFS
  - **SFDR:** 85dBc

- **f_{S}:** 250MSPS
  - 184.12MHz AT –7dBFS
  - 187.12MHz AT –7dBFS
  - **SFDR:** 84dBc
AD9250: 14-Bit 250-Msps 1.8V Dual ADC with JESD204B outputs

**Key Benefits**

- JESD204 Subclass 1 Device (deterministic latency through use of SYSREF)
- 70.6dBfs SNR at 185MHz Ain
- 88dBc SFDR at 185MHz Ain (@-1dBFs)
- +/-0.25 LSB DNL, +/-1.5 LSB INL
- Flexible Input range: 1.4Vp-p to 2Vp-p
- IF analog Input bandwidth up to 400 MHz
- +1.8V analog supply
- **711mW** total power at 250Msps (both channels)
- On chip internal voltage reference
- JESD204B outputs modes
  - (L=2, S=1, F=2, M=2) – 1 data lane per ADC up to 250Msps resulting in 5Gbps data rate
  - (L=1, S=1, F=4, M=2) – shared data lane up to 125Msps resulting in 5Gbps data rate
- Serial port control
  - Data out timing adjust
  - Clock duty cycle stabilizer
  - Integer clock divide by 1 to 8

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**Temp**

-40°C – +85°C

**Package**

48Pin LF-CSP 7x7 Pb-Free

**Sampling**

Now

**Production Qtys**

Now
AD9250 JESD204B output modes

- L=2, S=1, F=2, M=2
  - 1 data lane per ADC up to 250Msps resulting in 5Gbps data rate

- L=1, S=1, F=4, M=2
  - shared data lane up to 125Msps resulting in 5Gbps data rate

- Link Parameters
  - L – Number of lanes per converter device
  - S – Number of transmitted samples per converter per frame
  - F – Number of octets per frame
  - M – Number of converters per converter device

- Needs to be programmed into AD9250 core, as well as Xilinx IP
## AD9250 Register Map

<table>
<thead>
<tr>
<th>Address</th>
<th>Description</th>
<th>Value Example</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x6F</td>
<td>JESD204B number of octets per frame (F); calculated value</td>
<td></td>
<td>Read Only</td>
</tr>
<tr>
<td>0x70</td>
<td>JESD204B number of frames per multiframe (K); set value of K per JESD204B specifications, but also must be a multiple of 4 octets</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x71</td>
<td>JESD204B number of converters (M);</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = 1 converter;</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = 2 converters</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x72</td>
<td>Number of control bits (CS); CS/N</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>00 = no control bits (CS = 0);</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>01 = 1 control bit (CS = 1);</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10 = 2 control bits (CS = 2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x73</td>
<td>JESD204B subclass;</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0x0 = Subclass 0;</td>
<td>0x16</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0x1 = Subclass 1 (default)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x74</td>
<td>JESD204B samples per converter frame cycle (S);</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>reserved; set to 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x75</td>
<td>JESD204B control words per frame clock cycle per link (CF);</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>read only</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **All programmable, All flexible**
  - All easy to make not work
  - To alleviate, ADI provides easy to use/integrate HDL and software reference design

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AD9250 Register Map
Pricing / Availability / Design Support

- **AD9250-170/250**
  - Production Samples: Now
  - Production Quantities: Now
  - Behavior Model (ADIsimADC, IBIS): Now
  - Unit Price; 1K quantities (-250 / -170): $131.57/$72.49

- Evaluation Platforms:
  - AD9250-250EBZ: Now / $350
  - AD9250-170EBZ: Now / $350
  - Requires either:
    - HSC-ADC-EVALDZ data capture board: Now / $750
    - CVT-ADC-FMC-INTPZB FMC interposer: Now / $99
  - AD9250-FMC-250EBZ: End Nov 2012 / $550
Design and Evaluation Tools

◆ Complete Evaluation Platforms
  ● ADC Evaluation boards offer proven clocking and ADC driver signal paths

◆ ADC Behavior Models
  ● ADIsimADC
  ● IBIS

◆ Web-Based Design Wizards
  ● PLL (ADIsimPLL)
  ● Filter
  ● Op amp
  ● Clocking solutions (ADIsimCLK)

◆ Converter ‘Centric’ Application Notes
  ● Clocking, input networks, jitter effects, testing methodologies
Evaluation Platform for Dual ADC family

AD9250-250EBZ ($350)
AD9250-170EBZ ($350)

HSC-ADC-EVALDZ ($750)
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Rapid Prototyping AD9250 EVB-to-FPGA platform connection

CVT-ADC-FMC-INTPZB ($99)
Kintex-7 + Interposer + AD9250 Eval Card

- Xilinx KC705
Kintex-7 + AD9250-FMC-250EBZ

- Xilinx KC705 + AD9250-FMC-250EBZ
  - 2 x Dual 14-bit, 250 MSPS ADC (AD9250)
  - Clock Tree (AD9517)
  - 4 channels total
  - Bonding between ADCs
  - Requires HPC-FMC (4 lanes of GTX) for full performance
  - Can work on LPC (1 lane) with reduced sample rate, and 1 x AD9250
HDL Blocks

- Microblaze + Linux
- Linux Device Drivers for:
  - AD9250
  - AD9250 HDL Core
- Streams Data over Ethernet
Data to ChipScope Pro

- Part of Xilinx toolsuite.

- ChipScope™ Pro tool allows you to view any internal signal or node. Signals are captured in the system at the speed of operation. Captured signals are then displayed and analyzed using the ChipScope Pro Analyzer tool.
Data to VisualAnalog

- VisualAnalog™ is a software package that combines a powerful set of simulation, product evaluation and data analysis tools with a user-friendly graphical interface.

Figure 1. Typical VisualAnalog Canvas
Wiki project
Demo

Kintex-7 KC705 + CVT-ADC-FMC-INTPZB + AD9250-EVB250

OR

Kintex-7 KC705 + AD9250-FMC-250EBZ
What we saw....

- **JESD204B** between FPGA and single AD9250
JESD204 Terminology

- **octet** – a group of 8 bits, serving as input to 8B/10B encoder and output from the decoder
- **nibble** – a set of 4 bits which is the base working unit of JESD204x specifications
- **character** – a 10 bit symbol generated by the 8B/10B encoding scheme
- **character clock** – a clock running at the character rate used to process the characters of a system
- **code group** – a set of 10 bits in the serial data stream used to convey octets
- **Running disparity** – the measure of current DC imbalance on the link used to code and decode 8B/10B code groups
- **Frame** – a set of consecutive octets in which the position of each octet can be identified by reference to a frame alignment signal
JESD204 Terminology

- **frame clock** – a system clock which runs at the frames rate. In JESD204A systems, the frame clock is the absolute timing reference in the system.

- **multi-frame** – a set of consecutive frames in which the positions of the frames can be identified relative to a multi-frame alignment character.

- **Multi-frame clock or Local Multi-Frame Clock (LMFC)** – a clock in the system which runs at the multi-frame rate and determines the location of multi-frame characters which are used for lane alignment. Typically this clock is a divided version of the frame clock which is local to the transmitter/receiver. In the coming JESD204B systems, it is expected that this clock will be the absolute timing reference.
What we saw... (HDL)

- 64bits @ 200MHz
- Lane 0, 1 (5GHz)
- SYNC~ (125MHz)
- SYSREF (125MHz)
- Reference clock (250MHz) is sample clock
- Sample clock (250MHz)
- 64bits (2 lanes x 32-bits) @ 125MHz (1/2 sample rate)
- 32bits @ 250MHz (sample rate)
What we saw... (Software)

- **Linux operating system running on the Microblaze**
  - IIO driver for the AD9250
    - Industrial Input/Output (IIO) framework
    - The Industrial I/O subsystem is intended to provide support for devices that in some sense are analog to digital or digital to analog convertors (ADCs, DACs).
  - **lio-cmdsrv**
    - Configure device parameters via network
    - Stream data via UDP over the network

- **Visual Analog**
  - Connecting to the iio-cmdsrv over ethernet
  - Data analysis pipeline
    - FFT + performance analysis
System Clocks

- The system needs only one clock (this is the sample clock).
- At the maximum; this is 250MHz, line rate is 5Gbps.
- The GTX uses the same clock as the reference clock.
- The JESD core is 32bits per lane (125MHz).
- The AD9250 core runs at the sampling clock 250MHz. This allows post capture digital processing to be done at the sample clock.
- The system is therefore tunable/scalable to any sampling rate- simply by changing a single clock.
Clock Frequency Relationships JESD204

Once link parameters are set, certain frequency relationships need to be determined

- **Line Rate (Bit Rate)** – effective data rate of the serial link
  - Calculated from step 5

- **Character Clock**
  - Calculated from: Line Rate / 10

- **Frame Clock**
  - Calculated from steps 3 and 4

- **Multi-Frame Clock (MFC)**
  - Calculated from: Frame Clock / K
    - Where K is an integer number of frames and must be chosen such that the number of octets in a multi-frame not fall below 17
Setting up JESD204 Link Parameters

1) How many converters do you have in the device ($M$)?
2) What is the converter sample resolution in the device ($N$)?
   i.e. a 12-bit converter would set $N = 12$
3) What is the JESD204x word size ($N'$)?
   • The converter sample resolution is broken down into nibbles. 12 bit converters have 3 nibbles while 14 and 16 bit converters have 4 nibbles. Multiply the number of nibbles by 4 to determine the value of $N'$. It can be advantageous to have $N' = 16$ so that 8-16 bit converters can be handled with the same transmitter/receiver.
   • A non-complete nibble is padded with either Control Bits ($CS$) or Tail bits ($T$) and must satisfy: $N' = N + CS + T$
   • A 12-bit converter with a 16-bit JESD204x word size leaves 4 bits for either control bits and/or tail bits
Setting up JESD204 Link Parameters

4) How many samples easily fit into a frame (S)?
   • Determined by the frame rate and the transmitter/receiver internal characteristics. For low speed simple ADCs, often S is set to 1. For high speed, complex ADCs, the value of S should be based on:
     • the JESD204x data rate = (M x ADC sample rate) / (ADC decimation factor)
     • the desired frame clock rate
   • The value of S is determined by:
     • S = (JESD204x data rate) / Frame Clock Rate (FC)
   • Example 1: Simple ADC (no decimation) with sample rate = 156.25 MHz (JESD204x data rate = 156.25 MHz), the desired frame clock rate = 156.25 MHz then S = 1
   • Example 2: Two ADCs (with decimation = 2) with sample rate = 625 MHz, the desired frame rate = 156.25 MHz then S = (2 x 625 MHz) / 2 / 156.25 MHz = 4
Setting up JESD204 Link Parameters

5) How many lanes are needed (L)?
   • Determined by the maximum required line rate per lane. The line rate per lane can be calculated by the following equation (where FC = frame clock rate):
     • Lane Line Rate = \( \frac{M \times S \times N' \times 10/8 \times FC}{L} \)
   • Example 1: A single 14-bit ADC with 1 sample @ 312.5 MHz \((M = 1, S = 1, N' = 16, \text{and } FC = 312.5 \text{ MHz})\)
     • With \( L = 1 \), the lane line rate = 6250 Mbps
     • With \( L = 2 \), the lane line rate = 3125 Mbps
   • Example 2: Two 12-bit ADCs with 2 samples per frame clock (I/Q) @ 625 MHz \((M = 2, S = 2, \text{and } fs = 625 \text{ MHz})\)
     With \( N = 12, L = 4 \), the lane line rate = 9375 Mbps
     With \( N = 16, L = 4 \), the lane line rate = 12500 Mbps
     With \( N = 12, L = 8 \), the lane line rate = 4687.5 Mbps
     With \( N = 16, L = 8 \), the lane line rate = 6250 Mbps
Setting up JESD204 Link Parameters

6) How many octets are transmitted per Frame (F)?
   • This is calculated by the following equation:
     \[ F = \frac{M \times S \times N'}{8 \times L} \]
   • Example: A single 14-bit ADC with 1 sample on one lane (M = 1, S = 1, N' = 16, and fs = 312.5 MHz)
     \[ F = \frac{1 \times 1 \times 16}{8 \times 1} = 2 \]

7) Is High Density mode being used (HD)?
   • If samples are ever split between lanes, then HD = 1
AD9250 Link parameters

- Allows programmable CML levels (320mV, 400mV, 440mV and 500mV)
- Option to change the polarity of data
- Option to change transmission order of 8B/10B
- Option to change SYNC active low or high.
- Programmable delay for deterministic latency relative to SYSREF
AD9250 – debug facilities

- Lane end to end checking via PRBS sequences at SERDES.
- Lane swapping (the two lanes are interchangeable across the two ADC channels)
- Lane merging (it is possible to use a single lane at reduced sample rate)
- Trail bits can be programmed as PRBS sequence or status bits indicating over-range, under-range or valid data conditions
- Option to disable/enable scrambling
- Option to disable/enable character replacement
- Read back the configuration parameters
- Samples checking via PRBS sequences at ADC
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Analog Devices JESD204 Product Offerings

- AD9639 Quad 12-bit 170/210 MSPS ADC offering JESD204
  - SNR = 65 dBFS, SFDR = 77 dBc
- AD9644 Dual 14-bit 80 MSPS ADC offering JESD204A
  - SNR = 73.7 dBFS, SFDR = 92 dBc
- AD9641 Single 14-bit 80 MSPS ADC offering JESD204A
  - SNR = 73.7 dBFS, SFDR = 94 dBc
- AD9250 Dual 14-bit 250 MSPS ADC offering JESD204B
  - SNR = 70.6 dBfs, SFDR = 88 dBc
- AD9671 Octal Ultrasound AFE, offering JESD204B
  - 8 channels of LNA, VGA, AAF, ADC, and digital demodulator / decimator, SNR = 75 dBfs
Boards and Kits

♦ New FMC Modules supporting JESD204B
  ● Analog Devices AD9250-FMC-250EBZ ($550)
    ♦ 2 x Dual 14-bit 250Msps ADC (AD9250)
    ♦ www.em.avnet.com/ad9250fmc
  ● 4DSP AES-FMC-4DSP176-G ($2,995)
    ♦ 2 x Dual 14-bit 250Msps ADC (AD9250)
    ♦ 2 x 14-bit 5.6Gsps DAC (AD9129)
    ♦ www.em.avnet.com/4dsp176
  ● 4DSP also has a non-JESD204B DAC only FMC module that can be used as an analog signal generator
    ♦ 2 x 14-bit 5.6Gsps DAC (AD9129)
    ♦ 4DSP AES-FMC-4DSP230-G ($2,495)
    ♦ www.em.avnet.com/4dsp230
  ● ADI also provides an FMC interposer board
    ♦ Analog Devices CVT-ADC-FMC-INTPZB ($99)
    ♦ Connects AD9250-EVB250 ($350) to Xilinx/Avnet FMC-enable baseboards

* FMC modules will be shipping in late November
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Application Issues Overview (JESD204)

- Good layout practices are critical for optimal link performance.
- When signal rise/fall times become short compared to length of transmission lines, overshoot, reflections, and cross talk will begin to occur.
- Various sources of signal skew can become issue.
- Return currents and paths become very important at high speeds.
- Differential traces need to have the same impedance and approximately the same length (within reason!).
- Differential traces must be properly terminated to avoid signal reflections which may lead to signal degradation.
- Broadside vs coplanar differential traces.
- Tightly coupled vs loosely coupled differential traces.
Rise/Fall Times vs Transmission Line Length

- With the speed of data transfer rising, the corresponding rise/fall times increase also.
- As shown in the table on slide 21, the rise/fall times specified in OIF-SxI5-01.0 and CEI-6G-SR have mins of 50 ps and 30 ps.
- An importance factor comes into play with times that are this low.
  - Transition Electrical Length (TEL) = (Rise/Fall Time) x Velocity Factor
- As an example, let’s look at a signal with a rise/fall time of 50 ps traveling on standard FR-4 6000 material (Velocity Factor = 5.8 in/nsec)
  - TEL = 0.05 nsec x 5.8 in/nsec = 290 mils
- At only ¼ of this length overshoot, reflections, and cross talk may be come an issue.
  - This means that these could occur at just 72.5 mils!!
Skew Sources

- Several possible causes of skew can arise
- Skew within the ADC device (between transmitters) and within the logic device (between receivers) – intra-device skew
- Skew between two ADC devices – inter-device skew
- Skew within and between links – interconnect skew
- SYNC~ and Frame Clock distribution skew
- Care must be taken in the layout to minimize additional skew
Return Currents and Paths

- In high speed circuits, it is important to know the current return path
- Common misconception: Return current for one member of a pair flows on the other member – THIS IS NOT TRUE
- Return currents do not flow in other member of differential pair, but in reference plane
  - Follows path of least impedance
- Important not to break plane layer under traces
  - Can cause cross talk with other signals
  - Can increase unwanted EMI
Differential Traces

- To avoid overshoot and reflections, proper terminations must exist.
- Transmitter and receiver source impedances must be closely matched – termination resistance may also need to be used external to the transmitter and receiver.
- Transmission lines need to have controlled impedance and match that of the transmitter/receiver.
- If not matched, the serial link can become compromised and data transmission can be lost.
Differential Traces

- Lengths of transmission lines used for differential traces need to be approximately the same
- A common misconception is that these need to be tightly matched
  - Example at right shows extra measures used to ensure extremely tight length tolerances
  - This is not necessary
- For a 3.125 Gbps data path with 100 ps rise time at the receiver on FR-4 6000 material, the mismatch tolerance is calculated to be one TEL
  - Mismatch = 0.1 nsec x 5.8 in/nsec
    - Mismatch = 580 mils
Differential Traces

- Neither offer common mode noise coupling immunity
  - Coupling to lines A and B is approximately the same in either case
- Important to keep lines away from noise source
- Broadside differential Tx lines are difficult to fabricate
  - Difficult for PCB designer to route
  - Difficult for board fabricator to register two signal layers with precision to guarantee overlay
- Coplanar differential Tx lines are most common
  - Not necessarily from coupling benefits but from ease of layout and fabrication
**Differential Traces**

- **Common misconception:** Tightly coupled transmission lines are best
  - THIS IS NOT TRUE
- **Skin effect losses are increased, crosstalk is increased, impedance becomes skewed because of geometries**
  - Individual trace impedances go up (≠ 50Ω) because of decreased widths to accommodate differential impedances
- **When traces separate, differential impedance changes**
## Signal Integrity Measurements – Tx Eye Diagram

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>UI</td>
<td>Unit Interval</td>
<td>Baud Rate (BR) = 1/UI</td>
<td>320</td>
<td>3200</td>
<td>ps</td>
</tr>
<tr>
<td>TRr/TRf</td>
<td>Rise and Fall Times</td>
<td>20-80% into 100 Ω load</td>
<td>50</td>
<td>Eye Mask</td>
<td>ps</td>
</tr>
<tr>
<td>V_{dcm}</td>
<td>Transmitter Common Mode Voltage</td>
<td>Required only if DC compliance is claimed</td>
<td>0.72</td>
<td>1.23</td>
<td>V</td>
</tr>
<tr>
<td>Z_{dse}</td>
<td>Single-Ended Impedance</td>
<td>At DC</td>
<td>35</td>
<td>65</td>
<td>Ω</td>
</tr>
<tr>
<td>Z_{ddiff}</td>
<td>Differential Impedance</td>
<td>At DC</td>
<td>75</td>
<td>125</td>
<td>Ω</td>
</tr>
<tr>
<td>R_{L_{dse}}</td>
<td>Single-Ended Return Loss</td>
<td>From 0.004<em>BR to 0.75</em>BR relative to 50 Ω</td>
<td>7.5</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>R_{L_{ddiff}}</td>
<td>Differential Return Loss</td>
<td>From 0.004<em>BR to 0.75</em>BR relative to 100 Ω</td>
<td>7.5</td>
<td>dB</td>
<td></td>
</tr>
</tbody>
</table>

### Parameter Values

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>XT1</td>
<td>0.175</td>
<td>UI</td>
</tr>
<tr>
<td>XT2</td>
<td>0.45</td>
<td>UI</td>
</tr>
<tr>
<td>YT1</td>
<td>0.50</td>
<td>UI</td>
</tr>
<tr>
<td>YT2</td>
<td>0.25</td>
<td>UI</td>
</tr>
<tr>
<td>DJ</td>
<td>0.17</td>
<td>pp UI</td>
</tr>
<tr>
<td>TJ</td>
<td>0.35</td>
<td>pp UI</td>
</tr>
</tbody>
</table>
# Signal Integrity Measurements – Rx Eye Diagram

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{rcm} )</td>
<td>Input Common Mode Voltage</td>
<td>Required only if DC compliance is claimed</td>
<td>0.70</td>
<td>( V_{tt} )</td>
<td>V</td>
</tr>
<tr>
<td>( V_{tt} )</td>
<td>Termination Voltage</td>
<td>Required only if DC compliance is claimed</td>
<td>1.10</td>
<td>1.30</td>
<td>V</td>
</tr>
<tr>
<td>( Z_{tt} )</td>
<td>( V_{tt} ) Source Impedance</td>
<td>At DC</td>
<td>-</td>
<td>30</td>
<td>Ω</td>
</tr>
<tr>
<td>( Z_{rdiff} )</td>
<td>Receiver Differential impedance</td>
<td>At DC</td>
<td>75</td>
<td>125</td>
<td>Ω</td>
</tr>
<tr>
<td>( R_{Lrdiff} )</td>
<td>Differential Return Loss</td>
<td>From 0.004<em>BR to 0.75</em>BR relative to 100 Ω</td>
<td>10</td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>XR1</td>
<td>0.28</td>
<td>UI</td>
</tr>
<tr>
<td>XR2</td>
<td>0.39</td>
<td>UI</td>
</tr>
<tr>
<td>YR1</td>
<td>0.5</td>
<td>UI</td>
</tr>
<tr>
<td>YR2</td>
<td>0.0875</td>
<td>UI</td>
</tr>
<tr>
<td>DJ</td>
<td>0.32</td>
<td>pp UI</td>
</tr>
<tr>
<td>TJ</td>
<td>0.56</td>
<td>pp UI</td>
</tr>
</tbody>
</table>

![Eye Diagram Image](image-url)
Summary

- JESD204x has evolved and continues to evolve into a solid standard to meet current and new ADC interface requirements
  - As the standard progresses, improvements are being made to make the serial link more scalable and robust
- As resolution and speed of ADCs increase the standard must progress towards faster data rates
  - Current speeds are pushing data rates up to 3.125 Gbps and future speeds are looking toward 6.375 Gbps and higher
- As the standard progress towards faster data rates, physical design becomes increasingly important
  - Good design of transmission lines becomes imperative
  - Proper terminations are a necessity
  - Understanding of return current paths is crucial
  - Measuring and understanding measurements of signal integrity important to design a robust JESD204x system
Learn all about JESD204 at:
www.analog.com/JESD204

Buy Card(s):
Avnet Link KC705
Avnet Link FMC174 Card

Download Project:
Wiki.analog.com
References

- JESD204 Serial Interface for Data Converters, April 2006.
- JESD204A Serial Interface for Data Converters, April 2008.
- System Interface Level 5: Common Electrical Characteristics for 2.488-3.125 Gbps Parallel Interfaces - OIF-SxI5-01.0, October 2002.
Helpful Information and Links

- [http://www.jedec.org/sites/default/files/docs/JESD204A.pdf](http://www.jedec.org/sites/default/files/docs/JESD204A.pdf)
  - Free Download - registration required
  - Optical Internetworking Forum OIF-SxI5-01.0 specification
  - Optical Internetworking Forum OIF-CEI-02.0 (includes CEI-6G-SR)
- [http://www.analog.com/jesd204](http://www.analog.com/jesd204)
  - Analog Devices JESD204 parts and information
  - Some useful information about using JESD204A from Xilinx
- [http://www.speedingedge.com/](http://www.speedingedge.com/)
  - Good information about high speed design from Lee Ritchey
Backup Slides – Additional Information
JESD204 Terminology

- **octet** – a group of 8 bits, serving as input to 8B/10B encoder and output from the decoder
- **nibble** – a set of 4 bits which is the base working unit of JESD204x specifications
- **character** – a 10 bit symbol generated by the 8B/10B encoding scheme
- **character clock** – a clock running at the character rate used to process the characters of a system
- **code group** – a set of 10 bits in the serial data stream used to convey octets
- **Running disparity** – the measure of current DC imbalance on the link used to code and decode 8B/10B code groups
- **Frame** – a set of consecutive octets in which the position of each octet can be identified by reference to a frame alignment signal
JESD204 Terminology

- **frame clock** – a system clock which runs at the frames rate. In JESD204A systems, the frame clock is the absolute timing reference in the system.

- **multi-frame** – a set of consecutive frames in which the positions of the frames can be identified relative to a multi-frame alignment character.

- **Multi-frame clock or Local Multi-Frame Clock (LMFC)** – a clock in the system which runs at the multi-frame rate and determines the location of multi-frame characters which are used for lane alignment. Typically this clock is a divided version of the frame clock which is local to the transmitter/receiver. In the coming JESD204B systems, it is expected that this clock will be the absolute timing reference.
## JESD204 Terminology

- **lane** — a differential pair between transmitter and receiver
- **data link or link** — a set of data lanes which provide a conduit for data to be transferred from transmitter to receiver
- **mult-point link** — a data communication link with three or more devices. These three devices may be two transmitters and one receiver or may be two receivers and one transmitter.
- **transmitter** — a single lane’s worth of encoding, serialization, and driving
- **transmitter block** — all transmitters for a link
- **receiver** — a single lane’s worth of capture, deserialization, and decoding
- **receiver block** — all receivers for a link
- **converter** — a single ADC in a package
- **converter device** — a package with one or more converters
JESD204x Transport Layer

- The transport layer maps conversion samples to/from framed, non-scrambled octets for 4 primary mappings.
  - A single converter to a single-lane link
  - A single converter to a multi-lane line
  - Multiple converters in the same device to a single-lane link
  - Multiple converters in the same device to a multi-lane link
- Conversion samples are recommended to be mapped to JESD204x Words on 4-bit nibble boundaries.
- The diagram on the right shows the mapping of converter samples to octets for each lane.
JESD204x Scrambling Layer

- Between the Transport layer and the Link Layer exists a data scrambler/descrambler
  - The data scrambler is implemented to lower the spectral peak emissions on the lanes between the transmitter block and receiver block.
  - The scrambler uses a self synchronous scrambling pattern with polynomial = $1 + x^{14} + x^{15}$
  - Data is scrambled prior to the 8B/10B encoder and descrambled after decoding.
  - As the scrambling pattern is self-synchronous, the two shift registers at input and output need not be set to the same initial state for scrambling to work.
    - The descrambler will always “catch-up” and self-synchronize to the scrambler after two octets of data.
  - The scrambling block should have the ability to be bypassed as not all systems will require it.
Data Link Layer – How is a link established?

There are three distinct phases of link establishment:

1. Code Group Synchronization (CGS)
   - In this phase, each receiver must locate K28.5 characters in its input data stream using Clock and Data Recovery (CDR) techniques.
   - Once a certain number of consecutive K28.5 characters have been detected on all link lanes, the receiver block de-asserts the SYNC~ signal to the transmitter block.
   - In JESD204A, the transmit block captures the change in SYNC~ and after a fixed number of frame clocks, starts the Initial Lane Alignment Sequence (ILAS).
   - In JESD204B, the transmit block captures the change in SYNC~ and starts the Initial Lane Alignment Sequence (ILAS) on the next LMFC boundary.

2. Initial Lane Alignment Sequence (ILAS)
   - The main purpose of this phase is to align all the lanes of the link and verify the parameters of the link.
   - During ILAS, the link parameters are sent to the receiver device to designate how data will be sent to the receiver block.
   - ILAS consists of 4 or more multi-frames. The last character or each multi-frame is a multi-frame alignment character /A/.
   - The first, third, and fourth multi-frames begin with an /R/ character and end with an /A/ character. The data in between them is ramp data. The receiver uses the final /A/ of each lane to align the ends of the multi-frames within the receiver.
   - The second multi-frame contains an /R/ and /Q/ character followed by link parameters.
Data Link Layer – How is a link established?

- There are three distinct phases of link establishment:
  - 2. ILAS - continued
    - Additional multi-frames can be added to ILAS if needed by the receiver.
    - After the last /A/ character of the last ILAS multi-frame, User Data starts.
    - *In systems were no inter-lane skew management is needed, ILAS can be bypassed given both the transmitter and receiver support the mode.*
  - 3. User Data
    - In this phase, user data is streamed from the transmitter block to the receiver block.
      - Data can be optionally scrambled, yet scrambling does not start until the very first octet following the ILAS.
    - The receiver block processes and monitors the data it receives for errors including:
      - Incorrect running disparity (8B/10B error)
      - Not in Table (8B/10B error)
      - Unexpected control-character
      - Incorrect ILAS
      - Inter-lane skew error - This is monitored through a practice called character replacement
    - If any of these errors exists, it is reported back to the transmitter in one of a few ways.
      - SYNC~ assertion – Resynchronization (SYNC~ pulled low) is called for at each error.
      - SYNC~ reporting – The SYNC~ is pulsed high for a frame clock period if an error occurs.
      - Reporting may also be done via interrupt if so equipped. This is not covered by the spec.

The following slide shows the three phases of link establishment
Data Link Layer – Link Establishment

- K=K28.5 code group synchronization comma character
- A=K28.3 lane alignment symbol
- F=K28.7 frame alignment symbol
- R=K28.0 start of Multi-Frame
- Q=K28.4 start of link configuration data
- C= JESD204 link configuration parameters
- D=Dx.y data symbol
- LMFC=Local Multi-Frame Clock
Data Link Layer – Lane Alignment

- During ILAS, the Data Link layers are responsible for aligning lanes in the receiver:
  - Placement of /A/ characters in ILAS are used to align lanes in the receiver block.
  - JESD204 specification requires that /A/ characters be separated by >17 octets. This allows a large amount of system skew to be mitigated.
  - Skew is defined in JESD204 for three possible setups:
    - One transmitter block and one receiver block.
    - Multiple transmitter blocks and one receiver block. (Multiple converters driving one Logic Device)
    - One transmitter block and multiple receiver blocks. (one Logic Device driving multiple DACs)

See next slide shows lane alignment in a receiver using /A/ characters.
Data Link Layer – Character Replacement

Once the User Data phase has been reached, Character Replacement in the Data Link Layer allows frame and lane alignment to be monitored and corrected.

Character Replacement is performed on both Frame and Multi-Frame Boundaries:

Transmitter Character Replacement:
- Frame based – If the last character of a frame is identical to the last character of the previous frame on a given lane (or equals 0xFC if scrambling is enabled), then the transmitter will substitute the character with an /F/ character.
- Multi-frame based – If the last character of a multiframe is identical to the last character of the previous multiframe on a given lane (or equals 0x7C if scrambling is enabled), then the transmitter will substitute the character with an /A/ character.

Receiver Character Replacement:
- The receiver must do the exact opposite from the transmitter.
- If an /F/ character is detected, it is replaced with the final character of the previous frame, or if an /A/ is detected, it is replaced with the final character of the previous multiframe.
- If scrambling is enabled, /F/ characters are replaced with 0xFC and /A/ characters with 0x7C.

If /A/ and /F/ characters are found in incorrect places, then the receiver can realign the lanes on the fly. Data will be corrupted during this operation.
## Data Link Layer – Character Replacement

### Implications of character replacement/realignment

- **/A/ and /F/ characters may not come along that often, so if data goes bad it may take a while for the receiver to know.**
  - Garbage data might be sent for some period of time.
  - If the error is in the CDR or high speed link somewhere, the 8B/10B error detector is expected to see it well in advance.

- **If realignment is supported, each lane can realign to an /A/ or /F/ character.**
  - The JESD204 specification makes comments about realigning characters or alignment counters on the fly.
  - Unless either transmitter or receiver skipped a character clock, this should not be a problem.

### Where would this make sense?

- This makes sense for sparse data systems, or packet systems, where data can be lost.
- For systems with dense data transfer, realignment will be preceded by a stream of garbage data.
JESD204x Physical Layer

- The Physical Layer (PHY) is where characters are transmitted and received at line rate speeds
  - This layer includes Serial/Deserializer (SERDES) blocks, drivers, receivers, Clock and Data Recovery (CDR)
    - Often designed using custom cells due to high speed of data transfer
- JESD204 and JESD204A supported speeds up to 3.125 Gbps
- JESD204B supports speeds up to 12.5 Gbps
## JESD204x Physical Layer Comparison

<table>
<thead>
<tr>
<th>Parameter</th>
<th>OIF-SxI5-01.0</th>
<th>CEI-6G-SR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line Rate</td>
<td>( \leq 3.125 ) Gbps</td>
<td>( \leq 6.375 ) Gbps</td>
</tr>
<tr>
<td>Output Differential Voltage (mVppd)</td>
<td>250 (min) [250]</td>
<td>200 (min) [200]</td>
</tr>
<tr>
<td></td>
<td>500 (max) [500]</td>
<td>375 (max) [375]</td>
</tr>
<tr>
<td>Output Rise/Fall Time (ps)</td>
<td>( &gt; 50 )</td>
<td>( &gt; 30 )</td>
</tr>
<tr>
<td>Output Total Jitter (pp UI)</td>
<td>0.35</td>
<td>0.30</td>
</tr>
</tbody>
</table>

- High speed, fast rising signals place tighter constraints on board level design
- Careful attention needed for trace impedance, trace lengths, layer stackup, etc.
- A good set of physical design rules is imperative