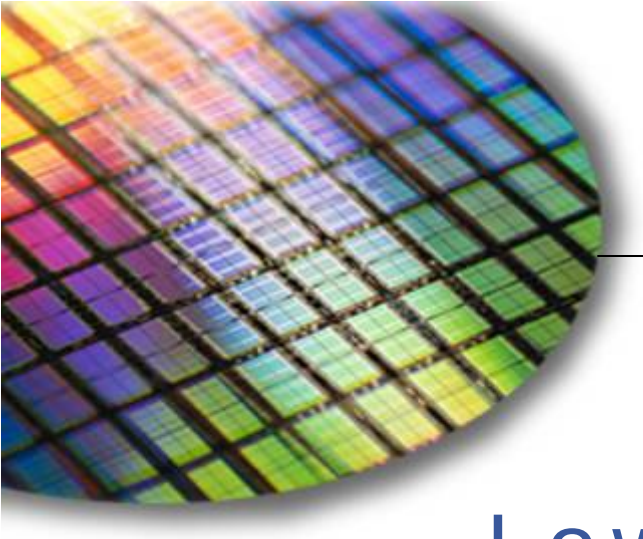


The World Leader in High Performance Signal Processing Solutions

Low Level Leakage Measurements on Switches and Multiplexers

Analog Devices

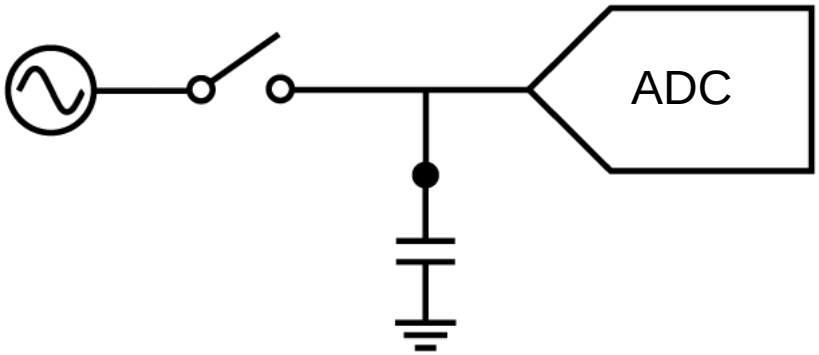
ANALOG DEVICES

Contents

- **This presentation will discuss the best practice PCB layout techniques to be used for making low level current leakage measurements**
- **These techniques should be used when accurate low level current levels are needed**

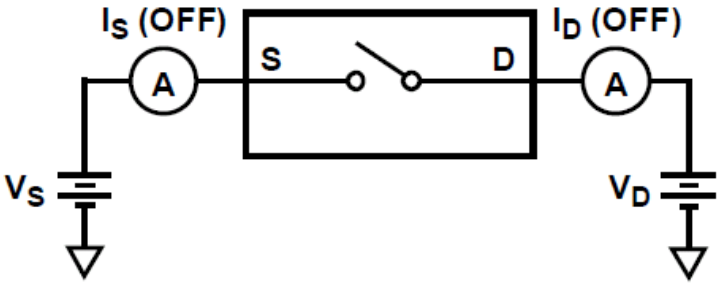
Background

- Low leakage switches or multiplexers can be used in high impedance systems to accurately charge and maintain a voltage on a sample & hold capacitor
- When the switch is closed the capacitor is charged to the input voltage
- The switch is then opened and the voltage on the capacitor is sampled by an ADC
- When the switch is off, there is a large off resistance across the switch which results in a low current leakage path
- Measuring this low leakage is difficult due to the effect of parasitics on PCBs
- This tutorial will outline a method for reducing the effect of PCB parasitics

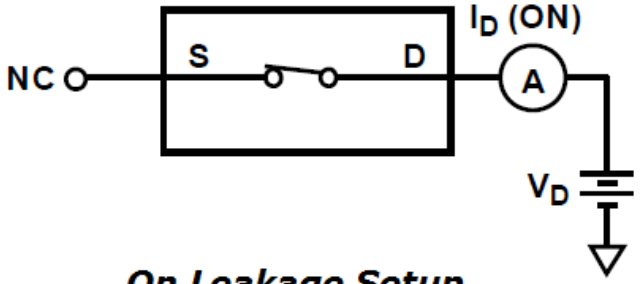


Leakage Testing Setup

- **All ADI switch & multiplexer products are production tested for on & off leakage**
- **Off Leakage**
  - **This occurs when the switch is disabled, & is a measure of the level of current that flows from the load back through the switch to ground**
  - **Test conditions**
    - Switch between Source and Drain is open
    - Source and Drain are biased at different potentials
    - Off Leakage is measured at both the Source and Drain
- **On Leakage**
  - **This occurs when the switch is enabled, & is a measure of the level of current that flows from the source back through the switch parasitics to ground**
  - **Test conditions**
    - Switch between Source and Drain is closed.
    - Only the Drain side is biased
    - On Leakage is measured at the Drain side only.



Off Leakage setup

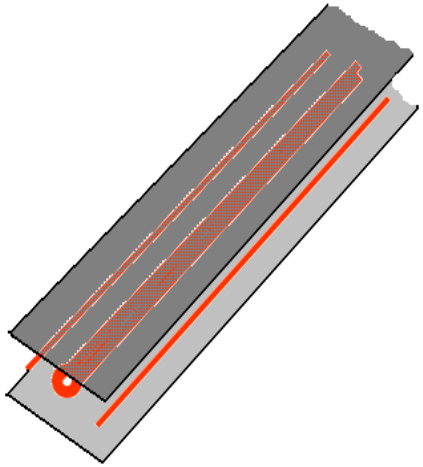


On Leakage Setup

Layout Practice

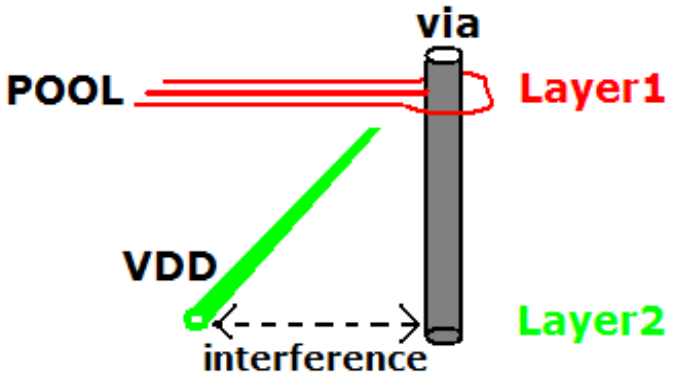
Box Guarding Low Leakage Signals

- **Signals which require low levels of current leakage should be buried within the board and not exposed on the top or bottom layers to eliminate exposing the PCB trace to contaminants which can cause leakage paths**
- **Within the board, the signal should be guarded from all sides (as shown in bottom diagram)**
  - **Left and right**
  - **Top and bottom**
- **Every signal actually consists of 3 layers (top, middle and bottom guard)**
- **This has the effect of creating a coaxial cable, which reduces the potential difference between the signal trace and the guard, With no potential difference no leakage currents flow form the signal trace**

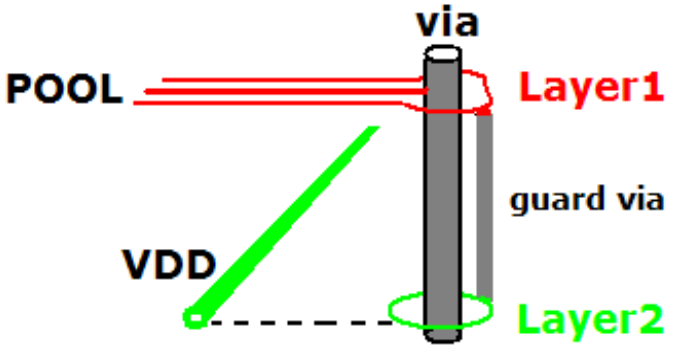


Layout Practice
Box Guarding Guidelines

- **To reduce leakage paths any via that carries a signal should be guarded on that layer (Layer1)**
- **The via is now at the same potential as the signal, no potential difference exists and so no currents flow between the two paths**
- **This via is open to interference on another layer, if a different signal runs close to it, creating a potential leakage path**
- **To limit any such interference, the via should be box guarded on this layer and every other layer**
- **The same is true for the pin of any through-hole part carrying a signal**



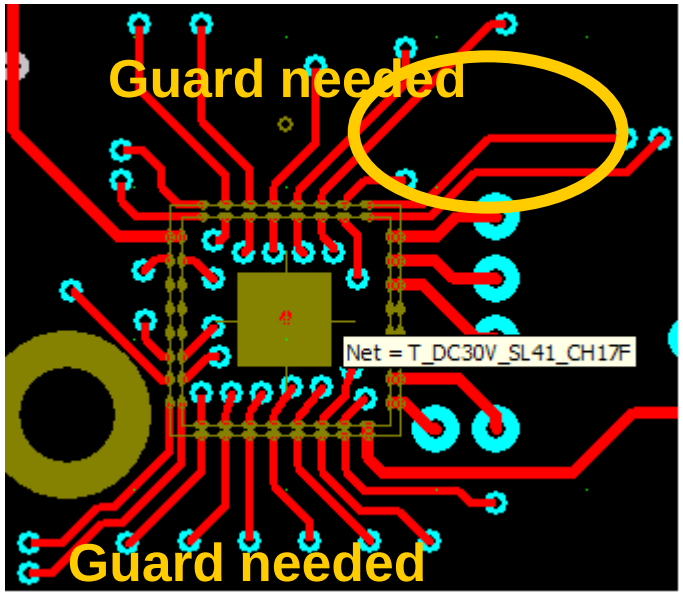
Ref diagram with arrows if necessary

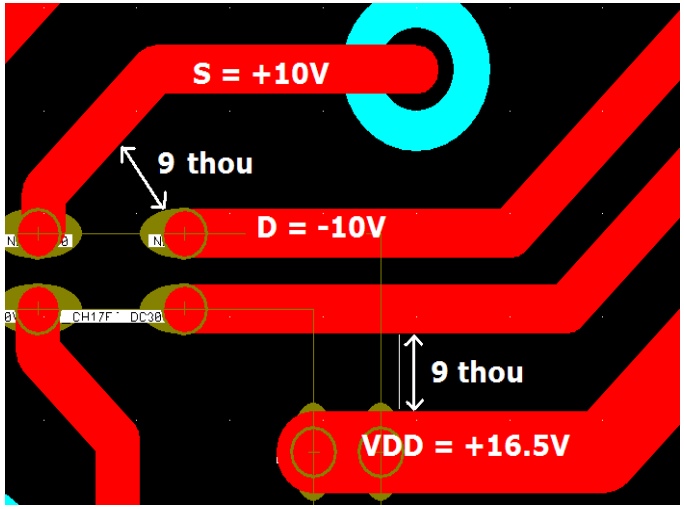


Guarding Signals at the Pin

High Voltage Parts

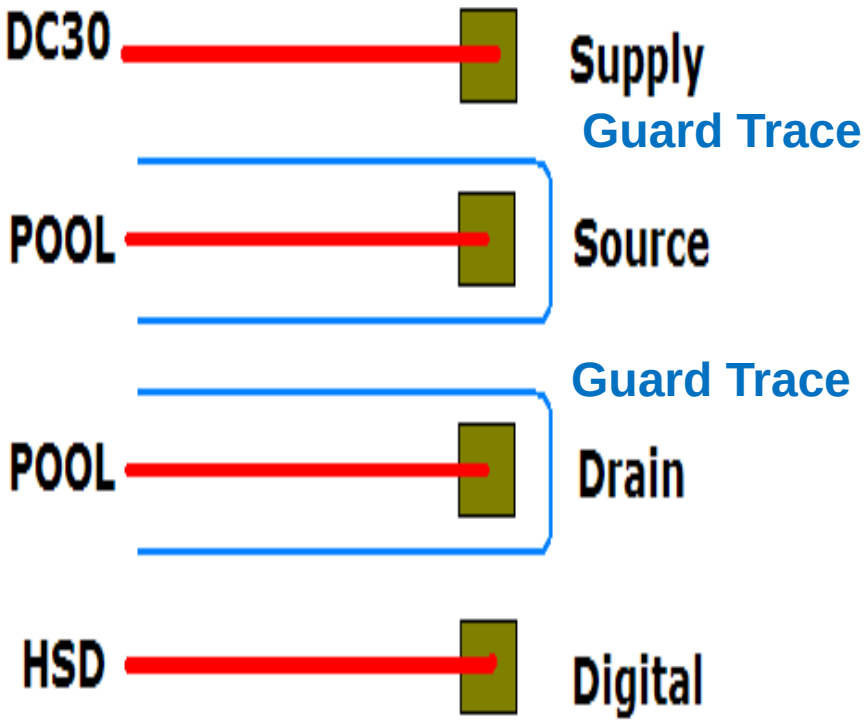
- **High voltage parts are more susceptible to leakage paths, due to the large voltage differential across the junctions**
- **When measuring leakage, the analog pins are biased to voltages slightly within the max signal range so as not to include leakage caused by the internal ESD diodes**
- **Potential differences of over 20V between signals that are less than 15 mil apart can cause significant leakage current between the PCB traces**
- **To make accurate low leakage measurements, signals must be guarded from**
  - **supply signals**
  - **digital signals**
  - **other signals at a different potential**





Guarding Signals at the Pin
Ideal Setup

- **The width of a guard can be brought down to 3 thou using modern PCB manufacturing techniques**
- **This guard trace (in blue) must have 3 thou clearance on either side**
- **When pins are far enough apart (15 thou), the ideal guarding situation is shown on the right**
- **The signals of different potential are fully guarded from each other and from the supply and digital signals**



Guarding Signals at the Pin in Narrow Pitch Packages

- As the pitch becomes narrower, it may only be possible to fit only one guard between the parts pins (Figure1)
- This is not recommended. The different potential on the Source guard is brought closer to the unguarded Drain, providing a potential leakage path
- A better solution is shown in Figure2. Guard both signals as close as possible to the parts pins
- The material between the pins is providing the isolation

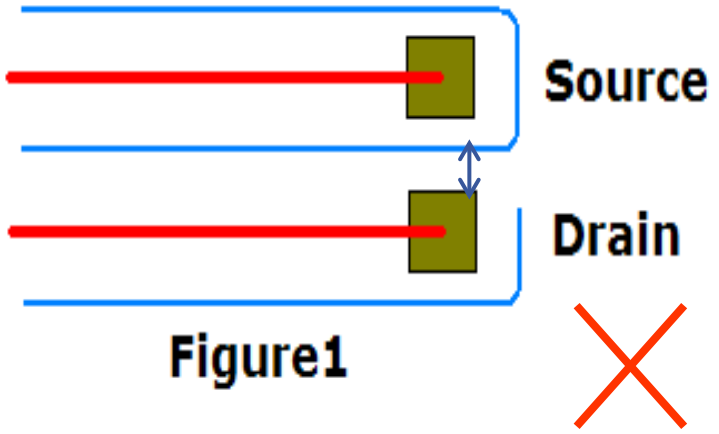


Figure1

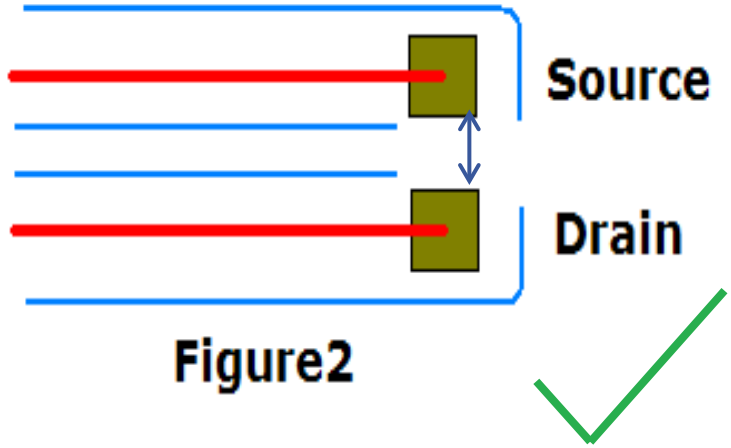
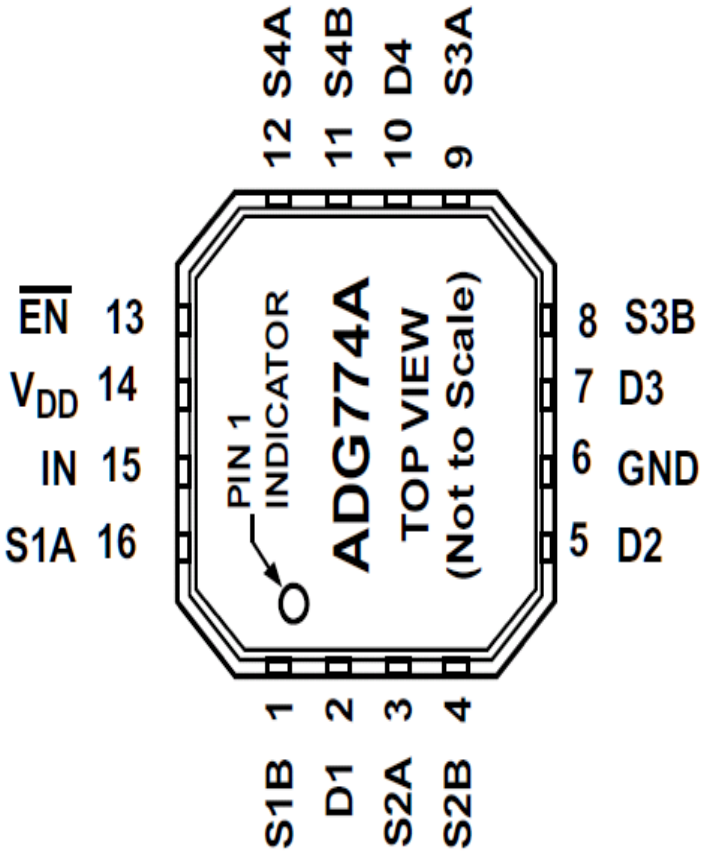
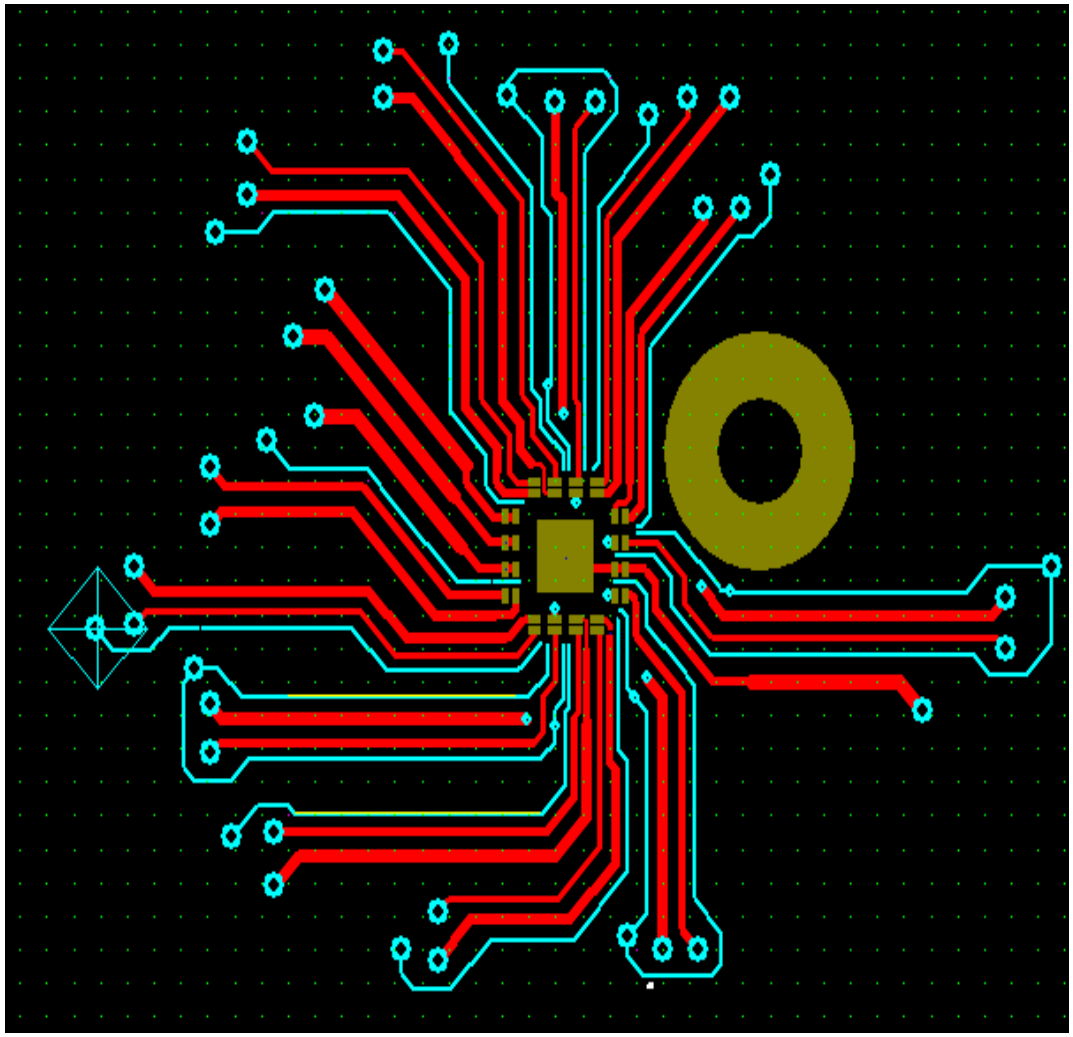


Figure2

Layout Examples

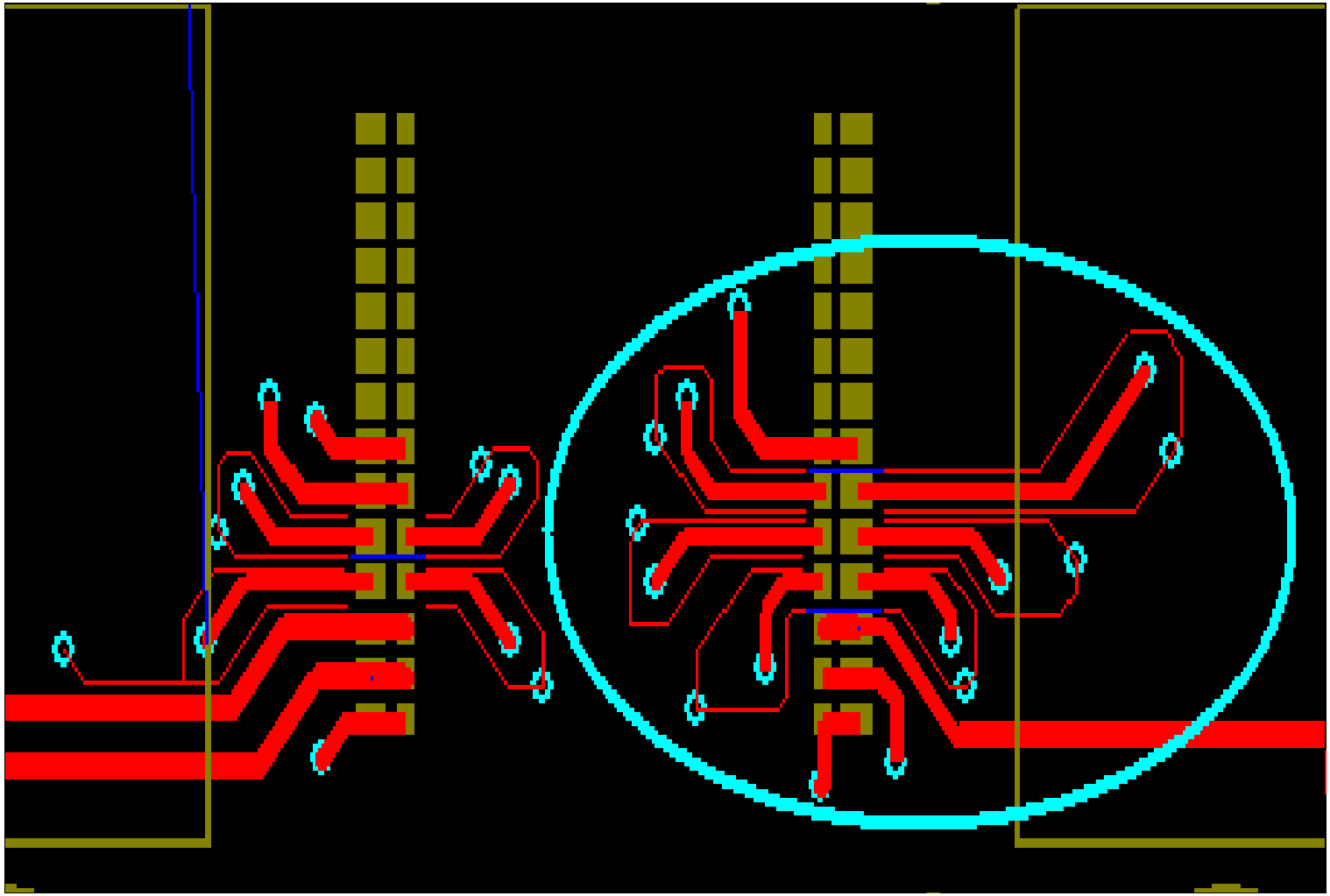
3x3 16ld LFCSP (0.5mm)





Layout Examples

14ld Kelvin TSSOP (0.5mm)



Conclusion

- **PCB traces that require low levels of leakage need special design considerations**
- **Tight pitch packages present some difficulties in achieving guard traces but modern PCB construction techniques allow for narrow trace widths that enable guarding**
- **Where pin pitches are too tight an alternate scheme is shown**