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AD9915 Evaluation Board for 2.5 GSPS DDS with 12-Bit DAC

FEATURES

Full-featured evaluation board for the AD9915
PC evaluation software for control and measurement of the AD9915
USB interface
Graphic user interface (GUI) software with frequency sweep capability and programmable modulus for board control and data analysis
Factory tested and ready to use

PACKAGE CONTENTS

AD9915 evaluation board
AD9915PCBZ installation software CD
USB cable

GENERAL DESCRIPTION

This user guide describes how to set up and use the AD9915evaluation board. The AD9915 is a 2.5GSPS DDS with a 12-bit DAC.

The evaluation board provides a graphical user interface (GUI) for easy communication with the device along with many user-friendly features such as the mouse-over effect.

This user guide is intended for use in conjunction with the AD9915 data sheet.

EVALUATION BOARD

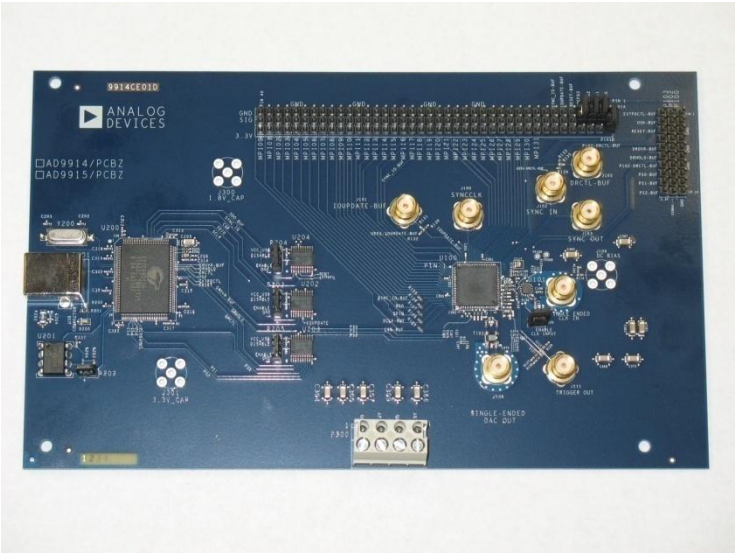

Figure 1.

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REVISION HISTORY

8/1—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

REQUIREMENTS

The user must install the evaluation software prior to connecting the evaluation board. Administrative privileges are required for software installation.

The following sections are for setting up the physical connections to the AD9915 evaluation board.

POWER SUPPLY CONNECTIONS

The AD9915 evaluation board has one power supply connector (four pins): P300. P300 powers the USB interface circuitry and the AD9915.

Table 1shows the necessary connections and the appropriate biasing voltage.

Table 1. Connections and Biasing Voltage

Connector	Pin No.	Label	Voltage (V)
P300	1,3	GND	0
P300	2	3.3V	3.3
P300	4	1.8V	1.8

INPUT CLOCK OPTIONS

The AD9915 architecture provides the user with two options when providing an input CLOCK signal to the part. The first option allows the user to provide a high frequency input signal, connected to J104. The second option allows the user to connect using a lower input reference frequency, enabling the clock multiplier, and connects through J104.

Note: The input CLOCK path on the AD9915 evaluation board uses an ADCLK925 clock buffer to drive the AD9915 differentially. That said, a slow slew rate into the ADCLK925 could dramatically limit the AD9915 in-close phase noise performance.

Refer to theADCLK925 data sheet for details on the maximum input speeds and input sensitivities.

JUMPERS SETTINGS

Use the jumper settings listed in Table 2 to enable different modes of communication.

Table 2. Jumper Settings for Communication Modes

Mode	Settings
PC Control, USB Port (Factory set)	Set Jumpers P203, P204, and P205 to enable. Install jumpers P105, P202. Set Jumpers IOCFG0 to IOCFG4 to 1000 respectively.
External Control	Set Jumpers P203, P204, and P205 to disable. Control the AD9915 via external header connectors.

Note, this document does not cover all aspects of externally controlling the AD9915 evaluation board.

Device Communication

The AD9915 has a serial mode or parallel mode interface option via the function pin settings (IOCFG0 to IOCFG3). Refer to **Programming and Function Pins** Section in the **AD9915** datasheet for other possible configurations. However, the AD9915 software GUI supports only serial mode operation only. To drive the AD9915 in a parallel fashion requires external control. As a result, header connectors are provided for direct access to the AD9915 pins.

- USB 1.1/2.0
- Header connector P101 is used to place the DUT under the control of an external controller (such as a microprocessor, FPGA, or DSP).

Analog Devices provides a GUI for the PC; it does not provide control software for external controllers.

EVALUATION BOARD LAYOUT

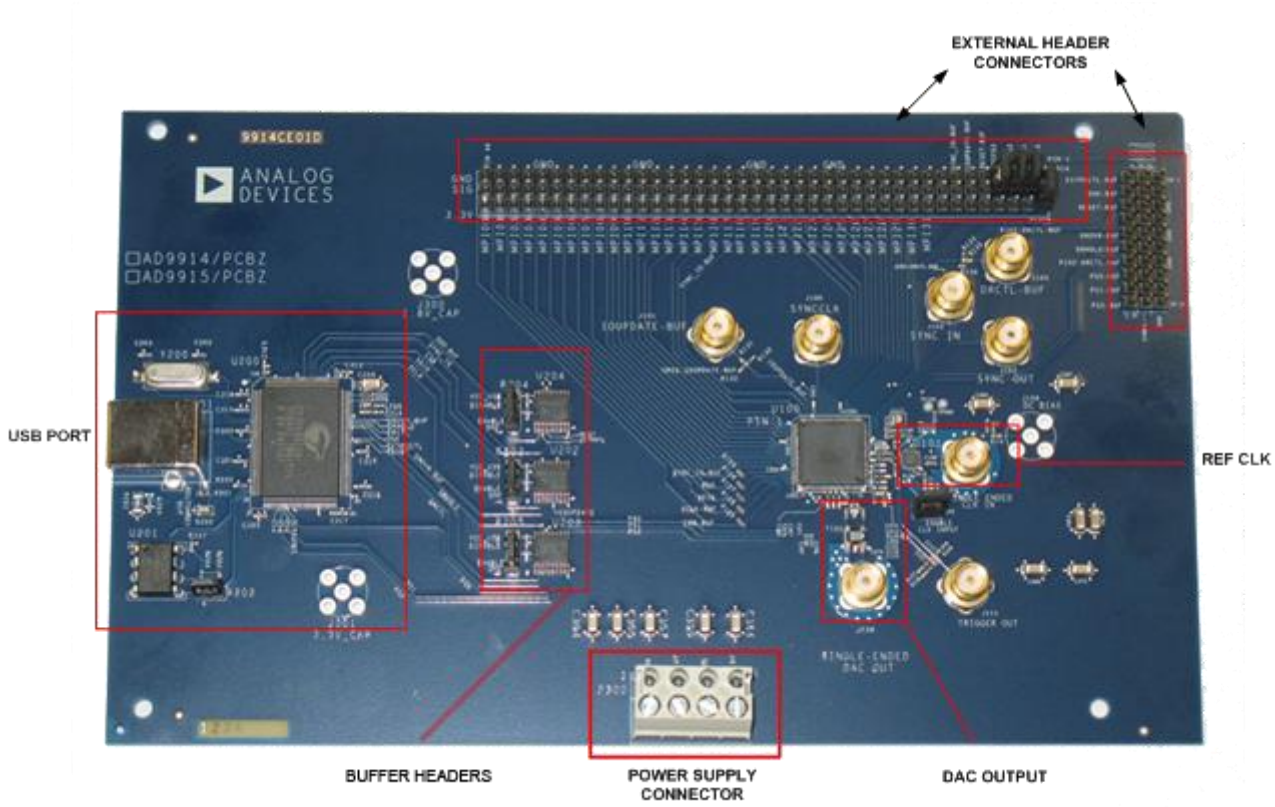


Figure 2. AD9915 PCB Evaluation Board

External I/O Control Headers

Header connectors provide a communication interface for the AD9915 when the part is under the command of an external controller.

DAC Output

Connection for the unfiltered output of the DAC.

Ref Clock Input

This is the input for the external reference clock signal. Refer to AD9915 datasheet for reference input range.

Power Supply Connections

Provides all necessary supply voltages needed by the AD9915 and the evaluation board.

USB Port

When the part is under PC control (default mode), the evaluation board communicates with the AD9915 via this port.

Buffer Headers

These header connections can be set to enable or disable. Disable means to allow external serial control by configuring buffer in its high-impedance state. Default setting is enabled.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

Do not connect the evaluation board until the software installation is complete. An installation CD is provided with each evaluation board.

NOTE: The software requires a Windows XP operating system.

Follow these steps to install the evaluation board software:

1. Log into your computer system with administrative privileges.

2. Insert the evaluation board software CD into your CD-ROM drive.

3. For computers that do not have **.NET Framework 3.5 installed,** use the **"AD9915_Setup_v1.0.4002.29083_Full**" executable file to install the prerequisite and the evaluation board software. For computers that have it, the installation can be made by using "**AD9915_Setup_v1.0.4002.29083**".

4. The next step would be the driver installation.

DEVICE DRIVER INSTALLATION

1. Power up the evaluation board.

2. Connect the evaluation board to the computer via the USB port using a USB cable. Then, a green LED light**(D200)**would illuminate to indicate USB connection.

3. When the USB cable is connected, the *Found New Hardware Wizard* appears. Click **Next** to continue the installation of a new driver.

4. Click **Continue Anyway** when the *Hardware Installation Warning* window appears.

5. Click **Finish** in the *Found New Hardware Wizard* when installation is complete.

6. When a second *Found New Hardware Wizard* dialog box appears, just repeat steps 3-5.

STARTING THE SOFTWARE

Before you start the software, make sure that the AD9915 evaluation board is powered up and connected to the PC, and the LED D200 (USB status) is on. Refer to Power Supply Connections in this user guide for correct settings.

To start the AD9915 evaluation software, follow these steps:

1. Click the **Start** button (located at the bottom left corner of your desktop).
2. Select **All Programs** >**Analog Devices** >**AD9915 Evaluation Software**.
3. Click **AD9915 Evaluation Software** to start the software.

A **successful connection** of the software to the board is indicated by this green icon, which can be found at the bottom right corner of the window. An **unsuccessful connection** is indicated by this flashing red icon.

Most installation errors can be resolved by checking jumper settings, making sure that the evaluation board is powered up correctly, and inspecting the USB port and cable connections.

When all power, USB port/cable connections, and jumper settings are correct, an error may still appear if the clock input is not properly configured. Check to make sure that the clock input source is connected and properly configured.

Another reason is due to conflicting device driver. This can be fixed by updating the driver. You can do this by plugging the USB connector into another USB port. The computer would then inform you to install a device driver and a window would come into display.

Figure 3. Found New Hardware Wizard Dialog Box.

Choose the selection indicated by Figure 3.

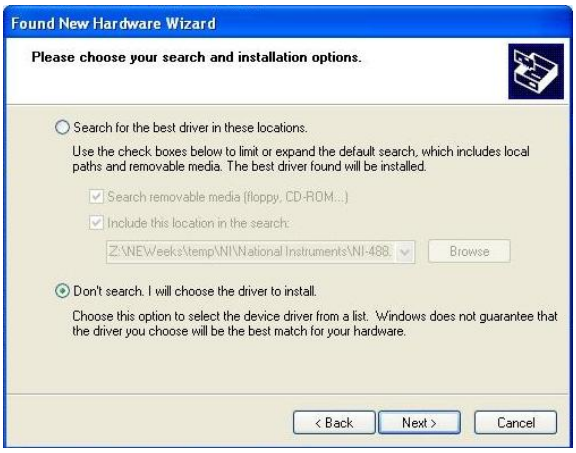


Figure 4. Choose Driver to Install

Again, choose the indicated selection as in Figure 4 then click **Next**.

Figure 5. Choosing the device driver

There are times that the operating system would load a wrong driver. The reason for that is the OS detects multiple drivers that can be used by the hardware, in our case it would be the evaluation board. If that happens, multiple drivers can be seen in this window. Select only the **AD9915 Firmware Loader**, and then click **Next**. A Hardware Installation box will then appear, just click **Continue Anyway**. Lastly, close the wizard by clicking **Finish.**

RUNNING THE SOFTWARE UNDER WINDOWS 7

The software is compatible on Windows XP, however you can run it using Windows 7 by **running Windows XP under Windows 7**. You can do this by using the **Windows Virtual PC**. The main website is indicated below.

http://www.microsoft.com/windows/virtual-pc/

They have specific instructions for the installation depending on the version of Windows 7 that your computer has, so refer to the site for the detailed information.

When you have installed the Windows Virtual PC, it would typically look like Figure 6.

Install the software within the virtual machine by following the same procedure as indicated in the software installation guide. Then connect the USB connector of the evaluation board. You will then notice that the USB interfaces are not shown in the notification area at the right side of the taskbar. Since you are using a virtual machine, all of the USB notifications can be found at the pane at the top of the desktop window. Just "**Attach**" the **Version 1.2.2.0** USB device, and you would be able to get the software running.

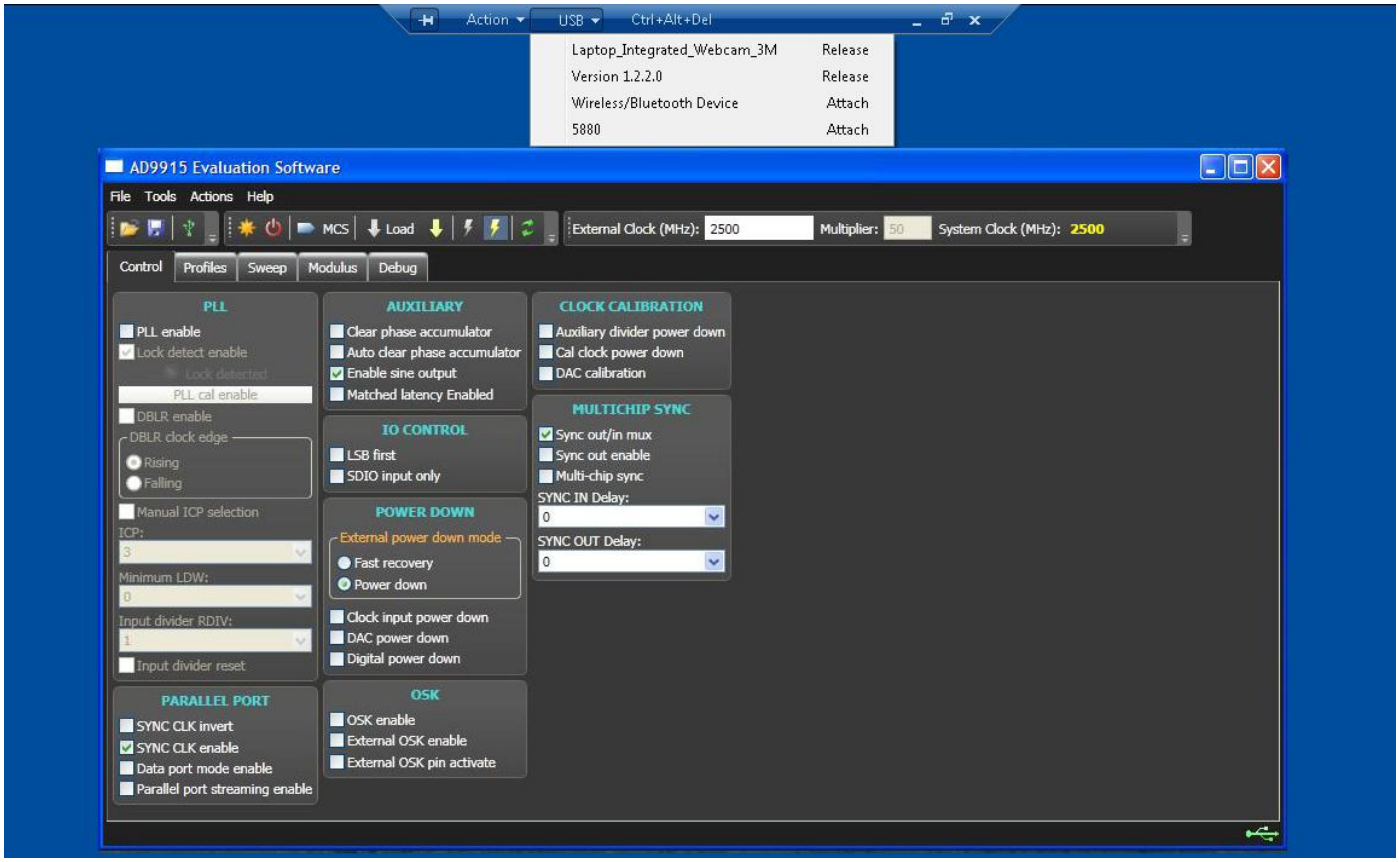
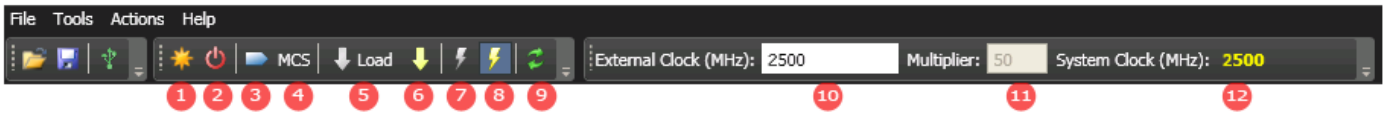


Figure 6. Evaluation Board Software in Windows 7 using Virtual XP machine

ICON DESCRIPTION OF CONTROL WINDOW

The ICON description window is built to allow ease of access to different actions. Another way of accessing these icons is by clicking the **Actions** tab and select among the actions in the drop-down menu.



1. **Master reset** - The master reset is required after the device is powered up. This button will initiate a master reset pulse every time it is pressed or clicked. A master reset will force the internal registers to their default state value.
2. **Power down** - Controls the state of the power down pin. This will power down features in the AD9914. See data sheet for detailed description. This button function is either static low or static high. A static high enables the power down function. In static high state the button will have different background color.
3. **DAC calibration** - This button initiates a routine that automatically sets the proper setup and hold times for the internal D/A converter. NOTE. A DAC Calibration is required if the External Clock is changed. Flashing red means DAC needs calibration.
4. **MCS** - Multiple Chip Synchronization.
5. **Load** - This button forces an IO_UPDATE to activate changes. NOTE. This ICON will flash if a change is registered. The user must click or press the flashing Load button to make the change occur.
6. **Disables/Enables Auto Load Registers** - Enabling it would mean that any user interface updates are reflected automatically to the registers. No need to click LOAD button.
7. Click to send **Manual IO_UPDATE**
8. **Disables/Enables Auto IO_UPDATE**
9. **Click to Read Register**
10. **External Clock (MHz)** - Provides entry window for desired REF_CLK frequency operation. Must be entered to calculate correct frequency tuning word(s)
11. **Multiplier** - Used in combination with the internal PLL. If the PLL is enabled the number entered (8 to 255) multiplied by the External Clock entry determines the system clock frequency.
12. **System Clock (MHz)** - This number represent the internal clock frequency of the of the DDS.

Figure 7. ICON Description

EVALUATION BOARD SOFTWARE COMPONENTS

FULL CONTROLWINDOW

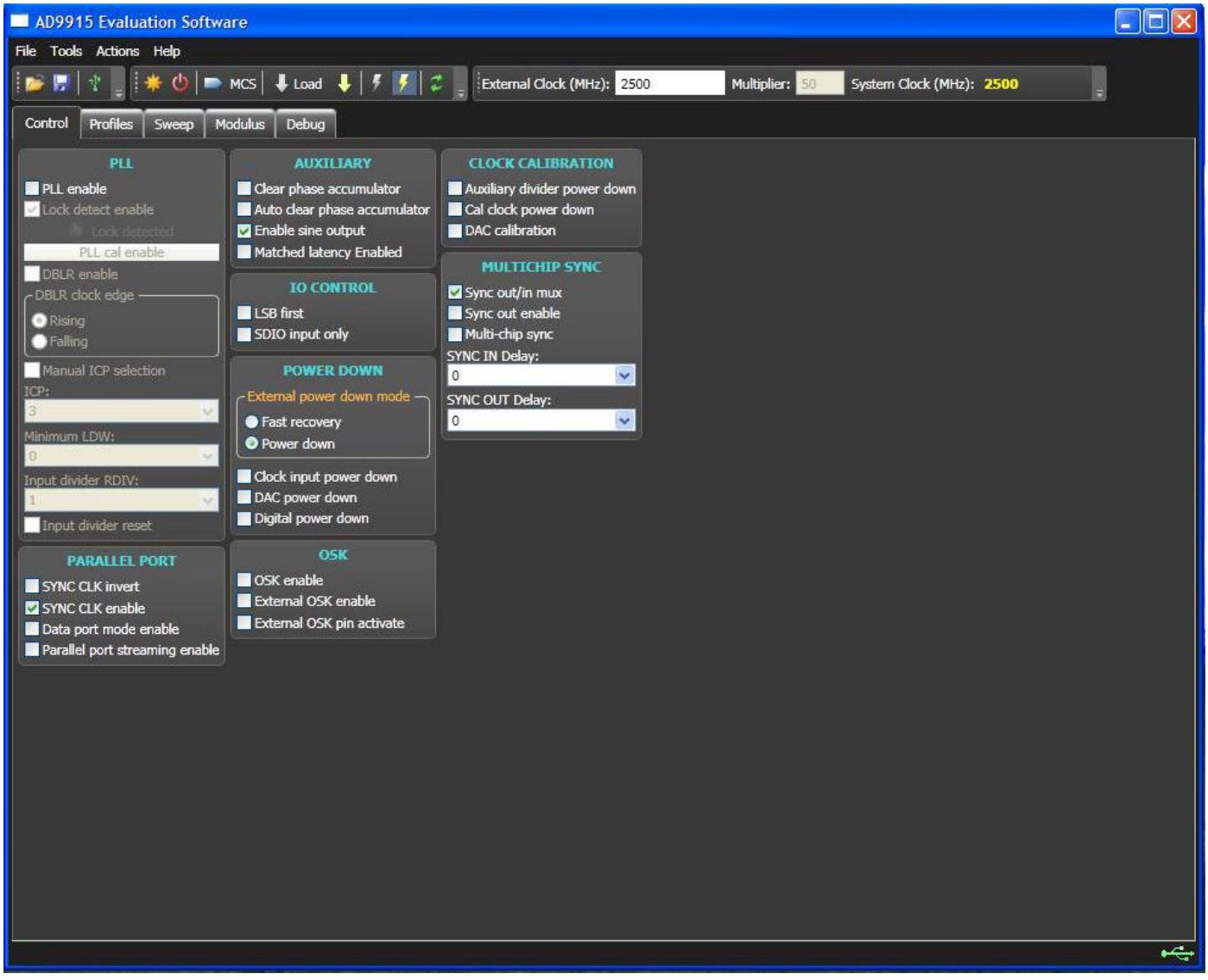


Figure8.Evaluation Software Control Window

The **Control** window provides control of the internal PLL, parallel port, auxiliary functions, I/O control, power down functions, OSK, clock calibration and multichip sync function of the AD9915 (see Figure 8).

Setting the Internal PLL

The **PLL** section allows you to enable the internal PLL of AD9915.

PLL enable is used to activate internal PLL of AD9915. The default setting of this box is disabled (check box cleared), indicating that the internal PLL is bypassed and the reference clock input is the system clock. Once **PLL enable** box is checked, the **Multiplier** option and the **PLL Cal Enable** button are activated, as well as all other options in the PLL section.

If using internal PLL, the external clock input and the multiplier must be within the range defined in AD9915 datasheet. Refer to AC Specifications Table of the datasheet.

Once values are set, click **PLL cal enable** to calibrate internal PLL and allow PLL lock detect.

Note: PLL Cal Enable must be performed always every time the External Clock frequency and/or multiplier is changed. Always follow with DAC calibration by clicking the DAC calibration ICON.

Enabling **PLL enable** automaticallyactivates **Lock detect enable.** Default value is enabled (checked box). The indicator **Lock detected**displays green light once the PLL is locked.

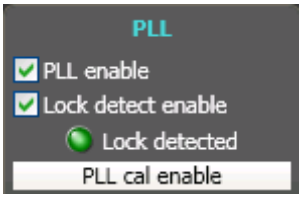


Figure 9. PLL lock detection

DBLR enableallows an additional x2 multiplication to the reference clock.

ICP selects the charge pump current output of the PLL in the reference clock multiplier circuitry. Refer to the PLL charge pump current table of the AD9915 datasheet for the corresponding current values (0-7) in the drop-down menu. The default setting is 3 which is 500uA.

Setting the Parallel Port

The default value of **SYNC CLK invert** is disabled (unchecked box), which sets the normal SYNC_CLK polarity. The **SYNC CLK enable** sets the internal SYNC_CLK signal to appear at the SYNC_CLK pin. Refer to Bit Descriptions for CFR2 table in AD9915 datasheet for more information. The **Data port mode enable** allows parallel data port modulation in which the modulated DDS signal control parameter(s) are supplied directly from the 32-bit parallel data port. Make sure the profile mode and the sweep mode are disabled to allow parallel data port mode. The 32-bit port can be accessed through the external I/O header P101. Refer to **Programming and Function Pins** Section in **AD9915** datasheet for different configurations. The **Parallel Port Streaming Disable** default value is logic 0 (unchecked box). This means the Parallel port streaming bit is disabled. To enable, change it to logic 1 (check the box). Enabled parallel port streaming means that the data port continuously samples from the 32-bit parallel data without the need of IO_UPDATE. See CFR1[17] in the datasheet for more information.

Auxiliary and IO Control

Clear Phase Accumulator holds the DDS phase accumulator in a reset state as long as this bit (Bit 11) is set. **Auto Clear Phase Accumulator** sets the DDS phase accumulator to a reset state when the I/O update pin is set high or when a profile changes.The default output of AD9915 is sine output. To enable cosine output of DDS, just uncheck the **Enable sine output** checkbox.

Matched Latency Enabled allows you to align the application of the frequency tuning word, the phase offset word, and the amplitude scale factor at the same time. If this bit is cleared (default value), then those words arrive at the output in the order listed in the data sheet.

LSB first configures the serial I/O port for LSB-first format. **SDIO** configures the serial data I/O pin (SDIO). Refer to AD9915 data sheet for more information on SDIO settings.

Setting Power-Down Controls

These power-down controls allows you to power down each of the specific circuit blocks individually.

External Power Down Mode allows you to control which power-down mode is used in conjunction with the External Power Down Pin button. The **Fast Recovery** mode maintains power to the DAC bias circuitry, PLL, VCO and input clock circuitry. This mode uses significantly more power than the **Power Down** mode but allows the device to be awaken very quickly from power-down state. The **Power Down** mode stops clocks and powers down bias circuits. This mode takes significantly longer to power back up from a power-down state. See the Power-Down Control section in AD9915 data sheet for more information. Checked **Clock input power down** box will disable REFCLK input circuits and PLL. Default value is enabled (unchecked box). **DAC power-down** default value (unchecked box) sets the DAC clock signals and bias circuits active. To disable, check the checkbox. **Digital power down** default value sets the digital core active. To disable, just change logic to 1 (check the box).

OSK

To select the OSK function of the AD9915, select the **OSK Enable** check box. **External OSK enable**allows you to use manual (default) or automatic OSK function. Refer to AD9915 data sheet for more information on these bits on CFR1. Use of **External OSK pin activate** functionality depends on the state of the external OSK control bit and OSK enable bit. Refer to Figure 31.OSK Block Diagram of AD9915 data sheet for more information.

Clock Calibration

Checking the **DAC calibration** checkbox has the same function with the **DAC calibration ICON**.

Auxiliary divider is an internal divider in AD9915that is used as a part of clock calibration process. The default value is enabled. Once the **Auxiliary divider power down** is checked, the auxiliary divider is powered down, thus disabling clock calibration.

The default value of **Cal clock power down** is unchecked. It means that the clock calibration is enabled. To disable internal clock calibration, activate the power down function by checking the checkbox.

Multichip Sync Control

The **Multi-Chip Sync** control allows you to set up the sync function. This allows you to synchronize multiple chips to one master AD9915. Refer to the AD9915 data sheet for a full discussion on multichip sync functions. The **Sync out enable** checkbox allows activation of SYNC_OUT pin. Default value is disabled. To enable multi-chip synchronization, select **Multi-chip sync**. **SYNC IN delay** drop-down menu allows the user to delay the SYNC_IN signal by programming the 3-bit word. **SYNC OUT** delay can also be programmed.

PROFILE MODE

In Profile Mode, the DDS signal control parameters are supplied directly from the profile programming registers. A profile is an independent register that contains the DDS signal control parameters.

SINGLE-TONE OPERATION

For single tone operation, follow these steps:

1) Power-up the AD9915 evaluation board (Refer to power connections in this user guide).
2) Put REF CLK source for the REF CLK input. (Refer to datasheet for reference frequency values).
3) Load the AD9915 evaluation software.
4) Click the Master reset ICON.

   Note: Every time you connect an evaluation board, always do the Master Reset. This clears all memory elements and sets registers to default values.
5) Enter desired REF CLK frequency value in External Clock window.
6) Click DAC CALIBRATION ICON.

   Note this ICON must be clicked for all initial setups andevery time the REF CLK frequency is changed.
7) Click the profile tab to go to the profile windows.
8) Enable profile mode via check box and enter the desired output frequency in profile 0.
9) Click the flashing LOAD button top of GUI.
10) View the DAC output performance via oscilloscope or spectrum analyzer.

There are eight profile registers (Profile 0 – Profile 7) that are available but only a single profile can be loaded to the DDS at a time. They cannot be loaded simultaneously.

To load a profile, check first the **Enable Profile Mode** checkbox and then select a profile at the **Selected Profile** drop-down menu.

Data Entry

Frequency is used to set the frequency generated by the DDS. The input values are in MHz (refer to datasheet for acceptable range of output frequencies)

Phase Offset controls the phase of the DDS output. The input is in degrees and this can be changed from 0° to 360° with 16-bit resolution.

Amplitude Scale Factor digitally controls the amplitude of the carrier from the DDS. This scalar ranges from 0 to 1 and has a 12-bit resolution. Note that this function only works if the **OSK enable** is activated in the **Control Tab**.

Note that Frequency, Phase Offset, and Amplitude Scale Factor can accept native data that are going to be loaded directly to the registers. This data is binary in form but can also be expressed as hexadecimal, or decimal. This can be done by pressing the drop-down button at the side of each input.

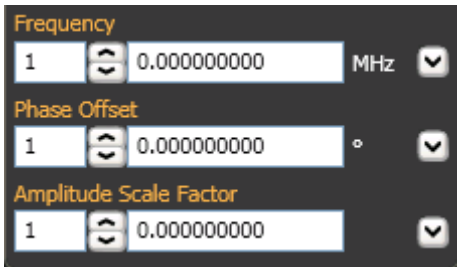


Figure 10. Default Profile Display

Figure 11. Profile Data Entry Expanded

DIGITAL RAMP GENERATOR (DRG)

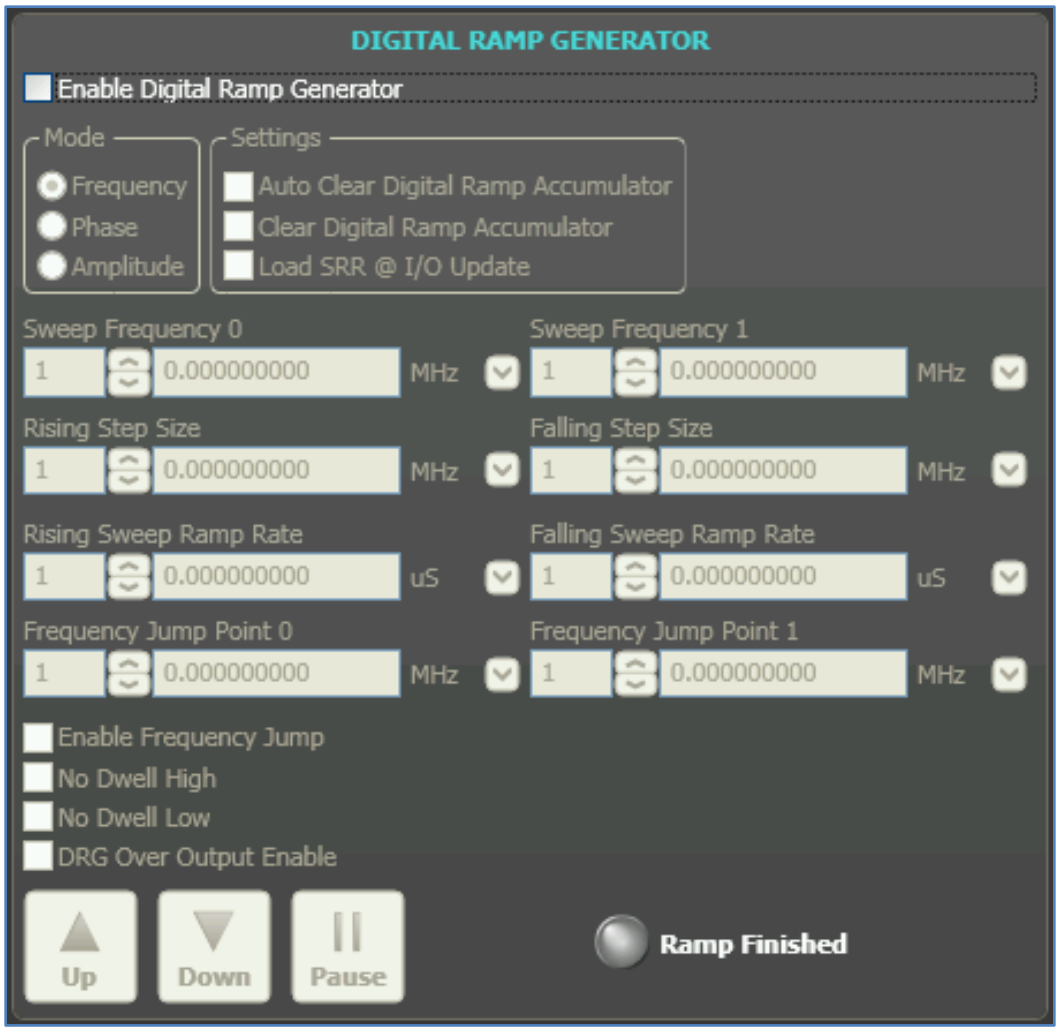


Figure 12. Digital Ramp Generator Window

Digital Ramp Generator is synonymous to linear sweep. The ramp generation parameters allow the user to control both the rising and falling slopes of the ramp, the upper and lower boundaries of the ramp, the step size and step rate of the rising portion of the ramp, and the step size and step rate of the falling portion of the ramp. This is digitally generated with a 32-bit output resolution that can be programmed to represent frequency, phase, or amplitude. Refer to AD9915 datasheet for more information on DRG.

There are three general parameters that a DRG requires: region for the linear sweep, step size, and step rate. In order to specify the region, two values must be chosen (Sweep 0 and Sweep 1 wherein each contains a different representation, depending on the mode; MHz for frequency, degree for phase, and a scalar value for amplitude) and it must be within the allowable range. Step size indicates the value that would be incremented while step rate determines the time interval/period for that increment (in µs).

To use the digital ramp generator (DRG) function of the AD9915, select the **Enable Digital Ramp Generator** checkbox. Under **Mode** section, select the parameter to be generated –frequency, phase, or amplitude. In the **Settings** section, The **Auto Clear Digital Ramp Accumulator** checkbox allows you to set the clear digital ramp accumulator bit when the I/O update signal is applied or when there is a profile change. The clear bit is then released.

The **Clear Digital Ramp Accumulator** checkbox allows you to set and keep the digital ramp accumulator cleared until that bit is cleared. The **Load DRR @I/O Update** checkbox allows you to reload the digital ramp rate when an I/O update is issued or when there is a profile change.

Sweep Frequency 0 and **Sweep Frequency 1** are the starting and stopping frequencies of the ramp, respectively. Note that this is frequency, phase, or amplitude depending on which ramp generator is selected. It is important that the value in the Sweep 0 register is always less than the value in the Sweep 1 register.

Use the **Rising Step Size** and **Falling Step Size** checkboxes to set the step size of the rising or falling ramp. The unit for these changes depending on what type of ramp is being generated.

The **Rising Sweep Ramp Rate** and **Falling Sweep Ramp Rate** are used to set the time between each rising or falling step on the ramp. This is in units of microseconds.

The **No Dwell High** and **No Dwell Low** boxes set the corresponding bit functions in the register map. Use the Up, Down, and Pause buttons at the bottom of the window to control the direction or to hold the ramp. The Ramp Finished indicator turns on when the ramp is complete.

PROGRAMMABLE MODULUS WINDOW

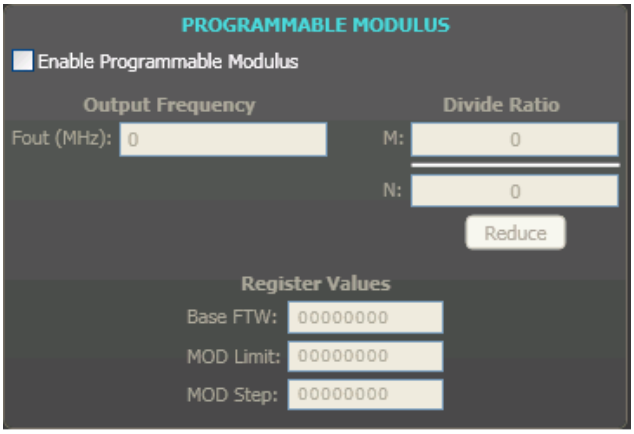


Figure 13. Programmable Modulus Window

The chip is in programmable modulus mode when the **Enable Programmable Modulus** check box is selected. The digital ramp generator mode will automatically be disabled.

The **Programmable Modulus** window is used to alter the frequency equation of the DDS core, making it possible to implement fractions that are not restricted to a power of 2 in the denominator.

When you enter the desired output frequency (in terms of MHz) in the **Fout** box, the values in the **Register Value**s boxes and the **Divide Ratio** boxes are automatically updated. You can also directly input a divide ratio, which in this case will automatically update the R**egister Values** boxes and **the Output Frequency** box.

DEBUG

To access the Debug window, select **Debug** from the tab selection.

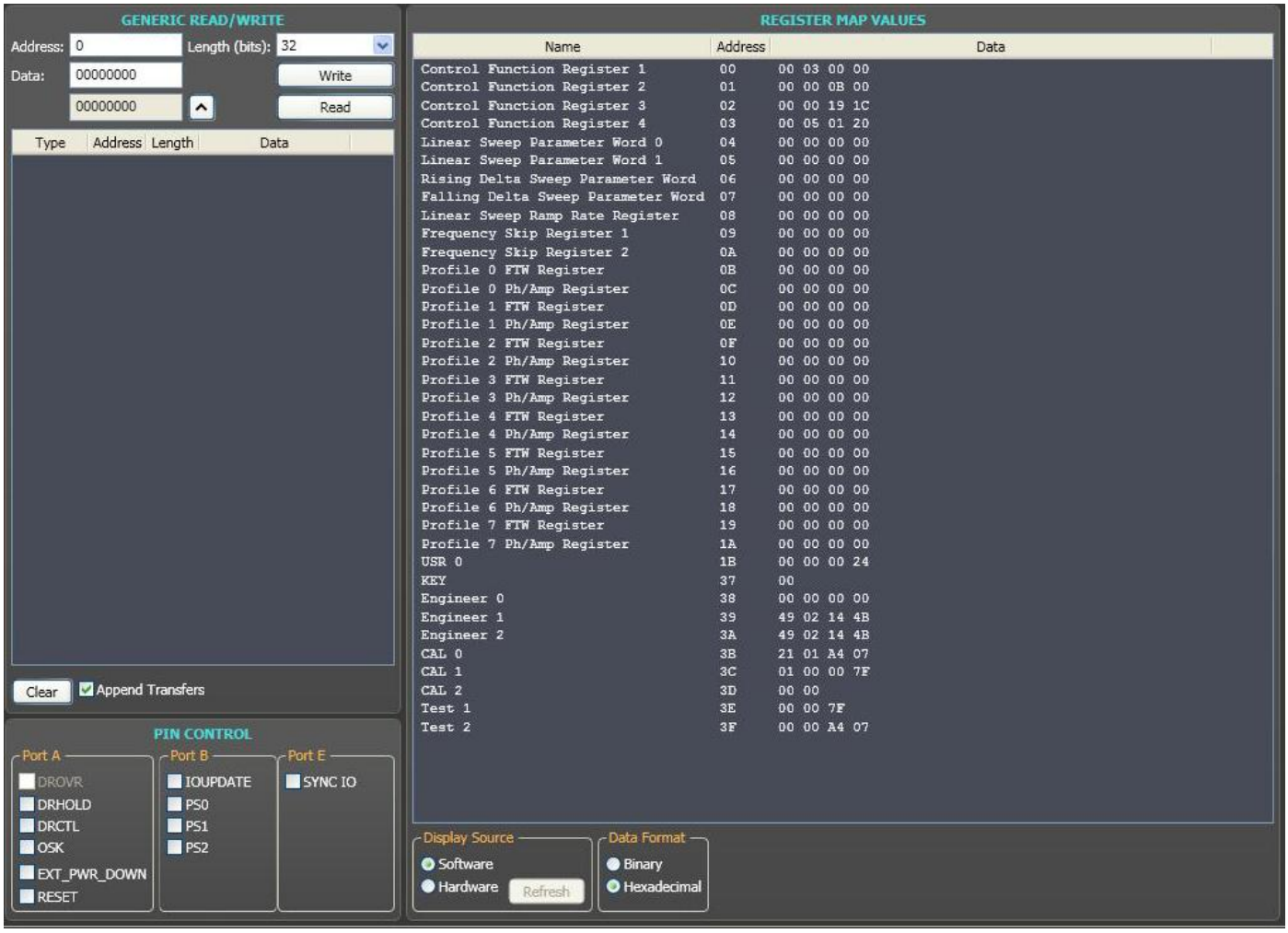


Figure 14. Debug Window

The Debug window gives you complete direct access to the register map as well as control of many external pins. The Debug window is intended for debugging issues with the AD9915. It can be used for all programming, but is not user-friendly; this may result in improper programming of reserved bits.

DROVR alerts when ramp generation is over. The ramp direction (rising or falling) is externally controlled by the **DRCTL**. Logic 0 causes the DRG to ramp with a negative slope, whereas logic 1 causes the DRG to ramp with a positive slope. **DRHOLD** allows the user to suspend the ramp generator in its present state. When this is set to logic 1, the DRG is stalled at its last state; otherwise, the DRG operates normally. **EXTAMPCTL** sets the OSK feature on either manual or automatic mode. **EXTPDCTL** is a flag input that would initiate the programmed power-down mode. **RESET** is the master reset that clears all memory elements and sets registers to default values.

IOUPDATE transfers the contents of the I/O buffers to the corresponding internal registers. **PS0**, **PS1**, and **PS2** control the profile register pins. See the AD9915 data sheet for the logic to control the profiles via the external pins.

SYNC IO controls the SYNCIO pin.This pin is used to reset the serial port.

The **REGISTER MAP** shows the values of all the registers in AD9915. Note that there are two sources (buffer) for the register map; software and hardware. Using the **Software** source allows to display the values that reflects the current user interface settings. On the other hand, the **Hardware** source displays the register values that are written to, or read from the part which requires a **Refresh**.

The **GENERIC READ/WRITE** provides the interface and controls for the REGISTER MAP. This can be done by specifying an instruction composed of the **Data**, the **Address**, the **Length (Bits)**, and the **Type of Instruction (Read/Write)**. The order of the instructions can be seen from the small window which is on the left side of the REGISTER MAP. This only happens when the **Append Transfers** option is enabled. In addition, the current display of the GENERIC READ/WRITE window can be cleared by the **Clear** button.