ANALOG DEVICES

HSI TECHNICAL NOTE

EVALZ-ADN2871/ADN2873 APPLICATION NOTE

Introduction:

This technical note describes 24-Lead ADN2871/ADN2873 laser diode driver evaluation kit. The evaluation kit provides an AC-coupled, differential optical evaluation platform for the device ADN2871/ADN2873, called device under test (DUT) below. The evaluation kit supports two DUT operation modes to set laser optical average power (Pav) and extinction ratio(ER) outputs: Voltage setting mode and Resistor Setting mode. The voltage settings mode uses a micro-converter's DAC voltage outputs to DUT pin PAVREF and ERREF. The resistor setting mode uses potentiometers connected to DUT pin PAVSET and ERSET, respectively.

This document describes how to configure the evaluation kit to either voltage or resistor setting mode to correctly set the DUT optical average power and extinction ratio driving capabilities. The document contains:

1. Board Description
2. Capacitor Selection
3. Quick Start Operation using Voltage setpoint Calibration
4. Quick Start Operation using Resistor setpoint Calibration
5. Description of board settings
6. BOM and Schematic of board
7. Laser to PCB footprints
8. Discussions

Board Description:

The EVALZ-ADN2871/ADN2873 board provides on-board configurable jumpers to setup the DUT in either voltage or resistor setting mode. The board is convenient to evaluate the DUT optical performance worked with various differential TOSA lasers, and to optimize, debug, and confirm new optical transmitter design.

The DUT is a 3.3V, APC (average power control) single loop capable, laser diode driver device, available for data rate support from 50Mbps up to 4.25Gbps. To evaluate the DUT performance, a suitable coax laser diode must be soldered onto the evaluation board. A photo-current, produced from the laser companion monitor photo diode, MPD, is fed into the DUT to close the APC loop. This board is configured for differential ended coaxial lasers only. LEDs on board present the DUT power supply, and FAIL alarm status.

Capacitor Selection

The EVALZ-ADN2871/ADN2873 needs only one high isolation impedance capacitor: PAVCAP for the stable APC loop control. The bandwidth of APC control loop is centered between a maximum bandwidth to avoid data dependency and loop instability, and a minimum bandwidth to ensure compliance to SFP start up time. The following equations can be used to determine the nominal values of the average power loop capacitor (PAVCAP) for a design based on the laser slope efficiency and the required average output power. There is a +/-15% tolerance allowed for the capacitors value calculated.

VOLTAGE SETPOINT CALIBRATION:
At the voltage setting calibration mode, The PAVCAP should be:

$$Pavcap = \frac{1.28 \times 10^{-6} \times LI}{Pav} \text{ (F)}$$

RESISTOR SETPOINT CALIBRATION:
At the resistor setting calibration mode, The PAVCAP should be:

$$Pavcap = \frac{3.2 \times 10^{-6} \times LI}{Pav} \text{ (F)}$$

where: LI (mW/mA) is the typical laser slope efficiency at 25 Degrees Celsius.
PAV is the average power (mW) required.

For example, if a designed transmitter needs optical average power output of -4dBm, the selected laser has about typical 0.07mW/mA slope efficiency, the calculated Pavcap in
Voltage Setting Mode: Pavcap = 225nF
Resistor Setting Mode: Pavcap = 560nF

Quick start for voltage setpoint calibration of Pav:

In Voltage setpoint calibration, the evaluation board offers two different methods of providing the controlled reference voltages to DUT pin PAVREF and ERREF. The ADN2871/ADN2873 evaluation board has on board voltage regulators and potentiometers that allow the user to adjust the reference voltages to DUT pin PAVREF and ERREF that set the average power and extinction ratio. Alternatively the user can provide two external reference voltages to DUT pin PAVREF and ERREF.

Voltage Setting Method 1:

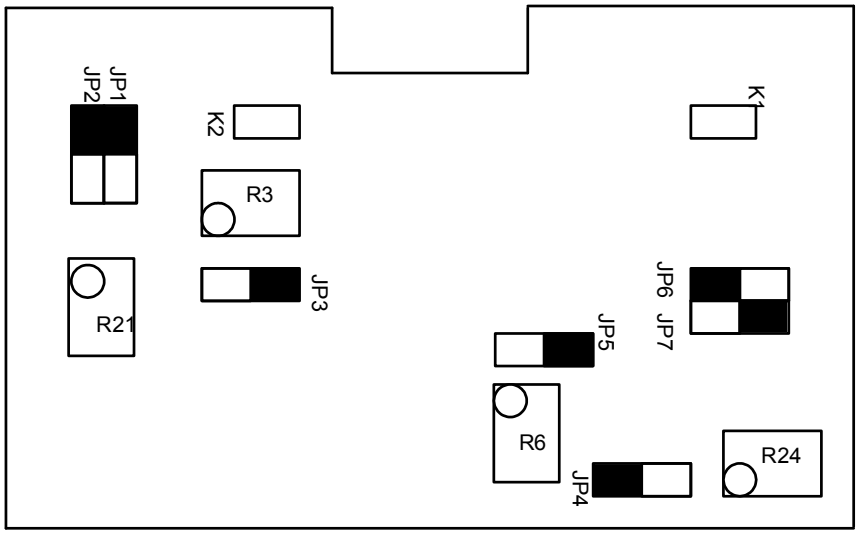


Figure 1. Jumper settings for voltage setpoint calibration using external DAC reference voltages to DUT pin PAVREF and ERREF.

To operate an EVALZ-ADN2871 in Voltage Setting mode using external DACs input, verify the following:

1. Remove jumper K2 and connect jumpers JP1, JP2, JP3, JP5 to JP6 to position A (connected as shown in black box), JP4 and JP7 to position B as shown in figure 1.
2. The power supply is diode protected to ensure the DUT safety if a negative power supply is accidentally connected. The user may connect Jumper K1 (short circuit) and power up the board by applying +3.3V to the POWER input SMA, J1. If Jumper K1 is not connected then the user should supply the sufficiently +3.3V to jumper K1, on the head connected to pin R1 and C2. The actual DUT supply voltage can be confirmed at the anode of D1.
3. Connect external power supplies, PAVREF and ERREF reference voltages to J2 and J3. Adjust both external supply reference voltages to 0.1volt.
4. Apply a differential signal, typically 500mV p-p, to J4 and J5 (DATAN and DATAP). Single ended operation may result in a degraded eye.
5. The optical eye and switching characteristics of the DUT may be observed using a digital communications analyzer which has an optical input channel with the required bandwidth.
6. The bias and modulation currents can also be monitored by observing Ibmon and Immon respectively. Ibmon is a 1:100 ratio of Ibias and Immon is a 1:50 ratio of Imod. Both are terminated with resistors and so can be viewed at test points TP2 and TP1 using a voltmeter or oscilloscope.
7. To establish the desired optical average power and extinction ratio the user should do:
   - Turn on the power supply to the evaluation board, and hook up a differential data signal,
   - Slowly increase the external voltage supplied to pin PAVREF to establish the desired average optical power.
   - After satisfy the initial average optical power output, slowly increase the external voltage supplied to pin ERREF to increase the extinction ratio. The bias current will decrease as the modulation current increases. The bias and modulation currents can be monitored using Ibmon and Immon (through test points TP2 and TP1).

When adjusting the extinction ratio the user should allow adequate time for the eye to settle. The range of allowable voltage supplied to DUT pin (PAVREF) for average power is 0.1volt to 1.0volt and the allowable voltage range supplied to input (ERREF) for at extinction ratio is between 0.1volt and 1.0 volt.

Voltage Setting Method 2:

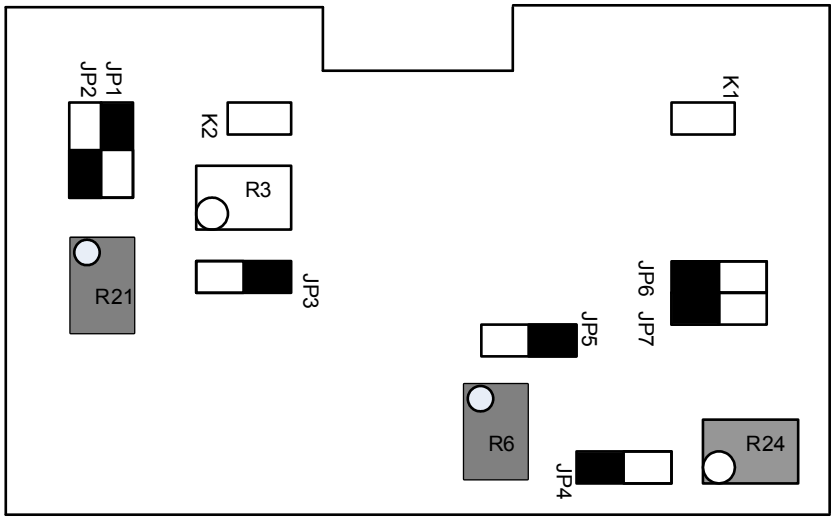


Figure 2. Jumper settings for voltage setpoint calibration using on board regulator voltages for PAVREF and ERREF.

To operate the evaluation board using voltage setpoint calibration using on board regulators for PAVREF and ERREF, verify the following:

1. On the evaluation board remove jumper K2 and connect jumpers JP2 and JP4 to position B and connect jumpers JP1 (connected as shown in black box), JP3, JP5, JP6 and JP7 to position A as shown in figure 2.
2. With the power supply turned off adjust potentiometer R6 (ERSET) to approx zero ohms.
3. With the power supply turned off adjust potentiometers R21 and R24 (shown in grey) to approx 25K ohms.
4. The power supply is diode protected to ensure the DUT safety if a negative power supply is accidentally connected. The user may connect Jumper K1 (short circuit) and power up the board by applying +3.3V to the POWER input SMA, J1. If Jumper K1 is not connected then the user should supply the sufficiently +3.3V to jumper K1, on the head connected to pin R1 and C2. The actual DUT supply voltage can be measured at the anode of D1.
5. Apply a differential signal, typically 500mVp-p, to J4 and J5 (DATAN and DATAP). Single ended operation may result in a degraded eye
6. The optical eye and switching characteristics of the DUT may be observed using a digital communications analyzer which has an optical input channel with the required bandwidth.
7. The bias and modulation currents can also be monitored by observing Ibmon and Immon respectively. Ibmon is a 1:100 ratio of Ibias and Immon is a 1:50 ratio of Imod. Both are terminated with resistors and so can be viewed at test points TP2 and TP1 using a voltmeter or oscilloscope.
8. To establish the desired average power and extinction ratio the user should follow the below procedure:

   - Power up the evaluation board and hook up a switching data signal, reduce the value of potentiometer R21 to establish the desired average optical power.
   - Reduce the value of potentiometer R24 to increase the modulation current, and hence increase the extinction ratio. The bias current will decrease as the modulation current increases. Monitor the bias and modulation currents by using Ibmon and Immon (through test points of TP2 and TP1).

When adjusting the extinction ratio the user should allow adequate time for the eye to settle. The range of allowable voltage supplied to DUT pin (PAVREF) for average power is 0.1volt to 1.0volt and the allowable voltage range supplied to input (ERREF) for at extinction ratio is between 0.1volt and 1.0 volt.

Quick start for Resistor Setting Mode of average power Pav:

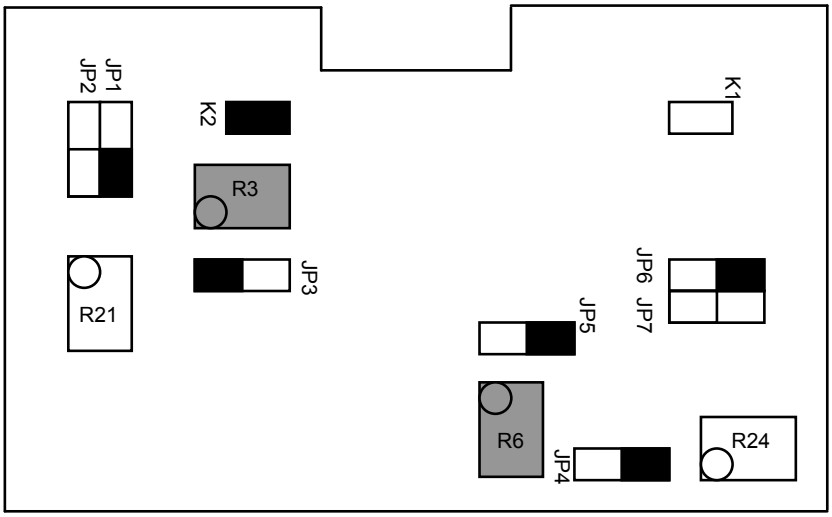


Figure 3. Jumper settings for resistor setpoint calibration using potentiometers connected to the PAVSET and ERSET pins.

To operate the evaluation board in resistor setpoint calibration using potentiometers at the PAVSET and ERSET pins, verify the following:

1. Connect Jumper K2, connect jumpers JP1,JP3 and JP6 to position B (connected as shown in black box) and connect jumpers JP4 and JP5 to position A as shown in figure 3.
2. The power supply is diode protected to ensure the DUT safety if a negative power supply is accidentally connected. The user may connect Jumper K1 (short circuit) and power up the board by applying +3.3V to the POWER input SMA, J1. If Jumper K1 is not connected then a +3.3V should be supplied to jumper K1, on the head connected to pin R1 and C2. The actual DUT supply voltage can be measured at the anode of D1.
3. Apply a differential signal, typically 500mVp-p, to J4 and J5 (DATAN and DATAP). Single ended operation may result in a degraded eye.
4. The optical eye and switching characteristics of the ADN2870 may be observed using a digital communications analyser which has an optical input channel with the required bandwidth.
5. The bias and modulation currents can also be monitored by observing Ibmon and Immon respectively. Ibmon is a 1:100 ratio of Ibias and Immon is a 1:50 ratio of Imod. Both are terminated with resistors and so can be viewed at test points TP2 and TP1 using a voltmeter or oscilloscope.
6. To establish the desired average power and extinction ratio, user should follow the procedure:
   - turn off the power supply, adjust potentiometers R3 (PAVSET) and R6 (ERSET) (shown in grey) to approximately 20k.
   - turn on the board power supply and the data signal switching, reduce the value of potentiometer R3 to establish the desired average optical power.
   - after get satisfied Pav, reduce potentiometer R6 value to increase the modulation current, and Hence to increase the extinction ratio. The bias current will decrease as the modulation current increases. The bias and modulation currents are available from monitoring IBMON and IMMON.

When adjusting the extinction ratio the user should allow adequate time for the eye to settle. The allowable resistance range at the Power Set Input (PAVSET) and the allowable resistance at the Extinction Ratio Set

Input (ERSET) is between 1Kohm and 20K ohm. Resistors R4 and R7 ensure that the resistance at these nodes never falls below the minimum allowable value. If the node resistances increase above 25Kohm the DUT may not operate within its specifications.

With a known laser diode, there is a quick way to get Rpavset and Rerset values:
Assume the known laser diode a has a typical slope efficiency = 0.07mW/mA, the typical threshold current is about 10mA, the companion MPD responsivity = 0.85mA/mW, and requested average optical power is about 0.4mW, ER = 5dB.

$$Rpavset = \frac{1.23}{Pav \times \mathrm{Re}} = \frac{1.23}{0.4 \times 0.85} = 3.61 \text{(kohm)}$$

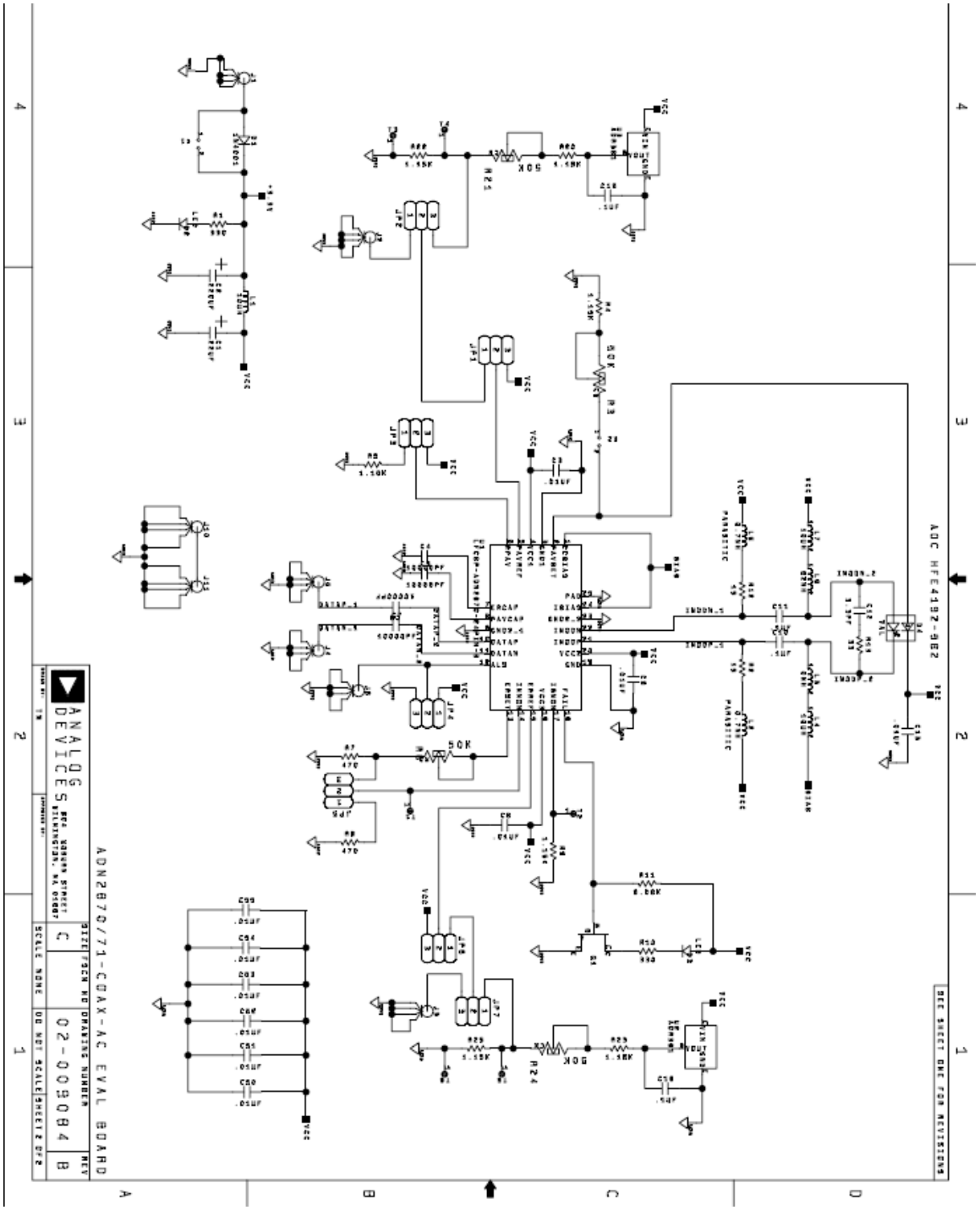
$$\mathrm{Re}rset = \frac{1.23 \times 40}{I_{MOD}} = \frac{1.23 \times 40}{5.91} = 8.325 \text{ (kohm)}$$

The above Rpavset and Rerset resistance values could be a good start to get the fine tuned optical performance in resistor setting mode.

Description of Board Settings:

COMPONENT	NAME	FUNCTION
J1	POWER	+3.3V power input to board
J2	PAVREF	PAVREF external reference input
J3	ERREF	ERREF external reference input
J4	DATAN	Data N input
J5	DATAP	Data P input
J6	ALS	ALS external input
TP1	IMMON	Imod Current Mirror Monitor
TP2	IBMON	Ibias Current Mirror Monitor
TP3/TP4	PAVREFmon	PAVREF reference voltage
TP5/TP6	ERREFmon	ERREF reference voltage
R3	PAVSET	POTENTIOMETER Adjusts bias current (in Resistor set mode)
R6	ERSET	POTENTIOMETER Adjusts mod current (in Resistor set mode)
R21	PAVREF	POTENTIOMETER Adjusts bias current (in Voltage set mode)
R24	ERREF	POTENTIOMETER Adjusts mod current (in Voltage set mode)
K1	K1	Jumper to bypass supply protection diode
K2	K2	Jumper for PAVSET (in Resistor set mode)
JP1	JP1	Jumper to select voltage or resistor mode for PAVREF
JP2	JP2	Jumper to select onboard or external ref for PAVREF
JP3	JP3	Jumper to select voltage/resistor mode for RPAV
JP4	JP4	Jumper to select external input for ALS
JP5	JP5	Jumper to select Immon
JP6	JP6	Jumper to select voltage/resistor mode for ERREF
JP7	JP7	Jumper to select onboard or external ref for ERREF

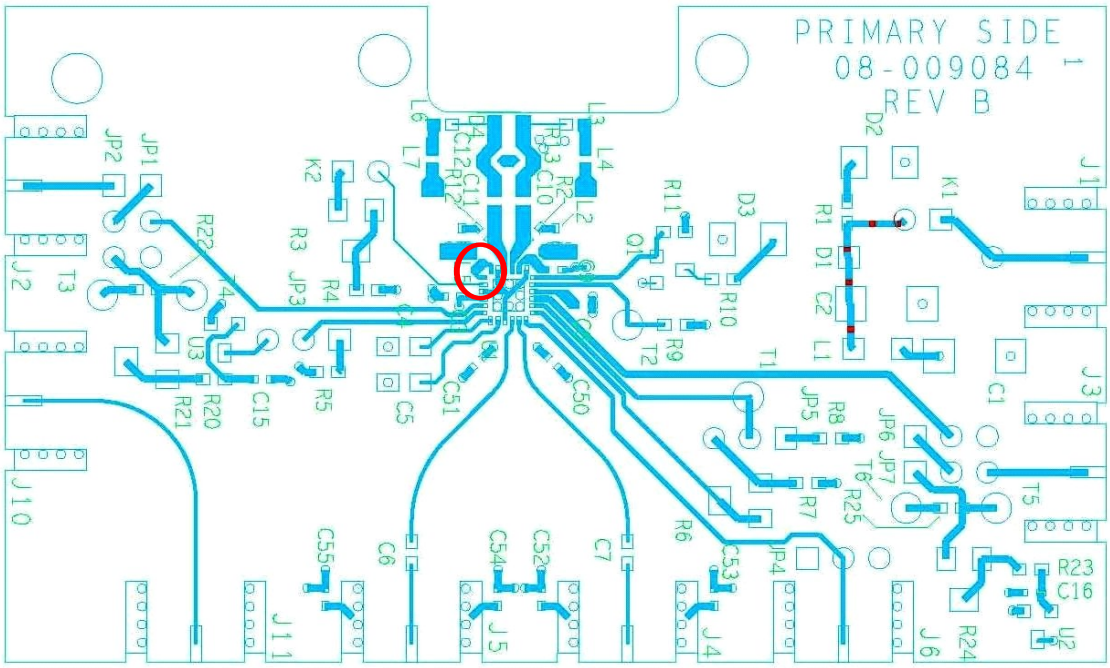
EVALZ-ADN2871/ADN2873 Schematic



EVALZ-ADN2871/ADN2873 Bill of Materials

Part No.	Device number	Quantity	Value	Package
AD381(A)	ADR381*	2		SOT23
C1	CAP+	1	22UF	TYPE "C" Case
C2	CAP+	1	220UF	TYPE "C" Case
C3, C8, C9, C13	CAP	4	10NF	201A
C4*	CAP		Not populated*	805
C5	CAP	1	560NF	805
C6, C7	CAP	2	10NF	603
C15, C16, C11, C10	CAP	4	100NF	402
C50, C51, C52, C53, C54, C55	CAP	6	10NF	402
C12	CAP	1	3.3PF	402
D1	Diode	1	1N4001	Not populated
D2	LED	1		LED_SMT
D3	LED	1		LED_SMT
J1, J2, J3, J4, J5, J6	SMA	6		SMA CONNECTOR
J10, J11	SMA		Not populated*	SMA CONNECTOR
JP1, JP2, JP3, JP4, JP5, JP6, JP7	JUMPER2\SIP3	7		LINK-3P
K1, K2	JUMPER	2		SIP-2P
L1	IND	1	10uH	1206
L2, L5	IND	2	0.6nH*	402
L3	IND	1	0nH	402
L4, L7	IND	2	10uH	603
L6	IND	1	82nH	603
Q1	FET	1		SOT23
R1	RES		330R	603
R2, R12	RES	2	15R	201
R3, R6, R21, R24	VRES	4	50K	SMD POT VRES_SMD
R4, R5, R9, R22, R25	RES	5	1K	603
R13	RES	1	30	603
R7, R8	RES	2	470	603
R10	RES	1	330R	603
R11	RES	1	9K1*	603
R20, R23	RES	2	1.1K	603
T1 - T6	TESTPOINT	6		TESTPOINT
U1	LFCSP-ADN2873ACPZ			LFCSP-ADN2873-24PIN-B
D4	HSN_COAX_LASER_TYPEC		Not Populated*	HSN_COAX_LASER_TYPEC

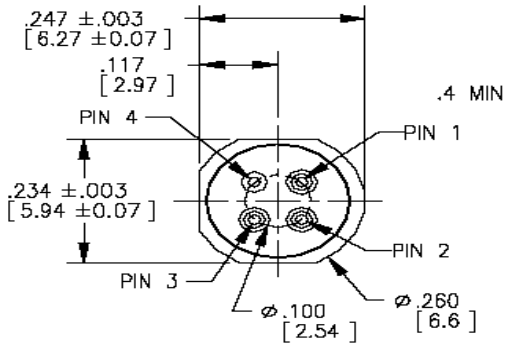
EVALZ-ADN2871/ADN2873 top layer Layout



In the latest revision D, the PCB offers one option to cut off the BIAS and CCBIS pin connection. At the Red circled place, one 402 surface mount pad designed in between the pins BIAS and CCBIS. If populated DUT is ADN2871, an 0 ohm resistor is needed to connect BIAS and CCBIAS pins. If the DUT is ADN2873, leave this component pad OPEN, and the pad offers test points for BIAS and CCBIAS pins, respectively.

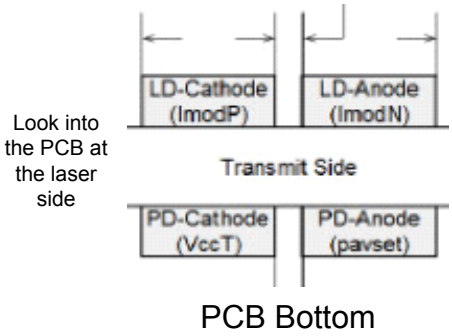
Laser and EVALZ-ADN2871/ADN2873 footprints

The EVALZ-ADN2871/ADN2873 board supports differential ended coaxial lasers only. The compliant laser footprint should be like:



1	VCSEL Anode
2	VCSEL Cathode
3	Monitor Diode Cathode
4	Monitor Diode Anode (Case)

On the EVALZ-ADN2871/ADN2873 board, the differential laser footprints are:



As a default setting of the EVALZ-ADN2871/ADN2873 board, the laser diode driver (DUT) to a laser diode (LD) interface circuit been optimized to work with a VCSEL TOSA: HFE4192-582.

When use this EVALZ-ADN2871/ADN2873 board to evaluate other differential lasers LDs, one optimization work is necessary on the circuitry between the DUT to the LD. Please contact ADI sales for the necessary technical support.

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