



Issue #1 (1/6)

Environment Setting

- 1. SG1 : set to 1.0dBm CW@153.6MHz and connect to “REF_IN” port.**
 - at “REF_IN” port is ~0dBm@153.6MHz.
- 2. SG2 : set to 1.2dBm CW@1700MHz and connect to “RF0” port.**
 - at “RF0” port is ~0dBm@1700MHz.
- 3. Oscilloscope : port impedance set to 1Mohm.**
- 4. Evaluation Board : modify to differential IQ mode.**
 - remove R35-R38, R39-R46, R51-R52 and T5-T6.
 - add 0R to R35-R38, R47-R50 and R67-R68.



Issue #1 (2/6)

Operating Procedure

1. Turn on DC power.
2. Open control software (ADRF6820 Customer Evaluation Software).
3. Turn on SG1.
4. SW set LO frequency to 1890. (see page 3)
5. Turn on SG2.
6. Read register data. (see page 4)

Issue #1 (3/6)

Control Software Setting

ADRF6820 Customer Evaluation Software rev 0.0.0

ADRF6820 Engineering

ILO 0 QLO 0
POLI Normal POLQ Normal
DCOFFI 0 DCOFFQ 0
IP2CRTI 0 IP2CRTQ 0

BWSEL 3 BB_BIAS 10 mA

BWSEL	Gain	BW
0	High	High
1	High	Low
2	Low	High
3	Low	Low

Mixer MIX_BIAS 4 MIX_RDAC 8 MIX_CDAC 1

RFIN0 RFIN1
RFSW_MUX Pin CTRL
RFSW_SEL RFIN0

BAL_CIN 0 BAL_COUT 0
RFDSA 0 dB

PLL Reference Input
PLL REF IN (MHz) 153.6
PLL REF DIVIDER DIV4

REFIN REF_MUX_SEL Lock_det

Charge Pump
CSCALE 500 uA
BLEED up 93.75 u
ABLDLY 0 nsec
CPCTRL PFD
CLKEDGE Div 1, Ref 1

38.4 PFD FREQ (MHz)

DIV_NGDIV FRAC
INT 49
FRAC 336
MOD 1536

DITH_EN Enable
DITH_MAG 3
DITH_VAL 0

VCO_SEL 3.5 - 4.02 GHz
VCO Freq (MHz) 3780

LO Freq (MHz) 1890
FREQ (MHz) 1890
STEP SIZE (kHz) 25
STEP SIZE MULT 1

Register Write Log
0x05:0x0000
0x01:0xfe7f
0x01:0xfe7f
0x05:0x0000
0x05:0x0000
0x05:0x0000
0x05:0x0000
0x05:0x0000
0x20:0x0026
0x20:0x0c26
0x05:0x0000
0x05:0x0000
0x21:0x0003
0x22:0x0002

Green box, enter value
Yellow box, read only

Update GUI
Save Register File
Open Register File

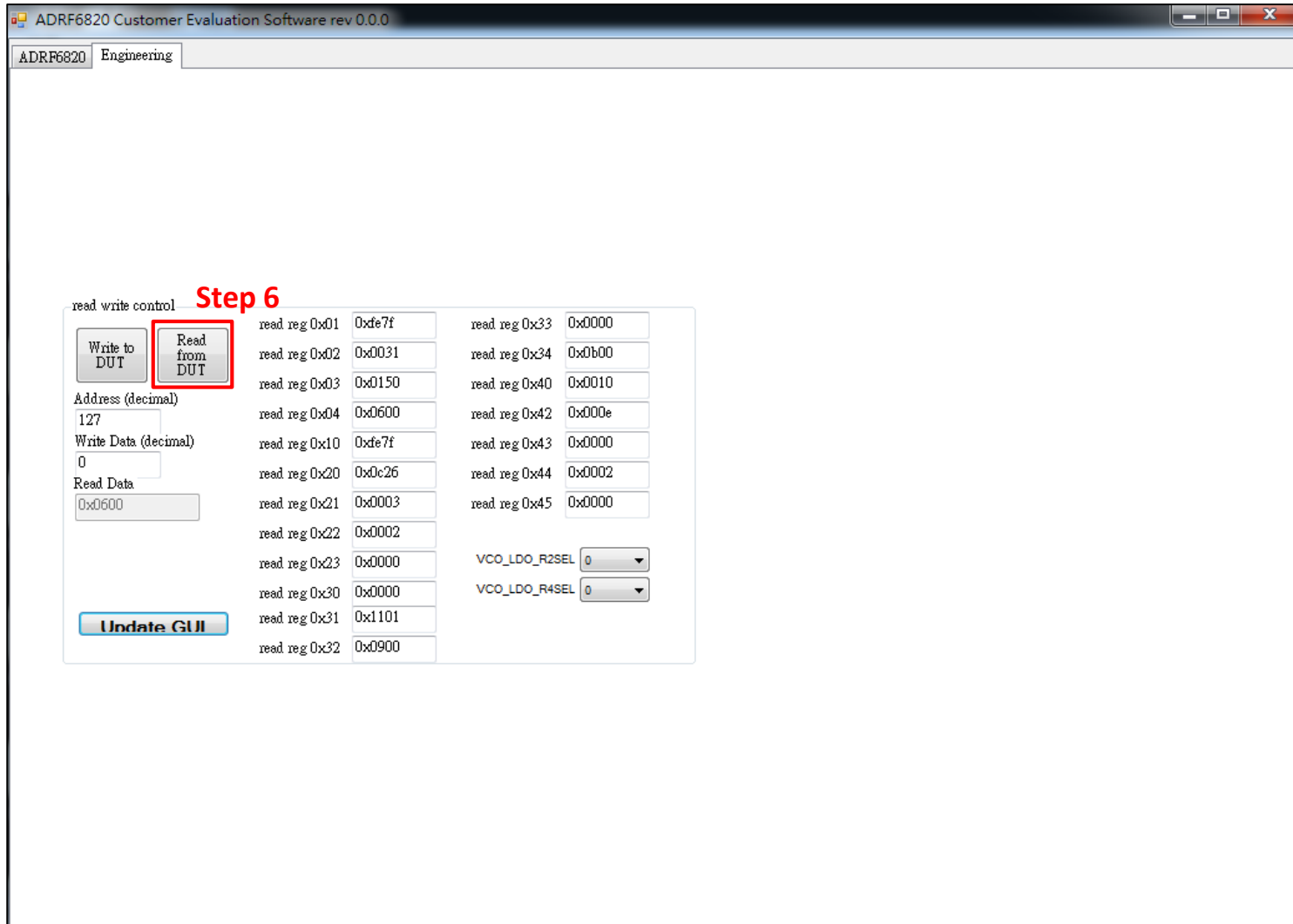
USB Connection
FX2 USB device found, con
hex file successfully loaded

Enable All Disable All Software Reset

PWR_DWN Pin CTRL
VCO_LDO VCO LO_DRV1X
Charge Pump VCO LO_DRV2X
DIV VCO QUAD_DIV
VCO DMOD
REF_BUF REF_BUF

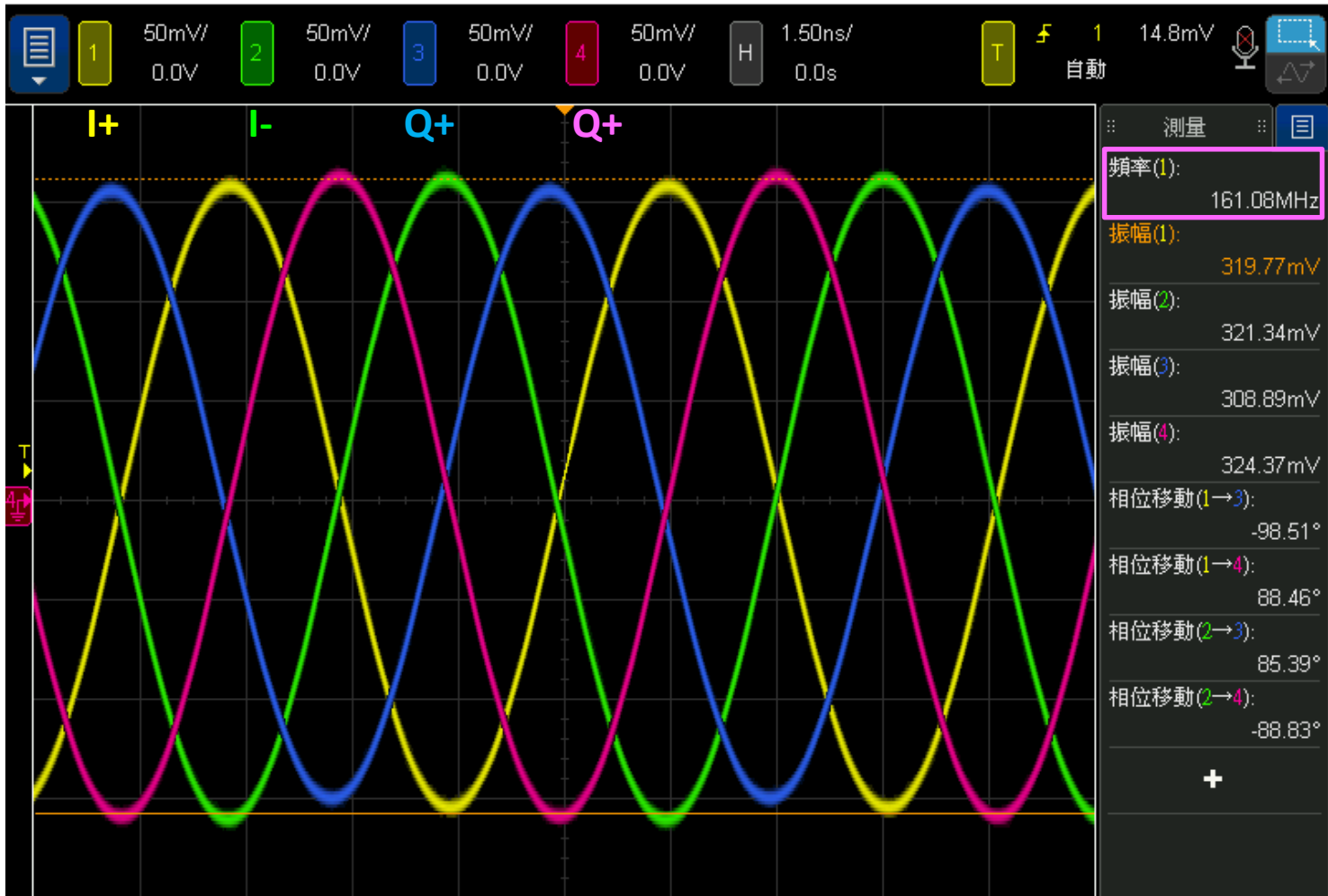
Issue #1 (4/6)

Read Register



Issue #1 (5/6)

IQ Plot





Issue #1 (6/6)

Issue

1. When switch “PWRDWN” to “high” or “low”, ADRF6820 is always working.
Why??
2. Why IQ frequency is ~160MHz?? (RF is 1700MHz, LO is 1890MHz)



Issue #2 (1/6)

Environment Setting

- 1. SG1 : set to 1.25dBm CW@1890MHz and connect to “LO_IP” port.**
 - at “LO_IP” port is ~0dBm@1890MHz.
- 2. SG2 : set to 1.2dBm CW@1700MHz and connect to “RF0” port.**
 - at “RF0” port is ~0dBm@1700MHz.
- 3. Oscilloscope : port impedance set to 1Mohm.**
- 4. Evaluation Board : modify to differential IQ mode.**
 - remove R35-R38, R39-R46, R51-R52 and T5-T6.
 - add 0R to R35-R38, R47-R50 and R67-R68.



Issue #2 (2/6)

Operating Procedure

1. Turn on DC power.
2. Open control software (ADRF6820 Customer Evaluation Software).
3. Turn on SG1.
4. SW set to “EXT VCO/LO”, “Polyphase Filter” and “BWSEL 0” (see page 9).
5. Turn on SG2.
6. Read register data. (see page 10)

Issue #2 (3/6)

Control Software Setting

ADRF6820 Customer Evaluation Software rev 0.0.0

Engineering

ILO 0 QLO 0
POLI Normal POLQ Normal
DCOFFI 0 DCOFFQ 0
IP2CRTI 0 IP2CRTq 0

BWSEL 0 **Step 4**
BB_BIAS 10 mA

BWSEL	Gain	BW
0	High	High
1	High	Low
2	Low	High
3	Low	Low

RFIN0 RFIN1
RFSW_MUX Pin CTRL
RFSW_SEL RFIN0

BAL_CIN BAL_COUT
RFDSA 0 dB

Mixer
MIX_BIAS 4
MIX_RDAC 8
MIX_CDAC 1

QUAD_DIV_EN
Polyphase Filter F **Step 4**
Polyphase Filter
LO_OUTPUT Disable Output
LO_DRV_LVL 0

LO Freq (MHz)
FREQ (MHz) 2000
STEP SIZE (kHz) 25
STEP SIZE MULT 1
INC DEC

PLL Reference Input
PLL REF IN (MHz) 153.6
PLL REF DIVIDER DIV4

REFIN
REF_MUX_SEL Lock_det

Charge Pump
CSCALE 500 uA
BLEED up 93.75 u
ABLDLY 0 nsec
CPCTRL PFD
CLKEDGE Div \, Ref \ CP

38.4
PFD FREQ (MHz)

EXT VCO/LO **Step 4**
VCO_SEL
VCO Freq (MHz) 4000

DRVDIV2_EN
Div 2 Phase Splitter

DIV_NGDIV FRAC
INT 52
FRAC 128
MOD 1536

DITH_EN Enable
DITH_MAG 3
DITH_VAL 0

Lock_det
Vpstat
Scan

USB Connection
FX2 USB device found, com
hex file successfully loaded

Enable All Disable All Software Reset

VCC_PLL_EN VCO_LDO_EN DIV_EN CP_EN VCO_EN REF_BUF_EN DMOD_EN

PWR_DWN Pin CTRL
VCO_LDO Charge Pump DIV VCO REF_BUF LO_DRV1X LO_DRV2X QUAD_DIV DMOD

Register Write Log
0x05:0x0000
0x01:0xfe7f
0x01:0xfe7f
0x05:0x0000
0x05:0x0000
0x05:0x0000
0x05:0x0000
0x20:0x0026
0x20:0xc26
0x05:0x0000
0x05:0x0000
0x21:0x0003
0x22:0x0002
Clear

Green box, enter value
Yellow box, read only

Update GUI
Save Register File
Open Register File

Issue #2 (4/6)

Read Register

ADRF6820 Engineering

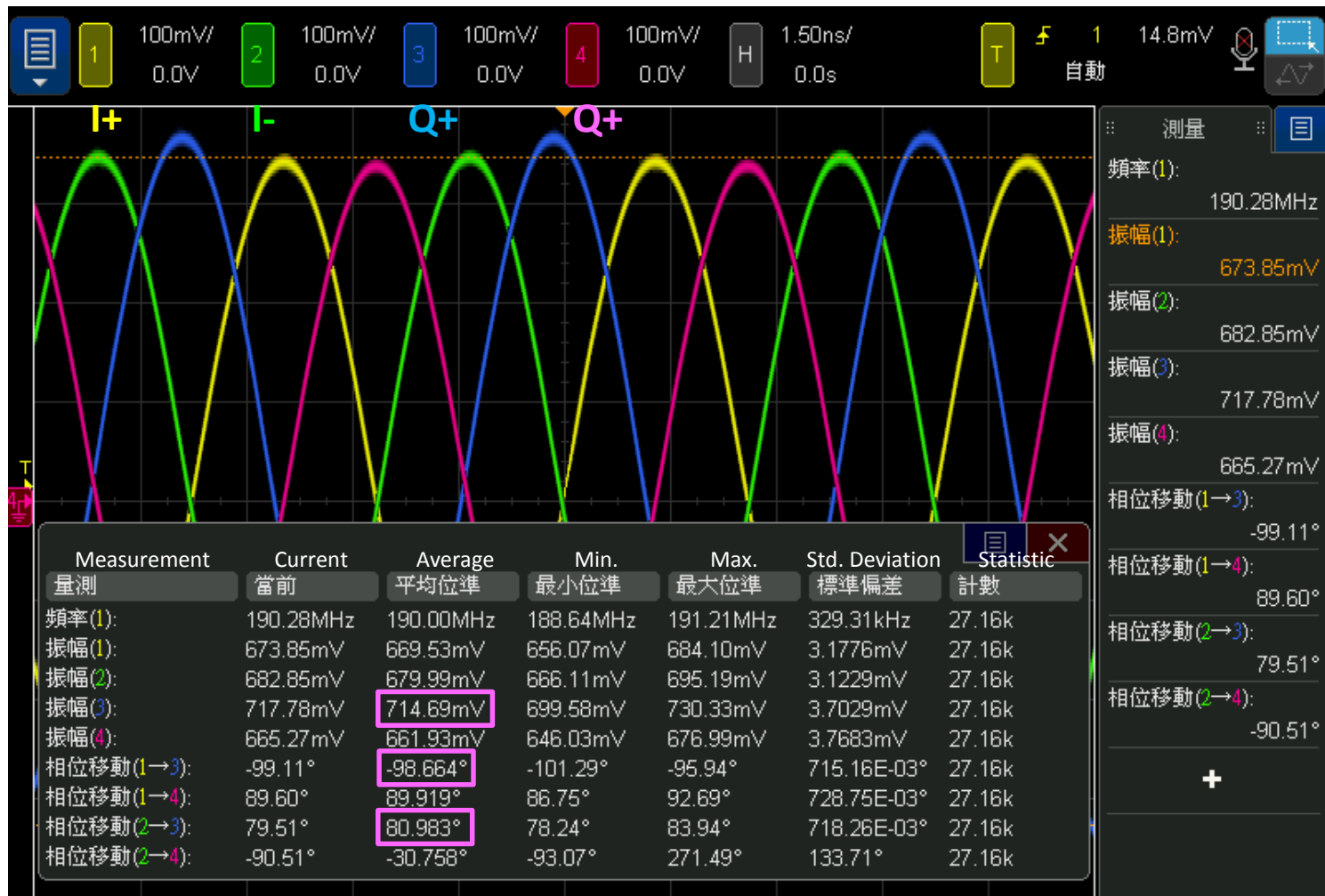
read write control **Step 6**

Write to DUT	Read from DUT	read reg 0x01	0xfc7f	read reg 0x33	0x0000
		read reg 0x02	0x0034	read reg 0x34	0x0800
		read reg 0x03	0x0080	read reg 0x40	0x0010
		read reg 0x04	0x0600	read reg 0x42	0x000e
Address (decimal)		read reg 0x10	0xfc7f	read reg 0x43	0x0000
127		read reg 0x20	0x0c26	read reg 0x44	0x0002
Write Data (decimal)		read reg 0x21	0x0003	read reg 0x45	0x0000
0		read reg 0x22	0x0004		
Read Data		read reg 0x23	0x0000	VCO_LDO_R2SEL	0
0		read reg 0x30	0x0000	VCO_LDO_R4SEL	0
		read reg 0x31	0x1101		
		read reg 0x32	0x0900		

Update GUI

Issue #2 (5/6)

IQ Plot





Issue #2 (6/6)

Issue

- 1. The amplitude of Q+ is much bigger than others, is it reasonable??**
- 2. The phase of Q+ is much bigger than others, is it reasonable???**
 - I+ to Q- and I- to Q- are both ~ 90 degree. So, the deviation comes from Q+.**
- 3. The differential IQ Vpp is ~ 670 mV, is it reasonable (RF_IN is ~ 0 dBm and BWSEL is "0")?? Has any formula to calculate the RF input power vs. differential IQ Vpp??**