ADV7182

Script Update Document

Changeover from Revision 4.6 to Revision 5.0 of the ADV7182 Recommended Scripts

December 2014

TABLE OF CONTENTS

INTRODUCTION

This document describes changes between revision 4.6 and revision 5.0 of the ADV7182 recommended scripts. Revision 4.6 of the recommended scripts are described in Revision B of the Recommended Settings Document (RSD). Revision 5.0 of the recommended scripts are described in Revision C of the Recommended Settings Document (RSD).

LEGAL TERMS AND CONDITIONS

REVISION HISTORY

12/14—Revision 0: Initial Version

1 SINGLE ENDED CVBS

Script Revision 4.6		Script Changes	Script Revision 5.0	
I2C Write	**Comment**		**I2C Write**	**Comment**
	Hardware reset implied	**New Write ->**	42 0F 80	Reset ADV7182
delay 10	Wait 10 ms	**Same**	delay 10	Wait 10 ms
42 0F 00	Exit Power Down Mode	**Same**	42 0F 00	Exit Power Down Mode
		Position of Write Changed ->	42 52 CD	SE_CVBS AFE IBIAS
42 00 00	CVBS in on Ain 1	**Same**	42 00 00	CVBS in on AIN1
42 0E 80	ADI Required Write	**Same**	42 0E 80	ADI Required Write
42 9C 00	Reset Coarse Clamp Circuitry [step1]	**Same**	42 9C 00	Reset Coarse Clamp Circuitry [step1]
42 9C FF	Reset Coarse Clamp Circuitry [step2]	**Same**	42 9C FF	Reset Coarse Clamp Circuitry [step2]
42 0E 00	Enter User Sub Map	**Same**	42 0E 00	Enter User Sub Map
		Position of Write Changed ->	42 17 41	Select SH1 chroma shaping filter
42 03 0C	Enable Pixel & Sync output drivers	**Same**	42 03 0C	Enable Pixel & Sync output drivers
42 04 07	Power-up INTRQ, HS & VS pads	**Same**	42 04 07	Power-up INTRQ, HS & VS pads
42 13 00	Enable INTRQ output driver [1]	**Same**	42 13 00	Enable ADV7182 for 28.63636MHz crystal [1]
42 17 41	Select SH1 chroma shaping filter	**-> Position of Write Changed**		
42 1D 40	Enable LLC output driver	**Same**	42 1D 40	Enable LLC output driver
42 52 CD	ADI Required Writes [IBIAS]	**-> Position of Write Changed**		

Changes to single ended CVBS script:

- Software reset was inserted at the start of the script. This was done to explicitly state that a reset is needed when switching from one input format to another (e.g. switching from differential CVBS to single ended CVBS).
- The bias current setting for the analog front end (AFE) was moved to the first write after exiting power down mode. This was done to optimize the performance of the ADV7182.
- The write to select the SH1 chroma shaping filter was moved up above the write to enable the pixel and synchronization pin output drivers. This was done to optimize the performance of the ADV7182.

[1] The comment in relation to the write 42 13 00, was changed from 'Enable INTRQ output driver' to 'Enable ADV7182 for 28.63636MHz crystal'. This was done in order to explain more accurately the operation of this write.

2 DIFFERENTIAL CVBS

Script Revision 4.6		Script Changes	Script Revision 5.0	
I2C Write	Comment		I2C Write	Comment
	Hardware reset implied	New Write ->	42 0F 80	Reset ADV7182
delay 10	Wait 10 ms	Same	delay 10	Wait 10 ms
42 0F 00	Exit Power Down Mode	Same	42 0F 00	Exit Power Down Mode
		Position of Write Changed ->	42 52 C0	Diff_CVBS AFE IBIAS
		New Write ->	42 00 10	INSEL =unconnected input [INSEL Switch]
42 00 0E	INSEL = CVBS_P in on Ain 1, CVBS_N in on Ain2	Same	42 00 0E	INSEL = CVBS_P in on Ain 1, CVBS_N in on Ain2
42 0E 80	ADI Required Write	Same	42 0E 80	ADI Required Write
42 9C 00	Reset Current Clamp Circuitry [step1]	Same	42 9C 00	Reset Current Clamp Circuitry [step1]
42 9C FF	Reset Current Clamp Circuitry [step2]	Same	42 9C FF	Reset Current Clamp Circuitry [step2]
42 0E 00	Enter User Sub Map	Same	42 0E 00	Enter User Sub Map
		Position of Write Changed ->	42 5A 90	ADI Required Write [common mode clamp setup]
		New Write ->	42 60 A0	ADI Required Write [common mode clamp setup]
		New Write ->	delay 25	Force common mode clamps on for 25 ms
		Position of Write Changed ->	42 60 B0	ADI Required Writes [common mode clamp setup]
42 03 0C	Enable Pixel & Sync output drivers	-> Position of Write Changed		
42 04 07	Power-up INTRQ, HS & VS pads	-> Position of Write Changed		
42 13 00	Enable INTRQ output driver [1]	-> Position of Write Changed		
42 17 41	Select SH1	-> Position of Write Changed		
42 1D 40	Enable LLC output driver	-> Position of Write Changed		
42 52 C0	ADI Required Writes [AFE IBIAS]	-> Position of Write Changed		
42 5F A8	SHA gain for Div4	Same	42 5F A8	SHA gain for Div4
42 5A 90	ADI Required Writes [common mode clamp setup]	-> Position of Write Changed		
42 60 B0	ADI Required Writes [common mode clamp setup]	-> Position of Write Changed		
42 0E 80	ADI Required Writes	Same	42 0E 80	ADI Required Writes
42 B6 08	ADI Required Writes [differential CVBS required write]	Same	42 B6 08	ADI Required Writes [differential CVBS required write]

42 C0 A0	ADI Required Writes [differential CVBS required write]	**Same**	42 C0 A0	ADI Required Writes [differential CVBS required write]
42 0E 00	Enter User Map	**Same**	42 0E 00	Enter User Map
		Position of Write Changed ->	42 17 41	Select SH1
		Position of Write Changed ->	42 03 0C	Enable Pixel & Sync output drivers
		Position of Write Changed ->	42 04 07	Power-up INTRQ, HS & VS pads
		Position of Write Changed ->	42 13 00	Enable ADV7182 for 28.63636MHz crystal [1]
		Position of Write Changed ->	42 1D 40	Enable LLC output driver

Changes to differential CVBS script:

- Software reset was inserted at the start of the script. This was done to explicitly state that a reset is needed when switching from one input format to another (e.g. switching from differential CVBS to single ended CVBS).
- The bias current setting for the analog front end (AFE) was moved to the first write after exiting power down mode. This was done to optimize the performance of the ADV7182.
- An INSEL switch write was inserted into the script revision 5.0. The INSEL switch write sets the INSEL bits to an intermediate value before setting the INSEL bits to the desired value. Doing this optimizes the lock time of the ADV7182 in differential CVBS mode.
- The writes to setup the common mode clamp circuitry were moved up to just after the reset current clamp writes.
    - The common mode clamps are also forced on for 25 ms.
    - These writes are optimizations that allow the ADV7182 to lock to analog video more quickly.
    - The common mode clamp setup writes are recommended for new product designs to offer optimal performance. These writes are not required for existing designs which have already been quality approved and released.
- The write to select the SH1 chroma shaping filter was moved below the differential CVBS required writes. The write to select the SH1 chroma shaping filter was moved up above the write to enable the pixel and synchronization pin output drivers. This was done to optimize the performance of the ADV7182.
- The writes to enable the digital output pins and 28.63636MHz crystal were moved down to the bottom of the script. This is an optimization that minimizes the time that the ADV7182 will output incorrect video data before it locks to the incoming analog video input.

[1] The comment in relation to the write 42 13 00, was changed from 'Enable INTRQ output driver' to 'Enable ADV7182 for 28.63636MHz crystal'. This was done in order to explain more accurately the operation of this write.

3 FAST SWITCH SINGLE ENDED CVBS

Script Revision 4.6		Script Changes	Script Revision 5.0	
I2C Write	**Comment**		**I2C Write**	**Comment**
	Hardware reset implied	**New Write ->**	42 0F 80	Reset ADV7182
delay 10	Wait 10 ms	**Same**	delay 10	Wait 10 ms
42 0F 00	Exit Power Down Mode	**Same**	42 0F 00	Exit Power Down Mode
		Position of Write Changed ->	42 52 CD	ADI Required Write [AFE IBIAS]
42 00 00	CVBS in on Ain 1	**Same**	42 00 00	CVBS in on AIN1
42 0E 80	ADI Required Write	**Same**	42 0E 80	ADI Required Write
42 9C 00	Reset Current Clamp Circuitry [step1]	**Same**	42 9C 00	Reset Current Clamp Circuitry [step1]
42 9C FF	Reset Current Clamp Circuitry [step2]	**Same**	42 9C FF	Reset Current Clamp Circuitry [step2]
42 0E 00	Enter User Sub Map	**Same**	42 0E 00	Enter User Map
42 03 0C	Enable Pixel & Sync output drivers	**-> Position of Write Changed**		
42 04 07	Power-up INTRQ, HS & VS pads	**-> Position of Write Changed**		
42 13 00	Enable INTRQ output driver [1]	**-> Position of Write Changed**		
42 17 41	Select SH1	**-> Position of Write Changed**		
42 1D 40	Enable LLC output driver	**-> Position of Write Changed**		
42 52 CD	ADI Required Writes [AFE IBIAS]	**-> Position of Write Changed**		
42 0E 80	ADI Required Writes [Fast Switch]	**Same**	42 0E 80	ADI Required Write [Fast Switch]
42 D9 44	ADI Required Writes [Fast Switch]	**Same**	42 D9 44	ADI Required Write [Fast Switch]
42 0E 00	*Enter User Map [Fast Switch]* [2]	Not Needed		
42 0E 40	Enter User Sub Map 2 [Fast Switch]	**Same**	42 0E 40	Enter User Sub Map 2 [Fast Switch]
42 E0 01	Select fast Switching Mode [Fast Switch]	**Same**	42 E0 01	Enable Fast Switch Mode [Fast Switch]
42 0E 00	Select User Map	**Same**	42 0E 00	Enter User Sub Map
		Position of Write Changed ->	42 17 41	Enable SH1
		Position of Write Changed ->	42 03 0C	Enable Pixel & Sync output drivers
		Position of Write Changed ->	42 04 07	Power-up INTRQ, HS & VS pads
		Position of Write Changed ->	42 13 00	Enable ADV7182 for 28.63636MHz crystal [1]
		Position of Write Changed ->	42 1D 40	Enable LLC output driver

Changes to single ended CVBS fast switch script:

- The writes to enable the digital output pins and 28.63636 MHz crystal were moved down to the bottom of the script. This is an optimization that minimizes the time that the ADV7182 will output incorrect video data before it locks to the incoming analog video input.
- All other changes to the script are the same as those discussed in section 1 Single Ended CVBS.

[1] The comment in relation to the write 42 13 00, was changed from 'Enable INTRQ output driver' to 'Enable ADV7182 for 28.63636MHz crystal'. This was done in order to explain more accurately the operation of this write.

[2] Note the writes in italics are not strictly needed. These writes involve switching from one sub map in the ADV7182 and then immediately switching into another sub map. They are included merely to aid in documentation of the software writes.

4 FAST SWITCH DIFFERENTIAL CVBS

Script Revision 4.6		Script Changes	Script Revision 5.0	
I2C Write	**Comment**		**I2C Write**	**Comment**
	Hardware reset implied	**New Write ->**	42 0F 80	Reset ADV7182
delay 10	Wait 10 ms	**Same**	delay 10	Wait 10 ms
42 0F 00	Exit Power Down Mode	**Same**	42 0F 00	Exit Power Down Mode
		Position of Write Changed ->	42 52 C0	Diff_CVBS AFE IBIAS
		New Write ->	42 00 10	INSEL =unconnected input [INSEL Switch]
42 00 0E	INSEL = CVBS_P in on Ain 1, CVBS_N in on Ain2	**Same**	42 00 0E ;	INSEL = CVBS_P in on Ain 1, CVBS_N in on Ain2
42 0E 80	ADI Required Write	**Same**	42 0E 80	ADI Required Write
42 9C 00	Reset Current Clamp Circuitry [step1]	**Same**	42 9C 00	Reset Current Clamp Circuitry [step1]
42 9C FF	Reset Current Clamp Circuitry [step2]	**Same**	42 9C FF	Reset Current Clamp Circuitry [step2]
42 0E 00	Enter User Sub Map	**Same**	42 0E 00	Enter User Sub Map
42 03 0C	Enable Pixel & Sync output drivers	**-> Position of Write Changed**		
42 04 07	Power-up INTRQ, HS & VS pads	**-> Position of Write Changed**		
42 13 00	Enable INTRQ output driver [1]	**-> Position of Write Changed**		
42 17 41	Select SH1	**-> Position of Write Changed**		
42 1D 40	Enable LLC output driver	**-> Position of Write Changed**		
42 52 C0	ADI Required Writes [AFE IBIAS]	**-> Position of Write Changed**		
		Position of Write Changed ->	42 5A 90 ;	ADI Required Write [common mode clamp setup]
		New Write ->	42 60 A0	ADI Required Write [common mode clamp setup]
		New Write ->	delay 25	Force common mode clamps on for 25 ms
		Position of Write Changed ->	42 60 B0 ;	ADI Required Writes [common mode clamp setup]
42 5F A8	SHA gain for Div4	**Same**	42 5F A8	SHA gain for Div4
42 5A 90	ADI Required Writes [common mode clamp setup]	**-> Position of Write Changed**		
42 60 B0	ADI Required Writes [common mode clamp setup]	**-> Position of Write Changed**		
42 0E 80	ADI Required Writes	**Same**	42 0E 80	ADI Required Writes
42 B6 08	ADI Required Writes [differential CVBS required write]	**Same**	42 B6 08	ADI Required Writes [differential CVBS required write]
42 C0 A0	ADI Required Writes [differential CVBS required write]	**Same**	42 C0 A0	ADI Required Writes [differential CVBS required write]

		Not Needed	*42 0E 00*	*Enter User Map* [2]
		Not Needed	*42 0E 80*	*ADI Required Writes* [Fast Switch] [2]
42 D9 44	ADI Required Writes [Fast Switch]	**Same**	42 D9 44	ADI Required Write [Fast Switch]
42 0E 00	*Enter User Map* [2]	Not Needed		
42 0E 40	Enter User Sub Map 2 [Fast Switch]	**Same**	42 0E 40	Enter User Sub Map 2 [Fast Switch]
42 E0 01	Select fast Switching Mode [Fast Switch]	**Same**	42 E0 01	Enable Fast Switch Mode [Fast Switch]
42 0E 00	Enter User Map	**Same**	42 0E 00	Enter User Map
		Position of Write Changed ->	42 17 41	Select SH1
		Position of Write Changed ->	42 03 0C	Enable Pixel & Sync output drivers
		Position of Write Changed ->	42 04 07	Power-up INTRQ, HS & VS pads
		Position of Write Changed ->	42 13 00	Enable ADV7182 for 28.63636MHz crystal [1]
		Position of Write Changed ->	42 1D 40	Enable LLC output driver

Changes to differential CVBS fast switch script:
All the changes to the differential CVBS fast switch script are the same as those discussed in section 2 Differential CVBS2.

[1] The comment in relation to the write 42 13 00, was changed from 'Enable INTRQ output driver' to 'Enable ADV7182 for 28.63636MHz crystal'. This was done in order to explain more accurately the operation of this write.

[2] Note the writes in italics are not strictly needed. These writes involve switching from one sub map in the ADV7182 and then immediately switching into another sub map. They are included merely to aid in documentation of the software writes.

5 YC (S-VIDEO)

Script Revision 4.6		Script Changes	Script Revision 5.0	
I2C Write	**Comment**		**I2C Write**	**Comment**
	Hardware reset implied	**New Write ->**	42 0F 80	Reset ADV7182
delay 10	Wait 10 ms	**Same**	delay 10	Wait 10 ms
42 0F 00	Exit Power Down Mode	**Same**	42 0F 00	Exit Power Down Mode
		Position of Write Changed ->	42 53 CE	YC AFE IBIAS
42 00 08	Insel=YC-1, Y=Ain1, C=Ain2	**Same**	42 00 08	INSEL = YC, Y - Ain1, C - Ain2
42 0E 80	ADI Required Write	**Same**	42 0E 80	ADI Required Write
42 9C 00	Reset Current Clamp Circuitry [step1]	**Same**	42 9C 00	Reset Current Clamp Circuitry [step1]
42 9C FF	Reset Current Clamp Circuitry [step2]	**Same**	42 9C FF	Reset Current Clamp Circuitry [step2]
42 0E 00	Enter User Sub Map	**Same**	42 0E 00	Enter User Map
42 03 0C	Enable Pixel & Sync output drivers	**Same**	42 03 0C	Enable Pixel & Sync output drivers
42 04 07	Power-up INTRQ, HS & VS pads	**Same**	42 04 07	Power-up INTRQ pad, Enable SFL & VS pin
42 13 00	Enable INTRQ output driver [1]	**Same**	42 13 00	Enable ADV7182 for 28.63636MHz crystal [1]
42 1D 40	Enable LLC output driver	**Same**	42 1D 40	Enable LLC output driver
42 53 CE	ADI Required Writes [AFE IBIAS]	**-> Position of Write Changed**		

Changes to YC script:

- Software reset was inserted at the start of the script. This was done to explicitly state that a reset is needed when switching from one input format to another (e.g. switching from differential CVBS to YC).
- The bias current setting for the analog front end (AFE) was moved to the first write after exiting power down mode. This was done to optimize the performance of the ADV7182.

[1] The comment in relation to the write 42 13 00, was changed from 'Enable INTRQ output driver' to 'Enable ADV7182 for 28.63636MHz crystal'. This was done in order to explain more accurately the operation of this write.

6 YP_BP_R MODE (COMPONENT)

Script Revision 4.6		Script Changes	Script Revision 5.0	
I2C Write	**Comment**		**I2C Write**	**Comment**
	Hardware reset implied	**New Write ->**	42 0F 80	Reset ADV7182
delay 10	Wait 10 ms	**Same**	delay 10	Wait 10 ms
42 0F 00	Exit Power Down Mode	**Same**	42 0F 00	Exit Power Down Mode
		Position of Write Changed ->	42 54 C0	YPbPr AFE IBIAS
42 00 0C	INSEL = YPbPr, Y=Ain1, Pb=Ain2, Pr=Ain3	**Same**	42 00 0C	INSEL = YPrPb, Y on AIn1, Pb on Ain2, Pr on Ain3
42 0E 80	ADI Required Write	**Same**	42 0E 80	ADI Required Write
42 9C 00	ADI Required Write	**Same**	42 9C 00	Reset Current Clamp Circuitry [step1]
42 9C FF	ADI Required Write	**Same**	42 9C FF	Reset Current Clamp Circuitry [step2]
42 0E 00	Enter User Sub Map	**Same**	42 0E 00	Enter User Sub Map
42 03 0C	Enable Pixel & Sync output drivers	**Same**	42 03 0C	Enable Pixel & Sync output drivers
42 04 07	Power-up INTRQ pad & Enable SFL	**Same**	42 04 07	Power-up INTRQ pad, Enable SFL & VS pin
42 13 00	Enable ADV7182 for 28.63636MHz crystal [1]	**Same**	42 13 00	Enable ADV7182 for 28.63636MHz crystal [1]
42 1D 40	Enable LLC output driver	**Same**	42 1D 40	Enable LLC output driver
42 54 C0	ADI Required Writes [AFE IBIAS]	**-> Position of Write Changed**		

Changes to YPbPr script:

- Software reset was inserted at the start of the script. This was done to explicitly state that a reset is needed when switching from one input format to another (e.g. switching from differential CVBS to YPbPr).
- The bias current setting for the analog front end (AFE) was moved to the first write after exiting power down mode. This was done to optimize the performance of the ADV7182.

[1] The comment in relation to the write 42 13 00, was changed from 'Enable INTRQ output driver' to 'Enable ADV7182 for 28.63636MHz crystal'. This was done in order to explain more accurately the operation of this write.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).