ADV7630 REGISTER MAP DOCUMENTATION

ADV7630 Software Manual

SOFTWARE MANUAL

Rev.A

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TABLE OF CONTENTS

1 Register Tables 4
1.1 IO Map 4
1.2 HDMI Map 8
1.3 Repeater Map 10
1.4 Infoframe Map 17
1.5 CEC Map 29
1.6 TXA Main Map 33
1.7 TXA EDID Map 35
1.8 TXB Main Map 47
1.9 TXB EDID Map 49
2 Signal Documentation 61
2.1 IO Map 61
2.2 HDMI Map 92
2.3 Repeater Map 99
2.4 Infoframe Map 111
2.5 CEC Map 118
2.6 TXA Main Map 126
2.7 TXA EDID Map 133
2.8 TXB Main Map 147
2.9 TXB EDID Map 154
3 Index 168

1 REGISTER TABLES

1.1 IO MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x04	0x00	IO_REG_04	rw	-	-	-	-	-	CLK_IN_FREQ_SEL [1]	CLK_IN_FREQ_SEL [0]	-
0x0B	0x00	IO_REG_0B	rw	-	-	-	-	-	-	CORE_PDN	CLK_IN_PDN
0x0C	0x60	IO_REG_0C	rw	-	-	POWER_DOWN	-	PWR_SAVE_MODE	-	-	-
0x14	0x60	IO_REG_14	rw	-	-	DR_STR[1]	DR_STR[0]	-	-	-	-
0x1B	0x00	IO_REG_1B	sc	TXA SOFT RESET	TXB SOFT RESET	-	-	-	-	-	-
0x20	0x00	IO_REG_20	rw	HPA_MAN_VALUE _A	HPA_MAN_VALUE _B	HPA_MAN_VALUE _C	HPA_MAN_VALUE _D	HPA_TRISTATE_A	HPA_TRISTATE_B	HPA_TRISTATE_C	HPA_TRISTATE_D
0x21	0x00	IO_REG_21	r	-	-	-	-	HPA_STATUS_POR T_A	HPA_STATUS_POR T_B	HPA_STATUS_POR T_C	HPA_STATUS_POR T_D
0x2C	0x00	IO_REG_2C	rw	-	-	-	-	-	-	SET INPUT TXA DDC SDA	-
0x32	0x00	IO_REG_32	rw	-	-	-	-	-	-	SET INPUT TXB DDC SDA	-
0x3F	0x00	IO_REG_3F	r	-	-	-	-	-	INTRQ_TX_B_RAW	INTRQ_TX_A_RAW	INTRQ_RAW
0x40	0x20	IO_REG_40	rw	INTRQ_DUR_SEL[1]	INTRQ_DUR_SEL[0]	-	STORE_UNMASKE D_IRQS	EN_UMASK_RAW_ INTRQ	MPU_STIM_INTRQ	INTRQ_OP_SEL[1]	INTRQ_OP_SEL[0]
0x47	0x00	IO_REG_47	r	MPU_STIM_INTRQ _RAW	-	-	-	-	-	-	-
0x48	0x00	IO_REG_48	r	MPU_STIM_INTRQ _ST	-	-	-	-	-	-	-
0x49	0x00	IO_REG_49	sc	MPU_STIM_INTRQ _CLR	-	-	-	-	-	-	-
0x4B	0x00	IO_REG_4B	rw	MPU_STIM_INTRQ _MB1	-	-	-	-	-	-	-
0x60	0x00	IO_REG_60	r	ISRC2_PCKT_RAW	ISRC1_PCKT_RAW	ACP_PCKT_RAW	VS_INFO_RAW	MS_INFO_RAW	SPD_INFO_RAW	AUDIO_INFO_RA W	AVI_INFO_RAW
0x61	0x00	IO_REG_61	r	ISRC2_PCKT_ST	ISRC1_PCKT_ST	ACP_PCKT_ST	VS_INFO_ST	MS_INFO_ST	SPD_INFO_ST	AUDIO_INFO_ST	AVI_INFO_ST
0x62	0x00	IO_REG_62	sc	ISRC2_PCKT_CLR	ISRC1_PCKT_CLR	ACP_PCKT_CLR	VS_INFO_CLR	MS_INFO_CLR	SPD_INFO_CLR	AUDIO_INFO_CLR	AVI_INFO_CLR
0x63	0x00	IO_REG_63	rw	ISRC2_PCKT_MB2	ISRC1_PCKT_MB2	ACP_PCKT_MB2	VS_INFO_MB2	MS_INFO_MB2	SPD_INFO_MB2	AUDIO_INFO_MB2	AVI_INFO_MB2
0x64	0x00	IO_REG_64	rw	ISRC2_PCKT_MB1	ISRC1_PCKT_MB1	ACP_PCKT_MB1	VS_INFO_MB1	MS_INFO_MB1	SPD_INFO_MB1	AUDIO_INFO_MB1	AVI_INFO_MB1
0x65	0x00	IO_REG_65	r	-	-	AV_MUTE_RAW	-	-	GEN_CTL_PCKT_R AW	AUDIO_C_PCKT_R AW	GAMUT_MDATA_R AW
0x66	0x00	IO_REG_66	r	-	-	AV_MUTE_ST	-	-	GEN_CTL_PCKT_S T	AUDIO_C_PCKT_S T	GAMUT_MDATA_S T
0x67	0x00	IO_REG_67	sc	-	-	AV_MUTE_CLR	-	-	GEN_CTL_PCKT_C LR	AUDIO_C_PCKT_C LR	GAMUT_MDATA_ CLR
0x68	0x00	IO_REG_68	rw	-	-	AV_MUTE_MB2	-	-	GEN_CTL_PCKT_ MB2	AUDIO_C_PCKT_ MB2	GAMUT_MDATA_ MB2

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x69	0x00	IO_REG_69	rw	-	-	AV_MUTE_MB1	-	-	GEN_CTL_PCKT_MB1	AUDIO_C_PCKT_MB1	GAMUT_MDATA_MB1
0x6A	0x00	IO_REG_6A	r	TMDSPLL_LCK_A_RAW	TMDSPLL_LCK_B_RAW	TMDSPLL_LCK_C_RAW	TMDSPLL_LCK_D_RAW	TMDS_CLK_A_RAW	TMDS_CLK_B_RAW	TMDS_CLK_C_RAW	TMDS_CLK_D_RAW
0x6B	0x00	IO_REG_6B	r	TMDSPLL_LCK_A_ST	TMDSPLL_LCK_B_ST	TMDSPLL_LCK_C_ST	TMDSPLL_LCK_D_ST	TMDS_CLK_A_ST	TMDS_CLK_B_ST	TMDS_CLK_C_ST	TMDS_CLK_D_ST
0x6C	0x00	IO_REG_6C	sc	TMDSPLL_LCK_A_CLR	TMDSPLL_LCK_B_CLR	TMDSPLL_LCK_C_CLR	TMDSPLL_LCK_D_CLR	TMDS_CLK_A_CLR	TMDS_CLK_B_CLR	TMDS_CLK_C_CLR	TMDS_CLK_D_CLR
0x6E	0x00	IO_REG_6E	rw	TMDSPLL_LCK_A_MB1	TMDSPLL_LCK_B_MB1	TMDSPLL_LCK_C_MB1	TMDSPLL_LCK_D_MB1	TMDS_CLK_A_MB1	TMDS_CLK_B_MB1	TMDS_CLK_C_MB1	TMDS_CLK_D_MB1
0x6F	0x00	IO_REG_6F	r	HDMI_ENCRPT_A_RAW	HDMI_ENCRPT_B_RAW	HDMI_ENCRPT_C_RAW	HDMI_ENCRPT_D_RAW	CABLE_DET_A_RAW	CABLE_DET_B_RAW	CABLE_DET_C_RAW	CABLE_DET_D_RAW
0x70	0x00	IO_REG_70	r	HDMI_ENCRPT_A_ST	HDMI_ENCRPT_B_ST	HDMI_ENCRPT_C_ST	HDMI_ENCRPT_D_ST	CABLE_DET_A_ST	CABLE_DET_B_ST	CABLE_DET_C_ST	CABLE_DET_D_ST
0x71	0x00	IO_REG_71	sc	HDMI_ENCRPT_A_CLR	HDMI_ENCRPT_B_CLR	HDMI_ENCRPT_C_CLR	HDMI_ENCRPT_D_CLR	CABLE_DET_A_CLR	CABLE_DET_B_CLR	CABLE_DET_C_CLR	CABLE_DET_D_CLR
0x73	0x00	IO_REG_73	rw	HDMI_ENCRPT_A_MB1	HDMI_ENCRPT_B_MB1	HDMI_ENCRPT_C_MB1	HDMI_ENCRPT_D_MB1	CABLE_DET_A_MB1	CABLE_DET_B_MB1	CABLE_DET_C_MB1	CABLE_DET_D_MB1
0x74	0x00	IO_REG_74	r	-	-	-	-	-	VIDEO_3D_RAW	-	-
0x75	0x00	IO_REG_75	r	-	-	-	-	-	VIDEO_3D_ST	-	-
0x76	0x00	IO_REG_76	sc	-	-	-	-	-	VIDEO_3D_CLR	-	-
0x77	0x00	IO_REG_77	rw	-	-	-	-	-	VIDEO_3D_MB2	-	-
0x78	0x00	IO_REG_78	rw	-	-	-	-	-	VIDEO_3D_MB1	-	-
0x79	0x00	IO_REG_79	r	NEW_ISRC2_PCKT_RAW	NEW_ISRC1_PCKT_RAW	NEW_ACP_PCKT_RAW	NEW_VS_INFO_RAW	NEW_MS_INFO_RAW	NEW_SPD_INFO_RAW	NEW_AUDIO_INFO_RAW	NEW_AVI_INFO_RAW
0x7A	0x00	IO_REG_7A	r	NEW_ISRC2_PCKT_ST	NEW_ISRC1_PCKT_ST	NEW_ACP_PCKT_ST	NEW_VS_INFO_ST	NEW_MS_INFO_ST	NEW_SPD_INFO_ST	NEW_AUDIO_INFO_ST	NEW_AVI_INFO_ST
0x7B	0x00	IO_REG_7B	sc	NEW_ISRC2_PCKT_CLR	NEW_ISRC1_PCKT_CLR	NEW_ACP_PCKT_CLR	NEW_VS_INFO_CLR	NEW_MS_INFO_CLR	NEW_SPD_INFO_CLR	NEW_AUDIO_INFO_CLR	NEW_AVI_INFO_CLR
0x7C	0x00	IO_REG_7C	rw	NEW_ISRC2_PCKT_MB2	NEW_ISRC1_PCKT_MB2	NEW_ACP_PCKT_MB2	NEW_VS_INFO_MB2	NEW_MS_INFO_MB2	NEW_SPD_INFO_MB2	NEW_AUDIO_INFO_MB2	NEW_AVI_INFO_MB2
0x7D	0x00	IO_REG_7D	rw	NEW_ISRC2_PCKT_MB1	NEW_ISRC1_PCKT_MB1	NEW_ACP_PCKT_MB1	NEW_VS_INFO_MB1	NEW_MS_INFO_MB1	NEW_SPD_INFO_MB1	NEW_AUDIO_INFO_MB1	NEW_AVI_INFO_MB1
0x7E	0x00	IO_REG_7E	r	-	-	-	-	-	PACKET_ERROR_RAW	-	NEW_GAMUT_MDATA_RAW
0x7F	0x00	IO_REG_7F	r	-	-	-	-	-	PACKET_ERROR_ST	-	NEW_GAMUT_MDATA_ST
0x80	0x00	IO_REG_80	sc	-	-	-	-	-	PACKET_ERROR_CLR	-	NEW_GAMUT_MDATA_CLR
0x81	0x00	IO_REG_81	rw	-	-	-	-	-	PACKET_ERROR_MB2	-	NEW_GAMUT_MDATA_MB2
0x82	0x00	IO_REG_82	rw	-	-	-	-	-	PACKET_ERROR_MB1	-	NEW_GAMUT_MDATA_MB1
0x83	0x00	IO_REG_83	r	DEEP_COLOR_CHNG_RAW	VCLK_CHNG_RAW	-	-	-	-	NEW_TMDS_FRQ_RAW	-

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x84	0x00	IO_REG_84	r	DEEP_COLOR_CHNG_ST	VCLK_CHNG_ST	-	-	-	-	NEW_TMDS_FRQ_ST	-
0x85	0x00	IO_REG_85	sc	DEEP_COLOR_CHNG_CLR	VCLK_CHNG_CLR	-	-	-	-	NEW_TMDS_FRQ_CLR	-
0x86	0x00	IO_REG_86	rw	DEEP_COLOR_CHNG_MB2	-	-	-	-	-	-	-
0x87	0x00	IO_REG_87	rw	DEEP_COLOR_CHNG_MB1	VCLK_CHNG_MB1	-	-	-	-	NEW_TMDS_FRQ_MB1	-
0x88	0x00	IO_REG_88	r	MS_INF_CKS_ERR_RAW	SPD_INF_CKS_ERR_RAW	AUD_INF_CKS_ERR_RAW	AVI_INF_CKS_ERR_RAW	AKSV_UPDATE_A_RAW	AKSV_UPDATE_B_RAW	AKSV_UPDATE_C_RAW	AKSV_UPDATE_D_RAW
0x89	0x00	IO_REG_89	r	MS_INF_CKS_ERR_ST	SPD_INF_CKS_ERR_ST	AUD_INF_CKS_ERR_ST	AVI_INF_CKS_ERR_ST	AKSV_UPDATE_A_ST	AKSV_UPDATE_B_ST	AKSV_UPDATE_C_ST	AKSV_UPDATE_D_ST
0x8A	0x00	IO_REG_8A	sc	MS_INF_CKS_ERR_CLR	SPD_INF_CKS_ERR_CLR	AUD_INF_CKS_ERR_CLR	AVI_INF_CKS_ERR_CLR	AKSV_UPDATE_A_CLR	AKSV_UPDATE_B_CLR	AKSV_UPDATE_C_CLR	AKSV_UPDATE_D_CLR
0x8B	0x00	IO_REG_8B	rw	MS_INF_CKS_ERR_MB2	SPD_INF_CKS_ERR_MB2	AUD_INF_CKS_ERR_MB2	AVI_INF_CKS_ERR_MB2	-	-	-	-
0x8C	0x00	IO_REG_8C	rw	MS_INF_CKS_ERR_MB1	SPD_INF_CKS_ERR_MB1	AUD_INF_CKS_ERR_MB1	AVI_INF_CKS_ERR_MB1	AKSV_UPDATE_A_MB1	AKSV_UPDATE_B_MB1	AKSV_UPDATE_C_MB1	AKSV_UPDATE_D_MB1
0x8D	0x00	IO_REG_8D	r	RI_EXPIRED_A_RAW	RI_EXPIRED_B_RAW	RI_EXPIRED_C_RAW	RI_EXPIRED_D_RAW	-	-	BG_MEAS_DONE_RAW	VS_INF_CKS_ERR_RAW
0x8E	0x00	IO_REG_8E	r	RI_EXPIRED_A_ST	RI_EXPIRED_B_ST	RI_EXPIRED_C_ST	RI_EXPIRED_D_ST	-	-	BG_MEAS_DONE_ST	VS_INF_CKS_ERR_ST
0x8F	0x00	IO_REG_8F	sc	RI_EXPIRED_A_CLR	RI_EXPIRED_B_CLR	RI_EXPIRED_C_CLR	RI_EXPIRED_D_CLR	-	-	BG_MEAS_DONE_CLR	VS_INF_CKS_ERR_CLR
0x90	0x00	IO_REG_90	rw	-	-	-	-	-	-	-	VS_INF_CKS_ERR_MB2
0x91	0x00	IO_REG_91	rw	RI_EXPIRED_A_MB1	RI_EXPIRED_B_MB1	RI_EXPIRED_C_MB1	RI_EXPIRED_D_MB1	-	-	BG_MEAS_DONE_MB1	VS_INF_CKS_ERR_MB1
0x92	0x00	IO_REG_92	r	-	-	CEC_RX_RDY2_RAW	CEC_RX_RDY1_RAW	CEC_RX_RDY0_RAW	CEC_TX_RETRY_TIMEOUT_RAW	CEC_TX_ARBITRATION_LOST_RAW	CEC_TX_READY_RAW
0x93	0x00	IO_REG_93	r	-	-	CEC_RX_RDY2_ST	CEC_RX_RDY1_ST	CEC_RX_RDY0_ST	CEC_TX_RETRY_TIMEOUT_ST	CEC_TX_ARBITRATION_LOST_ST	CEC_TX_READY_ST
0x94	0x00	IO_REG_94	sc	-	-	CEC_RX_RDY2_CLR	CEC_RX_RDY1_CLR	CEC_RX_RDY0_CLR	CEC_TX_RETRY_TIMEOUT_CLR	CEC_TX_ARBITRATION_LOST_CLR	CEC_TX_READY_CLR
0x96	0x00	IO_REG_96	rw	-	-	CEC_RX_RDY2_MB1	CEC_RX_RDY1_MB1	CEC_RX_RDY0_MB1	CEC_TX_RETRY_TIMEOUT_MB1	CEC_TX_ARBITRATION_LOST_MB1	CEC_TX_READY_MB1
0x97	0x00	IO_REG_97	r	CEC_INTERRUPT_BYTE[7]	CEC_INTERRUPT_BYTE[6]	CEC_INTERRUPT_BYTE[5]	CEC_INTERRUPT_BYTE[4]	CEC_INTERRUPT_BYTE[3]	CEC_INTERRUPT_BYTE[2]	CEC_INTERRUPT_BYTE[1]	CEC_INTERRUPT_BYTE[0]
0x98	0x00	IO_REG_98	r	CEC_INTERRUPT_BYTE_ST[7]	CEC_INTERRUPT_BYTE_ST[6]	CEC_INTERRUPT_BYTE_ST[5]	CEC_INTERRUPT_BYTE_ST[4]	CEC_INTERRUPT_BYTE_ST[3]	CEC_INTERRUPT_BYTE_ST[2]	CEC_INTERRUPT_BYTE_ST[1]	CEC_INTERRUPT_BYTE_ST[0]
0x99	0x00	IO_REG_99	sc	CEC_INTERRUPT_BYTE_CLR[7]	CEC_INTERRUPT_BYTE_CLR[6]	CEC_INTERRUPT_BYTE_CLR[5]	CEC_INTERRUPT_BYTE_CLR[4]	CEC_INTERRUPT_BYTE_CLR[3]	CEC_INTERRUPT_BYTE_CLR[2]	CEC_INTERRUPT_BYTE_CLR[1]	CEC_INTERRUPT_BYTE_CLR[0]
0x9B	0x00	IO_REG_9B	rw	CEC_INTERRUPT_BYTE_MB1[7]	CEC_INTERRUPT_BYTE_MB1[6]	CEC_INTERRUPT_BYTE_MB1[5]	CEC_INTERRUPT_BYTE_MB1[4]	CEC_INTERRUPT_BYTE_MB1[3]	CEC_INTERRUPT_BYTE_MB1[2]	CEC_INTERRUPT_BYTE_MB1[1]	CEC_INTERRUPT_BYTE_MB1[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xAC	0x0F	IO_REG_AC	rw	-	-	-	-	ARC_TX_PWRDN[3]	ARC_TX_PWRDN[2]	ARC_TX_PWRDN[1]	ARC_TX_PWRDN[0]
0xAD	0x00	IO_REG_AD	rw	INV_SPDIF_IN[3]	INV_SPDIF_IN[2]	INV_SPDIF_IN[1]	INV_SPDIF_IN[0]	ZERO_SPDIF_IN[3]	ZERO_SPDIF_IN[2]	ZERO_SPDIF_IN[1]	ZERO_SPDIF_IN[0]
0xC5	0x00	IO_REG_C5	rw	-	-	-	-	ARC_RX_I2C_PWRDN	SPDIF_OUT_EN	ARC_RX_SINGLE_ENDED	ARC_RX_SPDIF_INV
0xE1	0x00	IO_REG_E1	r	RD_INFO[15]	RD_INFO[14]	RD_INFO[13]	RD_INFO[12]	RD_INFO[11]	RD_INFO[10]	RD_INFO[9]	RD_INFO[8]
0xE2	0x00	IO_REG_E2	r	RD_INFO[7]	RD_INFO[6]	RD_INFO[5]	RD_INFO[4]	RD_INFO[3]	RD_INFO[2]	RD_INFO[1]	RD_INFO[0]
0xEA	0x00	IO_REG_EA	rw	TXB_MAIN_SLAVE_ADDR[6]	TXB_MAIN_SLAVE_ADDR[5]	TXB_MAIN_SLAVE_ADDR[4]	TXB_MAIN_SLAVE_ADDR[3]	TXB_MAIN_SLAVE_ADDR[2]	TXB_MAIN_SLAVE_ADDR[1]	TXB_MAIN_SLAVE_ADDR[0]	-
0xEC	0x00	IO_REG_EC	rw	TXB_EDID_SLAVE_ADDR[6]	TXB_EDID_SLAVE_ADDR[5]	TXB_EDID_SLAVE_ADDR[4]	TXB_EDID_SLAVE_ADDR[3]	TXB_EDID_SLAVE_ADDR[2]	TXB_EDID_SLAVE_ADDR[1]	TXB_EDID_SLAVE_ADDR[0]	-
0xEE	0x00	IO_REG_EE	rw	TXA_MAIN_SLAVE_ADDR[6]	TXA_MAIN_SLAVE_ADDR[5]	TXA_MAIN_SLAVE_ADDR[4]	TXA_MAIN_SLAVE_ADDR[3]	TXA_MAIN_SLAVE_ADDR[2]	TXA_MAIN_SLAVE_ADDR[1]	TXA_MAIN_SLAVE_ADDR[0]	-
0xEF	0x00	IO_REG_EF	rw	TXA_UDP_SLAVE_ADDR[6]	TXA_UDP_SLAVE_ADDR[5]	TXA_UDP_SLAVE_ADDR[4]	TXA_UDP_SLAVE_ADDR[3]	TXA_UDP_SLAVE_ADDR[2]	TXA_UDP_SLAVE_ADDR[1]	TXA_UDP_SLAVE_ADDR[0]	-
0xF0	0x00	IO_REG_F0	rw	TXA_EDID_SLAVE_ADDR[6]	TXA_EDID_SLAVE_ADDR[5]	TXA_EDID_SLAVE_ADDR[4]	TXA_EDID_SLAVE_ADDR[3]	TXA_EDID_SLAVE_ADDR[2]	TXA_EDID_SLAVE_ADDR[1]	TXA_EDID_SLAVE_ADDR[0]	-
0xF4	0x00	IO_REG_F4	rw	CEC_SLAVE_ADDR[6]	CEC_SLAVE_ADDR[5]	CEC_SLAVE_ADDR[4]	CEC_SLAVE_ADDR[3]	CEC_SLAVE_ADDR[2]	CEC_SLAVE_ADDR[1]	CEC_SLAVE_ADDR[0]	-
0xF5	0x00	IO_REG_F5	rw	INFOFRAME_SLAVE_ADDR[6]	INFOFRAME_SLAVE_ADDR[5]	INFOFRAME_SLAVE_ADDR[4]	INFOFRAME_SLAVE_ADDR[3]	INFOFRAME_SLAVE_ADDR[2]	INFOFRAME_SLAVE_ADDR[1]	INFOFRAME_SLAVE_ADDR[0]	-
0xF9	0x00	IO_REG_F9	rw	KSV_SLAVE_ADDR[6]	KSV_SLAVE_ADDR[5]	KSV_SLAVE_ADDR[4]	KSV_SLAVE_ADDR[3]	KSV_SLAVE_ADDR[2]	KSV_SLAVE_ADDR[1]	KSV_SLAVE_ADDR[0]	-
0xFA	0x00	IO_REG_FA	rw	EDID_SLAVE_ADDR[6]	EDID_SLAVE_ADDR[5]	EDID_SLAVE_ADDR[4]	EDID_SLAVE_ADDR[3]	EDID_SLAVE_ADDR[2]	EDID_SLAVE_ADDR[1]	EDID_SLAVE_ADDR[0]	-
0xFB	0x00	IO_REG_FB	rw	HDMI_SLAVE_ADDR[6]	HDMI_SLAVE_ADDR[5]	HDMI_SLAVE_ADDR[4]	HDMI_SLAVE_ADDR[3]	HDMI_SLAVE_ADDR[2]	HDMI_SLAVE_ADDR[1]	HDMI_SLAVE_ADDR[0]	-
0xFF	0x00	IO_REG_FF	sc	MAIN_RESET	-	-	-	-	-	-	-

1.2 HDMI MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00	HDMI_REG_00	rw	-	-	BG_MEAS_PORT_SEL[2]	BG_MEAS_PORT_SEL[1]	BG_MEAS_PORT_SEL[0]	HDMI_PORT_SELECT_TX_A[2]	HDMI_PORT_SELECT_TX_A[1]	HDMI_PORT_SELECT_TX_A[0]
0x01	0x00	HDMI_REG_01	rw	-	-	-	-	-	-	-	TERM_AUTO
0x02	0x00	HDMI_REG_02	rw	-	-	-	-	EN_BG_PORT_D	EN_BG_PORT_C	EN_BG_PORT_B	EN_BG_PORT_A
0x04	0x00	HDMI_REG_04	r	-	AV_MUTE	HDCP_KEYS_READ	HDCP_KEY_ERROR	HDCP_RI_EXPIRED	-	TMDS_PLL_LOCKED	-
0x05	0x00	HDMI_REG_05	r	HDMI_MODE	HDMI_CONTENT_ENCRYPTED	DVI_HSYNC_POLARITY	DVI_VSYNC_POLARITY	HDMI_PIXEL_REPETITION[3]	HDMI_PIXEL_REPETITION[2]	HDMI_PIXEL_REPETITION[1]	HDMI_PIXEL_REPETITION[0]
0x0B	0x00	HDMI_REG_0B	r	DEEP_COLOR_MODE[1]	DEEP_COLOR_MODE[0]	-	-	-	-	-	-
0x0D	0x04	HDMI_REG_0D	rw	-	HDMI_PORT_SELECT_TX_B[2]	HDMI_PORT_SELECT_TX_B[1]	HDMI_PORT_SELECT_TX_B[0]	FREQTOLERANCE[3]	FREQTOLERANCE[2]	FREQTOLERANCE[1]	FREQTOLERANCE[0]
0x1D	0x00	HDMI_REG_1D	rw	-	PDN_PKT_PROCESSOR	-	-	-	-	-	-
0x47	0x00	HDMI_REG_47	rw	-	-	-	-	-	-	-	ALWAYS_STORE_INF
0x48	0x00	HDMI_REG_48	rw	-	DIS_CABLE_DET_RST	-	-	-	-	-	-
0x4C	0x40	HDMI_REG_4C	rw	-	-	-	-	-	NEW_VS_PARAM	-	-
0x50	0x00	HDMI_REG_50	rw	-	-	-	GAMUT_IRQ_NEXT_FIELD	-	-	-	-
0x51	0x00	HDMI_REG_51	r	TMDSFREQ[8]	TMDSFREQ[7]	TMDSFREQ[6]	TMDSFREQ[5]	TMDSFREQ[4]	TMDSFREQ[3]	TMDSFREQ[2]	TMDSFREQ[1]
0x52	0x00	HDMI_REG_52	r	TMDSFREQ[0]	TMDSFREQ_FRAC[6]	TMDSFREQ_FRAC[5]	TMDSFREQ_FRAC[4]	TMDSFREQ_FRAC[3]	TMDSFREQ_FRAC[2]	TMDSFREQ_FRAC[1]	TMDSFREQ_FRAC[0]
0x53	0x00	HDMI_REG_53	r	-	-	-	-	HDMI_COLORSPACE[3]	HDMI_COLORSPACE[2]	HDMI_COLORSPACE[1]	HDMI_COLORSPACE[0]
0x56	0x58	HDMI_REG_56	rw	FILT_5V_DET_DIS	FILT_5V_DET_TIMER[6]	FILT_5V_DET_TIMER[5]	FILT_5V_DET_TIMER[4]	FILT_5V_DET_TIMER[3]	FILT_5V_DET_TIMER[2]	FILT_5V_DET_TIMER[1]	FILT_5V_DET_TIMER[0]
0x5A	0x00	HDMI_REG_5A	sc	-	HDCP_I2C_RESET_TX	BG_MEAS_REQ	-	HDCP_REPT_EDID_RESET	-	-	-
0x6C	0xA3	HDMI_REG_6C	rw	HPA_DELAY_SEL[3]	HPA_DELAY_SEL[2]	HPA_DELAY_SEL[1]	HPA_DELAY_SEL[0]	HPA_OVR_TERM	HPA_AUTO_INT_EDID[1]	HPA_AUTO_INT_EDID[0]	HPA_MANUAL
0x73	0x00	HDMI_REG_73	rw	DDC_PWRDN[7]	DDC_PWRDN[6]	DDC_PWRDN[5]	DDC_PWRDN[4]	DDC_PWRDN[3]	DDC_PWRDN[2]	DDC_PWRDN[1]	DDC_PWRDN[0]
0x83	0xFF	HDMI_REG_83	rw	-	-	-	-	CLOCK_TERMD_DISABLE	CLOCK_TERMC_DISABLE	CLOCK_TERMB_DISABLE	CLOCK_TERMA_DISABLE
0xE0	0x00	HDMI_REG_E0	r	BG_TMDSFREQ[8]	BG_TMDSFREQ[7]	BG_TMDSFREQ[6]	BG_TMDSFREQ[5]	BG_TMDSFREQ[4]	BG_TMDSFREQ[3]	BG_TMDSFREQ[2]	BG_TMDSFREQ[1]
0xE1	0x00	HDMI_REG_E1	r	BG_TMDSFREQ[0]	BG_TMDSFREQ_FRAC[6]	BG_TMDSFREQ_FRAC[5]	BG_TMDSFREQ_FRAC[4]	BG_TMDSFREQ_FRAC[3]	BG_TMDSFREQ_FRAC[2]	BG_TMDSFREQ_FRAC[1]	BG_TMDSFREQ_FRAC[0]
0xE2	0x00	HDMI_REG_E2	r	-	-	-	BG_LINE_WIDTH[12]	BG_LINE_WIDTH[11]	BG_LINE_WIDTH[10]	BG_LINE_WIDTH[9]	BG_LINE_WIDTH[8]
0xE3	0x00	HDMI_REG_E3	r	BG_LINE_WIDTH[7]	BG_LINE_WIDTH[6]	BG_LINE_WIDTH[5]	BG_LINE_WIDTH[4]	BG_LINE_WIDTH[3]	BG_LINE_WIDTH[2]	BG_LINE_WIDTH[1]	BG_LINE_WIDTH[0]
0xE4	0x00	HDMI_REG_E4	r	-	-	BG_TOTAL_LINE_WIDTH[13]	BG_TOTAL_LINE_WIDTH[12]	BG_TOTAL_LINE_WIDTH[11]	BG_TOTAL_LINE_WIDTH[10]	BG_TOTAL_LINE_WIDTH[9]	BG_TOTAL_LINE_WIDTH[8]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xE5	0x00	HDMI_REG_E5	r	BG_TOTAL_LINE_WIDTH[7]	BG_TOTAL_LINE_WIDTH[6]	BG_TOTAL_LINE_WIDTH[5]	BG_TOTAL_LINE_WIDTH[4]	BG_TOTAL_LINE_WIDTH[3]	BG_TOTAL_LINE_WIDTH[2]	BG_TOTAL_LINE_WIDTH[1]	BG_TOTAL_LINE_WIDTH[0]
0xE6	0x00	HDMI_REG_E6	r	-	-	-	BG_FIELD_HEIGHT[12]	BG_FIELD_HEIGHT[11]	BG_FIELD_HEIGHT[10]	BG_FIELD_HEIGHT[9]	BG_FIELD_HEIGHT[8]
0xE7	0x00	HDMI_REG_E7	r	BG_FIELD_HEIGHT[7]	BG_FIELD_HEIGHT[6]	BG_FIELD_HEIGHT[5]	BG_FIELD_HEIGHT[4]	BG_FIELD_HEIGHT[3]	BG_FIELD_HEIGHT[2]	BG_FIELD_HEIGHT[1]	BG_FIELD_HEIGHT[0]
0xE8	0x00	HDMI_REG_E8	r	-	-	-	BG_TOTAL_FIELD_HEIGHT[12]	BG_TOTAL_FIELD_HEIGHT[11]	BG_TOTAL_FIELD_HEIGHT[10]	BG_TOTAL_FIELD_HEIGHT[9]	BG_TOTAL_FIELD_HEIGHT[8]
0xE9	0x00	HDMI_REG_E9	r	BG_TOTAL_FIELD_HEIGHT[7]	BG_TOTAL_FIELD_HEIGHT[6]	BG_TOTAL_FIELD_HEIGHT[5]	BG_TOTAL_FIELD_HEIGHT[4]	BG_TOTAL_FIELD_HEIGHT[3]	BG_TOTAL_FIELD_HEIGHT[2]	BG_TOTAL_FIELD_HEIGHT[1]	BG_TOTAL_FIELD_HEIGHT[0]
0xEA	0x00	HDMI_REG_EA	r	BG_PIX_REP[3]	BG_PIX_REP[2]	BG_PIX_REP[1]	BG_PIX_REP[0]	BG_DEEP_COLOR_MODE[1]	BG_DEEP_COLOR_MODE[0]	BG_PARAM_LOCK	BG_HDMI_INTERLACED
0xEB	0x00	HDMI_REG_EB	r	-	-	-	-	-	-	-	BG_HDMI_MODE
0xEE	0x00	HDMI_REG_EE	r	-	-	BG_AUDIO_LAYOUT	BG_DST_DOUBLE	BG_AUDIO_DETECTED[3]	BG_AUDIO_DETECTED[2]	BG_AUDIO_DETECTED[1]	BG_AUDIO_DETECTED[0]
0xEF	0x82	HDMI_REG_EF	rw	BG_HEADER_REQUESTED[7]	BG_HEADER_REQUESTED[6]	BG_HEADER_REQUESTED[5]	BG_HEADER_REQUESTED[4]	BG_HEADER_REQUESTED[3]	BG_HEADER_REQUESTED[2]	BG_HEADER_REQUESTED[1]	BG_HEADER_REQUESTED[0]
0xF0	0x00	HDMI_REG_F0	r	BG_HEADER_BYTE1[7]	BG_HEADER_BYTE1[6]	BG_HEADER_BYTE1[5]	BG_HEADER_BYTE1[4]	BG_HEADER_BYTE1[3]	BG_HEADER_BYTE1[2]	BG_HEADER_BYTE1[1]	BG_HEADER_BYTE1[0]
0xF1	0x00	HDMI_REG_F1	r	BG_PACKET_BYTE1[7]	BG_PACKET_BYTE1[6]	BG_PACKET_BYTE1[5]	BG_PACKET_BYTE1[4]	BG_PACKET_BYTE1[3]	BG_PACKET_BYTE1[2]	BG_PACKET_BYTE1[1]	BG_PACKET_BYTE1[0]
0xF2	0x00	HDMI_REG_F2	r	BG_PACKET_BYTE2[7]	BG_PACKET_BYTE2[6]	BG_PACKET_BYTE2[5]	BG_PACKET_BYTE2[4]	BG_PACKET_BYTE2[3]	BG_PACKET_BYTE2[2]	BG_PACKET_BYTE2[1]	BG_PACKET_BYTE2[0]
0xF3	0x00	HDMI_REG_F3	r	BG_PACKET_BYTE3[7]	BG_PACKET_BYTE3[6]	BG_PACKET_BYTE3[5]	BG_PACKET_BYTE3[4]	BG_PACKET_BYTE3[3]	BG_PACKET_BYTE3[2]	BG_PACKET_BYTE3[1]	BG_PACKET_BYTE3[0]
0xF4	0x00	HDMI_REG_F4	r	BG_PACKET_BYTE4[7]	BG_PACKET_BYTE4[6]	BG_PACKET_BYTE4[5]	BG_PACKET_BYTE4[4]	BG_PACKET_BYTE4[3]	BG_PACKET_BYTE4[2]	BG_PACKET_BYTE4[1]	BG_PACKET_BYTE4[0]
0xF5	0x00	HDMI_REG_F5	r	BG_PACKET_BYTE5[7]	BG_PACKET_BYTE5[6]	BG_PACKET_BYTE5[5]	BG_PACKET_BYTE5[4]	BG_PACKET_BYTE5[3]	BG_PACKET_BYTE5[2]	BG_PACKET_BYTE5[1]	BG_PACKET_BYTE5[0]
0xF6	0x00	HDMI_REG_F6	r	-	-	-	-	-	-	-	BG_VALID_PACKET

1.3 REPEATER MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00	REPEATER_REG_00	r	BKSV[7]	BKSV[6]	BKSV[5]	BKSV[4]	BKSV[3]	BKSV[2]	BKSV[1]	BKSV[0]
0x01	0x00	REPEATER_REG_01	r	BKSV[15]	BKSV[14]	BKSV[13]	BKSV[12]	BKSV[11]	BKSV[10]	BKSV[9]	BKSV[8]
0x02	0x00	REPEATER_REG_02	r	BKSV[23]	BKSV[22]	BKSV[21]	BKSV[20]	BKSV[19]	BKSV[18]	BKSV[17]	BKSV[16]
0x03	0x00	REPEATER_REG_03	r	BKSV[31]	BKSV[30]	BKSV[29]	BKSV[28]	BKSV[27]	BKSV[26]	BKSV[25]	BKSV[24]
0x04	0x00	REPEATER_REG_04	r	BKSV[39]	BKSV[38]	BKSV[37]	BKSV[36]	BKSV[35]	BKSV[34]	BKSV[33]	BKSV[32]
0x08	0x00	REPEATER_REG_08	r	RI[7]	RI[6]	RI[5]	RI[4]	RI[3]	RI[2]	RI[1]	RI[0]
0x09	0x00	REPEATER_REG_09	r	RI[15]	RI[14]	RI[13]	RI[12]	RI[11]	RI[10]	RI[9]	RI[8]
0x0A	0x00	REPEATER_REG_0A	r	PJ[7]	PJ[6]	PJ[5]	PJ[4]	PJ[3]	PJ[2]	PJ[1]	PJ[0]
0x10	0x00	REPEATER_REG_10	rw	AKSV[7]	AKSV[6]	AKSV[5]	AKSV[4]	AKSV[3]	AKSV[2]	AKSV[1]	AKSV[0]
0x11	0x00	REPEATER_REG_11	rw	AKSV[15]	AKSV[14]	AKSV[13]	AKSV[12]	AKSV[11]	AKSV[10]	AKSV[9]	AKSV[8]
0x12	0x00	REPEATER_REG_12	rw	AKSV[23]	AKSV[22]	AKSV[21]	AKSV[20]	AKSV[19]	AKSV[18]	AKSV[17]	AKSV[16]
0x13	0x00	REPEATER_REG_13	rw	AKSV[31]	AKSV[30]	AKSV[29]	AKSV[28]	AKSV[27]	AKSV[26]	AKSV[25]	AKSV[24]
0x14	0x00	REPEATER_REG_14	rw	AKSV[39]	AKSV[38]	AKSV[37]	AKSV[36]	AKSV[35]	AKSV[34]	AKSV[33]	AKSV[32]
0x15	0x00	REPEATER_REG_15	rw	AINFO[7]	AINFO[6]	AINFO[5]	AINFO[4]	AINFO[3]	AINFO[2]	AINFO[1]	AINFO[0]
0x16	0x00	REPEATER_REG_16	r	AINFO_RB[7]	AINFO_RB[6]	AINFO_RB[5]	AINFO_RB[4]	AINFO_RB[3]	AINFO_RB[2]	AINFO_RB[1]	AINFO_RB[0]
0x18	0x00	REPEATER_REG_18	rw	AN[7]	AN[6]	AN[5]	AN[4]	AN[3]	AN[2]	AN[1]	AN[0]
0x19	0x00	REPEATER_REG_19	rw	AN[15]	AN[14]	AN[13]	AN[12]	AN[11]	AN[10]	AN[9]	AN[8]
0x1A	0x00	REPEATER_REG_1A	rw	AN[23]	AN[22]	AN[21]	AN[20]	AN[19]	AN[18]	AN[17]	AN[16]
0x1B	0x00	REPEATER_REG_1B	rw	AN[31]	AN[30]	AN[29]	AN[28]	AN[27]	AN[26]	AN[25]	AN[24]
0x1C	0x00	REPEATER_REG_1C	rw	AN[39]	AN[38]	AN[37]	AN[36]	AN[35]	AN[34]	AN[33]	AN[32]
0x1D	0x00	REPEATER_REG_1D	rw	AN[47]	AN[46]	AN[45]	AN[44]	AN[43]	AN[42]	AN[41]	AN[40]
0x1E	0x00	REPEATER_REG_1E	rw	AN[55]	AN[54]	AN[53]	AN[52]	AN[51]	AN[50]	AN[49]	AN[48]
0x1F	0x00	REPEATER_REG_1F	rw	AN[63]	AN[62]	AN[61]	AN[60]	AN[59]	AN[58]	AN[57]	AN[56]
0x20	0x00	REPEATER_REG_20	rw	SHA_A[7]	SHA_A[6]	SHA_A[5]	SHA_A[4]	SHA_A[3]	SHA_A[2]	SHA_A[1]	SHA_A[0]
0x21	0x00	REPEATER_REG_21	rw	SHA_A[15]	SHA_A[14]	SHA_A[13]	SHA_A[12]	SHA_A[11]	SHA_A[10]	SHA_A[9]	SHA_A[8]
0x22	0x00	REPEATER_REG_22	rw	SHA_A[23]	SHA_A[22]	SHA_A[21]	SHA_A[20]	SHA_A[19]	SHA_A[18]	SHA_A[17]	SHA_A[16]
0x23	0x00	REPEATER_REG_23	rw	SHA_A[31]	SHA_A[30]	SHA_A[29]	SHA_A[28]	SHA_A[27]	SHA_A[26]	SHA_A[25]	SHA_A[24]
0x24	0x00	REPEATER_REG_24	rw	SHA_B[7]	SHA_B[6]	SHA_B[5]	SHA_B[4]	SHA_B[3]	SHA_B[2]	SHA_B[1]	SHA_B[0]
0x25	0x00	REPEATER_REG_25	rw	SHA_B[15]	SHA_B[14]	SHA_B[13]	SHA_B[12]	SHA_B[11]	SHA_B[10]	SHA_B[9]	SHA_B[8]
0x26	0x00	REPEATER_REG_26	rw	SHA_B[23]	SHA_B[22]	SHA_B[21]	SHA_B[20]	SHA_B[19]	SHA_B[18]	SHA_B[17]	SHA_B[16]
0x27	0x00	REPEATER_REG_27	rw	SHA_B[31]	SHA_B[30]	SHA_B[29]	SHA_B[28]	SHA_B[27]	SHA_B[26]	SHA_B[25]	SHA_B[24]
0x28	0x00	REPEATER_REG_28	rw	SHA_C[7]	SHA_C[6]	SHA_C[5]	SHA_C[4]	SHA_C[3]	SHA_C[2]	SHA_C[1]	SHA_C[0]
0x29	0x00	REPEATER_REG_29	rw	SHA_C[15]	SHA_C[14]	SHA_C[13]	SHA_C[12]	SHA_C[11]	SHA_C[10]	SHA_C[9]	SHA_C[8]
0x2A	0x00	REPEATER_REG_2A	rw	SHA_C[23]	SHA_C[22]	SHA_C[21]	SHA_C[20]	SHA_C[19]	SHA_C[18]	SHA_C[17]	SHA_C[16]
0x2B	0x00	REPEATER_REG_2B	rw	SHA_C[31]	SHA_C[30]	SHA_C[29]	SHA_C[28]	SHA_C[27]	SHA_C[26]	SHA_C[25]	SHA_C[24]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x2C	0x00	REPEATER_REG_2C	rw	SHA_D[7]	SHA_D[6]	SHA_D[5]	SHA_D[4]	SHA_D[3]	SHA_D[2]	SHA_D[1]	SHA_D[0]
0x2D	0x00	REPEATER_REG_2D	rw	SHA_D[15]	SHA_D[14]	SHA_D[13]	SHA_D[12]	SHA_D[11]	SHA_D[10]	SHA_D[9]	SHA_D[8]
0x2E	0x00	REPEATER_REG_2E	rw	SHA_D[23]	SHA_D[22]	SHA_D[21]	SHA_D[20]	SHA_D[19]	SHA_D[18]	SHA_D[17]	SHA_D[16]
0x2F	0x00	REPEATER_REG_2F	rw	SHA_D[31]	SHA_D[30]	SHA_D[29]	SHA_D[28]	SHA_D[27]	SHA_D[26]	SHA_D[25]	SHA_D[24]
0x30	0x00	REPEATER_REG_30	rw	SHA_E[7]	SHA_E[6]	SHA_E[5]	SHA_E[4]	SHA_E[3]	SHA_E[2]	SHA_E[1]	SHA_E[0]
0x31	0x00	REPEATER_REG_31	rw	SHA_E[15]	SHA_E[14]	SHA_E[13]	SHA_E[12]	SHA_E[11]	SHA_E[10]	SHA_E[9]	SHA_E[8]
0x32	0x00	REPEATER_REG_32	rw	SHA_E[23]	SHA_E[22]	SHA_E[21]	SHA_E[20]	SHA_E[19]	SHA_E[18]	SHA_E[17]	SHA_E[16]
0x33	0x00	REPEATER_REG_33	rw	SHA_E[31]	SHA_E[30]	SHA_E[29]	SHA_E[28]	SHA_E[27]	SHA_E[26]	SHA_E[25]	SHA_E[24]
0x40	0x83	REPEATER_REG_40	rw	BCAPS[7]	BCAPS[6]	BCAPS[5]	BCAPS[4]	BCAPS[3]	BCAPS[2]	BCAPS[1]	BCAPS[0]
0x41	0x00	REPEATER_REG_41	rw	BSTATUS[7]	BSTATUS[6]	BSTATUS[5]	BSTATUS[4]	BSTATUS[3]	BSTATUS[2]	BSTATUS[1]	BSTATUS[0]
0x42	0x00	REPEATER_REG_42	rw	BSTATUS[15]	BSTATUS[14]	BSTATUS[13]	BSTATUS[12]	BSTATUS[11]	BSTATUS[10]	BSTATUS[9]	BSTATUS[8]
0x52	0x00	REPEATER_REG_52	rw	SPA_PORT_B[15]	SPA_PORT_B[14]	SPA_PORT_B[13]	SPA_PORT_B[12]	SPA_PORT_B[11]	SPA_PORT_B[10]	SPA_PORT_B[9]	SPA_PORT_B[8]
0x53	0x00	REPEATER_REG_53	rw	SPA_PORT_B[7]	SPA_PORT_B[6]	SPA_PORT_B[5]	SPA_PORT_B[4]	SPA_PORT_B[3]	SPA_PORT_B[2]	SPA_PORT_B[1]	SPA_PORT_B[0]
0x54	0x00	REPEATER_REG_54	rw	SPA_PORT_C[15]	SPA_PORT_C[14]	SPA_PORT_C[13]	SPA_PORT_C[12]	SPA_PORT_C[11]	SPA_PORT_C[10]	SPA_PORT_C[9]	SPA_PORT_C[8]
0x55	0x00	REPEATER_REG_55	rw	SPA_PORT_C[7]	SPA_PORT_C[6]	SPA_PORT_C[5]	SPA_PORT_C[4]	SPA_PORT_C[3]	SPA_PORT_C[2]	SPA_PORT_C[1]	SPA_PORT_C[0]
0x56	0x00	REPEATER_REG_56	rw	SPA_PORT_D[15]	SPA_PORT_D[14]	SPA_PORT_D[13]	SPA_PORT_D[12]	SPA_PORT_D[11]	SPA_PORT_D[10]	SPA_PORT_D[9]	SPA_PORT_D[8]
0x57	0x00	REPEATER_REG_57	rw	SPA_PORT_D[7]	SPA_PORT_D[6]	SPA_PORT_D[5]	SPA_PORT_D[4]	SPA_PORT_D[3]	SPA_PORT_D[2]	SPA_PORT_D[1]	SPA_PORT_D[0]
0x61	0x00	REPEATER_REG_61	rw	PORT_B_CHECKSUM[7]	PORT_B_CHECKSUM[6]	PORT_B_CHECKSUM[5]	PORT_B_CHECKSUM[4]	PORT_B_CHECKSUM[3]	PORT_B_CHECKSUM[2]	PORT_B_CHECKSUM[1]	PORT_B_CHECKSUM[0]
0x62	0x00	REPEATER_REG_62	rw	PORT_C_CHECKSUM[7]	PORT_C_CHECKSUM[6]	PORT_C_CHECKSUM[5]	PORT_C_CHECKSUM[4]	PORT_C_CHECKSUM[3]	PORT_C_CHECKSUM[2]	PORT_C_CHECKSUM[1]	PORT_C_CHECKSUM[0]
0x63	0x00	REPEATER_REG_63	rw	PORT_D_CHECKSUM[7]	PORT_D_CHECKSUM[6]	PORT_D_CHECKSUM[5]	PORT_D_CHECKSUM[4]	PORT_D_CHECKSUM[3]	PORT_D_CHECKSUM[2]	PORT_D_CHECKSUM[1]	PORT_D_CHECKSUM[0]
0x70	0xC0	REPEATER_REG_70	rw	SPA_LOCATION[7]	SPA_LOCATION[6]	SPA_LOCATION[5]	SPA_LOCATION[4]	SPA_LOCATION[3]	SPA_LOCATION[2]	SPA_LOCATION[1]	SPA_LOCATION[0]
0x71	0x00	REPEATER_REG_71	rw	KSV_LIST_READY	-	-	-	-	-	-	SPA_LOCATION_MSB
0x72	0x00	REPEATER_REG_72	rw	-	EXT_EEPROM_TRI	EXT_EEPROM_MAN_SELECT	EXT_EEPROM_MAN_VALUE	-	-	-	-
0x74	0x00	REPEATER_REG_74	rw	-	-	-	-	MAN_EDID_D_ENABLE	MAN_EDID_C_ENABLE	MAN_EDID_B_ENABLE	MAN_EDID_A_ENABLE
0x76	0x00	REPEATER_REG_76	r	-	-	-	-	EDID_D_ENABLED	EDID_C_ENABLED	EDID_B_ENABLED	EDID_A_ENABLED
0x77	0x00	REPEATER_REG_77	sc	-	-	-	-	CLEAR_KSV_LIST	CKSUM_CALC	LOAD_EDID	STORE_EDID
0x78	0x00	REPEATER_REG_78	sc	-	-	-	-	KSV_LIST_READY_CLR_D	KSV_LIST_READY_CLR_C	KSV_LIST_READY_CLR_B	KSV_LIST_READY_CLR_A
0x79	0x88	REPEATER_REG_79	rw	-	KSV_MAP_SELECT[2]	KSV_MAP_SELECT[1]	KSV_MAP_SELECT[0]	AUTO_HDCP_MAP_ENABLE	HDCP_MAP_SELECT[2]	HDCP_MAP_SELECT[1]	HDCP_MAP_SELECT[0]
0x7A	0x04	REPEATER_REG_7A	rw	-	-	-	-	DISABLE_AUTO_EDID	-	-	HDMI_EDID_SEGMENT_SEL
0x7C	0x00	REPEATER_REG_7C	rw	-	-	SPI_CFG[5]	SPI_CFG[4]	SPI_CFG[3]	SPI_CFG[2]	SPI_CFG[1]	SPI_CFG[0]
0x7D	0x00	REPEATER_REG_7D	rw	-	-	-	-	DUAL_EDID_ENABLE_PORT_D	DUAL_EDID_ENABLE_PORT_C	DUAL_EDID_ENABLE_PORT_B	DUAL_EDID_ENABLE_PORT_A

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x7E	0xC0	REPEATER_REG_7E	rw	SPA_SECONDARY_LOCATION[7]	SPA_SECONDARY_LOCATION[6]	SPA_SECONDARY_LOCATION[5]	SPA_SECONDARY_LOCATION[4]	SPA_SECONDARY_LOCATION[3]	SPA_SECONDARY_LOCATION[2]	SPA_SECONDARY_LOCATION[1]	SPA_SECONDARY_LOCATION[0]
0x80	0x00	REPEATER_REG_80	rw	KSV_BYTE_0[7]	KSV_BYTE_0[6]	KSV_BYTE_0[5]	KSV_BYTE_0[4]	KSV_BYTE_0[3]	KSV_BYTE_0[2]	KSV_BYTE_0[1]	KSV_BYTE_0[0]
0x81	0x00	REPEATER_REG_81	rw	KSV_BYTE_1[7]	KSV_BYTE_1[6]	KSV_BYTE_1[5]	KSV_BYTE_1[4]	KSV_BYTE_1[3]	KSV_BYTE_1[2]	KSV_BYTE_1[1]	KSV_BYTE_1[0]
0x82	0x00	REPEATER_REG_82	rw	KSV_BYTE_2[7]	KSV_BYTE_2[6]	KSV_BYTE_2[5]	KSV_BYTE_2[4]	KSV_BYTE_2[3]	KSV_BYTE_2[2]	KSV_BYTE_2[1]	KSV_BYTE_2[0]
0x83	0x00	REPEATER_REG_83	rw	KSV_BYTE_3[7]	KSV_BYTE_3[6]	KSV_BYTE_3[5]	KSV_BYTE_3[4]	KSV_BYTE_3[3]	KSV_BYTE_3[2]	KSV_BYTE_3[1]	KSV_BYTE_3[0]
0x84	0x00	REPEATER_REG_84	rw	KSV_BYTE_4[7]	KSV_BYTE_4[6]	KSV_BYTE_4[5]	KSV_BYTE_4[4]	KSV_BYTE_4[3]	KSV_BYTE_4[2]	KSV_BYTE_4[1]	KSV_BYTE_4[0]
0x85	0x00	REPEATER_REG_85	rw	KSV_BYTE_5[7]	KSV_BYTE_5[6]	KSV_BYTE_5[5]	KSV_BYTE_5[4]	KSV_BYTE_5[3]	KSV_BYTE_5[2]	KSV_BYTE_5[1]	KSV_BYTE_5[0]
0x86	0x00	REPEATER_REG_86	rw	KSV_BYTE_6[7]	KSV_BYTE_6[6]	KSV_BYTE_6[5]	KSV_BYTE_6[4]	KSV_BYTE_6[3]	KSV_BYTE_6[2]	KSV_BYTE_6[1]	KSV_BYTE_6[0]
0x87	0x00	REPEATER_REG_87	rw	KSV_BYTE_7[7]	KSV_BYTE_7[6]	KSV_BYTE_7[5]	KSV_BYTE_7[4]	KSV_BYTE_7[3]	KSV_BYTE_7[2]	KSV_BYTE_7[1]	KSV_BYTE_7[0]
0x88	0x00	REPEATER_REG_88	rw	KSV_BYTE_8[7]	KSV_BYTE_8[6]	KSV_BYTE_8[5]	KSV_BYTE_8[4]	KSV_BYTE_8[3]	KSV_BYTE_8[2]	KSV_BYTE_8[1]	KSV_BYTE_8[0]
0x89	0x00	REPEATER_REG_89	rw	KSV_BYTE_9[7]	KSV_BYTE_9[6]	KSV_BYTE_9[5]	KSV_BYTE_9[4]	KSV_BYTE_9[3]	KSV_BYTE_9[2]	KSV_BYTE_9[1]	KSV_BYTE_9[0]
0x8A	0x00	REPEATER_REG_8A	rw	KSV_BYTE_10[7]	KSV_BYTE_10[6]	KSV_BYTE_10[5]	KSV_BYTE_10[4]	KSV_BYTE_10[3]	KSV_BYTE_10[2]	KSV_BYTE_10[1]	KSV_BYTE_10[0]
0x8B	0x00	REPEATER_REG_8B	rw	KSV_BYTE_11[7]	KSV_BYTE_11[6]	KSV_BYTE_11[5]	KSV_BYTE_11[4]	KSV_BYTE_11[3]	KSV_BYTE_11[2]	KSV_BYTE_11[1]	KSV_BYTE_11[0]
0x8C	0x00	REPEATER_REG_8C	rw	KSV_BYTE_12[7]	KSV_BYTE_12[6]	KSV_BYTE_12[5]	KSV_BYTE_12[4]	KSV_BYTE_12[3]	KSV_BYTE_12[2]	KSV_BYTE_12[1]	KSV_BYTE_12[0]
0x8D	0x00	REPEATER_REG_8D	rw	KSV_BYTE_13[7]	KSV_BYTE_13[6]	KSV_BYTE_13[5]	KSV_BYTE_13[4]	KSV_BYTE_13[3]	KSV_BYTE_13[2]	KSV_BYTE_13[1]	KSV_BYTE_13[0]
0x8E	0x00	REPEATER_REG_8E	rw	KSV_BYTE_14[7]	KSV_BYTE_14[6]	KSV_BYTE_14[5]	KSV_BYTE_14[4]	KSV_BYTE_14[3]	KSV_BYTE_14[2]	KSV_BYTE_14[1]	KSV_BYTE_14[0]
0x8F	0x00	REPEATER_REG_8F	rw	KSV_BYTE_15[7]	KSV_BYTE_15[6]	KSV_BYTE_15[5]	KSV_BYTE_15[4]	KSV_BYTE_15[3]	KSV_BYTE_15[2]	KSV_BYTE_15[1]	KSV_BYTE_15[0]
0x90	0x00	REPEATER_REG_90	rw	KSV_BYTE_16[7]	KSV_BYTE_16[6]	KSV_BYTE_16[5]	KSV_BYTE_16[4]	KSV_BYTE_16[3]	KSV_BYTE_16[2]	KSV_BYTE_16[1]	KSV_BYTE_16[0]
0x91	0x00	REPEATER_REG_91	rw	KSV_BYTE_17[7]	KSV_BYTE_17[6]	KSV_BYTE_17[5]	KSV_BYTE_17[4]	KSV_BYTE_17[3]	KSV_BYTE_17[2]	KSV_BYTE_17[1]	KSV_BYTE_17[0]
0x92	0x00	REPEATER_REG_92	rw	KSV_BYTE_18[7]	KSV_BYTE_18[6]	KSV_BYTE_18[5]	KSV_BYTE_18[4]	KSV_BYTE_18[3]	KSV_BYTE_18[2]	KSV_BYTE_18[1]	KSV_BYTE_18[0]
0x93	0x00	REPEATER_REG_93	rw	KSV_BYTE_19[7]	KSV_BYTE_19[6]	KSV_BYTE_19[5]	KSV_BYTE_19[4]	KSV_BYTE_19[3]	KSV_BYTE_19[2]	KSV_BYTE_19[1]	KSV_BYTE_19[0]
0x94	0x00	REPEATER_REG_94	rw	KSV_BYTE_20[7]	KSV_BYTE_20[6]	KSV_BYTE_20[5]	KSV_BYTE_20[4]	KSV_BYTE_20[3]	KSV_BYTE_20[2]	KSV_BYTE_20[1]	KSV_BYTE_20[0]
0x95	0x00	REPEATER_REG_95	rw	KSV_BYTE_21[7]	KSV_BYTE_21[6]	KSV_BYTE_21[5]	KSV_BYTE_21[4]	KSV_BYTE_21[3]	KSV_BYTE_21[2]	KSV_BYTE_21[1]	KSV_BYTE_21[0]
0x96	0x00	REPEATER_REG_96	rw	KSV_BYTE_22[7]	KSV_BYTE_22[6]	KSV_BYTE_22[5]	KSV_BYTE_22[4]	KSV_BYTE_22[3]	KSV_BYTE_22[2]	KSV_BYTE_22[1]	KSV_BYTE_22[0]
0x97	0x00	REPEATER_REG_97	rw	KSV_BYTE_23[7]	KSV_BYTE_23[6]	KSV_BYTE_23[5]	KSV_BYTE_23[4]	KSV_BYTE_23[3]	KSV_BYTE_23[2]	KSV_BYTE_23[1]	KSV_BYTE_23[0]
0x98	0x00	REPEATER_REG_98	rw	KSV_BYTE_24[7]	KSV_BYTE_24[6]	KSV_BYTE_24[5]	KSV_BYTE_24[4]	KSV_BYTE_24[3]	KSV_BYTE_24[2]	KSV_BYTE_24[1]	KSV_BYTE_24[0]
0x99	0x00	REPEATER_REG_99	rw	KSV_BYTE_25[7]	KSV_BYTE_25[6]	KSV_BYTE_25[5]	KSV_BYTE_25[4]	KSV_BYTE_25[3]	KSV_BYTE_25[2]	KSV_BYTE_25[1]	KSV_BYTE_25[0]
0x9A	0x00	REPEATER_REG_9A	rw	KSV_BYTE_26[7]	KSV_BYTE_26[6]	KSV_BYTE_26[5]	KSV_BYTE_26[4]	KSV_BYTE_26[3]	KSV_BYTE_26[2]	KSV_BYTE_26[1]	KSV_BYTE_26[0]
0x9B	0x00	REPEATER_REG_9B	rw	KSV_BYTE_27[7]	KSV_BYTE_27[6]	KSV_BYTE_27[5]	KSV_BYTE_27[4]	KSV_BYTE_27[3]	KSV_BYTE_27[2]	KSV_BYTE_27[1]	KSV_BYTE_27[0]
0x9C	0x00	REPEATER_REG_9C	rw	KSV_BYTE_28[7]	KSV_BYTE_28[6]	KSV_BYTE_28[5]	KSV_BYTE_28[4]	KSV_BYTE_28[3]	KSV_BYTE_28[2]	KSV_BYTE_28[1]	KSV_BYTE_28[0]
0x9D	0x00	REPEATER_REG_9D	rw	KSV_BYTE_29[7]	KSV_BYTE_29[6]	KSV_BYTE_29[5]	KSV_BYTE_29[4]	KSV_BYTE_29[3]	KSV_BYTE_29[2]	KSV_BYTE_29[1]	KSV_BYTE_29[0]
0x9E	0x00	REPEATER_REG_9E	rw	KSV_BYTE_30[7]	KSV_BYTE_30[6]	KSV_BYTE_30[5]	KSV_BYTE_30[4]	KSV_BYTE_30[3]	KSV_BYTE_30[2]	KSV_BYTE_30[1]	KSV_BYTE_30[0]
0x9F	0x00	REPEATER_REG_9F	rw	KSV_BYTE_31[7]	KSV_BYTE_31[6]	KSV_BYTE_31[5]	KSV_BYTE_31[4]	KSV_BYTE_31[3]	KSV_BYTE_31[2]	KSV_BYTE_31[1]	KSV_BYTE_31[0]
0xA0	0x00	REPEATER_REG_A0	rw	KSV_BYTE_32[7]	KSV_BYTE_32[6]	KSV_BYTE_32[5]	KSV_BYTE_32[4]	KSV_BYTE_32[3]	KSV_BYTE_32[2]	KSV_BYTE_32[1]	KSV_BYTE_32[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xA1	0x00	REPEATER_REG_A1	rw	KSV_BYTE_33[7]	KSV_BYTE_33[6]	KSV_BYTE_33[5]	KSV_BYTE_33[4]	KSV_BYTE_33[3]	KSV_BYTE_33[2]	KSV_BYTE_33[1]	KSV_BYTE_33[0]
0xA2	0x00	REPEATER_REG_A2	rw	KSV_BYTE_34[7]	KSV_BYTE_34[6]	KSV_BYTE_34[5]	KSV_BYTE_34[4]	KSV_BYTE_34[3]	KSV_BYTE_34[2]	KSV_BYTE_34[1]	KSV_BYTE_34[0]
0xA3	0x00	REPEATER_REG_A3	rw	KSV_BYTE_35[7]	KSV_BYTE_35[6]	KSV_BYTE_35[5]	KSV_BYTE_35[4]	KSV_BYTE_35[3]	KSV_BYTE_35[2]	KSV_BYTE_35[1]	KSV_BYTE_35[0]
0xA4	0x00	REPEATER_REG_A4	rw	KSV_BYTE_36[7]	KSV_BYTE_36[6]	KSV_BYTE_36[5]	KSV_BYTE_36[4]	KSV_BYTE_36[3]	KSV_BYTE_36[2]	KSV_BYTE_36[1]	KSV_BYTE_36[0]
0xA5	0x00	REPEATER_REG_A5	rw	KSV_BYTE_37[7]	KSV_BYTE_37[6]	KSV_BYTE_37[5]	KSV_BYTE_37[4]	KSV_BYTE_37[3]	KSV_BYTE_37[2]	KSV_BYTE_37[1]	KSV_BYTE_37[0]
0xA6	0x00	REPEATER_REG_A6	rw	KSV_BYTE_38[7]	KSV_BYTE_38[6]	KSV_BYTE_38[5]	KSV_BYTE_38[4]	KSV_BYTE_38[3]	KSV_BYTE_38[2]	KSV_BYTE_38[1]	KSV_BYTE_38[0]
0xA7	0x00	REPEATER_REG_A7	rw	KSV_BYTE_39[7]	KSV_BYTE_39[6]	KSV_BYTE_39[5]	KSV_BYTE_39[4]	KSV_BYTE_39[3]	KSV_BYTE_39[2]	KSV_BYTE_39[1]	KSV_BYTE_39[0]
0xA8	0x00	REPEATER_REG_A8	rw	KSV_BYTE_40[7]	KSV_BYTE_40[6]	KSV_BYTE_40[5]	KSV_BYTE_40[4]	KSV_BYTE_40[3]	KSV_BYTE_40[2]	KSV_BYTE_40[1]	KSV_BYTE_40[0]
0xA9	0x00	REPEATER_REG_A9	rw	KSV_BYTE_41[7]	KSV_BYTE_41[6]	KSV_BYTE_41[5]	KSV_BYTE_41[4]	KSV_BYTE_41[3]	KSV_BYTE_41[2]	KSV_BYTE_41[1]	KSV_BYTE_41[0]
0xAA	0x00	REPEATER_REG_AA	rw	KSV_BYTE_42[7]	KSV_BYTE_42[6]	KSV_BYTE_42[5]	KSV_BYTE_42[4]	KSV_BYTE_42[3]	KSV_BYTE_42[2]	KSV_BYTE_42[1]	KSV_BYTE_42[0]
0xAB	0x00	REPEATER_REG_AB	rw	KSV_BYTE_43[7]	KSV_BYTE_43[6]	KSV_BYTE_43[5]	KSV_BYTE_43[4]	KSV_BYTE_43[3]	KSV_BYTE_43[2]	KSV_BYTE_43[1]	KSV_BYTE_43[0]
0xAC	0x00	REPEATER_REG_AC	rw	KSV_BYTE_44[7]	KSV_BYTE_44[6]	KSV_BYTE_44[5]	KSV_BYTE_44[4]	KSV_BYTE_44[3]	KSV_BYTE_44[2]	KSV_BYTE_44[1]	KSV_BYTE_44[0]
0xAD	0x00	REPEATER_REG_AD	rw	KSV_BYTE_45[7]	KSV_BYTE_45[6]	KSV_BYTE_45[5]	KSV_BYTE_45[4]	KSV_BYTE_45[3]	KSV_BYTE_45[2]	KSV_BYTE_45[1]	KSV_BYTE_45[0]
0xAE	0x00	REPEATER_REG_AE	rw	KSV_BYTE_46[7]	KSV_BYTE_46[6]	KSV_BYTE_46[5]	KSV_BYTE_46[4]	KSV_BYTE_46[3]	KSV_BYTE_46[2]	KSV_BYTE_46[1]	KSV_BYTE_46[0]
0xAF	0x00	REPEATER_REG_AF	rw	KSV_BYTE_47[7]	KSV_BYTE_47[6]	KSV_BYTE_47[5]	KSV_BYTE_47[4]	KSV_BYTE_47[3]	KSV_BYTE_47[2]	KSV_BYTE_47[1]	KSV_BYTE_47[0]
0xB0	0x00	REPEATER_REG_B0	rw	KSV_BYTE_48[7]	KSV_BYTE_48[6]	KSV_BYTE_48[5]	KSV_BYTE_48[4]	KSV_BYTE_48[3]	KSV_BYTE_48[2]	KSV_BYTE_48[1]	KSV_BYTE_48[0]
0xB1	0x00	REPEATER_REG_B1	rw	KSV_BYTE_49[7]	KSV_BYTE_49[6]	KSV_BYTE_49[5]	KSV_BYTE_49[4]	KSV_BYTE_49[3]	KSV_BYTE_49[2]	KSV_BYTE_49[1]	KSV_BYTE_49[0]
0xB2	0x00	REPEATER_REG_B2	rw	KSV_BYTE_50[7]	KSV_BYTE_50[6]	KSV_BYTE_50[5]	KSV_BYTE_50[4]	KSV_BYTE_50[3]	KSV_BYTE_50[2]	KSV_BYTE_50[1]	KSV_BYTE_50[0]
0xB3	0x00	REPEATER_REG_B3	rw	KSV_BYTE_51[7]	KSV_BYTE_51[6]	KSV_BYTE_51[5]	KSV_BYTE_51[4]	KSV_BYTE_51[3]	KSV_BYTE_51[2]	KSV_BYTE_51[1]	KSV_BYTE_51[0]
0xB4	0x00	REPEATER_REG_B4	rw	KSV_BYTE_52[7]	KSV_BYTE_52[6]	KSV_BYTE_52[5]	KSV_BYTE_52[4]	KSV_BYTE_52[3]	KSV_BYTE_52[2]	KSV_BYTE_52[1]	KSV_BYTE_52[0]
0xB5	0x00	REPEATER_REG_B5	rw	KSV_BYTE_53[7]	KSV_BYTE_53[6]	KSV_BYTE_53[5]	KSV_BYTE_53[4]	KSV_BYTE_53[3]	KSV_BYTE_53[2]	KSV_BYTE_53[1]	KSV_BYTE_53[0]
0xB6	0x00	REPEATER_REG_B6	rw	KSV_BYTE_54[7]	KSV_BYTE_54[6]	KSV_BYTE_54[5]	KSV_BYTE_54[4]	KSV_BYTE_54[3]	KSV_BYTE_54[2]	KSV_BYTE_54[1]	KSV_BYTE_54[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xB7	0x00	REPEATER_REG_B7	rw	KSV_BYTE_55[7]	KSV_BYTE_55[6]	KSV_BYTE_55[5]	KSV_BYTE_55[4]	KSV_BYTE_55[3]	KSV_BYTE_55[2]	KSV_BYTE_55[1]	KSV_BYTE_55[0]
0xB8	0x00	REPEATER_REG_B8	rw	KSV_BYTE_56[7]	KSV_BYTE_56[6]	KSV_BYTE_56[5]	KSV_BYTE_56[4]	KSV_BYTE_56[3]	KSV_BYTE_56[2]	KSV_BYTE_56[1]	KSV_BYTE_56[0]
0xB9	0x00	REPEATER_REG_B9	rw	KSV_BYTE_57[7]	KSV_BYTE_57[6]	KSV_BYTE_57[5]	KSV_BYTE_57[4]	KSV_BYTE_57[3]	KSV_BYTE_57[2]	KSV_BYTE_57[1]	KSV_BYTE_57[0]
0xBA	0x00	REPEATER_REG_BA	rw	KSV_BYTE_58[7]	KSV_BYTE_58[6]	KSV_BYTE_58[5]	KSV_BYTE_58[4]	KSV_BYTE_58[3]	KSV_BYTE_58[2]	KSV_BYTE_58[1]	KSV_BYTE_58[0]
0xBB	0x00	REPEATER_REG_BB	rw	KSV_BYTE_59[7]	KSV_BYTE_59[6]	KSV_BYTE_59[5]	KSV_BYTE_59[4]	KSV_BYTE_59[3]	KSV_BYTE_59[2]	KSV_BYTE_59[1]	KSV_BYTE_59[0]
0xBC	0x00	REPEATER_REG_BC	rw	KSV_BYTE_60[7]	KSV_BYTE_60[6]	KSV_BYTE_60[5]	KSV_BYTE_60[4]	KSV_BYTE_60[3]	KSV_BYTE_60[2]	KSV_BYTE_60[1]	KSV_BYTE_60[0]
0xBD	0x00	REPEATER_REG_BD	rw	KSV_BYTE_61[7]	KSV_BYTE_61[6]	KSV_BYTE_61[5]	KSV_BYTE_61[4]	KSV_BYTE_61[3]	KSV_BYTE_61[2]	KSV_BYTE_61[1]	KSV_BYTE_61[0]
0xBE	0x00	REPEATER_REG_BE	rw	KSV_BYTE_62[7]	KSV_BYTE_62[6]	KSV_BYTE_62[5]	KSV_BYTE_62[4]	KSV_BYTE_62[3]	KSV_BYTE_62[2]	KSV_BYTE_62[1]	KSV_BYTE_62[0]
0xBF	0x00	REPEATER_REG_BF	rw	KSV_BYTE_63[7]	KSV_BYTE_63[6]	KSV_BYTE_63[5]	KSV_BYTE_63[4]	KSV_BYTE_63[3]	KSV_BYTE_63[2]	KSV_BYTE_63[1]	KSV_BYTE_63[0]
0xC0	0x00	REPEATER_REG_C0	rw	KSV_BYTE_64[7]	KSV_BYTE_64[6]	KSV_BYTE_64[5]	KSV_BYTE_64[4]	KSV_BYTE_64[3]	KSV_BYTE_64[2]	KSV_BYTE_64[1]	KSV_BYTE_64[0]
0xC1	0x00	REPEATER_REG_C1	rw	KSV_BYTE_65[7]	KSV_BYTE_65[6]	KSV_BYTE_65[5]	KSV_BYTE_65[4]	KSV_BYTE_65[3]	KSV_BYTE_65[2]	KSV_BYTE_65[1]	KSV_BYTE_65[0]
0xC2	0x00	REPEATER_REG_C2	rw	KSV_BYTE_66[7]	KSV_BYTE_66[6]	KSV_BYTE_66[5]	KSV_BYTE_66[4]	KSV_BYTE_66[3]	KSV_BYTE_66[2]	KSV_BYTE_66[1]	KSV_BYTE_66[0]
0xC3	0x00	REPEATER_REG_C3	rw	KSV_BYTE_67[7]	KSV_BYTE_67[6]	KSV_BYTE_67[5]	KSV_BYTE_67[4]	KSV_BYTE_67[3]	KSV_BYTE_67[2]	KSV_BYTE_67[1]	KSV_BYTE_67[0]
0xC4	0x00	REPEATER_REG_C4	rw	KSV_BYTE_68[7]	KSV_BYTE_68[6]	KSV_BYTE_68[5]	KSV_BYTE_68[4]	KSV_BYTE_68[3]	KSV_BYTE_68[2]	KSV_BYTE_68[1]	KSV_BYTE_68[0]
0xC5	0x00	REPEATER_REG_C5	rw	KSV_BYTE_69[7]	KSV_BYTE_69[6]	KSV_BYTE_69[5]	KSV_BYTE_69[4]	KSV_BYTE_69[3]	KSV_BYTE_69[2]	KSV_BYTE_69[1]	KSV_BYTE_69[0]
0xC6	0x00	REPEATER_REG_C6	rw	KSV_BYTE_70[7]	KSV_BYTE_70[6]	KSV_BYTE_70[5]	KSV_BYTE_70[4]	KSV_BYTE_70[3]	KSV_BYTE_70[2]	KSV_BYTE_70[1]	KSV_BYTE_70[0]
0xC7	0x00	REPEATER_REG_C7	rw	KSV_BYTE_71[7]	KSV_BYTE_71[6]	KSV_BYTE_71[5]	KSV_BYTE_71[4]	KSV_BYTE_71[3]	KSV_BYTE_71[2]	KSV_BYTE_71[1]	KSV_BYTE_71[0]
0xC8	0x00	REPEATER_REG_C8	rw	KSV_BYTE_72[7]	KSV_BYTE_72[6]	KSV_BYTE_72[5]	KSV_BYTE_72[4]	KSV_BYTE_72[3]	KSV_BYTE_72[2]	KSV_BYTE_72[1]	KSV_BYTE_72[0]
0xC9	0x00	REPEATER_REG_C9	rw	KSV_BYTE_73[7]	KSV_BYTE_73[6]	KSV_BYTE_73[5]	KSV_BYTE_73[4]	KSV_BYTE_73[3]	KSV_BYTE_73[2]	KSV_BYTE_73[1]	KSV_BYTE_73[0]
0xCA	0x00	REPEATER_REG_CA	rw	KSV_BYTE_74[7]	KSV_BYTE_74[6]	KSV_BYTE_74[5]	KSV_BYTE_74[4]	KSV_BYTE_74[3]	KSV_BYTE_74[2]	KSV_BYTE_74[1]	KSV_BYTE_74[0]
0xCB	0x00	REPEATER_REG_CB	rw	KSV_BYTE_75[7]	KSV_BYTE_75[6]	KSV_BYTE_75[5]	KSV_BYTE_75[4]	KSV_BYTE_75[3]	KSV_BYTE_75[2]	KSV_BYTE_75[1]	KSV_BYTE_75[0]
0xCC	0x00	REPEATER_REG_CC	rw	KSV_BYTE_76[7]	KSV_BYTE_76[6]	KSV_BYTE_76[5]	KSV_BYTE_76[4]	KSV_BYTE_76[3]	KSV_BYTE_76[2]	KSV_BYTE_76[1]	KSV_BYTE_76[0]
0xCD	0x00	REPEATER_REG_CD	rw	KSV_BYTE_77[7]	KSV_BYTE_77[6]	KSV_BYTE_77[5]	KSV_BYTE_77[4]	KSV_BYTE_77[3]	KSV_BYTE_77[2]	KSV_BYTE_77[1]	KSV_BYTE_77[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xCE	0x00	REPEATER_REG_CE	rw	KSV_BYTE_78[7]	KSV_BYTE_78[6]	KSV_BYTE_78[5]	KSV_BYTE_78[4]	KSV_BYTE_78[3]	KSV_BYTE_78[2]	KSV_BYTE_78[1]	KSV_BYTE_78[0]
0xCF	0x00	REPEATER_REG_CF	rw	KSV_BYTE_79[7]	KSV_BYTE_79[6]	KSV_BYTE_79[5]	KSV_BYTE_79[4]	KSV_BYTE_79[3]	KSV_BYTE_79[2]	KSV_BYTE_79[1]	KSV_BYTE_79[0]
0xD0	0x00	REPEATER_REG_D0	rw	KSV_BYTE_80[7]	KSV_BYTE_80[6]	KSV_BYTE_80[5]	KSV_BYTE_80[4]	KSV_BYTE_80[3]	KSV_BYTE_80[2]	KSV_BYTE_80[1]	KSV_BYTE_80[0]
0xD1	0x00	REPEATER_REG_D1	rw	KSV_BYTE_81[7]	KSV_BYTE_81[6]	KSV_BYTE_81[5]	KSV_BYTE_81[4]	KSV_BYTE_81[3]	KSV_BYTE_81[2]	KSV_BYTE_81[1]	KSV_BYTE_81[0]
0xD2	0x00	REPEATER_REG_D2	rw	KSV_BYTE_82[7]	KSV_BYTE_82[6]	KSV_BYTE_82[5]	KSV_BYTE_82[4]	KSV_BYTE_82[3]	KSV_BYTE_82[2]	KSV_BYTE_82[1]	KSV_BYTE_82[0]
0xD3	0x00	REPEATER_REG_D3	rw	KSV_BYTE_83[7]	KSV_BYTE_83[6]	KSV_BYTE_83[5]	KSV_BYTE_83[4]	KSV_BYTE_83[3]	KSV_BYTE_83[2]	KSV_BYTE_83[1]	KSV_BYTE_83[0]
0xD4	0x00	REPEATER_REG_D4	rw	KSV_BYTE_84[7]	KSV_BYTE_84[6]	KSV_BYTE_84[5]	KSV_BYTE_84[4]	KSV_BYTE_84[3]	KSV_BYTE_84[2]	KSV_BYTE_84[1]	KSV_BYTE_84[0]
0xD5	0x00	REPEATER_REG_D5	rw	KSV_BYTE_85[7]	KSV_BYTE_85[6]	KSV_BYTE_85[5]	KSV_BYTE_85[4]	KSV_BYTE_85[3]	KSV_BYTE_85[2]	KSV_BYTE_85[1]	KSV_BYTE_85[0]
0xD6	0x00	REPEATER_REG_D6	rw	KSV_BYTE_86[7]	KSV_BYTE_86[6]	KSV_BYTE_86[5]	KSV_BYTE_86[4]	KSV_BYTE_86[3]	KSV_BYTE_86[2]	KSV_BYTE_86[1]	KSV_BYTE_86[0]
0xD7	0x00	REPEATER_REG_D7	rw	KSV_BYTE_87[7]	KSV_BYTE_87[6]	KSV_BYTE_87[5]	KSV_BYTE_87[4]	KSV_BYTE_87[3]	KSV_BYTE_87[2]	KSV_BYTE_87[1]	KSV_BYTE_87[0]
0xD8	0x00	REPEATER_REG_D8	rw	KSV_BYTE_88[7]	KSV_BYTE_88[6]	KSV_BYTE_88[5]	KSV_BYTE_88[4]	KSV_BYTE_88[3]	KSV_BYTE_88[2]	KSV_BYTE_88[1]	KSV_BYTE_88[0]
0xD9	0x00	REPEATER_REG_D9	rw	KSV_BYTE_89[7]	KSV_BYTE_89[6]	KSV_BYTE_89[5]	KSV_BYTE_89[4]	KSV_BYTE_89[3]	KSV_BYTE_89[2]	KSV_BYTE_89[1]	KSV_BYTE_89[0]
0xDA	0x00	REPEATER_REG_DA	rw	KSV_BYTE_90[7]	KSV_BYTE_90[6]	KSV_BYTE_90[5]	KSV_BYTE_90[4]	KSV_BYTE_90[3]	KSV_BYTE_90[2]	KSV_BYTE_90[1]	KSV_BYTE_90[0]
0xDB	0x00	REPEATER_REG_DB	rw	KSV_BYTE_91[7]	KSV_BYTE_91[6]	KSV_BYTE_91[5]	KSV_BYTE_91[4]	KSV_BYTE_91[3]	KSV_BYTE_91[2]	KSV_BYTE_91[1]	KSV_BYTE_91[0]
0xDC	0x00	REPEATER_REG_DC	rw	KSV_BYTE_92[7]	KSV_BYTE_92[6]	KSV_BYTE_92[5]	KSV_BYTE_92[4]	KSV_BYTE_92[3]	KSV_BYTE_92[2]	KSV_BYTE_92[1]	KSV_BYTE_92[0]
0xDD	0x00	REPEATER_REG_DD	rw	KSV_BYTE_93[7]	KSV_BYTE_93[6]	KSV_BYTE_93[5]	KSV_BYTE_93[4]	KSV_BYTE_93[3]	KSV_BYTE_93[2]	KSV_BYTE_93[1]	KSV_BYTE_93[0]
0xDE	0x00	REPEATER_REG_DE	rw	KSV_BYTE_94[7]	KSV_BYTE_94[6]	KSV_BYTE_94[5]	KSV_BYTE_94[4]	KSV_BYTE_94[3]	KSV_BYTE_94[2]	KSV_BYTE_94[1]	KSV_BYTE_94[0]
0xDF	0x00	REPEATER_REG_DF	rw	KSV_BYTE_95[7]	KSV_BYTE_95[6]	KSV_BYTE_95[5]	KSV_BYTE_95[4]	KSV_BYTE_95[3]	KSV_BYTE_95[2]	KSV_BYTE_95[1]	KSV_BYTE_95[0]
0xE0	0x00	REPEATER_REG_E0	rw	KSV_BYTE_96[7]	KSV_BYTE_96[6]	KSV_BYTE_96[5]	KSV_BYTE_96[4]	KSV_BYTE_96[3]	KSV_BYTE_96[2]	KSV_BYTE_96[1]	KSV_BYTE_96[0]
0xE1	0x00	REPEATER_REG_E1	rw	KSV_BYTE_97[7]	KSV_BYTE_97[6]	KSV_BYTE_97[5]	KSV_BYTE_97[4]	KSV_BYTE_97[3]	KSV_BYTE_97[2]	KSV_BYTE_97[1]	KSV_BYTE_97[0]
0xE2	0x00	REPEATER_REG_E2	rw	KSV_BYTE_98[7]	KSV_BYTE_98[6]	KSV_BYTE_98[5]	KSV_BYTE_98[4]	KSV_BYTE_98[3]	KSV_BYTE_98[2]	KSV_BYTE_98[1]	KSV_BYTE_98[0]
0xE3	0x00	REPEATER_REG_E3	rw	KSV_BYTE_99[7]	KSV_BYTE_99[6]	KSV_BYTE_99[5]	KSV_BYTE_99[4]	KSV_BYTE_99[3]	KSV_BYTE_99[2]	KSV_BYTE_99[1]	KSV_BYTE_99[0]
0xE4	0x00	REPEATER_REG_E4	rw	KSV_BYTE_100[7]	KSV_BYTE_100[6]	KSV_BYTE_100[5]	KSV_BYTE_100[4]	KSV_BYTE_100[3]	KSV_BYTE_100[2]	KSV_BYTE_100[1]	KSV_BYTE_100[0]
0xE5	0x00	REPEATER_REG_E5	rw	KSV_BYTE_101[7]	KSV_BYTE_101[6]	KSV_BYTE_101[5]	KSV_BYTE_101[4]	KSV_BYTE_101[3]	KSV_BYTE_101[2]	KSV_BYTE_101[1]	KSV_BYTE_101[0]
0xE6	0x00	REPEATER_REG_E6	rw	KSV_BYTE_102[7]	KSV_BYTE_102[6]	KSV_BYTE_102[5]	KSV_BYTE_102[4]	KSV_BYTE_102[3]	KSV_BYTE_102[2]	KSV_BYTE_102[1]	KSV_BYTE_102[0]
0xE7	0x00	REPEATER_REG_E7	rw	KSV_BYTE_103[7]	KSV_BYTE_103[6]	KSV_BYTE_103[5]	KSV_BYTE_103[4]	KSV_BYTE_103[3]	KSV_BYTE_103[2]	KSV_BYTE_103[1]	KSV_BYTE_103[0]
0xE8	0x00	REPEATER_REG_E8	rw	KSV_BYTE_104[7]	KSV_BYTE_104[6]	KSV_BYTE_104[5]	KSV_BYTE_104[4]	KSV_BYTE_104[3]	KSV_BYTE_104[2]	KSV_BYTE_104[1]	KSV_BYTE_104[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xE9	0x00	REPEATER_REG_E9	rw	KSV_BYTE_105[7]	KSV_BYTE_105[6]	KSV_BYTE_105[5]	KSV_BYTE_105[4]	KSV_BYTE_105[3]	KSV_BYTE_105[2]	KSV_BYTE_105[1]	KSV_BYTE_105[0]
0xEA	0x00	REPEATER_REG_EA	rw	KSV_BYTE_106[7]	KSV_BYTE_106[6]	KSV_BYTE_106[5]	KSV_BYTE_106[4]	KSV_BYTE_106[3]	KSV_BYTE_106[2]	KSV_BYTE_106[1]	KSV_BYTE_106[0]
0xEB	0x00	REPEATER_REG_EB	rw	KSV_BYTE_107[7]	KSV_BYTE_107[6]	KSV_BYTE_107[5]	KSV_BYTE_107[4]	KSV_BYTE_107[3]	KSV_BYTE_107[2]	KSV_BYTE_107[1]	KSV_BYTE_107[0]
0xEC	0x00	REPEATER_REG_EC	rw	KSV_BYTE_108[7]	KSV_BYTE_108[6]	KSV_BYTE_108[5]	KSV_BYTE_108[4]	KSV_BYTE_108[3]	KSV_BYTE_108[2]	KSV_BYTE_108[1]	KSV_BYTE_108[0]
0xED	0x00	REPEATER_REG_ED	rw	KSV_BYTE_109[7]	KSV_BYTE_109[6]	KSV_BYTE_109[5]	KSV_BYTE_109[4]	KSV_BYTE_109[3]	KSV_BYTE_109[2]	KSV_BYTE_109[1]	KSV_BYTE_109[0]
0xEE	0x00	REPEATER_REG_EE	rw	KSV_BYTE_110[7]	KSV_BYTE_110[6]	KSV_BYTE_110[5]	KSV_BYTE_110[4]	KSV_BYTE_110[3]	KSV_BYTE_110[2]	KSV_BYTE_110[1]	KSV_BYTE_110[0]
0xEF	0x00	REPEATER_REG_EF	rw	KSV_BYTE_111[7]	KSV_BYTE_111[6]	KSV_BYTE_111[5]	KSV_BYTE_111[4]	KSV_BYTE_111[3]	KSV_BYTE_111[2]	KSV_BYTE_111[1]	KSV_BYTE_111[0]
0xF0	0x00	REPEATER_REG_F0	rw	KSV_BYTE_112[7]	KSV_BYTE_112[6]	KSV_BYTE_112[5]	KSV_BYTE_112[4]	KSV_BYTE_112[3]	KSV_BYTE_112[2]	KSV_BYTE_112[1]	KSV_BYTE_112[0]
0xF1	0x00	REPEATER_REG_F1	rw	KSV_BYTE_113[7]	KSV_BYTE_113[6]	KSV_BYTE_113[5]	KSV_BYTE_113[4]	KSV_BYTE_113[3]	KSV_BYTE_113[2]	KSV_BYTE_113[1]	KSV_BYTE_113[0]
0xF2	0x00	REPEATER_REG_F2	rw	KSV_BYTE_114[7]	KSV_BYTE_114[6]	KSV_BYTE_114[5]	KSV_BYTE_114[4]	KSV_BYTE_114[3]	KSV_BYTE_114[2]	KSV_BYTE_114[1]	KSV_BYTE_114[0]
0xF3	0x00	REPEATER_REG_F3	rw	KSV_BYTE_115[7]	KSV_BYTE_115[6]	KSV_BYTE_115[5]	KSV_BYTE_115[4]	KSV_BYTE_115[3]	KSV_BYTE_115[2]	KSV_BYTE_115[1]	KSV_BYTE_115[0]
0xF4	0x00	REPEATER_REG_F4	rw	KSV_BYTE_116[7]	KSV_BYTE_116[6]	KSV_BYTE_116[5]	KSV_BYTE_116[4]	KSV_BYTE_116[3]	KSV_BYTE_116[2]	KSV_BYTE_116[1]	KSV_BYTE_116[0]
0xF5	0x00	REPEATER_REG_F5	rw	KSV_BYTE_117[7]	KSV_BYTE_117[6]	KSV_BYTE_117[5]	KSV_BYTE_117[4]	KSV_BYTE_117[3]	KSV_BYTE_117[2]	KSV_BYTE_117[1]	KSV_BYTE_117[0]
0xF6	0x00	REPEATER_REG_F6	rw	KSV_BYTE_118[7]	KSV_BYTE_118[6]	KSV_BYTE_118[5]	KSV_BYTE_118[4]	KSV_BYTE_118[3]	KSV_BYTE_118[2]	KSV_BYTE_118[1]	KSV_BYTE_118[0]
0xF7	0x00	REPEATER_REG_F7	rw	KSV_BYTE_119[7]	KSV_BYTE_119[6]	KSV_BYTE_119[5]	KSV_BYTE_119[4]	KSV_BYTE_119[3]	KSV_BYTE_119[2]	KSV_BYTE_119[1]	KSV_BYTE_119[0]
0xF8	0x00	REPEATER_REG_F8	rw	KSV_BYTE_120[7]	KSV_BYTE_120[6]	KSV_BYTE_120[5]	KSV_BYTE_120[4]	KSV_BYTE_120[3]	KSV_BYTE_120[2]	KSV_BYTE_120[1]	KSV_BYTE_120[0]
0xF9	0x00	REPEATER_REG_F9	rw	KSV_BYTE_121[7]	KSV_BYTE_121[6]	KSV_BYTE_121[5]	KSV_BYTE_121[4]	KSV_BYTE_121[3]	KSV_BYTE_121[2]	KSV_BYTE_121[1]	KSV_BYTE_121[0]
0xFA	0x00	REPEATER_REG_FA	rw	KSV_BYTE_122[7]	KSV_BYTE_122[6]	KSV_BYTE_122[5]	KSV_BYTE_122[4]	KSV_BYTE_122[3]	KSV_BYTE_122[2]	KSV_BYTE_122[1]	KSV_BYTE_122[0]
0xFB	0x00	REPEATER_REG_FB	rw	KSV_BYTE_123[7]	KSV_BYTE_123[6]	KSV_BYTE_123[5]	KSV_BYTE_123[4]	KSV_BYTE_123[3]	KSV_BYTE_123[2]	KSV_BYTE_123[1]	KSV_BYTE_123[0]
0xFC	0x00	REPEATER_REG_FC	rw	KSV_BYTE_124[7]	KSV_BYTE_124[6]	KSV_BYTE_124[5]	KSV_BYTE_124[4]	KSV_BYTE_124[3]	KSV_BYTE_124[2]	KSV_BYTE_124[1]	KSV_BYTE_124[0]
0xFD	0x00	REPEATER_REG_FD	rw	KSV_BYTE_125[7]	KSV_BYTE_125[6]	KSV_BYTE_125[5]	KSV_BYTE_125[4]	KSV_BYTE_125[3]	KSV_BYTE_125[2]	KSV_BYTE_125[1]	KSV_BYTE_125[0]
0xFE	0x00	REPEATER_REG_FE	rw	KSV_BYTE_126[7]	KSV_BYTE_126[6]	KSV_BYTE_126[5]	KSV_BYTE_126[4]	KSV_BYTE_126[3]	KSV_BYTE_126[2]	KSV_BYTE_126[1]	KSV_BYTE_126[0]
0xFF	0x00	REPEATER_REG_FF	rw	KSV_BYTE_127[7]	KSV_BYTE_127[6]	KSV_BYTE_127[5]	KSV_BYTE_127[4]	KSV_BYTE_127[3]	KSV_BYTE_127[2]	KSV_BYTE_127[1]	KSV_BYTE_127[0]

1.4 INFOFRAME MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00	INFOFRAME_REG_00	r	AVI_INF_PB[7]	AVI_INF_PB[6]	AVI_INF_PB[5]	AVI_INF_PB[4]	AVI_INF_PB[3]	AVI_INF_PB[2]	AVI_INF_PB[1]	AVI_INF_PB[0]
0x01	0x00	INFOFRAME_REG_01	r	AVI_INF_PB[15]	AVI_INF_PB[14]	AVI_INF_PB[13]	AVI_INF_PB[12]	AVI_INF_PB[11]	AVI_INF_PB[10]	AVI_INF_PB[9]	AVI_INF_PB[8]
0x02	0x00	INFOFRAME_REG_02	r	AVI_INF_PB[23]	AVI_INF_PB[22]	AVI_INF_PB[21]	AVI_INF_PB[20]	AVI_INF_PB[19]	AVI_INF_PB[18]	AVI_INF_PB[17]	AVI_INF_PB[16]
0x03	0x00	INFOFRAME_REG_03	r	AVI_INF_PB[31]	AVI_INF_PB[30]	AVI_INF_PB[29]	AVI_INF_PB[28]	AVI_INF_PB[27]	AVI_INF_PB[26]	AVI_INF_PB[25]	AVI_INF_PB[24]
0x04	0x00	INFOFRAME_REG_04	r	AVI_INF_PB[39]	AVI_INF_PB[38]	AVI_INF_PB[37]	AVI_INF_PB[36]	AVI_INF_PB[35]	AVI_INF_PB[34]	AVI_INF_PB[33]	AVI_INF_PB[32]
0x05	0x00	INFOFRAME_REG_05	r	AVI_INF_PB[47]	AVI_INF_PB[46]	AVI_INF_PB[45]	AVI_INF_PB[44]	AVI_INF_PB[43]	AVI_INF_PB[42]	AVI_INF_PB[41]	AVI_INF_PB[40]
0x06	0x00	INFOFRAME_REG_06	r	AVI_INF_PB[55]	AVI_INF_PB[54]	AVI_INF_PB[53]	AVI_INF_PB[52]	AVI_INF_PB[51]	AVI_INF_PB[50]	AVI_INF_PB[49]	AVI_INF_PB[48]
0x07	0x00	INFOFRAME_REG_07	r	AVI_INF_PB[63]	AVI_INF_PB[62]	AVI_INF_PB[61]	AVI_INF_PB[60]	AVI_INF_PB[59]	AVI_INF_PB[58]	AVI_INF_PB[57]	AVI_INF_PB[56]
0x08	0x00	INFOFRAME_REG_08	r	AVI_INF_PB[71]	AVI_INF_PB[70]	AVI_INF_PB[69]	AVI_INF_PB[68]	AVI_INF_PB[67]	AVI_INF_PB[66]	AVI_INF_PB[65]	AVI_INF_PB[64]
0x09	0x00	INFOFRAME_REG_09	r	AVI_INF_PB[79]	AVI_INF_PB[78]	AVI_INF_PB[77]	AVI_INF_PB[76]	AVI_INF_PB[75]	AVI_INF_PB[74]	AVI_INF_PB[73]	AVI_INF_PB[72]
0x0A	0x00	INFOFRAME_REG_0A	r	AVI_INF_PB[87]	AVI_INF_PB[86]	AVI_INF_PB[85]	AVI_INF_PB[84]	AVI_INF_PB[83]	AVI_INF_PB[82]	AVI_INF_PB[81]	AVI_INF_PB[80]
0x0B	0x00	INFOFRAME_REG_0B	r	AVI_INF_PB[95]	AVI_INF_PB[94]	AVI_INF_PB[93]	AVI_INF_PB[92]	AVI_INF_PB[91]	AVI_INF_PB[90]	AVI_INF_PB[89]	AVI_INF_PB[88]
0x0C	0x00	INFOFRAME_REG_0C	r	AVI_INF_PB[103]	AVI_INF_PB[102]	AVI_INF_PB[101]	AVI_INF_PB[100]	AVI_INF_PB[99]	AVI_INF_PB[98]	AVI_INF_PB[97]	AVI_INF_PB[96]
0x0D	0x00	INFOFRAME_REG_0D	r	AVI_INF_PB[111]	AVI_INF_PB[110]	AVI_INF_PB[109]	AVI_INF_PB[108]	AVI_INF_PB[107]	AVI_INF_PB[106]	AVI_INF_PB[105]	AVI_INF_PB[104]
0x0E	0x00	INFOFRAME_REG_0E	r	AVI_INF_PB[119]	AVI_INF_PB[118]	AVI_INF_PB[117]	AVI_INF_PB[116]	AVI_INF_PB[115]	AVI_INF_PB[114]	AVI_INF_PB[113]	AVI_INF_PB[112]
0x0F	0x00	INFOFRAME_REG_0F	r	AVI_INF_PB[127]	AVI_INF_PB[126]	AVI_INF_PB[125]	AVI_INF_PB[124]	AVI_INF_PB[123]	AVI_INF_PB[122]	AVI_INF_PB[121]	AVI_INF_PB[120]
0x10	0x00	INFOFRAME_REG_10	r	AVI_INF_PB[135]	AVI_INF_PB[134]	AVI_INF_PB[133]	AVI_INF_PB[132]	AVI_INF_PB[131]	AVI_INF_PB[130]	AVI_INF_PB[129]	AVI_INF_PB[128]
0x11	0x00	INFOFRAME_REG_11	r	AVI_INF_PB[143]	AVI_INF_PB[142]	AVI_INF_PB[141]	AVI_INF_PB[140]	AVI_INF_PB[139]	AVI_INF_PB[138]	AVI_INF_PB[137]	AVI_INF_PB[136]
0x12	0x00	INFOFRAME_REG_12	r	AVI_INF_PB[151]	AVI_INF_PB[150]	AVI_INF_PB[149]	AVI_INF_PB[148]	AVI_INF_PB[147]	AVI_INF_PB[146]	AVI_INF_PB[145]	AVI_INF_PB[144]
0x13	0x00	INFOFRAME_REG_13	r	AVI_INF_PB[159]	AVI_INF_PB[158]	AVI_INF_PB[157]	AVI_INF_PB[156]	AVI_INF_PB[155]	AVI_INF_PB[154]	AVI_INF_PB[153]	AVI_INF_PB[152]
0x14	0x00	INFOFRAME_REG_14	r	AVI_INF_PB[167]	AVI_INF_PB[166]	AVI_INF_PB[165]	AVI_INF_PB[164]	AVI_INF_PB[163]	AVI_INF_PB[162]	AVI_INF_PB[161]	AVI_INF_PB[160]
0x15	0x00	INFOFRAME_REG_15	r	AVI_INF_PB[175]	AVI_INF_PB[174]	AVI_INF_PB[173]	AVI_INF_PB[172]	AVI_INF_PB[171]	AVI_INF_PB[170]	AVI_INF_PB[169]	AVI_INF_PB[168]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x16	0x00	INFOFRAME_REG_16	r	AVI_INF_PB[183]	AVI_INF_PB[182]	AVI_INF_PB[181]	AVI_INF_PB[180]	AVI_INF_PB[179]	AVI_INF_PB[178]	AVI_INF_PB[177]	AVI_INF_PB[176]
0x17	0x00	INFOFRAME_REG_17	r	AVI_INF_PB[191]	AVI_INF_PB[190]	AVI_INF_PB[189]	AVI_INF_PB[188]	AVI_INF_PB[187]	AVI_INF_PB[186]	AVI_INF_PB[185]	AVI_INF_PB[184]
0x18	0x00	INFOFRAME_REG_18	r	AVI_INF_PB[199]	AVI_INF_PB[198]	AVI_INF_PB[197]	AVI_INF_PB[196]	AVI_INF_PB[195]	AVI_INF_PB[194]	AVI_INF_PB[193]	AVI_INF_PB[192]
0x19	0x00	INFOFRAME_REG_19	r	AVI_INF_PB[207]	AVI_INF_PB[206]	AVI_INF_PB[205]	AVI_INF_PB[204]	AVI_INF_PB[203]	AVI_INF_PB[202]	AVI_INF_PB[201]	AVI_INF_PB[200]
0x1A	0x00	INFOFRAME_REG_1A	r	AVI_INF_PB[215]	AVI_INF_PB[214]	AVI_INF_PB[213]	AVI_INF_PB[212]	AVI_INF_PB[211]	AVI_INF_PB[210]	AVI_INF_PB[209]	AVI_INF_PB[208]
0x1B	0x00	INFOFRAME_REG_1B	r	AVI_INF_PB[223]	AVI_INF_PB[222]	AVI_INF_PB[221]	AVI_INF_PB[220]	AVI_INF_PB[219]	AVI_INF_PB[218]	AVI_INF_PB[217]	AVI_INF_PB[216]
0x1C	0x00	INFOFRAME_REG_1C	r	AUD_INF_PB[7]	AUD_INF_PB[6]	AUD_INF_PB[5]	AUD_INF_PB[4]	AUD_INF_PB[3]	AUD_INF_PB[2]	AUD_INF_PB[1]	AUD_INF_PB[0]
0x1D	0x00	INFOFRAME_REG_1D	r	AUD_INF_PB[15]	AUD_INF_PB[14]	AUD_INF_PB[13]	AUD_INF_PB[12]	AUD_INF_PB[11]	AUD_INF_PB[10]	AUD_INF_PB[9]	AUD_INF_PB[8]
0x1E	0x00	INFOFRAME_REG_1E	r	AUD_INF_PB[23]	AUD_INF_PB[22]	AUD_INF_PB[21]	AUD_INF_PB[20]	AUD_INF_PB[19]	AUD_INF_PB[18]	AUD_INF_PB[17]	AUD_INF_PB[16]
0x1F	0x00	INFOFRAME_REG_1F	r	AUD_INF_PB[31]	AUD_INF_PB[30]	AUD_INF_PB[29]	AUD_INF_PB[28]	AUD_INF_PB[27]	AUD_INF_PB[26]	AUD_INF_PB[25]	AUD_INF_PB[24]
0x20	0x00	INFOFRAME_REG_20	r	AUD_INF_PB[39]	AUD_INF_PB[38]	AUD_INF_PB[37]	AUD_INF_PB[36]	AUD_INF_PB[35]	AUD_INF_PB[34]	AUD_INF_PB[33]	AUD_INF_PB[32]
0x21	0x00	INFOFRAME_REG_21	r	AUD_INF_PB[47]	AUD_INF_PB[46]	AUD_INF_PB[45]	AUD_INF_PB[44]	AUD_INF_PB[43]	AUD_INF_PB[42]	AUD_INF_PB[41]	AUD_INF_PB[40]
0x22	0x00	INFOFRAME_REG_22	r	AUD_INF_PB[55]	AUD_INF_PB[54]	AUD_INF_PB[53]	AUD_INF_PB[52]	AUD_INF_PB[51]	AUD_INF_PB[50]	AUD_INF_PB[49]	AUD_INF_PB[48]
0x23	0x00	INFOFRAME_REG_23	r	AUD_INF_PB[63]	AUD_INF_PB[62]	AUD_INF_PB[61]	AUD_INF_PB[60]	AUD_INF_PB[59]	AUD_INF_PB[58]	AUD_INF_PB[57]	AUD_INF_PB[56]
0x24	0x00	INFOFRAME_REG_24	r	AUD_INF_PB[71]	AUD_INF_PB[70]	AUD_INF_PB[69]	AUD_INF_PB[68]	AUD_INF_PB[67]	AUD_INF_PB[66]	AUD_INF_PB[65]	AUD_INF_PB[64]
0x25	0x00	INFOFRAME_REG_25	r	AUD_INF_PB[79]	AUD_INF_PB[78]	AUD_INF_PB[77]	AUD_INF_PB[76]	AUD_INF_PB[75]	AUD_INF_PB[74]	AUD_INF_PB[73]	AUD_INF_PB[72]
0x26	0x00	INFOFRAME_REG_26	r	AUD_INF_PB[87]	AUD_INF_PB[86]	AUD_INF_PB[85]	AUD_INF_PB[84]	AUD_INF_PB[83]	AUD_INF_PB[82]	AUD_INF_PB[81]	AUD_INF_PB[80]
0x27	0x00	INFOFRAME_REG_27	r	AUD_INF_PB[95]	AUD_INF_PB[94]	AUD_INF_PB[93]	AUD_INF_PB[92]	AUD_INF_PB[91]	AUD_INF_PB[90]	AUD_INF_PB[89]	AUD_INF_PB[88]
0x28	0x00	INFOFRAME_REG_28	r	AUD_INF_PB[103]	AUD_INF_PB[102]	AUD_INF_PB[101]	AUD_INF_PB[100]	AUD_INF_PB[99]	AUD_INF_PB[98]	AUD_INF_PB[97]	AUD_INF_PB[96]
0x29	0x00	INFOFRAME_REG_29	r	AUD_INF_PB[111]	AUD_INF_PB[110]	AUD_INF_PB[109]	AUD_INF_PB[108]	AUD_INF_PB[107]	AUD_INF_PB[106]	AUD_INF_PB[105]	AUD_INF_PB[104]
0x2A	0x00	INFOFRAME_REG_2A	r	SPD_INF_PB[7]	SPD_INF_PB[6]	SPD_INF_PB[5]	SPD_INF_PB[4]	SPD_INF_PB[3]	SPD_INF_PB[2]	SPD_INF_PB[1]	SPD_INF_PB[0]
0x2B	0x00	INFOFRAME_REG_2B	r	SPD_INF_PB[15]	SPD_INF_PB[14]	SPD_INF_PB[13]	SPD_INF_PB[12]	SPD_INF_PB[11]	SPD_INF_PB[10]	SPD_INF_PB[9]	SPD_INF_PB[8]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x2C	0x00	INFOFRAME_REG_2C	r	SPD_INF_PB[23]	SPD_INF_PB[22]	SPD_INF_PB[21]	SPD_INF_PB[20]	SPD_INF_PB[19]	SPD_INF_PB[18]	SPD_INF_PB[17]	SPD_INF_PB[16]
0x2D	0x00	INFOFRAME_REG_2D	r	SPD_INF_PB[31]	SPD_INF_PB[30]	SPD_INF_PB[29]	SPD_INF_PB[28]	SPD_INF_PB[27]	SPD_INF_PB[26]	SPD_INF_PB[25]	SPD_INF_PB[24]
0x2E	0x00	INFOFRAME_REG_2E	r	SPD_INF_PB[39]	SPD_INF_PB[38]	SPD_INF_PB[37]	SPD_INF_PB[36]	SPD_INF_PB[35]	SPD_INF_PB[34]	SPD_INF_PB[33]	SPD_INF_PB[32]
0x2F	0x00	INFOFRAME_REG_2F	r	SPD_INF_PB[47]	SPD_INF_PB[46]	SPD_INF_PB[45]	SPD_INF_PB[44]	SPD_INF_PB[43]	SPD_INF_PB[42]	SPD_INF_PB[41]	SPD_INF_PB[40]
0x30	0x00	INFOFRAME_REG_30	r	SPD_INF_PB[55]	SPD_INF_PB[54]	SPD_INF_PB[53]	SPD_INF_PB[52]	SPD_INF_PB[51]	SPD_INF_PB[50]	SPD_INF_PB[49]	SPD_INF_PB[48]
0x31	0x00	INFOFRAME_REG_31	r	SPD_INF_PB[63]	SPD_INF_PB[62]	SPD_INF_PB[61]	SPD_INF_PB[60]	SPD_INF_PB[59]	SPD_INF_PB[58]	SPD_INF_PB[57]	SPD_INF_PB[56]
0x32	0x00	INFOFRAME_REG_32	r	SPD_INF_PB[71]	SPD_INF_PB[70]	SPD_INF_PB[69]	SPD_INF_PB[68]	SPD_INF_PB[67]	SPD_INF_PB[66]	SPD_INF_PB[65]	SPD_INF_PB[64]
0x33	0x00	INFOFRAME_REG_33	r	SPD_INF_PB[79]	SPD_INF_PB[78]	SPD_INF_PB[77]	SPD_INF_PB[76]	SPD_INF_PB[75]	SPD_INF_PB[74]	SPD_INF_PB[73]	SPD_INF_PB[72]
0x34	0x00	INFOFRAME_REG_34	r	SPD_INF_PB[87]	SPD_INF_PB[86]	SPD_INF_PB[85]	SPD_INF_PB[84]	SPD_INF_PB[83]	SPD_INF_PB[82]	SPD_INF_PB[81]	SPD_INF_PB[80]
0x35	0x00	INFOFRAME_REG_35	r	SPD_INF_PB[95]	SPD_INF_PB[94]	SPD_INF_PB[93]	SPD_INF_PB[92]	SPD_INF_PB[91]	SPD_INF_PB[90]	SPD_INF_PB[89]	SPD_INF_PB[88]
0x36	0x00	INFOFRAME_REG_36	r	SPD_INF_PB[103]	SPD_INF_PB[102]	SPD_INF_PB[101]	SPD_INF_PB[100]	SPD_INF_PB[99]	SPD_INF_PB[98]	SPD_INF_PB[97]	SPD_INF_PB[96]
0x37	0x00	INFOFRAME_REG_37	r	SPD_INF_PB[111]	SPD_INF_PB[110]	SPD_INF_PB[109]	SPD_INF_PB[108]	SPD_INF_PB[107]	SPD_INF_PB[106]	SPD_INF_PB[105]	SPD_INF_PB[104]
0x38	0x00	INFOFRAME_REG_38	r	SPD_INF_PB[119]	SPD_INF_PB[118]	SPD_INF_PB[117]	SPD_INF_PB[116]	SPD_INF_PB[115]	SPD_INF_PB[114]	SPD_INF_PB[113]	SPD_INF_PB[112]
0x39	0x00	INFOFRAME_REG_39	r	SPD_INF_PB[127]	SPD_INF_PB[126]	SPD_INF_PB[125]	SPD_INF_PB[124]	SPD_INF_PB[123]	SPD_INF_PB[122]	SPD_INF_PB[121]	SPD_INF_PB[120]
0x3A	0x00	INFOFRAME_REG_3A	r	SPD_INF_PB[135]	SPD_INF_PB[134]	SPD_INF_PB[133]	SPD_INF_PB[132]	SPD_INF_PB[131]	SPD_INF_PB[130]	SPD_INF_PB[129]	SPD_INF_PB[128]
0x3B	0x00	INFOFRAME_REG_3B	r	SPD_INF_PB[143]	SPD_INF_PB[142]	SPD_INF_PB[141]	SPD_INF_PB[140]	SPD_INF_PB[139]	SPD_INF_PB[138]	SPD_INF_PB[137]	SPD_INF_PB[136]
0x3C	0x00	INFOFRAME_REG_3C	r	SPD_INF_PB[151]	SPD_INF_PB[150]	SPD_INF_PB[149]	SPD_INF_PB[148]	SPD_INF_PB[147]	SPD_INF_PB[146]	SPD_INF_PB[145]	SPD_INF_PB[144]
0x3D	0x00	INFOFRAME_REG_3D	r	SPD_INF_PB[159]	SPD_INF_PB[158]	SPD_INF_PB[157]	SPD_INF_PB[156]	SPD_INF_PB[155]	SPD_INF_PB[154]	SPD_INF_PB[153]	SPD_INF_PB[152]
0x3E	0x00	INFOFRAME_REG_3E	r	SPD_INF_PB[167]	SPD_INF_PB[166]	SPD_INF_PB[165]	SPD_INF_PB[164]	SPD_INF_PB[163]	SPD_INF_PB[162]	SPD_INF_PB[161]	SPD_INF_PB[160]
0x3F	0x00	INFOFRAME_REG_3F	r	SPD_INF_PB[175]	SPD_INF_PB[174]	SPD_INF_PB[173]	SPD_INF_PB[172]	SPD_INF_PB[171]	SPD_INF_PB[170]	SPD_INF_PB[169]	SPD_INF_PB[168]
0x40	0x00	INFOFRAME_REG_40	r	SPD_INF_PB[183]	SPD_INF_PB[182]	SPD_INF_PB[181]	SPD_INF_PB[180]	SPD_INF_PB[179]	SPD_INF_PB[178]	SPD_INF_PB[177]	SPD_INF_PB[176]
0x41	0x00	INFOFRAME_REG_41	r	SPD_INF_PB[191]	SPD_INF_PB[190]	SPD_INF_PB[189]	SPD_INF_PB[188]	SPD_INF_PB[187]	SPD_INF_PB[186]	SPD_INF_PB[185]	SPD_INF_PB[184]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x42	0x00	INFOFRAME_REG_42	r	SPD_INF_PB[199]	SPD_INF_PB[198]	SPD_INF_PB[197]	SPD_INF_PB[196]	SPD_INF_PB[195]	SPD_INF_PB[194]	SPD_INF_PB[193]	SPD_INF_PB[192]
0x43	0x00	INFOFRAME_REG_43	r	SPD_INF_PB[207]	SPD_INF_PB[206]	SPD_INF_PB[205]	SPD_INF_PB[204]	SPD_INF_PB[203]	SPD_INF_PB[202]	SPD_INF_PB[201]	SPD_INF_PB[200]
0x44	0x00	INFOFRAME_REG_44	r	SPD_INF_PB[215]	SPD_INF_PB[214]	SPD_INF_PB[213]	SPD_INF_PB[212]	SPD_INF_PB[211]	SPD_INF_PB[210]	SPD_INF_PB[209]	SPD_INF_PB[208]
0x45	0x00	INFOFRAME_REG_45	r	SPD_INF_PB[223]	SPD_INF_PB[222]	SPD_INF_PB[221]	SPD_INF_PB[220]	SPD_INF_PB[219]	SPD_INF_PB[218]	SPD_INF_PB[217]	SPD_INF_PB[216]
0x46	0x00	INFOFRAME_REG_46	r	MS_INF_PB[7]	MS_INF_PB[6]	MS_INF_PB[5]	MS_INF_PB[4]	MS_INF_PB[3]	MS_INF_PB[2]	MS_INF_PB[1]	MS_INF_PB[0]
0x47	0x00	INFOFRAME_REG_47	r	MS_INF_PB[15]	MS_INF_PB[14]	MS_INF_PB[13]	MS_INF_PB[12]	MS_INF_PB[11]	MS_INF_PB[10]	MS_INF_PB[9]	MS_INF_PB[8]
0x48	0x00	INFOFRAME_REG_48	r	MS_INF_PB[23]	MS_INF_PB[22]	MS_INF_PB[21]	MS_INF_PB[20]	MS_INF_PB[19]	MS_INF_PB[18]	MS_INF_PB[17]	MS_INF_PB[16]
0x49	0x00	INFOFRAME_REG_49	r	MS_INF_PB[31]	MS_INF_PB[30]	MS_INF_PB[29]	MS_INF_PB[28]	MS_INF_PB[27]	MS_INF_PB[26]	MS_INF_PB[25]	MS_INF_PB[24]
0x4A	0x00	INFOFRAME_REG_4A	r	MS_INF_PB[39]	MS_INF_PB[38]	MS_INF_PB[37]	MS_INF_PB[36]	MS_INF_PB[35]	MS_INF_PB[34]	MS_INF_PB[33]	MS_INF_PB[32]
0x4B	0x00	INFOFRAME_REG_4B	r	MS_INF_PB[47]	MS_INF_PB[46]	MS_INF_PB[45]	MS_INF_PB[44]	MS_INF_PB[43]	MS_INF_PB[42]	MS_INF_PB[41]	MS_INF_PB[40]
0x4C	0x00	INFOFRAME_REG_4C	r	MS_INF_PB[55]	MS_INF_PB[54]	MS_INF_PB[53]	MS_INF_PB[52]	MS_INF_PB[51]	MS_INF_PB[50]	MS_INF_PB[49]	MS_INF_PB[48]
0x4D	0x00	INFOFRAME_REG_4D	r	MS_INF_PB[63]	MS_INF_PB[62]	MS_INF_PB[61]	MS_INF_PB[60]	MS_INF_PB[59]	MS_INF_PB[58]	MS_INF_PB[57]	MS_INF_PB[56]
0x4E	0x00	INFOFRAME_REG_4E	r	MS_INF_PB[71]	MS_INF_PB[70]	MS_INF_PB[69]	MS_INF_PB[68]	MS_INF_PB[67]	MS_INF_PB[66]	MS_INF_PB[65]	MS_INF_PB[64]
0x4F	0x00	INFOFRAME_REG_4F	r	MS_INF_PB[79]	MS_INF_PB[78]	MS_INF_PB[77]	MS_INF_PB[76]	MS_INF_PB[75]	MS_INF_PB[74]	MS_INF_PB[73]	MS_INF_PB[72]
0x50	0x00	INFOFRAME_REG_50	r	MS_INF_PB[87]	MS_INF_PB[86]	MS_INF_PB[85]	MS_INF_PB[84]	MS_INF_PB[83]	MS_INF_PB[82]	MS_INF_PB[81]	MS_INF_PB[80]
0x51	0x00	INFOFRAME_REG_51	r	MS_INF_PB[95]	MS_INF_PB[94]	MS_INF_PB[93]	MS_INF_PB[92]	MS_INF_PB[91]	MS_INF_PB[90]	MS_INF_PB[89]	MS_INF_PB[88]
0x52	0x00	INFOFRAME_REG_52	r	MS_INF_PB[103]	MS_INF_PB[102]	MS_INF_PB[101]	MS_INF_PB[100]	MS_INF_PB[99]	MS_INF_PB[98]	MS_INF_PB[97]	MS_INF_PB[96]
0x53	0x00	INFOFRAME_REG_53	r	MS_INF_PB[111]	MS_INF_PB[110]	MS_INF_PB[109]	MS_INF_PB[108]	MS_INF_PB[107]	MS_INF_PB[106]	MS_INF_PB[105]	MS_INF_PB[104]
0x54	0x00	INFOFRAME_REG_54	r	VS_INF_PB[7]	VS_INF_PB[6]	VS_INF_PB[5]	VS_INF_PB[4]	VS_INF_PB[3]	VS_INF_PB[2]	VS_INF_PB[1]	VS_INF_PB[0]
0x55	0x00	INFOFRAME_REG_55	r	VS_INF_PB[15]	VS_INF_PB[14]	VS_INF_PB[13]	VS_INF_PB[12]	VS_INF_PB[11]	VS_INF_PB[10]	VS_INF_PB[9]	VS_INF_PB[8]
0x56	0x00	INFOFRAME_REG_56	r	VS_INF_PB[23]	VS_INF_PB[22]	VS_INF_PB[21]	VS_INF_PB[20]	VS_INF_PB[19]	VS_INF_PB[18]	VS_INF_PB[17]	VS_INF_PB[16]
0x57	0x00	INFOFRAME_REG_57	r	VS_INF_PB[31]	VS_INF_PB[30]	VS_INF_PB[29]	VS_INF_PB[28]	VS_INF_PB[27]	VS_INF_PB[26]	VS_INF_PB[25]	VS_INF_PB[24]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x58	0x00	INFOFRAME_REG_58	r	VS_INF_PB[39]	VS_INF_PB[38]	VS_INF_PB[37]	VS_INF_PB[36]	VS_INF_PB[35]	VS_INF_PB[34]	VS_INF_PB[33]	VS_INF_PB[32]
0x59	0x00	INFOFRAME_REG_59	r	VS_INF_PB[47]	VS_INF_PB[46]	VS_INF_PB[45]	VS_INF_PB[44]	VS_INF_PB[43]	VS_INF_PB[42]	VS_INF_PB[41]	VS_INF_PB[40]
0x5A	0x00	INFOFRAME_REG_5A	r	VS_INF_PB[55]	VS_INF_PB[54]	VS_INF_PB[53]	VS_INF_PB[52]	VS_INF_PB[51]	VS_INF_PB[50]	VS_INF_PB[49]	VS_INF_PB[48]
0x5B	0x00	INFOFRAME_REG_5B	r	VS_INF_PB[63]	VS_INF_PB[62]	VS_INF_PB[61]	VS_INF_PB[60]	VS_INF_PB[59]	VS_INF_PB[58]	VS_INF_PB[57]	VS_INF_PB[56]
0x5C	0x00	INFOFRAME_REG_5C	r	VS_INF_PB[71]	VS_INF_PB[70]	VS_INF_PB[69]	VS_INF_PB[68]	VS_INF_PB[67]	VS_INF_PB[66]	VS_INF_PB[65]	VS_INF_PB[64]
0x5D	0x00	INFOFRAME_REG_5D	r	VS_INF_PB[79]	VS_INF_PB[78]	VS_INF_PB[77]	VS_INF_PB[76]	VS_INF_PB[75]	VS_INF_PB[74]	VS_INF_PB[73]	VS_INF_PB[72]
0x5E	0x00	INFOFRAME_REG_5E	r	VS_INF_PB[87]	VS_INF_PB[86]	VS_INF_PB[85]	VS_INF_PB[84]	VS_INF_PB[83]	VS_INF_PB[82]	VS_INF_PB[81]	VS_INF_PB[80]
0x5F	0x00	INFOFRAME_REG_5F	r	VS_INF_PB[95]	VS_INF_PB[94]	VS_INF_PB[93]	VS_INF_PB[92]	VS_INF_PB[91]	VS_INF_PB[90]	VS_INF_PB[89]	VS_INF_PB[88]
0x60	0x00	INFOFRAME_REG_60	r	VS_INF_PB[103]	VS_INF_PB[102]	VS_INF_PB[101]	VS_INF_PB[100]	VS_INF_PB[99]	VS_INF_PB[98]	VS_INF_PB[97]	VS_INF_PB[96]
0x61	0x00	INFOFRAME_REG_61	r	VS_INF_PB[111]	VS_INF_PB[110]	VS_INF_PB[109]	VS_INF_PB[108]	VS_INF_PB[107]	VS_INF_PB[106]	VS_INF_PB[105]	VS_INF_PB[104]
0x62	0x00	INFOFRAME_REG_62	r	VS_INF_PB[119]	VS_INF_PB[118]	VS_INF_PB[117]	VS_INF_PB[116]	VS_INF_PB[115]	VS_INF_PB[114]	VS_INF_PB[113]	VS_INF_PB[112]
0x63	0x00	INFOFRAME_REG_63	r	VS_INF_PB[127]	VS_INF_PB[126]	VS_INF_PB[125]	VS_INF_PB[124]	VS_INF_PB[123]	VS_INF_PB[122]	VS_INF_PB[121]	VS_INF_PB[120]
0x64	0x00	INFOFRAME_REG_64	r	VS_INF_PB[135]	VS_INF_PB[134]	VS_INF_PB[133]	VS_INF_PB[132]	VS_INF_PB[131]	VS_INF_PB[130]	VS_INF_PB[129]	VS_INF_PB[128]
0x65	0x00	INFOFRAME_REG_65	r	VS_INF_PB[143]	VS_INF_PB[142]	VS_INF_PB[141]	VS_INF_PB[140]	VS_INF_PB[139]	VS_INF_PB[138]	VS_INF_PB[137]	VS_INF_PB[136]
0x66	0x00	INFOFRAME_REG_66	r	VS_INF_PB[151]	VS_INF_PB[150]	VS_INF_PB[149]	VS_INF_PB[148]	VS_INF_PB[147]	VS_INF_PB[146]	VS_INF_PB[145]	VS_INF_PB[144]
0x67	0x00	INFOFRAME_REG_67	r	VS_INF_PB[159]	VS_INF_PB[158]	VS_INF_PB[157]	VS_INF_PB[156]	VS_INF_PB[155]	VS_INF_PB[154]	VS_INF_PB[153]	VS_INF_PB[152]
0x68	0x00	INFOFRAME_REG_68	r	VS_INF_PB[167]	VS_INF_PB[166]	VS_INF_PB[165]	VS_INF_PB[164]	VS_INF_PB[163]	VS_INF_PB[162]	VS_INF_PB[161]	VS_INF_PB[160]
0x69	0x00	INFOFRAME_REG_69	r	VS_INF_PB[175]	VS_INF_PB[174]	VS_INF_PB[173]	VS_INF_PB[172]	VS_INF_PB[171]	VS_INF_PB[170]	VS_INF_PB[169]	VS_INF_PB[168]
0x6A	0x00	INFOFRAME_REG_6A	r	VS_INF_PB[183]	VS_INF_PB[182]	VS_INF_PB[181]	VS_INF_PB[180]	VS_INF_PB[179]	VS_INF_PB[178]	VS_INF_PB[177]	VS_INF_PB[176]
0x6B	0x00	INFOFRAME_REG_6B	r	VS_INF_PB[191]	VS_INF_PB[190]	VS_INF_PB[189]	VS_INF_PB[188]	VS_INF_PB[187]	VS_INF_PB[186]	VS_INF_PB[185]	VS_INF_PB[184]
0x6C	0x00	INFOFRAME_REG_6C	r	VS_INF_PB[199]	VS_INF_PB[198]	VS_INF_PB[197]	VS_INF_PB[196]	VS_INF_PB[195]	VS_INF_PB[194]	VS_INF_PB[193]	VS_INF_PB[192]
0x6D	0x00	INFOFRAME_REG_6D	r	VS_INF_PB[207]	VS_INF_PB[206]	VS_INF_PB[205]	VS_INF_PB[204]	VS_INF_PB[203]	VS_INF_PB[202]	VS_INF_PB[201]	VS_INF_PB[200]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x6E	0x00	INFOFRAME_REG_6E	r	VS_INF_PB[215]	VS_INF_PB[214]	VS_INF_PB[213]	VS_INF_PB[212]	VS_INF_PB[211]	VS_INF_PB[210]	VS_INF_PB[209]	VS_INF_PB[208]
0x6F	0x00	INFOFRAME_REG_6F	r	VS_INF_PB[223]	VS_INF_PB[222]	VS_INF_PB[221]	VS_INF_PB[220]	VS_INF_PB[219]	VS_INF_PB[218]	VS_INF_PB[217]	VS_INF_PB[216]
0x70	0x00	INFOFRAME_REG_70	r	ACP_PB[7]	ACP_PB[6]	ACP_PB[5]	ACP_PB[4]	ACP_PB[3]	ACP_PB[2]	ACP_PB[1]	ACP_PB[0]
0x71	0x00	INFOFRAME_REG_71	r	ACP_PB[15]	ACP_PB[14]	ACP_PB[13]	ACP_PB[12]	ACP_PB[11]	ACP_PB[10]	ACP_PB[9]	ACP_PB[8]
0x72	0x00	INFOFRAME_REG_72	r	ACP_PB[23]	ACP_PB[22]	ACP_PB[21]	ACP_PB[20]	ACP_PB[19]	ACP_PB[18]	ACP_PB[17]	ACP_PB[16]
0x73	0x00	INFOFRAME_REG_73	r	ACP_PB[31]	ACP_PB[30]	ACP_PB[29]	ACP_PB[28]	ACP_PB[27]	ACP_PB[26]	ACP_PB[25]	ACP_PB[24]
0x74	0x00	INFOFRAME_REG_74	r	ACP_PB[39]	ACP_PB[38]	ACP_PB[37]	ACP_PB[36]	ACP_PB[35]	ACP_PB[34]	ACP_PB[33]	ACP_PB[32]
0x75	0x00	INFOFRAME_REG_75	r	ACP_PB[47]	ACP_PB[46]	ACP_PB[45]	ACP_PB[44]	ACP_PB[43]	ACP_PB[42]	ACP_PB[41]	ACP_PB[40]
0x76	0x00	INFOFRAME_REG_76	r	ACP_PB[55]	ACP_PB[54]	ACP_PB[53]	ACP_PB[52]	ACP_PB[51]	ACP_PB[50]	ACP_PB[49]	ACP_PB[48]
0x77	0x00	INFOFRAME_REG_77	r	ACP_PB[63]	ACP_PB[62]	ACP_PB[61]	ACP_PB[60]	ACP_PB[59]	ACP_PB[58]	ACP_PB[57]	ACP_PB[56]
0x78	0x00	INFOFRAME_REG_78	r	ACP_PB[71]	ACP_PB[70]	ACP_PB[69]	ACP_PB[68]	ACP_PB[67]	ACP_PB[66]	ACP_PB[65]	ACP_PB[64]
0x79	0x00	INFOFRAME_REG_79	r	ACP_PB[79]	ACP_PB[78]	ACP_PB[77]	ACP_PB[76]	ACP_PB[75]	ACP_PB[74]	ACP_PB[73]	ACP_PB[72]
0x7A	0x00	INFOFRAME_REG_7A	r	ACP_PB[87]	ACP_PB[86]	ACP_PB[85]	ACP_PB[84]	ACP_PB[83]	ACP_PB[82]	ACP_PB[81]	ACP_PB[80]
0x7B	0x00	INFOFRAME_REG_7B	r	ACP_PB[95]	ACP_PB[94]	ACP_PB[93]	ACP_PB[92]	ACP_PB[91]	ACP_PB[90]	ACP_PB[89]	ACP_PB[88]
0x7C	0x00	INFOFRAME_REG_7C	r	ACP_PB[103]	ACP_PB[102]	ACP_PB[101]	ACP_PB[100]	ACP_PB[99]	ACP_PB[98]	ACP_PB[97]	ACP_PB[96]
0x7D	0x00	INFOFRAME_REG_7D	r	ACP_PB[111]	ACP_PB[110]	ACP_PB[109]	ACP_PB[108]	ACP_PB[107]	ACP_PB[106]	ACP_PB[105]	ACP_PB[104]
0x7E	0x00	INFOFRAME_REG_7E	r	ACP_PB[119]	ACP_PB[118]	ACP_PB[117]	ACP_PB[116]	ACP_PB[115]	ACP_PB[114]	ACP_PB[113]	ACP_PB[112]
0x7F	0x00	INFOFRAME_REG_7F	r	ACP_PB[127]	ACP_PB[126]	ACP_PB[125]	ACP_PB[124]	ACP_PB[123]	ACP_PB[122]	ACP_PB[121]	ACP_PB[120]
0x80	0x00	INFOFRAME_REG_80	r	ACP_PB[135]	ACP_PB[134]	ACP_PB[133]	ACP_PB[132]	ACP_PB[131]	ACP_PB[130]	ACP_PB[129]	ACP_PB[128]
0x81	0x00	INFOFRAME_REG_81	r	ACP_PB[143]	ACP_PB[142]	ACP_PB[141]	ACP_PB[140]	ACP_PB[139]	ACP_PB[138]	ACP_PB[137]	ACP_PB[136]
0x82	0x00	INFOFRAME_REG_82	r	ACP_PB[151]	ACP_PB[150]	ACP_PB[149]	ACP_PB[148]	ACP_PB[147]	ACP_PB[146]	ACP_PB[145]	ACP_PB[144]
0x83	0x00	INFOFRAME_REG_83	r	ACP_PB[159]	ACP_PB[158]	ACP_PB[157]	ACP_PB[156]	ACP_PB[155]	ACP_PB[154]	ACP_PB[153]	ACP_PB[152]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x84	0x00	INFOFRAME_REG_84	r	ACP_PB[167]	ACP_PB[166]	ACP_PB[165]	ACP_PB[164]	ACP_PB[163]	ACP_PB[162]	ACP_PB[161]	ACP_PB[160]
0x85	0x00	INFOFRAME_REG_85	r	ACP_PB[175]	ACP_PB[174]	ACP_PB[173]	ACP_PB[172]	ACP_PB[171]	ACP_PB[170]	ACP_PB[169]	ACP_PB[168]
0x86	0x00	INFOFRAME_REG_86	r	ACP_PB[183]	ACP_PB[182]	ACP_PB[181]	ACP_PB[180]	ACP_PB[179]	ACP_PB[178]	ACP_PB[177]	ACP_PB[176]
0x87	0x00	INFOFRAME_REG_87	r	ACP_PB[191]	ACP_PB[190]	ACP_PB[189]	ACP_PB[188]	ACP_PB[187]	ACP_PB[186]	ACP_PB[185]	ACP_PB[184]
0x88	0x00	INFOFRAME_REG_88	r	ACP_PB[199]	ACP_PB[198]	ACP_PB[197]	ACP_PB[196]	ACP_PB[195]	ACP_PB[194]	ACP_PB[193]	ACP_PB[192]
0x89	0x00	INFOFRAME_REG_89	r	ACP_PB[207]	ACP_PB[206]	ACP_PB[205]	ACP_PB[204]	ACP_PB[203]	ACP_PB[202]	ACP_PB[201]	ACP_PB[200]
0x8A	0x00	INFOFRAME_REG_8A	r	ACP_PB[215]	ACP_PB[214]	ACP_PB[213]	ACP_PB[212]	ACP_PB[211]	ACP_PB[210]	ACP_PB[209]	ACP_PB[208]
0x8B	0x00	INFOFRAME_REG_8B	r	ACP_PB[223]	ACP_PB[222]	ACP_PB[221]	ACP_PB[220]	ACP_PB[219]	ACP_PB[218]	ACP_PB[217]	ACP_PB[216]
0x8C	0x00	INFOFRAME_REG_8C	r	ISRC1_PB[7]	ISRC1_PB[6]	ISRC1_PB[5]	ISRC1_PB[4]	ISRC1_PB[3]	ISRC1_PB[2]	ISRC1_PB[1]	ISRC1_PB[0]
0x8D	0x00	INFOFRAME_REG_8D	r	ISRC1_PB[15]	ISRC1_PB[14]	ISRC1_PB[13]	ISRC1_PB[12]	ISRC1_PB[11]	ISRC1_PB[10]	ISRC1_PB[9]	ISRC1_PB[8]
0x8E	0x00	INFOFRAME_REG_8E	r	ISRC1_PB[23]	ISRC1_PB[22]	ISRC1_PB[21]	ISRC1_PB[20]	ISRC1_PB[19]	ISRC1_PB[18]	ISRC1_PB[17]	ISRC1_PB[16]
0x8F	0x00	INFOFRAME_REG_8F	r	ISRC1_PB[31]	ISRC1_PB[30]	ISRC1_PB[29]	ISRC1_PB[28]	ISRC1_PB[27]	ISRC1_PB[26]	ISRC1_PB[25]	ISRC1_PB[24]
0x90	0x00	INFOFRAME_REG_90	r	ISRC1_PB[39]	ISRC1_PB[38]	ISRC1_PB[37]	ISRC1_PB[36]	ISRC1_PB[35]	ISRC1_PB[34]	ISRC1_PB[33]	ISRC1_PB[32]
0x91	0x00	INFOFRAME_REG_91	r	ISRC1_PB[47]	ISRC1_PB[46]	ISRC1_PB[45]	ISRC1_PB[44]	ISRC1_PB[43]	ISRC1_PB[42]	ISRC1_PB[41]	ISRC1_PB[40]
0x92	0x00	INFOFRAME_REG_92	r	ISRC1_PB[55]	ISRC1_PB[54]	ISRC1_PB[53]	ISRC1_PB[52]	ISRC1_PB[51]	ISRC1_PB[50]	ISRC1_PB[49]	ISRC1_PB[48]
0x93	0x00	INFOFRAME_REG_93	r	ISRC1_PB[63]	ISRC1_PB[62]	ISRC1_PB[61]	ISRC1_PB[60]	ISRC1_PB[59]	ISRC1_PB[58]	ISRC1_PB[57]	ISRC1_PB[56]
0x94	0x00	INFOFRAME_REG_94	r	ISRC1_PB[71]	ISRC1_PB[70]	ISRC1_PB[69]	ISRC1_PB[68]	ISRC1_PB[67]	ISRC1_PB[66]	ISRC1_PB[65]	ISRC1_PB[64]
0x95	0x00	INFOFRAME_REG_95	r	ISRC1_PB[79]	ISRC1_PB[78]	ISRC1_PB[77]	ISRC1_PB[76]	ISRC1_PB[75]	ISRC1_PB[74]	ISRC1_PB[73]	ISRC1_PB[72]
0x96	0x00	INFOFRAME_REG_96	r	ISRC1_PB[87]	ISRC1_PB[86]	ISRC1_PB[85]	ISRC1_PB[84]	ISRC1_PB[83]	ISRC1_PB[82]	ISRC1_PB[81]	ISRC1_PB[80]
0x97	0x00	INFOFRAME_REG_97	r	ISRC1_PB[95]	ISRC1_PB[94]	ISRC1_PB[93]	ISRC1_PB[92]	ISRC1_PB[91]	ISRC1_PB[90]	ISRC1_PB[89]	ISRC1_PB[88]
0x98	0x00	INFOFRAME_REG_98	r	ISRC1_PB[103]	ISRC1_PB[102]	ISRC1_PB[101]	ISRC1_PB[100]	ISRC1_PB[99]	ISRC1_PB[98]	ISRC1_PB[97]	ISRC1_PB[96]
0x99	0x00	INFOFRAME_REG_99	r	ISRC1_PB[111]	ISRC1_PB[110]	ISRC1_PB[109]	ISRC1_PB[108]	ISRC1_PB[107]	ISRC1_PB[106]	ISRC1_PB[105]	ISRC1_PB[104]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x9A	0x00	INFOFRAME_REG_9A	r	ISRC1_PB[119]	ISRC1_PB[118]	ISRC1_PB[117]	ISRC1_PB[116]	ISRC1_PB[115]	ISRC1_PB[114]	ISRC1_PB[113]	ISRC1_PB[112]
0x9B	0x00	INFOFRAME_REG_9B	r	ISRC1_PB[127]	ISRC1_PB[126]	ISRC1_PB[125]	ISRC1_PB[124]	ISRC1_PB[123]	ISRC1_PB[122]	ISRC1_PB[121]	ISRC1_PB[120]
0x9C	0x00	INFOFRAME_REG_9C	r	ISRC1_PB[135]	ISRC1_PB[134]	ISRC1_PB[133]	ISRC1_PB[132]	ISRC1_PB[131]	ISRC1_PB[130]	ISRC1_PB[129]	ISRC1_PB[128]
0x9D	0x00	INFOFRAME_REG_9D	r	ISRC1_PB[143]	ISRC1_PB[142]	ISRC1_PB[141]	ISRC1_PB[140]	ISRC1_PB[139]	ISRC1_PB[138]	ISRC1_PB[137]	ISRC1_PB[136]
0x9E	0x00	INFOFRAME_REG_9E	r	ISRC1_PB[151]	ISRC1_PB[150]	ISRC1_PB[149]	ISRC1_PB[148]	ISRC1_PB[147]	ISRC1_PB[146]	ISRC1_PB[145]	ISRC1_PB[144]
0x9F	0x00	INFOFRAME_REG_9F	r	ISRC1_PB[159]	ISRC1_PB[158]	ISRC1_PB[157]	ISRC1_PB[156]	ISRC1_PB[155]	ISRC1_PB[154]	ISRC1_PB[153]	ISRC1_PB[152]
0xA0	0x00	INFOFRAME_REG_A0	r	ISRC1_PB[167]	ISRC1_PB[166]	ISRC1_PB[165]	ISRC1_PB[164]	ISRC1_PB[163]	ISRC1_PB[162]	ISRC1_PB[161]	ISRC1_PB[160]
0xA1	0x00	INFOFRAME_REG_A1	r	ISRC1_PB[175]	ISRC1_PB[174]	ISRC1_PB[173]	ISRC1_PB[172]	ISRC1_PB[171]	ISRC1_PB[170]	ISRC1_PB[169]	ISRC1_PB[168]
0xA2	0x00	INFOFRAME_REG_A2	r	ISRC1_PB[183]	ISRC1_PB[182]	ISRC1_PB[181]	ISRC1_PB[180]	ISRC1_PB[179]	ISRC1_PB[178]	ISRC1_PB[177]	ISRC1_PB[176]
0xA3	0x00	INFOFRAME_REG_A3	r	ISRC1_PB[191]	ISRC1_PB[190]	ISRC1_PB[189]	ISRC1_PB[188]	ISRC1_PB[187]	ISRC1_PB[186]	ISRC1_PB[185]	ISRC1_PB[184]
0xA4	0x00	INFOFRAME_REG_A4	r	ISRC1_PB[199]	ISRC1_PB[198]	ISRC1_PB[197]	ISRC1_PB[196]	ISRC1_PB[195]	ISRC1_PB[194]	ISRC1_PB[193]	ISRC1_PB[192]
0xA5	0x00	INFOFRAME_REG_A5	r	ISRC1_PB[207]	ISRC1_PB[206]	ISRC1_PB[205]	ISRC1_PB[204]	ISRC1_PB[203]	ISRC1_PB[202]	ISRC1_PB[201]	ISRC1_PB[200]
0xA6	0x00	INFOFRAME_REG_A6	r	ISRC1_PB[215]	ISRC1_PB[214]	ISRC1_PB[213]	ISRC1_PB[212]	ISRC1_PB[211]	ISRC1_PB[210]	ISRC1_PB[209]	ISRC1_PB[208]
0xA7	0x00	INFOFRAME_REG_A7	r	ISRC1_PB[223]	ISRC1_PB[222]	ISRC1_PB[221]	ISRC1_PB[220]	ISRC1_PB[219]	ISRC1_PB[218]	ISRC1_PB[217]	ISRC1_PB[216]
0xA8	0x00	INFOFRAME_REG_A8	r	ISRC2_PB[7]	ISRC2_PB[6]	ISRC2_PB[5]	ISRC2_PB[4]	ISRC2_PB[3]	ISRC2_PB[2]	ISRC2_PB[1]	ISRC2_PB[0]
0xA9	0x00	INFOFRAME_REG_A9	r	ISRC2_PB[15]	ISRC2_PB[14]	ISRC2_PB[13]	ISRC2_PB[12]	ISRC2_PB[11]	ISRC2_PB[10]	ISRC2_PB[9]	ISRC2_PB[8]
0xAA	0x00	INFOFRAME_REG_AA	r	ISRC2_PB[23]	ISRC2_PB[22]	ISRC2_PB[21]	ISRC2_PB[20]	ISRC2_PB[19]	ISRC2_PB[18]	ISRC2_PB[17]	ISRC2_PB[16]
0xAB	0x00	INFOFRAME_REG_AB	r	ISRC2_PB[31]	ISRC2_PB[30]	ISRC2_PB[29]	ISRC2_PB[28]	ISRC2_PB[27]	ISRC2_PB[26]	ISRC2_PB[25]	ISRC2_PB[24]
0xAC	0x00	INFOFRAME_REG_AC	r	ISRC2_PB[39]	ISRC2_PB[38]	ISRC2_PB[37]	ISRC2_PB[36]	ISRC2_PB[35]	ISRC2_PB[34]	ISRC2_PB[33]	ISRC2_PB[32]
0xAD	0x00	INFOFRAME_REG_AD	r	ISRC2_PB[47]	ISRC2_PB[46]	ISRC2_PB[45]	ISRC2_PB[44]	ISRC2_PB[43]	ISRC2_PB[42]	ISRC2_PB[41]	ISRC2_PB[40]
0xAE	0x00	INFOFRAME_REG_AE	r	ISRC2_PB[55]	ISRC2_PB[54]	ISRC2_PB[53]	ISRC2_PB[52]	ISRC2_PB[51]	ISRC2_PB[50]	ISRC2_PB[49]	ISRC2_PB[48]
0xAF	0x00	INFOFRAME_REG_AF	r	ISRC2_PB[63]	ISRC2_PB[62]	ISRC2_PB[61]	ISRC2_PB[60]	ISRC2_PB[59]	ISRC2_PB[58]	ISRC2_PB[57]	ISRC2_PB[56]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xB0	0x00	INFOFRAME_REG_B0	r	ISRC2_PB[71]	ISRC2_PB[70]	ISRC2_PB[69]	ISRC2_PB[68]	ISRC2_PB[67]	ISRC2_PB[66]	ISRC2_PB[65]	ISRC2_PB[64]
0xB1	0x00	INFOFRAME_REG_B1	r	ISRC2_PB[79]	ISRC2_PB[78]	ISRC2_PB[77]	ISRC2_PB[76]	ISRC2_PB[75]	ISRC2_PB[74]	ISRC2_PB[73]	ISRC2_PB[72]
0xB2	0x00	INFOFRAME_REG_B2	r	ISRC2_PB[87]	ISRC2_PB[86]	ISRC2_PB[85]	ISRC2_PB[84]	ISRC2_PB[83]	ISRC2_PB[82]	ISRC2_PB[81]	ISRC2_PB[80]
0xB3	0x00	INFOFRAME_REG_B3	r	ISRC2_PB[95]	ISRC2_PB[94]	ISRC2_PB[93]	ISRC2_PB[92]	ISRC2_PB[91]	ISRC2_PB[90]	ISRC2_PB[89]	ISRC2_PB[88]
0xB4	0x00	INFOFRAME_REG_B4	r	ISRC2_PB[103]	ISRC2_PB[102]	ISRC2_PB[101]	ISRC2_PB[100]	ISRC2_PB[99]	ISRC2_PB[98]	ISRC2_PB[97]	ISRC2_PB[96]
0xB5	0x00	INFOFRAME_REG_B5	r	ISRC2_PB[111]	ISRC2_PB[110]	ISRC2_PB[109]	ISRC2_PB[108]	ISRC2_PB[107]	ISRC2_PB[106]	ISRC2_PB[105]	ISRC2_PB[104]
0xB6	0x00	INFOFRAME_REG_B6	r	ISRC2_PB[119]	ISRC2_PB[118]	ISRC2_PB[117]	ISRC2_PB[116]	ISRC2_PB[115]	ISRC2_PB[114]	ISRC2_PB[113]	ISRC2_PB[112]
0xB7	0x00	INFOFRAME_REG_B7	r	ISRC2_PB[127]	ISRC2_PB[126]	ISRC2_PB[125]	ISRC2_PB[124]	ISRC2_PB[123]	ISRC2_PB[122]	ISRC2_PB[121]	ISRC2_PB[120]
0xB8	0x00	INFOFRAME_REG_B8	r	ISRC2_PB[135]	ISRC2_PB[134]	ISRC2_PB[133]	ISRC2_PB[132]	ISRC2_PB[131]	ISRC2_PB[130]	ISRC2_PB[129]	ISRC2_PB[128]
0xB9	0x00	INFOFRAME_REG_B9	r	ISRC2_PB[143]	ISRC2_PB[142]	ISRC2_PB[141]	ISRC2_PB[140]	ISRC2_PB[139]	ISRC2_PB[138]	ISRC2_PB[137]	ISRC2_PB[136]
0xBA	0x00	INFOFRAME_REG_BA	r	ISRC2_PB[151]	ISRC2_PB[150]	ISRC2_PB[149]	ISRC2_PB[148]	ISRC2_PB[147]	ISRC2_PB[146]	ISRC2_PB[145]	ISRC2_PB[144]
0xBB	0x00	INFOFRAME_REG_BB	r	ISRC2_PB[159]	ISRC2_PB[158]	ISRC2_PB[157]	ISRC2_PB[156]	ISRC2_PB[155]	ISRC2_PB[154]	ISRC2_PB[153]	ISRC2_PB[152]
0xBC	0x00	INFOFRAME_REG_BC	r	ISRC2_PB[167]	ISRC2_PB[166]	ISRC2_PB[165]	ISRC2_PB[164]	ISRC2_PB[163]	ISRC2_PB[162]	ISRC2_PB[161]	ISRC2_PB[160]
0xBD	0x00	INFOFRAME_REG_BD	r	ISRC2_PB[175]	ISRC2_PB[174]	ISRC2_PB[173]	ISRC2_PB[172]	ISRC2_PB[171]	ISRC2_PB[170]	ISRC2_PB[169]	ISRC2_PB[168]
0xBE	0x00	INFOFRAME_REG_BE	r	ISRC2_PB[183]	ISRC2_PB[182]	ISRC2_PB[181]	ISRC2_PB[180]	ISRC2_PB[179]	ISRC2_PB[178]	ISRC2_PB[177]	ISRC2_PB[176]
0xBF	0x00	INFOFRAME_REG_BF	r	ISRC2_PB[191]	ISRC2_PB[190]	ISRC2_PB[189]	ISRC2_PB[188]	ISRC2_PB[187]	ISRC2_PB[186]	ISRC2_PB[185]	ISRC2_PB[184]
0xC0	0x00	INFOFRAME_REG_C0	r	ISRC2_PB[199]	ISRC2_PB[198]	ISRC2_PB[197]	ISRC2_PB[196]	ISRC2_PB[195]	ISRC2_PB[194]	ISRC2_PB[193]	ISRC2_PB[192]
0xC1	0x00	INFOFRAME_REG_C1	r	ISRC2_PB[207]	ISRC2_PB[206]	ISRC2_PB[205]	ISRC2_PB[204]	ISRC2_PB[203]	ISRC2_PB[202]	ISRC2_PB[201]	ISRC2_PB[200]
0xC2	0x00	INFOFRAME_REG_C2	r	ISRC2_PB[215]	ISRC2_PB[214]	ISRC2_PB[213]	ISRC2_PB[212]	ISRC2_PB[211]	ISRC2_PB[210]	ISRC2_PB[209]	ISRC2_PB[208]
0xC3	0x00	INFOFRAME_REG_C3	r	ISRC2_PB[223]	ISRC2_PB[222]	ISRC2_PB[221]	ISRC2_PB[220]	ISRC2_PB[219]	ISRC2_PB[218]	ISRC2_PB[217]	ISRC2_PB[216]
0xC4	0x00	INFOFRAME_REG_C4	r	GBD[7]	GBD[6]	GBD[5]	GBD[4]	GBD[3]	GBD[2]	GBD[1]	GBD[0]
0xC5	0x00	INFOFRAME_REG_C5	r	GBD[15]	GBD[14]	GBD[13]	GBD[12]	GBD[11]	GBD[10]	GBD[9]	GBD[8]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xC6	0x00	INFOFRAME_REG_C6	r	GBD[23]	GBD[22]	GBD[21]	GBD[20]	GBD[19]	GBD[18]	GBD[17]	GBD[16]
0xC7	0x00	INFOFRAME_REG_C7	r	GBD[31]	GBD[30]	GBD[29]	GBD[28]	GBD[27]	GBD[26]	GBD[25]	GBD[24]
0xC8	0x00	INFOFRAME_REG_C8	r	GBD[39]	GBD[38]	GBD[37]	GBD[36]	GBD[35]	GBD[34]	GBD[33]	GBD[32]
0xC9	0x00	INFOFRAME_REG_C9	r	GBD[47]	GBD[46]	GBD[45]	GBD[44]	GBD[43]	GBD[42]	GBD[41]	GBD[40]
0xCA	0x00	INFOFRAME_REG_CA	r	GBD[55]	GBD[54]	GBD[53]	GBD[52]	GBD[51]	GBD[50]	GBD[49]	GBD[48]
0xCB	0x00	INFOFRAME_REG_CB	r	GBD[63]	GBD[62]	GBD[61]	GBD[60]	GBD[59]	GBD[58]	GBD[57]	GBD[56]
0xCC	0x00	INFOFRAME_REG_CC	r	GBD[71]	GBD[70]	GBD[69]	GBD[68]	GBD[67]	GBD[66]	GBD[65]	GBD[64]
0xCD	0x00	INFOFRAME_REG_CD	r	GBD[79]	GBD[78]	GBD[77]	GBD[76]	GBD[75]	GBD[74]	GBD[73]	GBD[72]
0xCE	0x00	INFOFRAME_REG_CE	r	GBD[87]	GBD[86]	GBD[85]	GBD[84]	GBD[83]	GBD[82]	GBD[81]	GBD[80]
0xCF	0x00	INFOFRAME_REG_CF	r	GBD[95]	GBD[94]	GBD[93]	GBD[92]	GBD[91]	GBD[90]	GBD[89]	GBD[88]
0xD0	0x00	INFOFRAME_REG_D0	r	GBD[103]	GBD[102]	GBD[101]	GBD[100]	GBD[99]	GBD[98]	GBD[97]	GBD[96]
0xD1	0x00	INFOFRAME_REG_D1	r	GBD[111]	GBD[110]	GBD[109]	GBD[108]	GBD[107]	GBD[106]	GBD[105]	GBD[104]
0xD2	0x00	INFOFRAME_REG_D2	r	GBD[119]	GBD[118]	GBD[117]	GBD[116]	GBD[115]	GBD[114]	GBD[113]	GBD[112]
0xD3	0x00	INFOFRAME_REG_D3	r	GBD[127]	GBD[126]	GBD[125]	GBD[124]	GBD[123]	GBD[122]	GBD[121]	GBD[120]
0xD4	0x00	INFOFRAME_REG_D4	r	GBD[135]	GBD[134]	GBD[133]	GBD[132]	GBD[131]	GBD[130]	GBD[129]	GBD[128]
0xD5	0x00	INFOFRAME_REG_D5	r	GBD[143]	GBD[142]	GBD[141]	GBD[140]	GBD[139]	GBD[138]	GBD[137]	GBD[136]
0xD6	0x00	INFOFRAME_REG_D6	r	GBD[151]	GBD[150]	GBD[149]	GBD[148]	GBD[147]	GBD[146]	GBD[145]	GBD[144]
0xD7	0x00	INFOFRAME_REG_D7	r	GBD[159]	GBD[158]	GBD[157]	GBD[156]	GBD[155]	GBD[154]	GBD[153]	GBD[152]
0xD8	0x00	INFOFRAME_REG_D8	r	GBD[167]	GBD[166]	GBD[165]	GBD[164]	GBD[163]	GBD[162]	GBD[161]	GBD[160]
0xD9	0x00	INFOFRAME_REG_D9	r	GBD[175]	GBD[174]	GBD[173]	GBD[172]	GBD[171]	GBD[170]	GBD[169]	GBD[168]
0xDA	0x00	INFOFRAME_REG_DA	r	GBD[183]	GBD[182]	GBD[181]	GBD[180]	GBD[179]	GBD[178]	GBD[177]	GBD[176]
0xDB	0x00	INFOFRAME_REG_DB	r	GBD[191]	GBD[190]	GBD[189]	GBD[188]	GBD[187]	GBD[186]	GBD[185]	GBD[184]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xDC	0x00	INFOFRAME_REG_DC	r	GBD[199]	GBD[198]	GBD[197]	GBD[196]	GBD[195]	GBD[194]	GBD[193]	GBD[192]
0xDD	0x00	INFOFRAME_REG_DD	r	GBD[207]	GBD[206]	GBD[205]	GBD[204]	GBD[203]	GBD[202]	GBD[201]	GBD[200]
0xDE	0x00	INFOFRAME_REG_DE	r	GBD[215]	GBD[214]	GBD[213]	GBD[212]	GBD[211]	GBD[210]	GBD[209]	GBD[208]
0xDF	0x00	INFOFRAME_REG_DF	r	GBD[223]	GBD[222]	GBD[221]	GBD[220]	GBD[219]	GBD[218]	GBD[217]	GBD[216]
0xE0	0x82	INFOFRAME_REG_E0	rw	AVI_PACKET_ID[7]	AVI_PACKET_ID[6]	AVI_PACKET_ID[5]	AVI_PACKET_ID[4]	AVI_PACKET_ID[3]	AVI_PACKET_ID[2]	AVI_PACKET_ID[1]	AVI_PACKET_ID[0]
0xE1	0x00	INFOFRAME_REG_E1	r	AVI_INF_VERS[7]	AVI_INF_VERS[6]	AVI_INF_VERS[5]	AVI_INF_VERS[4]	AVI_INF_VERS[3]	AVI_INF_VERS[2]	AVI_INF_VERS[1]	AVI_INF_VERS[0]
0xE2	0x00	INFOFRAME_REG_E2	r	AVI_INF_LEN[7]	AVI_INF_LEN[6]	AVI_INF_LEN[5]	AVI_INF_LEN[4]	AVI_INF_LEN[3]	AVI_INF_LEN[2]	AVI_INF_LEN[1]	AVI_INF_LEN[0]
0xE3	0x84	INFOFRAME_REG_E3	rw	AUD_PACKET_ID[7]	AUD_PACKET_ID[6]	AUD_PACKET_ID[5]	AUD_PACKET_ID[4]	AUD_PACKET_ID[3]	AUD_PACKET_ID[2]	AUD_PACKET_ID[1]	AUD_PACKET_ID[0]
0xE4	0x00	INFOFRAME_REG_E4	r	AUD_INF_VERS[7]	AUD_INF_VERS[6]	AUD_INF_VERS[5]	AUD_INF_VERS[4]	AUD_INF_VERS[3]	AUD_INF_VERS[2]	AUD_INF_VERS[1]	AUD_INF_VERS[0]
0xE5	0x00	INFOFRAME_REG_E5	r	AUD_INF_LEN[7]	AUD_INF_LEN[6]	AUD_INF_LEN[5]	AUD_INF_LEN[4]	AUD_INF_LEN[3]	AUD_INF_LEN[2]	AUD_INF_LEN[1]	AUD_INF_LEN[0]
0xE6	0x83	INFOFRAME_REG_E6	rw	SPD_PACKET_ID[7]	SPD_PACKET_ID[6]	SPD_PACKET_ID[5]	SPD_PACKET_ID[4]	SPD_PACKET_ID[3]	SPD_PACKET_ID[2]	SPD_PACKET_ID[1]	SPD_PACKET_ID[0]
0xE7	0x00	INFOFRAME_REG_E7	r	SPD_INF_VERS[7]	SPD_INF_VERS[6]	SPD_INF_VERS[5]	SPD_INF_VERS[4]	SPD_INF_VERS[3]	SPD_INF_VERS[2]	SPD_INF_VERS[1]	SPD_INF_VERS[0]
0xE8	0x00	INFOFRAME_REG_E8	r	SPD_INF_LEN[7]	SPD_INF_LEN[6]	SPD_INF_LEN[5]	SPD_INF_LEN[4]	SPD_INF_LEN[3]	SPD_INF_LEN[2]	SPD_INF_LEN[1]	SPD_INF_LEN[0]
0xE9	0x85	INFOFRAME_REG_E9	rw	MS_PACKET_ID[7]	MS_PACKET_ID[6]	MS_PACKET_ID[5]	MS_PACKET_ID[4]	MS_PACKET_ID[3]	MS_PACKET_ID[2]	MS_PACKET_ID[1]	MS_PACKET_ID[0]
0xEA	0x00	INFOFRAME_REG_EA	r	MS_INF_VERS[7]	MS_INF_VERS[6]	MS_INF_VERS[5]	MS_INF_VERS[4]	MS_INF_VERS[3]	MS_INF_VERS[2]	MS_INF_VERS[1]	MS_INF_VERS[0]
0xEB	0x00	INFOFRAME_REG_EB	r	MS_INF_LEN[7]	MS_INF_LEN[6]	MS_INF_LEN[5]	MS_INF_LEN[4]	MS_INF_LEN[3]	MS_INF_LEN[2]	MS_INF_LEN[1]	MS_INF_LEN[0]
0xEC	0x81	INFOFRAME_REG_EC	rw	VS_PACKET_ID[7]	VS_PACKET_ID[6]	VS_PACKET_ID[5]	VS_PACKET_ID[4]	VS_PACKET_ID[3]	VS_PACKET_ID[2]	VS_PACKET_ID[1]	VS_PACKET_ID[0]
0xED	0x00	INFOFRAME_REG_ED	r	VS_INF_VERS[7]	VS_INF_VERS[6]	VS_INF_VERS[5]	VS_INF_VERS[4]	VS_INF_VERS[3]	VS_INF_VERS[2]	VS_INF_VERS[1]	VS_INF_VERS[0]
0xEE	0x00	INFOFRAME_REG_EE	r	VS_INF_LEN[7]	VS_INF_LEN[6]	VS_INF_LEN[5]	VS_INF_LEN[4]	VS_INF_LEN[3]	VS_INF_LEN[2]	VS_INF_LEN[1]	VS_INF_LEN[0]
0xEF	0x04	INFOFRAME_REG_EF	rw	ACP_PACKET_ID[7]	ACP_PACKET_ID[6]	ACP_PACKET_ID[5]	ACP_PACKET_ID[4]	ACP_PACKET_ID[3]	ACP_PACKET_ID[2]	ACP_PACKET_ID[1]	ACP_PACKET_ID[0]
0xF0	0x00	INFOFRAME_REG_F0	r	ACP_TYPE[7]	ACP_TYPE[6]	ACP_TYPE[5]	ACP_TYPE[4]	ACP_TYPE[3]	ACP_TYPE[2]	ACP_TYPE[1]	ACP_TYPE[0]
0xF1	0x00	INFOFRAME_REG_F1	r	ACP_HEADER2[7]	ACP_HEADER2[6]	ACP_HEADER2[5]	ACP_HEADER2[4]	ACP_HEADER2[3]	ACP_HEADER2[2]	ACP_HEADER2[1]	ACP_HEADER2[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xF2	0x05	INFOFRAME_REG_F2	rw	ISRC1_PACKET_ID[7]	ISRC1_PACKET_ID[6]	ISRC1_PACKET_ID[5]	ISRC1_PACKET_ID[4]	ISRC1_PACKET_ID[3]	ISRC1_PACKET_ID[2]	ISRC1_PACKET_ID[1]	ISRC1_PACKET_ID[0]
0xF3	0x00	INFOFRAME_REG_F3	r	ISRC1_HEADER1[7]	ISRC1_HEADER1[6]	ISRC1_HEADER1[5]	ISRC1_HEADER1[4]	ISRC1_HEADER1[3]	ISRC1_HEADER1[2]	ISRC1_HEADER1[1]	ISRC1_HEADER1[0]
0xF4	0x00	INFOFRAME_REG_F4	r	ISRC1_HEADER2[7]	ISRC1_HEADER2[6]	ISRC1_HEADER2[5]	ISRC1_HEADER2[4]	ISRC1_HEADER2[3]	ISRC1_HEADER2[2]	ISRC1_HEADER2[1]	ISRC1_HEADER2[0]
0xF5	0x06	INFOFRAME_REG_F5	rw	ISRC2_PACKET_ID[7]	ISRC2_PACKET_ID[6]	ISRC2_PACKET_ID[5]	ISRC2_PACKET_ID[4]	ISRC2_PACKET_ID[3]	ISRC2_PACKET_ID[2]	ISRC2_PACKET_ID[1]	ISRC2_PACKET_ID[0]
0xF6	0x00	INFOFRAME_REG_F6	r	ISRC2_HEADER1[7]	ISRC2_HEADER1[6]	ISRC2_HEADER1[5]	ISRC2_HEADER1[4]	ISRC2_HEADER1[3]	ISRC2_HEADER1[2]	ISRC2_HEADER1[1]	ISRC2_HEADER1[0]
0xF7	0x00	INFOFRAME_REG_F7	r	ISRC2_HEADER2[7]	ISRC2_HEADER2[6]	ISRC2_HEADER2[5]	ISRC2_HEADER2[4]	ISRC2_HEADER2[3]	ISRC2_HEADER2[2]	ISRC2_HEADER2[1]	ISRC2_HEADER2[0]
0xF8	0x0A	INFOFRAME_REG_F8	rw	GAMUT_PACKET_ID[7]	GAMUT_PACKET_ID[6]	GAMUT_PACKET_ID[5]	GAMUT_PACKET_ID[4]	GAMUT_PACKET_ID[3]	GAMUT_PACKET_ID[2]	GAMUT_PACKET_ID[1]	GAMUT_PACKET_ID[0]
0xF9	0x00	INFOFRAME_REG_F9	r	GAMUT_HEADER1[7]	GAMUT_HEADER1[6]	GAMUT_HEADER1[5]	GAMUT_HEADER1[4]	GAMUT_HEADER1[3]	GAMUT_HEADER1[2]	GAMUT_HEADER1[1]	GAMUT_HEADER1[0]
0xFA	0x00	INFOFRAME_REG_FA	r	GAMUT_HEADER2[7]	GAMUT_HEADER2[6]	GAMUT_HEADER2[5]	GAMUT_HEADER2[4]	GAMUT_HEADER2[3]	GAMUT_HEADER2[2]	GAMUT_HEADER2[1]	GAMUT_HEADER2[0]
0xFD	0x81	INFOFRAME_REG_FD	rw	PKT_CNT_ID[7]	PKT_CNT_ID[6]	PKT_CNT_ID[5]	PKT_CNT_ID[4]	PKT_CNT_ID[3]	PKT_CNT_ID[2]	PKT_CNT_ID[1]	PKT_CNT_ID[0]
0xFE	0x00	INFOFRAME_REG_FE	rw	-	-	-	EN_PKT_CNT_SEL	PKT_CNT_SEL[3]	PKT_CNT_SEL[2]	PKT_CNT_SEL[1]	PKT_CNT_SEL[0]
0xFF	0x00	INFOFRAME_REG_FF	r	-	-	-	-	RB_PKT_CNT[3]	RB_PKT_CNT[2]	RB_PKT_CNT[1]	RB_PKT_CNT[0]

1.5 CEC MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00	CEC_REG_00	rw	CEC_TX_FRAME_HEADER[7]	CEC_TX_FRAME_HEADER[6]	CEC_TX_FRAME_HEADER[5]	CEC_TX_FRAME_HEADER[4]	CEC_TX_FRAME_HEADER[3]	CEC_TX_FRAME_HEADER[2]	CEC_TX_FRAME_HEADER[1]	CEC_TX_FRAME_HEADER[0]
0x01	0x00	CEC_REG_01	rw	CEC_TX_FRAME_DATA0[7]	CEC_TX_FRAME_DATA0[6]	CEC_TX_FRAME_DATA0[5]	CEC_TX_FRAME_DATA0[4]	CEC_TX_FRAME_DATA0[3]	CEC_TX_FRAME_DATA0[2]	CEC_TX_FRAME_DATA0[1]	CEC_TX_FRAME_DATA0[0]
0x02	0x00	CEC_REG_02	rw	CEC_TX_FRAME_DATA1[7]	CEC_TX_FRAME_DATA1[6]	CEC_TX_FRAME_DATA1[5]	CEC_TX_FRAME_DATA1[4]	CEC_TX_FRAME_DATA1[3]	CEC_TX_FRAME_DATA1[2]	CEC_TX_FRAME_DATA1[1]	CEC_TX_FRAME_DATA1[0]
0x03	0x00	CEC_REG_03	rw	CEC_TX_FRAME_DATA2[7]	CEC_TX_FRAME_DATA2[6]	CEC_TX_FRAME_DATA2[5]	CEC_TX_FRAME_DATA2[4]	CEC_TX_FRAME_DATA2[3]	CEC_TX_FRAME_DATA2[2]	CEC_TX_FRAME_DATA2[1]	CEC_TX_FRAME_DATA2[0]
0x04	0x00	CEC_REG_04	rw	CEC_TX_FRAME_DATA3[7]	CEC_TX_FRAME_DATA3[6]	CEC_TX_FRAME_DATA3[5]	CEC_TX_FRAME_DATA3[4]	CEC_TX_FRAME_DATA3[3]	CEC_TX_FRAME_DATA3[2]	CEC_TX_FRAME_DATA3[1]	CEC_TX_FRAME_DATA3[0]
0x05	0x00	CEC_REG_05	rw	CEC_TX_FRAME_DATA4[7]	CEC_TX_FRAME_DATA4[6]	CEC_TX_FRAME_DATA4[5]	CEC_TX_FRAME_DATA4[4]	CEC_TX_FRAME_DATA4[3]	CEC_TX_FRAME_DATA4[2]	CEC_TX_FRAME_DATA4[1]	CEC_TX_FRAME_DATA4[0]
0x06	0x00	CEC_REG_06	rw	CEC_TX_FRAME_DATA5[7]	CEC_TX_FRAME_DATA5[6]	CEC_TX_FRAME_DATA5[5]	CEC_TX_FRAME_DATA5[4]	CEC_TX_FRAME_DATA5[3]	CEC_TX_FRAME_DATA5[2]	CEC_TX_FRAME_DATA5[1]	CEC_TX_FRAME_DATA5[0]
0x07	0x00	CEC_REG_07	rw	CEC_TX_FRAME_DATA6[7]	CEC_TX_FRAME_DATA6[6]	CEC_TX_FRAME_DATA6[5]	CEC_TX_FRAME_DATA6[4]	CEC_TX_FRAME_DATA6[3]	CEC_TX_FRAME_DATA6[2]	CEC_TX_FRAME_DATA6[1]	CEC_TX_FRAME_DATA6[0]
0x08	0x00	CEC_REG_08	rw	CEC_TX_FRAME_DATA7[7]	CEC_TX_FRAME_DATA7[6]	CEC_TX_FRAME_DATA7[5]	CEC_TX_FRAME_DATA7[4]	CEC_TX_FRAME_DATA7[3]	CEC_TX_FRAME_DATA7[2]	CEC_TX_FRAME_DATA7[1]	CEC_TX_FRAME_DATA7[0]
0x09	0x00	CEC_REG_09	rw	CEC_TX_FRAME_DATA8[7]	CEC_TX_FRAME_DATA8[6]	CEC_TX_FRAME_DATA8[5]	CEC_TX_FRAME_DATA8[4]	CEC_TX_FRAME_DATA8[3]	CEC_TX_FRAME_DATA8[2]	CEC_TX_FRAME_DATA8[1]	CEC_TX_FRAME_DATA8[0]
0x0A	0x00	CEC_REG_0A	rw	CEC_TX_FRAME_DATA9[7]	CEC_TX_FRAME_DATA9[6]	CEC_TX_FRAME_DATA9[5]	CEC_TX_FRAME_DATA9[4]	CEC_TX_FRAME_DATA9[3]	CEC_TX_FRAME_DATA9[2]	CEC_TX_FRAME_DATA9[1]	CEC_TX_FRAME_DATA9[0]
0x0B	0x00	CEC_REG_0B	rw	CEC_TX_FRAME_DATA10[7]	CEC_TX_FRAME_DATA10[6]	CEC_TX_FRAME_DATA10[5]	CEC_TX_FRAME_DATA10[4]	CEC_TX_FRAME_DATA10[3]	CEC_TX_FRAME_DATA10[2]	CEC_TX_FRAME_DATA10[1]	CEC_TX_FRAME_DATA10[0]
0x0C	0x00	CEC_REG_0C	rw	CEC_TX_FRAME_DATA11[7]	CEC_TX_FRAME_DATA11[6]	CEC_TX_FRAME_DATA11[5]	CEC_TX_FRAME_DATA11[4]	CEC_TX_FRAME_DATA11[3]	CEC_TX_FRAME_DATA11[2]	CEC_TX_FRAME_DATA11[1]	CEC_TX_FRAME_DATA11[0]
0x0D	0x00	CEC_REG_0D	rw	CEC_TX_FRAME_DATA12[7]	CEC_TX_FRAME_DATA12[6]	CEC_TX_FRAME_DATA12[5]	CEC_TX_FRAME_DATA12[4]	CEC_TX_FRAME_DATA12[3]	CEC_TX_FRAME_DATA12[2]	CEC_TX_FRAME_DATA12[1]	CEC_TX_FRAME_DATA12[0]
0x0E	0x00	CEC_REG_0E	rw	CEC_TX_FRAME_DATA13[7]	CEC_TX_FRAME_DATA13[6]	CEC_TX_FRAME_DATA13[5]	CEC_TX_FRAME_DATA13[4]	CEC_TX_FRAME_DATA13[3]	CEC_TX_FRAME_DATA13[2]	CEC_TX_FRAME_DATA13[1]	CEC_TX_FRAME_DATA13[0]
0x0F	0x00	CEC_REG_0F	rw	CEC_TX_FRAME_DATA14[7]	CEC_TX_FRAME_DATA14[6]	CEC_TX_FRAME_DATA14[5]	CEC_TX_FRAME_DATA14[4]	CEC_TX_FRAME_DATA14[3]	CEC_TX_FRAME_DATA14[2]	CEC_TX_FRAME_DATA14[1]	CEC_TX_FRAME_DATA14[0]
0x10	0x00	CEC_REG_10	rw	-	-	-	CEC_TX_FRAME_LENGTH[4]	CEC_TX_FRAME_LENGTH[3]	CEC_TX_FRAME_LENGTH[2]	CEC_TX_FRAME_LENGTH[1]	CEC_TX_FRAME_LENGTH[0]
0x11	0x00	CEC_REG_11	rw	-	-	-	-	-	-	-	CEC_TX_ENABLE
0x12	0x13	CEC_REG_12	rw	-	CEC_TX_RETRY[2]	CEC_TX_RETRY[1]	CEC_TX_RETRY[0]	CEC_RETRY_SFT[3]	CEC_RETRY_SFT[2]	CEC_RETRY_SFT[1]	CEC_RETRY_SFT[0]
0x13	0x57	CEC_REG_13	rw	CEC_TX_SFT[3]	CEC_TX_SFT[2]	CEC_TX_SFT[1]	CEC_TX_SFT[0]	CEC_TX_SFT[3]	CEC_TX_SFT[2]	CEC_TX_SFT[1]	CEC_TX_SFT[0]
0x14	0x00	CEC_REG_14	r	CEC_TX_LOWDRIVE_COUNTER[3]	CEC_TX_LOWDRIVE_COUNTER[2]	CEC_TX_LOWDRIVE_COUNTER[1]	CEC_TX_LOWDRIVE_COUNTER[0]	CEC_TX_NACK_COUNTER[3]	CEC_TX_NACK_COUNTER[2]	CEC_TX_NACK_COUNTER[1]	CEC_TX_NACK_COUNTER[0]
0x15	0x00	CEC_REG_15	r	CEC_BUF0_RX_FRAME_HEADER[7]	CEC_BUF0_RX_FRAME_HEADER[6]	CEC_BUF0_RX_FRAME_HEADER[5]	CEC_BUF0_RX_FRAME_HEADER[4]	CEC_BUF0_RX_FRAME_HEADER[3]	CEC_BUF0_RX_FRAME_HEADER[2]	CEC_BUF0_RX_FRAME_HEADER[1]	CEC_BUF0_RX_FRAME_HEADER[0]
0x16	0x00	CEC_REG_16	r	CEC_BUF0_RX_FRAME_DATA0[7]	CEC_BUF0_RX_FRAME_DATA0[6]	CEC_BUF0_RX_FRAME_DATA0[5]	CEC_BUF0_RX_FRAME_DATA0[4]	CEC_BUF0_RX_FRAME_DATA0[3]	CEC_BUF0_RX_FRAME_DATA0[2]	CEC_BUF0_RX_FRAME_DATA0[1]	CEC_BUF0_RX_FRAME_DATA0[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x17	0x00	CEC_REG_17	r	CEC_BUF0_RX_FRAME_DATA1[7]	CEC_BUF0_RX_FRAME_DATA1[6]	CEC_BUF0_RX_FRAME_DATA1[5]	CEC_BUF0_RX_FRAME_DATA1[4]	CEC_BUF0_RX_FRAME_DATA1[3]	CEC_BUF0_RX_FRAME_DATA1[2]	CEC_BUF0_RX_FRAME_DATA1[1]	CEC_BUF0_RX_FRAME_DATA1[0]
0x18	0x00	CEC_REG_18	r	CEC_BUF0_RX_FRAME_DATA2[7]	CEC_BUF0_RX_FRAME_DATA2[6]	CEC_BUF0_RX_FRAME_DATA2[5]	CEC_BUF0_RX_FRAME_DATA2[4]	CEC_BUF0_RX_FRAME_DATA2[3]	CEC_BUF0_RX_FRAME_DATA2[2]	CEC_BUF0_RX_FRAME_DATA2[1]	CEC_BUF0_RX_FRAME_DATA2[0]
0x19	0x00	CEC_REG_19	r	CEC_BUF0_RX_FRAME_DATA3[7]	CEC_BUF0_RX_FRAME_DATA3[6]	CEC_BUF0_RX_FRAME_DATA3[5]	CEC_BUF0_RX_FRAME_DATA3[4]	CEC_BUF0_RX_FRAME_DATA3[3]	CEC_BUF0_RX_FRAME_DATA3[2]	CEC_BUF0_RX_FRAME_DATA3[1]	CEC_BUF0_RX_FRAME_DATA3[0]
0x1A	0x00	CEC_REG_1A	r	CEC_BUF0_RX_FRAME_DATA4[7]	CEC_BUF0_RX_FRAME_DATA4[6]	CEC_BUF0_RX_FRAME_DATA4[5]	CEC_BUF0_RX_FRAME_DATA4[4]	CEC_BUF0_RX_FRAME_DATA4[3]	CEC_BUF0_RX_FRAME_DATA4[2]	CEC_BUF0_RX_FRAME_DATA4[1]	CEC_BUF0_RX_FRAME_DATA4[0]
0x1B	0x00	CEC_REG_1B	r	CEC_BUF0_RX_FRAME_DATA5[7]	CEC_BUF0_RX_FRAME_DATA5[6]	CEC_BUF0_RX_FRAME_DATA5[5]	CEC_BUF0_RX_FRAME_DATA5[4]	CEC_BUF0_RX_FRAME_DATA5[3]	CEC_BUF0_RX_FRAME_DATA5[2]	CEC_BUF0_RX_FRAME_DATA5[1]	CEC_BUF0_RX_FRAME_DATA5[0]
0x1C	0x00	CEC_REG_1C	r	CEC_BUF0_RX_FRAME_DATA6[7]	CEC_BUF0_RX_FRAME_DATA6[6]	CEC_BUF0_RX_FRAME_DATA6[5]	CEC_BUF0_RX_FRAME_DATA6[4]	CEC_BUF0_RX_FRAME_DATA6[3]	CEC_BUF0_RX_FRAME_DATA6[2]	CEC_BUF0_RX_FRAME_DATA6[1]	CEC_BUF0_RX_FRAME_DATA6[0]
0x1D	0x00	CEC_REG_1D	r	CEC_BUF0_RX_FRAME_DATA7[7]	CEC_BUF0_RX_FRAME_DATA7[6]	CEC_BUF0_RX_FRAME_DATA7[5]	CEC_BUF0_RX_FRAME_DATA7[4]	CEC_BUF0_RX_FRAME_DATA7[3]	CEC_BUF0_RX_FRAME_DATA7[2]	CEC_BUF0_RX_FRAME_DATA7[1]	CEC_BUF0_RX_FRAME_DATA7[0]
0x1E	0x00	CEC_REG_1E	r	CEC_BUF0_RX_FRAME_DATA8[7]	CEC_BUF0_RX_FRAME_DATA8[6]	CEC_BUF0_RX_FRAME_DATA8[5]	CEC_BUF0_RX_FRAME_DATA8[4]	CEC_BUF0_RX_FRAME_DATA8[3]	CEC_BUF0_RX_FRAME_DATA8[2]	CEC_BUF0_RX_FRAME_DATA8[1]	CEC_BUF0_RX_FRAME_DATA8[0]
0x1F	0x00	CEC_REG_1F	r	CEC_BUF0_RX_FRAME_DATA9[7]	CEC_BUF0_RX_FRAME_DATA9[6]	CEC_BUF0_RX_FRAME_DATA9[5]	CEC_BUF0_RX_FRAME_DATA9[4]	CEC_BUF0_RX_FRAME_DATA9[3]	CEC_BUF0_RX_FRAME_DATA9[2]	CEC_BUF0_RX_FRAME_DATA9[1]	CEC_BUF0_RX_FRAME_DATA9[0]
0x20	0x00	CEC_REG_20	r	CEC_BUF0_RX_FRAME_DATA10[7]	CEC_BUF0_RX_FRAME_DATA10[6]	CEC_BUF0_RX_FRAME_DATA10[5]	CEC_BUF0_RX_FRAME_DATA10[4]	CEC_BUF0_RX_FRAME_DATA10[3]	CEC_BUF0_RX_FRAME_DATA10[2]	CEC_BUF0_RX_FRAME_DATA10[1]	CEC_BUF0_RX_FRAME_DATA10[0]
0x21	0x00	CEC_REG_21	r	CEC_BUF0_RX_FRAME_DATA11[7]	CEC_BUF0_RX_FRAME_DATA11[6]	CEC_BUF0_RX_FRAME_DATA11[5]	CEC_BUF0_RX_FRAME_DATA11[4]	CEC_BUF0_RX_FRAME_DATA11[3]	CEC_BUF0_RX_FRAME_DATA11[2]	CEC_BUF0_RX_FRAME_DATA11[1]	CEC_BUF0_RX_FRAME_DATA11[0]
0x22	0x00	CEC_REG_22	r	CEC_BUF0_RX_FRAME_DATA12[7]	CEC_BUF0_RX_FRAME_DATA12[6]	CEC_BUF0_RX_FRAME_DATA12[5]	CEC_BUF0_RX_FRAME_DATA12[4]	CEC_BUF0_RX_FRAME_DATA12[3]	CEC_BUF0_RX_FRAME_DATA12[2]	CEC_BUF0_RX_FRAME_DATA12[1]	CEC_BUF0_RX_FRAME_DATA12[0]
0x23	0x00	CEC_REG_23	r	CEC_BUF0_RX_FRAME_DATA13[7]	CEC_BUF0_RX_FRAME_DATA13[6]	CEC_BUF0_RX_FRAME_DATA13[5]	CEC_BUF0_RX_FRAME_DATA13[4]	CEC_BUF0_RX_FRAME_DATA13[3]	CEC_BUF0_RX_FRAME_DATA13[2]	CEC_BUF0_RX_FRAME_DATA13[1]	CEC_BUF0_RX_FRAME_DATA13[0]
0x24	0x00	CEC_REG_24	r	CEC_BUF0_RX_FRAME_DATA14[7]	CEC_BUF0_RX_FRAME_DATA14[6]	CEC_BUF0_RX_FRAME_DATA14[5]	CEC_BUF0_RX_FRAME_DATA14[4]	CEC_BUF0_RX_FRAME_DATA14[3]	CEC_BUF0_RX_FRAME_DATA14[2]	CEC_BUF0_RX_FRAME_DATA14[1]	CEC_BUF0_RX_FRAME_DATA14[0]
0x25	0x00	CEC_REG_25	r	-	-	-	CEC_BUF0_RX_FRAME_LENGTH[4]	CEC_BUF0_RX_FRAME_LENGTH[3]	CEC_BUF0_RX_FRAME_LENGTH[2]	CEC_BUF0_RX_FRAME_LENGTH[1]	CEC_BUF0_RX_FRAME_LENGTH[0]
0x27	0x10	CEC_REG_27	rw	-	CEC_LOGICAL_ADDRESS_MASK[2]	CEC_LOGICAL_ADDRESS_MASK[1]	CEC_LOGICAL_ADDRESS_MASK[0]	CEC_ERROR_REPORT_MODE	CEC_ERROR_DET_MODE	CEC_FORCE_NACK	CEC_FORCE_IGNORE
0x28	0xFF	CEC_REG_28	rw	CEC_LOGICAL_ADDRESS1[3]	CEC_LOGICAL_ADDRESS1[2]	CEC_LOGICAL_ADDRESS1[1]	CEC_LOGICAL_ADDRESS1[0]	CEC_LOGICAL_ADDRESS0[3]	CEC_LOGICAL_ADDRESS0[2]	CEC_LOGICAL_ADDRESS0[1]	CEC_LOGICAL_ADDRESS0[0]
0x29	0x0F	CEC_REG_29	rw	-	-	-	-	CEC_LOGICAL_ADDRESS2[3]	CEC_LOGICAL_ADDRESS2[2]	CEC_LOGICAL_ADDRESS2[1]	CEC_LOGICAL_ADDRESS2[0]
0x2A	0x3E	CEC_REG_2A	rw	-	-	-	-	-	-	-	CEC_POWER_UP
0x2B	0x07	CEC_REG_2B	rw	-	-	CEC_GLITCH_FILTER_CTRL[5]	CEC_GLITCH_FILTER_CTRL[4]	CEC_GLITCH_FILTER_CTRL[3]	CEC_GLITCH_FILTER_CTRL[2]	CEC_GLITCH_FILTER_CTRL[1]	CEC_GLITCH_FILTER_CTRL[0]
0x2C	0x00	CEC_REG_2C	sc	-	-	-	-	CEC_CLR_RX_RDY2	CEC_CLR_RX_RDY1	CEC_CLR_RX_RDY0	CEC_SOFT_RESET
0x4C	0x00	CEC_REG_4C	rw	-	-	-	-	-	CEC_DIS_AUTO_MODE	-	-
0x53	0x00	CEC_REG_53	r	-	-	CEC_BUF2_TIMESTAMP[1]	CEC_BUF2_TIMESTAMP[0]	CEC_BUF1_TIMESTAMP[1]	CEC_BUF1_TIMESTAMP[0]	CEC_BUF0_TIMESTAMP[1]	CEC_BUF0_TIMESTAMP[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x54	0x00	CEC_REG_54	r	CEC_BUF1_RX_FRAME_HEADER[7]	CEC_BUF1_RX_FRAME_HEADER[6]	CEC_BUF1_RX_FRAME_HEADER[5]	CEC_BUF1_RX_FRAME_HEADER[4]	CEC_BUF1_RX_FRAME_HEADER[3]	CEC_BUF1_RX_FRAME_HEADER[2]	CEC_BUF1_RX_FRAME_HEADER[1]	CEC_BUF1_RX_FRAME_HEADER[0]
0x55	0x00	CEC_REG_55	r	CEC_BUF1_RX_FRAME_DATA0[7]	CEC_BUF1_RX_FRAME_DATA0[6]	CEC_BUF1_RX_FRAME_DATA0[5]	CEC_BUF1_RX_FRAME_DATA0[4]	CEC_BUF1_RX_FRAME_DATA0[3]	CEC_BUF1_RX_FRAME_DATA0[2]	CEC_BUF1_RX_FRAME_DATA0[1]	CEC_BUF1_RX_FRAME_DATA0[0]
0x56	0x00	CEC_REG_56	r	CEC_BUF1_RX_FRAME_DATA1[7]	CEC_BUF1_RX_FRAME_DATA1[6]	CEC_BUF1_RX_FRAME_DATA1[5]	CEC_BUF1_RX_FRAME_DATA1[4]	CEC_BUF1_RX_FRAME_DATA1[3]	CEC_BUF1_RX_FRAME_DATA1[2]	CEC_BUF1_RX_FRAME_DATA1[1]	CEC_BUF1_RX_FRAME_DATA1[0]
0x57	0x00	CEC_REG_57	r	CEC_BUF1_RX_FRAME_DATA2[7]	CEC_BUF1_RX_FRAME_DATA2[6]	CEC_BUF1_RX_FRAME_DATA2[5]	CEC_BUF1_RX_FRAME_DATA2[4]	CEC_BUF1_RX_FRAME_DATA2[3]	CEC_BUF1_RX_FRAME_DATA2[2]	CEC_BUF1_RX_FRAME_DATA2[1]	CEC_BUF1_RX_FRAME_DATA2[0]
0x58	0x00	CEC_REG_58	r	CEC_BUF1_RX_FRAME_DATA3[7]	CEC_BUF1_RX_FRAME_DATA3[6]	CEC_BUF1_RX_FRAME_DATA3[5]	CEC_BUF1_RX_FRAME_DATA3[4]	CEC_BUF1_RX_FRAME_DATA3[3]	CEC_BUF1_RX_FRAME_DATA3[2]	CEC_BUF1_RX_FRAME_DATA3[1]	CEC_BUF1_RX_FRAME_DATA3[0]
0x59	0x00	CEC_REG_59	r	CEC_BUF1_RX_FRAME_DATA4[7]	CEC_BUF1_RX_FRAME_DATA4[6]	CEC_BUF1_RX_FRAME_DATA4[5]	CEC_BUF1_RX_FRAME_DATA4[4]	CEC_BUF1_RX_FRAME_DATA4[3]	CEC_BUF1_RX_FRAME_DATA4[2]	CEC_BUF1_RX_FRAME_DATA4[1]	CEC_BUF1_RX_FRAME_DATA4[0]
0x5A	0x00	CEC_REG_5A	r	CEC_BUF1_RX_FRAME_DATA5[7]	CEC_BUF1_RX_FRAME_DATA5[6]	CEC_BUF1_RX_FRAME_DATA5[5]	CEC_BUF1_RX_FRAME_DATA5[4]	CEC_BUF1_RX_FRAME_DATA5[3]	CEC_BUF1_RX_FRAME_DATA5[2]	CEC_BUF1_RX_FRAME_DATA5[1]	CEC_BUF1_RX_FRAME_DATA5[0]
0x5B	0x00	CEC_REG_5B	r	CEC_BUF1_RX_FRAME_DATA6[7]	CEC_BUF1_RX_FRAME_DATA6[6]	CEC_BUF1_RX_FRAME_DATA6[5]	CEC_BUF1_RX_FRAME_DATA6[4]	CEC_BUF1_RX_FRAME_DATA6[3]	CEC_BUF1_RX_FRAME_DATA6[2]	CEC_BUF1_RX_FRAME_DATA6[1]	CEC_BUF1_RX_FRAME_DATA6[0]
0x5C	0x00	CEC_REG_5C	r	CEC_BUF1_RX_FRAME_DATA7[7]	CEC_BUF1_RX_FRAME_DATA7[6]	CEC_BUF1_RX_FRAME_DATA7[5]	CEC_BUF1_RX_FRAME_DATA7[4]	CEC_BUF1_RX_FRAME_DATA7[3]	CEC_BUF1_RX_FRAME_DATA7[2]	CEC_BUF1_RX_FRAME_DATA7[1]	CEC_BUF1_RX_FRAME_DATA7[0]
0x5D	0x00	CEC_REG_5D	r	CEC_BUF1_RX_FRAME_DATA8[7]	CEC_BUF1_RX_FRAME_DATA8[6]	CEC_BUF1_RX_FRAME_DATA8[5]	CEC_BUF1_RX_FRAME_DATA8[4]	CEC_BUF1_RX_FRAME_DATA8[3]	CEC_BUF1_RX_FRAME_DATA8[2]	CEC_BUF1_RX_FRAME_DATA8[1]	CEC_BUF1_RX_FRAME_DATA8[0]
0x5E	0x00	CEC_REG_5E	r	CEC_BUF1_RX_FRAME_DATA9[7]	CEC_BUF1_RX_FRAME_DATA9[6]	CEC_BUF1_RX_FRAME_DATA9[5]	CEC_BUF1_RX_FRAME_DATA9[4]	CEC_BUF1_RX_FRAME_DATA9[3]	CEC_BUF1_RX_FRAME_DATA9[2]	CEC_BUF1_RX_FRAME_DATA9[1]	CEC_BUF1_RX_FRAME_DATA9[0]
0x5F	0x00	CEC_REG_5F	r	CEC_BUF1_RX_FRAME_DATA10[7]	CEC_BUF1_RX_FRAME_DATA10[6]	CEC_BUF1_RX_FRAME_DATA10[5]	CEC_BUF1_RX_FRAME_DATA10[4]	CEC_BUF1_RX_FRAME_DATA10[3]	CEC_BUF1_RX_FRAME_DATA10[2]	CEC_BUF1_RX_FRAME_DATA10[1]	CEC_BUF1_RX_FRAME_DATA10[0]
0x60	0x00	CEC_REG_60	r	CEC_BUF1_RX_FRAME_DATA11[7]	CEC_BUF1_RX_FRAME_DATA11[6]	CEC_BUF1_RX_FRAME_DATA11[5]	CEC_BUF1_RX_FRAME_DATA11[4]	CEC_BUF1_RX_FRAME_DATA11[3]	CEC_BUF1_RX_FRAME_DATA11[2]	CEC_BUF1_RX_FRAME_DATA11[1]	CEC_BUF1_RX_FRAME_DATA11[0]
0x61	0x00	CEC_REG_61	r	CEC_BUF1_RX_FRAME_DATA12[7]	CEC_BUF1_RX_FRAME_DATA12[6]	CEC_BUF1_RX_FRAME_DATA12[5]	CEC_BUF1_RX_FRAME_DATA12[4]	CEC_BUF1_RX_FRAME_DATA12[3]	CEC_BUF1_RX_FRAME_DATA12[2]	CEC_BUF1_RX_FRAME_DATA12[1]	CEC_BUF1_RX_FRAME_DATA12[0]
0x62	0x00	CEC_REG_62	r	CEC_BUF1_RX_FRAME_DATA13[7]	CEC_BUF1_RX_FRAME_DATA13[6]	CEC_BUF1_RX_FRAME_DATA13[5]	CEC_BUF1_RX_FRAME_DATA13[4]	CEC_BUF1_RX_FRAME_DATA13[3]	CEC_BUF1_RX_FRAME_DATA13[2]	CEC_BUF1_RX_FRAME_DATA13[1]	CEC_BUF1_RX_FRAME_DATA13[0]
0x63	0x00	CEC_REG_63	r	CEC_BUF1_RX_FRAME_DATA14[7]	CEC_BUF1_RX_FRAME_DATA14[6]	CEC_BUF1_RX_FRAME_DATA14[5]	CEC_BUF1_RX_FRAME_DATA14[4]	CEC_BUF1_RX_FRAME_DATA14[3]	CEC_BUF1_RX_FRAME_DATA14[2]	CEC_BUF1_RX_FRAME_DATA14[1]	CEC_BUF1_RX_FRAME_DATA14[0]
0x64	0x00	CEC_REG_64	r	-	-	-	CEC_BUF1_RX_FRAME_LENGTH[4]	CEC_BUF1_RX_FRAME_LENGTH[3]	CEC_BUF1_RX_FRAME_LENGTH[2]	CEC_BUF1_RX_FRAME_LENGTH[1]	CEC_BUF1_RX_FRAME_LENGTH[0]
0x65	0x00	CEC_REG_65	r	CEC_BUF2_RX_FRAME_HEADER[7]	CEC_BUF2_RX_FRAME_HEADER[6]	CEC_BUF2_RX_FRAME_HEADER[5]	CEC_BUF2_RX_FRAME_HEADER[4]	CEC_BUF2_RX_FRAME_HEADER[3]	CEC_BUF2_RX_FRAME_HEADER[2]	CEC_BUF2_RX_FRAME_HEADER[1]	CEC_BUF2_RX_FRAME_HEADER[0]
0x66	0x00	CEC_REG_66	r	CEC_BUF2_RX_FRAME_DATA0[7]	CEC_BUF2_RX_FRAME_DATA0[6]	CEC_BUF2_RX_FRAME_DATA0[5]	CEC_BUF2_RX_FRAME_DATA0[4]	CEC_BUF2_RX_FRAME_DATA0[3]	CEC_BUF2_RX_FRAME_DATA0[2]	CEC_BUF2_RX_FRAME_DATA0[1]	CEC_BUF2_RX_FRAME_DATA0[0]
0x67	0x00	CEC_REG_67	r	CEC_BUF2_RX_FRAME_DATA1[7]	CEC_BUF2_RX_FRAME_DATA1[6]	CEC_BUF2_RX_FRAME_DATA1[5]	CEC_BUF2_RX_FRAME_DATA1[4]	CEC_BUF2_RX_FRAME_DATA1[3]	CEC_BUF2_RX_FRAME_DATA1[2]	CEC_BUF2_RX_FRAME_DATA1[1]	CEC_BUF2_RX_FRAME_DATA1[0]
0x68	0x00	CEC_REG_68	r	CEC_BUF2_RX_FRAME_DATA2[7]	CEC_BUF2_RX_FRAME_DATA2[6]	CEC_BUF2_RX_FRAME_DATA2[5]	CEC_BUF2_RX_FRAME_DATA2[4]	CEC_BUF2_RX_FRAME_DATA2[3]	CEC_BUF2_RX_FRAME_DATA2[2]	CEC_BUF2_RX_FRAME_DATA2[1]	CEC_BUF2_RX_FRAME_DATA2[0]
0x69	0x00	CEC_REG_69	r	CEC_BUF2_RX_FRAME_DATA3[7]	CEC_BUF2_RX_FRAME_DATA3[6]	CEC_BUF2_RX_FRAME_DATA3[5]	CEC_BUF2_RX_FRAME_DATA3[4]	CEC_BUF2_RX_FRAME_DATA3[3]	CEC_BUF2_RX_FRAME_DATA3[2]	CEC_BUF2_RX_FRAME_DATA3[1]	CEC_BUF2_RX_FRAME_DATA3[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x6A	0x00	CEC_REG_6A	r	CEC_BUF2_RX_FRAME_DATA4[7]	CEC_BUF2_RX_FRAME_DATA4[6]	CEC_BUF2_RX_FRAME_DATA4[5]	CEC_BUF2_RX_FRAME_DATA4[4]	CEC_BUF2_RX_FRAME_DATA4[3]	CEC_BUF2_RX_FRAME_DATA4[2]	CEC_BUF2_RX_FRAME_DATA4[1]	CEC_BUF2_RX_FRAME_DATA4[0]
0x6B	0x00	CEC_REG_6B	r	CEC_BUF2_RX_FRAME_DATA5[7]	CEC_BUF2_RX_FRAME_DATA5[6]	CEC_BUF2_RX_FRAME_DATA5[5]	CEC_BUF2_RX_FRAME_DATA5[4]	CEC_BUF2_RX_FRAME_DATA5[3]	CEC_BUF2_RX_FRAME_DATA5[2]	CEC_BUF2_RX_FRAME_DATA5[1]	CEC_BUF2_RX_FRAME_DATA5[0]
0x6C	0x00	CEC_REG_6C	r	CEC_BUF2_RX_FRAME_DATA6[7]	CEC_BUF2_RX_FRAME_DATA6[6]	CEC_BUF2_RX_FRAME_DATA6[5]	CEC_BUF2_RX_FRAME_DATA6[4]	CEC_BUF2_RX_FRAME_DATA6[3]	CEC_BUF2_RX_FRAME_DATA6[2]	CEC_BUF2_RX_FRAME_DATA6[1]	CEC_BUF2_RX_FRAME_DATA6[0]
0x6D	0x00	CEC_REG_6D	r	CEC_BUF2_RX_FRAME_DATA7[7]	CEC_BUF2_RX_FRAME_DATA7[6]	CEC_BUF2_RX_FRAME_DATA7[5]	CEC_BUF2_RX_FRAME_DATA7[4]	CEC_BUF2_RX_FRAME_DATA7[3]	CEC_BUF2_RX_FRAME_DATA7[2]	CEC_BUF2_RX_FRAME_DATA7[1]	CEC_BUF2_RX_FRAME_DATA7[0]
0x6E	0x00	CEC_REG_6E	r	CEC_BUF2_RX_FRAME_DATA8[7]	CEC_BUF2_RX_FRAME_DATA8[6]	CEC_BUF2_RX_FRAME_DATA8[5]	CEC_BUF2_RX_FRAME_DATA8[4]	CEC_BUF2_RX_FRAME_DATA8[3]	CEC_BUF2_RX_FRAME_DATA8[2]	CEC_BUF2_RX_FRAME_DATA8[1]	CEC_BUF2_RX_FRAME_DATA8[0]
0x6F	0x00	CEC_REG_6F	r	CEC_BUF2_RX_FRAME_DATA9[7]	CEC_BUF2_RX_FRAME_DATA9[6]	CEC_BUF2_RX_FRAME_DATA9[5]	CEC_BUF2_RX_FRAME_DATA9[4]	CEC_BUF2_RX_FRAME_DATA9[3]	CEC_BUF2_RX_FRAME_DATA9[2]	CEC_BUF2_RX_FRAME_DATA9[1]	CEC_BUF2_RX_FRAME_DATA9[0]
0x70	0x00	CEC_REG_70	r	CEC_BUF2_RX_FRAME_DATA10[7]	CEC_BUF2_RX_FRAME_DATA10[6]	CEC_BUF2_RX_FRAME_DATA10[5]	CEC_BUF2_RX_FRAME_DATA10[4]	CEC_BUF2_RX_FRAME_DATA10[3]	CEC_BUF2_RX_FRAME_DATA10[2]	CEC_BUF2_RX_FRAME_DATA10[1]	CEC_BUF2_RX_FRAME_DATA10[0]
0x71	0x00	CEC_REG_71	r	CEC_BUF2_RX_FRAME_DATA11[7]	CEC_BUF2_RX_FRAME_DATA11[6]	CEC_BUF2_RX_FRAME_DATA11[5]	CEC_BUF2_RX_FRAME_DATA11[4]	CEC_BUF2_RX_FRAME_DATA11[3]	CEC_BUF2_RX_FRAME_DATA11[2]	CEC_BUF2_RX_FRAME_DATA11[1]	CEC_BUF2_RX_FRAME_DATA11[0]
0x72	0x00	CEC_REG_72	r	CEC_BUF2_RX_FRAME_DATA12[7]	CEC_BUF2_RX_FRAME_DATA12[6]	CEC_BUF2_RX_FRAME_DATA12[5]	CEC_BUF2_RX_FRAME_DATA12[4]	CEC_BUF2_RX_FRAME_DATA12[3]	CEC_BUF2_RX_FRAME_DATA12[2]	CEC_BUF2_RX_FRAME_DATA12[1]	CEC_BUF2_RX_FRAME_DATA12[0]
0x73	0x00	CEC_REG_73	r	CEC_BUF2_RX_FRAME_DATA13[7]	CEC_BUF2_RX_FRAME_DATA13[6]	CEC_BUF2_RX_FRAME_DATA13[5]	CEC_BUF2_RX_FRAME_DATA13[4]	CEC_BUF2_RX_FRAME_DATA13[3]	CEC_BUF2_RX_FRAME_DATA13[2]	CEC_BUF2_RX_FRAME_DATA13[1]	CEC_BUF2_RX_FRAME_DATA13[0]
0x74	0x00	CEC_REG_74	r	CEC_BUF2_RX_FRAME_DATA14[7]	CEC_BUF2_RX_FRAME_DATA14[6]	CEC_BUF2_RX_FRAME_DATA14[5]	CEC_BUF2_RX_FRAME_DATA14[4]	CEC_BUF2_RX_FRAME_DATA14[3]	CEC_BUF2_RX_FRAME_DATA14[2]	CEC_BUF2_RX_FRAME_DATA14[1]	CEC_BUF2_RX_FRAME_DATA14[0]
0x75	0x00	CEC_REG_75	r	-	-	-	CEC_BUF2_RX_FRAME_LENGTH[4]	CEC_BUF2_RX_FRAME_LENGTH[3]	CEC_BUF2_RX_FRAME_LENGTH[2]	CEC_BUF2_RX_FRAME_LENGTH[1]	CEC_BUF2_RX_FRAME_LENGTH[0]
0x76	0x00	CEC_REG_76	r	-	-	-	-	-	CEC_RX_RDY2	CEC_RX_RDY1	CEC_RX_RDY0
0x77	0x00	CEC_REG_77	rw	-	-	-	-	-	-	-	CEC_USE_ALL_BUFS
0x78	0x6D	CEC_REG_78	rw	CEC_WAKE_OPCODE0[7]	CEC_WAKE_OPCODE0[6]	CEC_WAKE_OPCODE0[5]	CEC_WAKE_OPCODE0[4]	CEC_WAKE_OPCODE0[3]	CEC_WAKE_OPCODE0[2]	CEC_WAKE_OPCODE0[1]	CEC_WAKE_OPCODE0[0]
0x79	0x8F	CEC_REG_79	rw	CEC_WAKE_OPCODE1[7]	CEC_WAKE_OPCODE1[6]	CEC_WAKE_OPCODE1[5]	CEC_WAKE_OPCODE1[4]	CEC_WAKE_OPCODE1[3]	CEC_WAKE_OPCODE1[2]	CEC_WAKE_OPCODE1[1]	CEC_WAKE_OPCODE1[0]
0x7A	0x82	CEC_REG_7A	rw	CEC_WAKE_OPCODE2[7]	CEC_WAKE_OPCODE2[6]	CEC_WAKE_OPCODE2[5]	CEC_WAKE_OPCODE2[4]	CEC_WAKE_OPCODE2[3]	CEC_WAKE_OPCODE2[2]	CEC_WAKE_OPCODE2[1]	CEC_WAKE_OPCODE2[0]
0x7B	0x04	CEC_REG_7B	rw	CEC_WAKE_OPCODE3[7]	CEC_WAKE_OPCODE3[6]	CEC_WAKE_OPCODE3[5]	CEC_WAKE_OPCODE3[4]	CEC_WAKE_OPCODE3[3]	CEC_WAKE_OPCODE3[2]	CEC_WAKE_OPCODE3[1]	CEC_WAKE_OPCODE3[0]
0x7C	0x0D	CEC_REG_7C	rw	CEC_WAKE_OPCODE4[7]	CEC_WAKE_OPCODE4[6]	CEC_WAKE_OPCODE4[5]	CEC_WAKE_OPCODE4[4]	CEC_WAKE_OPCODE4[3]	CEC_WAKE_OPCODE4[2]	CEC_WAKE_OPCODE4[1]	CEC_WAKE_OPCODE4[0]
0x7D	0x70	CEC_REG_7D	rw	CEC_WAKE_OPCODE5[7]	CEC_WAKE_OPCODE5[6]	CEC_WAKE_OPCODE5[5]	CEC_WAKE_OPCODE5[4]	CEC_WAKE_OPCODE5[3]	CEC_WAKE_OPCODE5[2]	CEC_WAKE_OPCODE5[1]	CEC_WAKE_OPCODE5[0]
0x7E	0x42	CEC_REG_7E	rw	CEC_WAKE_OPCODE6[7]	CEC_WAKE_OPCODE6[6]	CEC_WAKE_OPCODE6[5]	CEC_WAKE_OPCODE6[4]	CEC_WAKE_OPCODE6[3]	CEC_WAKE_OPCODE6[2]	CEC_WAKE_OPCODE6[1]	CEC_WAKE_OPCODE6[0]
0x7F	0x41	CEC_REG_7F	rw	CEC_WAKE_OPCODE7[7]	CEC_WAKE_OPCODE7[6]	CEC_WAKE_OPCODE7[5]	CEC_WAKE_OPCODE7[4]	CEC_WAKE_OPCODE7[3]	CEC_WAKE_OPCODE7[2]	CEC_WAKE_OPCODE7[1]	CEC_WAKE_OPCODE7[0]

1.6 TXA MAIN MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x41	0x50	MAIN_REG_41	rw	-	SYSTEM_PD	-	-	-	-	-	-
0x92	0x00	MAIN_REG_92	rw	CEC_CMD_INTR_MASK[7]	CEC_CMD_INTR_MASK[6]	CEC_CMD_INTR_MASK[5]	CEC_CMD_INTR_MASK[4]	CEC_CMD_INTR_MASK[3]	CEC_CMD_INTR_MASK[2]	CEC_CMD_INTR_MASK[1]	CEC_CMD_INTR_MASK[0]
0x93	0x00	MAIN_REG_93	rw	CEC_CMD_INTR[7]	CEC_CMD_INTR[6]	CEC_CMD_INTR[5]	CEC_CMD_INTR[4]	CEC_CMD_INTR[3]	CEC_CMD_INTR[2]	CEC_CMD_INTR[1]	CEC_CMD_INTR[0]
0x94	0xC0	MAIN_REG_94	rw	HPD_INTR_MASK	MSEN_INTR_MASK	VS_INTR_MASK	-	-	EDID_RDY_INTR_MASK	HDCP_CONTROLLER_STATE_4_INTR_MASK	RI_RDY_INTR_MASK
0x95	0x00	MAIN_REG_95	rw	HDCP_ERROR_INTR_MASK	BKSV_FLAG_INTR_MASK	TX_READY_INTR_MASK	TX_ARBITRATION_LOST_INTR_MASK	TX_RETRY_TIMEOUT_INTR_MASK	RX_READY_INTR_MASK[2]	RX_READY_INTR_MASK[1]	RX_READY_INTR_MASK[0]
0x96	0x00	MAIN_REG_96	rw	HPD_ST	MSEN_ST	VSYNC_ST	-	-	EDID_RDY_ST	HDCP_AUTH_ST	RI_RDY_ST
0x97	0x00	MAIN_REG_97	rw	HDCP_ERROR_ST	BKSV_FLAG_ST	TX_READY_INTR	TX_ARBITRATION_LOST_INTR	TX_RETRY_TIMEOUT_INTR	RX_READY_INTR[2]	RX_READY_INTR[1]	RX_READY_INTR[0]
0x98	0x00	MAIN_REG_98	rw	-	-	-	CEC_PD	-	-	-	-
0x9E	0x00	MAIN_REG_9E	rw	HIGH_VSYNC[1]	HIGH_VSYNC[0]	-	-	-	-	-	-
0x9F	0x00	MAIN_REG_9F	rw	-	-	HPD_DISABLE[1]	HPD_DISABLE[0]	-	-	-	-
0xAB	0x00	MAIN_REG_AB	rw	-	-	HDCP_START_DELAY[2]	HDCP_START_DELAY[1]	HDCP_START_DELAY[0]	-	-	-
0xAC	0x00	MAIN_REG_AC	rw	RI_FREQ_SEL[1]	RI_FREQ_SEL[0]	RI_DELAY_SEL[2]	RI_DELAY_SEL[1]	RI_DELAY_SEL[0]	BCAPS_DELAY[2]	BCAPS_DELAY[1]	BCAPS_DELAY[0]
0xAD	0x00	MAIN_REG_AD	rw	AN_DELAY[2]	AN_DELAY[1]	AN_DELAY[0]	AKSV_DELAY[2]	AKSV_DELAY[1]	AKSV_DELAY[0]	-	-
0xAE	0x00	MAIN_REG_AE	rw	SKIP_RI_128	HDCP_1P1_DIS	R0_WAIT_TIME[1]	R0_WAIT_TIME[0]	HDCP_REPEATER_TIMEOUT[1]	HDCP_REPEATER_TIMEOUT[0]	-	-
0xAF	0x14	MAIN_REG_AF	rw	HDCP_DESIRED	-	-	FRAME_ENC	-	TX_HDMI_MODE	EXT_HDMI_MODE	-
0xB8	0x00	MAIN_REG_B8	r	-	ENC_ON	-	KEYS_READ_ERROR	-	-	-	-
0xBE	0x00	MAIN_REG_BE	r	BCAPS[7]	BCAPS[6]	BCAPS[5]	BCAPS[4]	BCAPS[3]	BCAPS[2]	BCAPS[1]	BCAPS[0]
0xBF	0x00	MAIN_REG_BF	r	BKSV0[7]	BKSV0[6]	BKSV0[5]	BKSV0[4]	BKSV0[3]	BKSV0[2]	BKSV0[1]	BKSV0[0]
0xC0	0x00	MAIN_REG_C0	r	BKSV1[7]	BKSV1[6]	BKSV1[5]	BKSV1[4]	BKSV1[3]	BKSV1[2]	BKSV1[1]	BKSV1[0]
0xC1	0x00	MAIN_REG_C1	r	BKSV2[7]	BKSV2[6]	BKSV2[5]	BKSV2[4]	BKSV2[3]	BKSV2[2]	BKSV2[1]	BKSV2[0]
0xC2	0x00	MAIN_REG_C2	r	BKSV3[7]	BKSV3[6]	BKSV3[5]	BKSV3[4]	BKSV3[3]	BKSV3[2]	BKSV3[1]	BKSV3[0]
0xC3	0x00	MAIN_REG_C3	r	BKSV4[7]	BKSV4[6]	BKSV4[5]	BKSV4[4]	BKSV4[3]	BKSV4[2]	BKSV4[1]	BKSV4[0]
0xC4	0x00	MAIN_REG_C4	rw	EDID_SEGMENT[7]	EDID_SEGMENT[6]	EDID_SEGMENT[5]	EDID_SEGMENT[4]	EDID_SEGMENT[3]	EDID_SEGMENT[2]	EDID_SEGMENT[1]	EDID_SEGMENT[0]
0xC5	0x00	MAIN_REG_C5	rw	ERROR_FLAG	AN_STOP	HDCP_ENABLED	EDID_READY_FLAG	I2C_INTERRUPT	RI_FLAG	BKSV_UPDATE_FLAG	PJ_FLAG
0xC6	0x00	MAIN_REG_C6	r	-	-	-	HDMI_MODE	HDCP_REQUESTED	RX_SENSE	EEPROM_READ_OK	TMDSOUTPUTPWRDN
0xC7	0x00	MAIN_REG_C7	rw	BKSV_FLAG	BKSV_COUNT[6]	BKSV_COUNT[5]	BKSV_COUNT[4]	BKSV_COUNT[3]	BKSV_COUNT[2]	BKSV_COUNT[1]	BKSV_COUNT[0]
0xC8	0x00	MAIN_REG_C8	r	HDCP_CONTROLLER_ERROR[3]	HDCP_CONTROLLER_ERROR[2]	HDCP_CONTROLLER_ERROR[1]	HDCP_CONTROLLER_ERROR[0]	HDCP_CONTROLLER_STATE[3]	HDCP_CONTROLLER_STATE[2]	HDCP_CONTROLLER_STATE[1]	HDCP_CONTROLLER_STATE[0]
0xC9	0x03	MAIN_REG_C9	rw	-	-	-	EDID_READ_EN	EDID_TRIES[3]	EDID_TRIES[2]	EDID_TRIES[1]	EDID_TRIES[0]
0xE4	0x00	MAIN_REG_E4	r	PLL_LOCK_STATUS	-	-	-	-	-	-	-
0xEA	0x84	MAIN_REG_EA	rw	-	-	-	-	-	-	TMDS_CLK_INV_I2C	ENABLE_XXI_CLK_I2C

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xEB	0xFC	MAIN_REG_EB	rw	TRANSDRVENABLE_I2C[2]	TRANSDRVENABLE_I2C[1]	TRANSDRVENABLE_I2C[0]	-	-	-	-	-
0xFE	0x00	MAIN_REG_FE	rw	-	-	-	-	-	-	-	CHANNEL_SWAP

1.7 TXA EDID MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00	EDIDMEMORY_REG_00	r	EDID_0[7]	EDID_0[6]	EDID_0[5]	EDID_0[4]	EDID_0[3]	EDID_0[2]	EDID_0[1]	EDID_0[0]
0x01	0x00	EDIDMEMORY_REG_01	r	EDID_1[7]	EDID_1[6]	EDID_1[5]	EDID_1[4]	EDID_1[3]	EDID_1[2]	EDID_1[1]	EDID_1[0]
0x02	0x00	EDIDMEMORY_REG_02	r	EDID_2[7]	EDID_2[6]	EDID_2[5]	EDID_2[4]	EDID_2[3]	EDID_2[2]	EDID_2[1]	EDID_2[0]
0x03	0x00	EDIDMEMORY_REG_03	r	EDID_3[7]	EDID_3[6]	EDID_3[5]	EDID_3[4]	EDID_3[3]	EDID_3[2]	EDID_3[1]	EDID_3[0]
0x04	0x00	EDIDMEMORY_REG_04	r	EDID_4[7]	EDID_4[6]	EDID_4[5]	EDID_4[4]	EDID_4[3]	EDID_4[2]	EDID_4[1]	EDID_4[0]
0x05	0x00	EDIDMEMORY_REG_05	r	EDID_5[7]	EDID_5[6]	EDID_5[5]	EDID_5[4]	EDID_5[3]	EDID_5[2]	EDID_5[1]	EDID_5[0]
0x06	0x00	EDIDMEMORY_REG_06	r	EDID_6[7]	EDID_6[6]	EDID_6[5]	EDID_6[4]	EDID_6[3]	EDID_6[2]	EDID_6[1]	EDID_6[0]
0x07	0x00	EDIDMEMORY_REG_07	r	EDID_7[7]	EDID_7[6]	EDID_7[5]	EDID_7[4]	EDID_7[3]	EDID_7[2]	EDID_7[1]	EDID_7[0]
0x08	0x00	EDIDMEMORY_REG_08	r	EDID_8[7]	EDID_8[6]	EDID_8[5]	EDID_8[4]	EDID_8[3]	EDID_8[2]	EDID_8[1]	EDID_8[0]
0x09	0x00	EDIDMEMORY_REG_09	r	EDID_9[7]	EDID_9[6]	EDID_9[5]	EDID_9[4]	EDID_9[3]	EDID_9[2]	EDID_9[1]	EDID_9[0]
0x0A	0x00	EDIDMEMORY_REG_0A	r	EDID_10[7]	EDID_10[6]	EDID_10[5]	EDID_10[4]	EDID_10[3]	EDID_10[2]	EDID_10[1]	EDID_10[0]
0x0B	0x00	EDIDMEMORY_REG_0B	r	EDID_11[7]	EDID_11[6]	EDID_11[5]	EDID_11[4]	EDID_11[3]	EDID_11[2]	EDID_11[1]	EDID_11[0]
0x0C	0x00	EDIDMEMORY_REG_0C	r	EDID_12[7]	EDID_12[6]	EDID_12[5]	EDID_12[4]	EDID_12[3]	EDID_12[2]	EDID_12[1]	EDID_12[0]
0x0D	0x00	EDIDMEMORY_REG_0D	r	EDID_13[7]	EDID_13[6]	EDID_13[5]	EDID_13[4]	EDID_13[3]	EDID_13[2]	EDID_13[1]	EDID_13[0]
0x0E	0x00	EDIDMEMORY_REG_0E	r	EDID_14[7]	EDID_14[6]	EDID_14[5]	EDID_14[4]	EDID_14[3]	EDID_14[2]	EDID_14[1]	EDID_14[0]
0x0F	0x00	EDIDMEMORY_REG_0F	r	EDID_15[7]	EDID_15[6]	EDID_15[5]	EDID_15[4]	EDID_15[3]	EDID_15[2]	EDID_15[1]	EDID_15[0]
0x10	0x00	EDIDMEMORY_REG_10	r	EDID_16[7]	EDID_16[6]	EDID_16[5]	EDID_16[4]	EDID_16[3]	EDID_16[2]	EDID_16[1]	EDID_16[0]
0x11	0x00	EDIDMEMORY_REG_11	r	EDID_17[7]	EDID_17[6]	EDID_17[5]	EDID_17[4]	EDID_17[3]	EDID_17[2]	EDID_17[1]	EDID_17[0]
0x12	0x00	EDIDMEMORY_REG_12	r	EDID_18[7]	EDID_18[6]	EDID_18[5]	EDID_18[4]	EDID_18[3]	EDID_18[2]	EDID_18[1]	EDID_18[0]
0x13	0x00	EDIDMEMORY_REG_13	r	EDID_19[7]	EDID_19[6]	EDID_19[5]	EDID_19[4]	EDID_19[3]	EDID_19[2]	EDID_19[1]	EDID_19[0]
0x14	0x00	EDIDMEMORY_REG_14	r	EDID_20[7]	EDID_20[6]	EDID_20[5]	EDID_20[4]	EDID_20[3]	EDID_20[2]	EDID_20[1]	EDID_20[0]
0x15	0x00	EDIDMEMORY_REG_15	r	EDID_21[7]	EDID_21[6]	EDID_21[5]	EDID_21[4]	EDID_21[3]	EDID_21[2]	EDID_21[1]	EDID_21[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x16	0x00	EDIDMEMORY_REG_16	r	EDID_22[7]	EDID_22[6]	EDID_22[5]	EDID_22[4]	EDID_22[3]	EDID_22[2]	EDID_22[1]	EDID_22[0]
0x17	0x00	EDIDMEMORY_REG_17	r	EDID_23[7]	EDID_23[6]	EDID_23[5]	EDID_23[4]	EDID_23[3]	EDID_23[2]	EDID_23[1]	EDID_23[0]
0x18	0x00	EDIDMEMORY_REG_18	r	EDID_24[7]	EDID_24[6]	EDID_24[5]	EDID_24[4]	EDID_24[3]	EDID_24[2]	EDID_24[1]	EDID_24[0]
0x19	0x00	EDIDMEMORY_REG_19	r	EDID_25[7]	EDID_25[6]	EDID_25[5]	EDID_25[4]	EDID_25[3]	EDID_25[2]	EDID_25[1]	EDID_25[0]
0x1A	0x00	EDIDMEMORY_REG_1A	r	EDID_26[7]	EDID_26[6]	EDID_26[5]	EDID_26[4]	EDID_26[3]	EDID_26[2]	EDID_26[1]	EDID_26[0]
0x1B	0x00	EDIDMEMORY_REG_1B	r	EDID_27[7]	EDID_27[6]	EDID_27[5]	EDID_27[4]	EDID_27[3]	EDID_27[2]	EDID_27[1]	EDID_27[0]
0x1C	0x00	EDIDMEMORY_REG_1C	r	EDID_28[7]	EDID_28[6]	EDID_28[5]	EDID_28[4]	EDID_28[3]	EDID_28[2]	EDID_28[1]	EDID_28[0]
0x1D	0x00	EDIDMEMORY_REG_1D	r	EDID_29[7]	EDID_29[6]	EDID_29[5]	EDID_29[4]	EDID_29[3]	EDID_29[2]	EDID_29[1]	EDID_29[0]
0x1E	0x00	EDIDMEMORY_REG_1E	r	EDID_30[7]	EDID_30[6]	EDID_30[5]	EDID_30[4]	EDID_30[3]	EDID_30[2]	EDID_30[1]	EDID_30[0]
0x1F	0x00	EDIDMEMORY_REG_1F	r	EDID_31[7]	EDID_31[6]	EDID_31[5]	EDID_31[4]	EDID_31[3]	EDID_31[2]	EDID_31[1]	EDID_31[0]
0x20	0x00	EDIDMEMORY_REG_20	r	EDID_32[7]	EDID_32[6]	EDID_32[5]	EDID_32[4]	EDID_32[3]	EDID_32[2]	EDID_32[1]	EDID_32[0]
0x21	0x00	EDIDMEMORY_REG_21	r	EDID_33[7]	EDID_33[6]	EDID_33[5]	EDID_33[4]	EDID_33[3]	EDID_33[2]	EDID_33[1]	EDID_33[0]
0x22	0x00	EDIDMEMORY_REG_22	r	EDID_34[7]	EDID_34[6]	EDID_34[5]	EDID_34[4]	EDID_34[3]	EDID_34[2]	EDID_34[1]	EDID_34[0]
0x23	0x00	EDIDMEMORY_REG_23	r	EDID_35[7]	EDID_35[6]	EDID_35[5]	EDID_35[4]	EDID_35[3]	EDID_35[2]	EDID_35[1]	EDID_35[0]
0x24	0x00	EDIDMEMORY_REG_24	r	EDID_36[7]	EDID_36[6]	EDID_36[5]	EDID_36[4]	EDID_36[3]	EDID_36[2]	EDID_36[1]	EDID_36[0]
0x25	0x00	EDIDMEMORY_REG_25	r	EDID_37[7]	EDID_37[6]	EDID_37[5]	EDID_37[4]	EDID_37[3]	EDID_37[2]	EDID_37[1]	EDID_37[0]
0x26	0x00	EDIDMEMORY_REG_26	r	EDID_38[7]	EDID_38[6]	EDID_38[5]	EDID_38[4]	EDID_38[3]	EDID_38[2]	EDID_38[1]	EDID_38[0]
0x27	0x00	EDIDMEMORY_REG_27	r	EDID_39[7]	EDID_39[6]	EDID_39[5]	EDID_39[4]	EDID_39[3]	EDID_39[2]	EDID_39[1]	EDID_39[0]
0x28	0x00	EDIDMEMORY_REG_28	r	EDID_40[7]	EDID_40[6]	EDID_40[5]	EDID_40[4]	EDID_40[3]	EDID_40[2]	EDID_40[1]	EDID_40[0]
0x29	0x00	EDIDMEMORY_REG_29	r	EDID_41[7]	EDID_41[6]	EDID_41[5]	EDID_41[4]	EDID_41[3]	EDID_41[2]	EDID_41[1]	EDID_41[0]
0x2A	0x00	EDIDMEMORY_REG_2A	r	EDID_42[7]	EDID_42[6]	EDID_42[5]	EDID_42[4]	EDID_42[3]	EDID_42[2]	EDID_42[1]	EDID_42[0]
0x2B	0x00	EDIDMEMORY_REG_2B	r	EDID_43[7]	EDID_43[6]	EDID_43[5]	EDID_43[4]	EDID_43[3]	EDID_43[2]	EDID_43[1]	EDID_43[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x2C	0x00	EDIDMEMORY_REG_2C	r	EDID_44[7]	EDID_44[6]	EDID_44[5]	EDID_44[4]	EDID_44[3]	EDID_44[2]	EDID_44[1]	EDID_44[0]
0x2D	0x00	EDIDMEMORY_REG_2D	r	EDID_45[7]	EDID_45[6]	EDID_45[5]	EDID_45[4]	EDID_45[3]	EDID_45[2]	EDID_45[1]	EDID_45[0]
0x2E	0x00	EDIDMEMORY_REG_2E	r	EDID_46[7]	EDID_46[6]	EDID_46[5]	EDID_46[4]	EDID_46[3]	EDID_46[2]	EDID_46[1]	EDID_46[0]
0x2F	0x00	EDIDMEMORY_REG_2F	r	EDID_47[7]	EDID_47[6]	EDID_47[5]	EDID_47[4]	EDID_47[3]	EDID_47[2]	EDID_47[1]	EDID_47[0]
0x30	0x00	EDIDMEMORY_REG_30	r	EDID_48[7]	EDID_48[6]	EDID_48[5]	EDID_48[4]	EDID_48[3]	EDID_48[2]	EDID_48[1]	EDID_48[0]
0x31	0x00	EDIDMEMORY_REG_31	r	EDID_49[7]	EDID_49[6]	EDID_49[5]	EDID_49[4]	EDID_49[3]	EDID_49[2]	EDID_49[1]	EDID_49[0]
0x32	0x00	EDIDMEMORY_REG_32	r	EDID_50[7]	EDID_50[6]	EDID_50[5]	EDID_50[4]	EDID_50[3]	EDID_50[2]	EDID_50[1]	EDID_50[0]
0x33	0x00	EDIDMEMORY_REG_33	r	EDID_51[7]	EDID_51[6]	EDID_51[5]	EDID_51[4]	EDID_51[3]	EDID_51[2]	EDID_51[1]	EDID_51[0]
0x34	0x00	EDIDMEMORY_REG_34	r	EDID_52[7]	EDID_52[6]	EDID_52[5]	EDID_52[4]	EDID_52[3]	EDID_52[2]	EDID_52[1]	EDID_52[0]
0x35	0x00	EDIDMEMORY_REG_35	r	EDID_53[7]	EDID_53[6]	EDID_53[5]	EDID_53[4]	EDID_53[3]	EDID_53[2]	EDID_53[1]	EDID_53[0]
0x36	0x00	EDIDMEMORY_REG_36	r	EDID_54[7]	EDID_54[6]	EDID_54[5]	EDID_54[4]	EDID_54[3]	EDID_54[2]	EDID_54[1]	EDID_54[0]
0x37	0x00	EDIDMEMORY_REG_37	r	EDID_55[7]	EDID_55[6]	EDID_55[5]	EDID_55[4]	EDID_55[3]	EDID_55[2]	EDID_55[1]	EDID_55[0]
0x38	0x00	EDIDMEMORY_REG_38	r	EDID_56[7]	EDID_56[6]	EDID_56[5]	EDID_56[4]	EDID_56[3]	EDID_56[2]	EDID_56[1]	EDID_56[0]
0x39	0x00	EDIDMEMORY_REG_39	r	EDID_57[7]	EDID_57[6]	EDID_57[5]	EDID_57[4]	EDID_57[3]	EDID_57[2]	EDID_57[1]	EDID_57[0]
0x3A	0x00	EDIDMEMORY_REG_3A	r	EDID_58[7]	EDID_58[6]	EDID_58[5]	EDID_58[4]	EDID_58[3]	EDID_58[2]	EDID_58[1]	EDID_58[0]
0x3B	0x00	EDIDMEMORY_REG_3B	r	EDID_59[7]	EDID_59[6]	EDID_59[5]	EDID_59[4]	EDID_59[3]	EDID_59[2]	EDID_59[1]	EDID_59[0]
0x3C	0x00	EDIDMEMORY_REG_3C	r	EDID_60[7]	EDID_60[6]	EDID_60[5]	EDID_60[4]	EDID_60[3]	EDID_60[2]	EDID_60[1]	EDID_60[0]
0x3D	0x00	EDIDMEMORY_REG_3D	r	EDID_61[7]	EDID_61[6]	EDID_61[5]	EDID_61[4]	EDID_61[3]	EDID_61[2]	EDID_61[1]	EDID_61[0]
0x3E	0x00	EDIDMEMORY_REG_3E	r	EDID_62[7]	EDID_62[6]	EDID_62[5]	EDID_62[4]	EDID_62[3]	EDID_62[2]	EDID_62[1]	EDID_62[0]
0x3F	0x00	EDIDMEMORY_REG_3F	r	EDID_63[7]	EDID_63[6]	EDID_63[5]	EDID_63[4]	EDID_63[3]	EDID_63[2]	EDID_63[1]	EDID_63[0]
0x40	0x00	EDIDMEMORY_REG_40	r	EDID_64[7]	EDID_64[6]	EDID_64[5]	EDID_64[4]	EDID_64[3]	EDID_64[2]	EDID_64[1]	EDID_64[0]
0x41	0x00	EDIDMEMORY_REG_41	r	EDID_65[7]	EDID_65[6]	EDID_65[5]	EDID_65[4]	EDID_65[3]	EDID_65[2]	EDID_65[1]	EDID_65[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x42	0x00	EDIDMEMORY_REG_42	r	EDID_66[7]	EDID_66[6]	EDID_66[5]	EDID_66[4]	EDID_66[3]	EDID_66[2]	EDID_66[1]	EDID_66[0]
0x43	0x00	EDIDMEMORY_REG_43	r	EDID_67[7]	EDID_67[6]	EDID_67[5]	EDID_67[4]	EDID_67[3]	EDID_67[2]	EDID_67[1]	EDID_67[0]
0x44	0x00	EDIDMEMORY_REG_44	r	EDID_68[7]	EDID_68[6]	EDID_68[5]	EDID_68[4]	EDID_68[3]	EDID_68[2]	EDID_68[1]	EDID_68[0]
0x45	0x00	EDIDMEMORY_REG_45	r	EDID_69[7]	EDID_69[6]	EDID_69[5]	EDID_69[4]	EDID_69[3]	EDID_69[2]	EDID_69[1]	EDID_69[0]
0x46	0x00	EDIDMEMORY_REG_46	r	EDID_70[7]	EDID_70[6]	EDID_70[5]	EDID_70[4]	EDID_70[3]	EDID_70[2]	EDID_70[1]	EDID_70[0]
0x47	0x00	EDIDMEMORY_REG_47	r	EDID_71[7]	EDID_71[6]	EDID_71[5]	EDID_71[4]	EDID_71[3]	EDID_71[2]	EDID_71[1]	EDID_71[0]
0x48	0x00	EDIDMEMORY_REG_48	r	EDID_72[7]	EDID_72[6]	EDID_72[5]	EDID_72[4]	EDID_72[3]	EDID_72[2]	EDID_72[1]	EDID_72[0]
0x49	0x00	EDIDMEMORY_REG_49	r	EDID_73[7]	EDID_73[6]	EDID_73[5]	EDID_73[4]	EDID_73[3]	EDID_73[2]	EDID_73[1]	EDID_73[0]
0x4A	0x00	EDIDMEMORY_REG_4A	r	EDID_74[7]	EDID_74[6]	EDID_74[5]	EDID_74[4]	EDID_74[3]	EDID_74[2]	EDID_74[1]	EDID_74[0]
0x4B	0x00	EDIDMEMORY_REG_4B	r	EDID_75[7]	EDID_75[6]	EDID_75[5]	EDID_75[4]	EDID_75[3]	EDID_75[2]	EDID_75[1]	EDID_75[0]
0x4C	0x00	EDIDMEMORY_REG_4C	r	EDID_76[7]	EDID_76[6]	EDID_76[5]	EDID_76[4]	EDID_76[3]	EDID_76[2]	EDID_76[1]	EDID_76[0]
0x4D	0x00	EDIDMEMORY_REG_4D	r	EDID_77[7]	EDID_77[6]	EDID_77[5]	EDID_77[4]	EDID_77[3]	EDID_77[2]	EDID_77[1]	EDID_77[0]
0x4E	0x00	EDIDMEMORY_REG_4E	r	EDID_78[7]	EDID_78[6]	EDID_78[5]	EDID_78[4]	EDID_78[3]	EDID_78[2]	EDID_78[1]	EDID_78[0]
0x4F	0x00	EDIDMEMORY_REG_4F	r	EDID_79[7]	EDID_79[6]	EDID_79[5]	EDID_79[4]	EDID_79[3]	EDID_79[2]	EDID_79[1]	EDID_79[0]
0x50	0x00	EDIDMEMORY_REG_50	r	EDID_80[7]	EDID_80[6]	EDID_80[5]	EDID_80[4]	EDID_80[3]	EDID_80[2]	EDID_80[1]	EDID_80[0]
0x51	0x00	EDIDMEMORY_REG_51	r	EDID_81[7]	EDID_81[6]	EDID_81[5]	EDID_81[4]	EDID_81[3]	EDID_81[2]	EDID_81[1]	EDID_81[0]
0x52	0x00	EDIDMEMORY_REG_52	r	EDID_82[7]	EDID_82[6]	EDID_82[5]	EDID_82[4]	EDID_82[3]	EDID_82[2]	EDID_82[1]	EDID_82[0]
0x53	0x00	EDIDMEMORY_REG_53	r	EDID_83[7]	EDID_83[6]	EDID_83[5]	EDID_83[4]	EDID_83[3]	EDID_83[2]	EDID_83[1]	EDID_83[0]
0x54	0x00	EDIDMEMORY_REG_54	r	EDID_84[7]	EDID_84[6]	EDID_84[5]	EDID_84[4]	EDID_84[3]	EDID_84[2]	EDID_84[1]	EDID_84[0]
0x55	0x00	EDIDMEMORY_REG_55	r	EDID_85[7]	EDID_85[6]	EDID_85[5]	EDID_85[4]	EDID_85[3]	EDID_85[2]	EDID_85[1]	EDID_85[0]
0x56	0x00	EDIDMEMORY_REG_56	r	EDID_86[7]	EDID_86[6]	EDID_86[5]	EDID_86[4]	EDID_86[3]	EDID_86[2]	EDID_86[1]	EDID_86[0]
0x57	0x00	EDIDMEMORY_REG_57	r	EDID_87[7]	EDID_87[6]	EDID_87[5]	EDID_87[4]	EDID_87[3]	EDID_87[2]	EDID_87[1]	EDID_87[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x58	0x00	EDIDMEMORY_REG_58	r	EDID_88[7]	EDID_88[6]	EDID_88[5]	EDID_88[4]	EDID_88[3]	EDID_88[2]	EDID_88[1]	EDID_88[0]
0x59	0x00	EDIDMEMORY_REG_59	r	EDID_89[7]	EDID_89[6]	EDID_89[5]	EDID_89[4]	EDID_89[3]	EDID_89[2]	EDID_89[1]	EDID_89[0]
0x5A	0x00	EDIDMEMORY_REG_5A	r	EDID_90[7]	EDID_90[6]	EDID_90[5]	EDID_90[4]	EDID_90[3]	EDID_90[2]	EDID_90[1]	EDID_90[0]
0x5B	0x00	EDIDMEMORY_REG_5B	r	EDID_91[7]	EDID_91[6]	EDID_91[5]	EDID_91[4]	EDID_91[3]	EDID_91[2]	EDID_91[1]	EDID_91[0]
0x5C	0x00	EDIDMEMORY_REG_5C	r	EDID_92[7]	EDID_92[6]	EDID_92[5]	EDID_92[4]	EDID_92[3]	EDID_92[2]	EDID_92[1]	EDID_92[0]
0x5D	0x00	EDIDMEMORY_REG_5D	r	EDID_93[7]	EDID_93[6]	EDID_93[5]	EDID_93[4]	EDID_93[3]	EDID_93[2]	EDID_93[1]	EDID_93[0]
0x5E	0x00	EDIDMEMORY_REG_5E	r	EDID_94[7]	EDID_94[6]	EDID_94[5]	EDID_94[4]	EDID_94[3]	EDID_94[2]	EDID_94[1]	EDID_94[0]
0x5F	0x00	EDIDMEMORY_REG_5F	r	EDID_95[7]	EDID_95[6]	EDID_95[5]	EDID_95[4]	EDID_95[3]	EDID_95[2]	EDID_95[1]	EDID_95[0]
0x60	0x00	EDIDMEMORY_REG_60	r	EDID_96[7]	EDID_96[6]	EDID_96[5]	EDID_96[4]	EDID_96[3]	EDID_96[2]	EDID_96[1]	EDID_96[0]
0x61	0x00	EDIDMEMORY_REG_61	r	EDID_97[7]	EDID_97[6]	EDID_97[5]	EDID_97[4]	EDID_97[3]	EDID_97[2]	EDID_97[1]	EDID_97[0]
0x62	0x00	EDIDMEMORY_REG_62	r	EDID_98[7]	EDID_98[6]	EDID_98[5]	EDID_98[4]	EDID_98[3]	EDID_98[2]	EDID_98[1]	EDID_98[0]
0x63	0x00	EDIDMEMORY_REG_63	r	EDID_99[7]	EDID_99[6]	EDID_99[5]	EDID_99[4]	EDID_99[3]	EDID_99[2]	EDID_99[1]	EDID_99[0]
0x64	0x00	EDIDMEMORY_REG_64	r	EDID_100[7]	EDID_100[6]	EDID_100[5]	EDID_100[4]	EDID_100[3]	EDID_100[2]	EDID_100[1]	EDID_100[0]
0x65	0x00	EDIDMEMORY_REG_65	r	EDID_101[7]	EDID_101[6]	EDID_101[5]	EDID_101[4]	EDID_101[3]	EDID_101[2]	EDID_101[1]	EDID_101[0]
0x66	0x00	EDIDMEMORY_REG_66	r	EDID_102[7]	EDID_102[6]	EDID_102[5]	EDID_102[4]	EDID_102[3]	EDID_102[2]	EDID_102[1]	EDID_102[0]
0x67	0x00	EDIDMEMORY_REG_67	r	EDID_103[7]	EDID_103[6]	EDID_103[5]	EDID_103[4]	EDID_103[3]	EDID_103[2]	EDID_103[1]	EDID_103[0]
0x68	0x00	EDIDMEMORY_REG_68	r	EDID_104[7]	EDID_104[6]	EDID_104[5]	EDID_104[4]	EDID_104[3]	EDID_104[2]	EDID_104[1]	EDID_104[0]
0x69	0x00	EDIDMEMORY_REG_69	r	EDID_105[7]	EDID_105[6]	EDID_105[5]	EDID_105[4]	EDID_105[3]	EDID_105[2]	EDID_105[1]	EDID_105[0]
0x6A	0x00	EDIDMEMORY_REG_6A	r	EDID_106[7]	EDID_106[6]	EDID_106[5]	EDID_106[4]	EDID_106[3]	EDID_106[2]	EDID_106[1]	EDID_106[0]
0x6B	0x00	EDIDMEMORY_REG_6B	r	EDID_107[7]	EDID_107[6]	EDID_107[5]	EDID_107[4]	EDID_107[3]	EDID_107[2]	EDID_107[1]	EDID_107[0]
0x6C	0x00	EDIDMEMORY_REG_6C	r	EDID_108[7]	EDID_108[6]	EDID_108[5]	EDID_108[4]	EDID_108[3]	EDID_108[2]	EDID_108[1]	EDID_108[0]
0x6D	0x00	EDIDMEMORY_REG_6D	r	EDID_109[7]	EDID_109[6]	EDID_109[5]	EDID_109[4]	EDID_109[3]	EDID_109[2]	EDID_109[1]	EDID_109[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x6E	0x00	EDIDMEMORY_REG_6E	r	EDID_110[7]	EDID_110[6]	EDID_110[5]	EDID_110[4]	EDID_110[3]	EDID_110[2]	EDID_110[1]	EDID_110[0]
0x6F	0x00	EDIDMEMORY_REG_6F	r	EDID_111[7]	EDID_111[6]	EDID_111[5]	EDID_111[4]	EDID_111[3]	EDID_111[2]	EDID_111[1]	EDID_111[0]
0x70	0x00	EDIDMEMORY_REG_70	r	EDID_112[7]	EDID_112[6]	EDID_112[5]	EDID_112[4]	EDID_112[3]	EDID_112[2]	EDID_112[1]	EDID_112[0]
0x71	0x00	EDIDMEMORY_REG_71	r	EDID_113[7]	EDID_113[6]	EDID_113[5]	EDID_113[4]	EDID_113[3]	EDID_113[2]	EDID_113[1]	EDID_113[0]
0x72	0x00	EDIDMEMORY_REG_72	r	EDID_114[7]	EDID_114[6]	EDID_114[5]	EDID_114[4]	EDID_114[3]	EDID_114[2]	EDID_114[1]	EDID_114[0]
0x73	0x00	EDIDMEMORY_REG_73	r	EDID_115[7]	EDID_115[6]	EDID_115[5]	EDID_115[4]	EDID_115[3]	EDID_115[2]	EDID_115[1]	EDID_115[0]
0x74	0x00	EDIDMEMORY_REG_74	r	EDID_116[7]	EDID_116[6]	EDID_116[5]	EDID_116[4]	EDID_116[3]	EDID_116[2]	EDID_116[1]	EDID_116[0]
0x75	0x00	EDIDMEMORY_REG_75	r	EDID_117[7]	EDID_117[6]	EDID_117[5]	EDID_117[4]	EDID_117[3]	EDID_117[2]	EDID_117[1]	EDID_117[0]
0x76	0x00	EDIDMEMORY_REG_76	r	EDID_118[7]	EDID_118[6]	EDID_118[5]	EDID_118[4]	EDID_118[3]	EDID_118[2]	EDID_118[1]	EDID_118[0]
0x77	0x00	EDIDMEMORY_REG_77	r	EDID_119[7]	EDID_119[6]	EDID_119[5]	EDID_119[4]	EDID_119[3]	EDID_119[2]	EDID_119[1]	EDID_119[0]
0x78	0x00	EDIDMEMORY_REG_78	r	EDID_120[7]	EDID_120[6]	EDID_120[5]	EDID_120[4]	EDID_120[3]	EDID_120[2]	EDID_120[1]	EDID_120[0]
0x79	0x00	EDIDMEMORY_REG_79	r	EDID_121[7]	EDID_121[6]	EDID_121[5]	EDID_121[4]	EDID_121[3]	EDID_121[2]	EDID_121[1]	EDID_121[0]
0x7A	0x00	EDIDMEMORY_REG_7A	r	EDID_122[7]	EDID_122[6]	EDID_122[5]	EDID_122[4]	EDID_122[3]	EDID_122[2]	EDID_122[1]	EDID_122[0]
0x7B	0x00	EDIDMEMORY_REG_7B	r	EDID_123[7]	EDID_123[6]	EDID_123[5]	EDID_123[4]	EDID_123[3]	EDID_123[2]	EDID_123[1]	EDID_123[0]
0x7C	0x00	EDIDMEMORY_REG_7C	r	EDID_124[7]	EDID_124[6]	EDID_124[5]	EDID_124[4]	EDID_124[3]	EDID_124[2]	EDID_124[1]	EDID_124[0]
0x7D	0x00	EDIDMEMORY_REG_7D	r	EDID_125[7]	EDID_125[6]	EDID_125[5]	EDID_125[4]	EDID_125[3]	EDID_125[2]	EDID_125[1]	EDID_125[0]
0x7E	0x00	EDIDMEMORY_REG_7E	r	EDID_126[7]	EDID_126[6]	EDID_126[5]	EDID_126[4]	EDID_126[3]	EDID_126[2]	EDID_126[1]	EDID_126[0]
0x7F	0x00	EDIDMEMORY_REG_7F	r	EDID_127[7]	EDID_127[6]	EDID_127[5]	EDID_127[4]	EDID_127[3]	EDID_127[2]	EDID_127[1]	EDID_127[0]
0x80	0x00	EDIDMEMORY_REG_80	r	EDID_128[7]	EDID_128[6]	EDID_128[5]	EDID_128[4]	EDID_128[3]	EDID_128[2]	EDID_128[1]	EDID_128[0]
0x81	0x00	EDIDMEMORY_REG_81	r	EDID_129[7]	EDID_129[6]	EDID_129[5]	EDID_129[4]	EDID_129[3]	EDID_129[2]	EDID_129[1]	EDID_129[0]
0x82	0x00	EDIDMEMORY_REG_82	r	EDID_130[7]	EDID_130[6]	EDID_130[5]	EDID_130[4]	EDID_130[3]	EDID_130[2]	EDID_130[1]	EDID_130[0]
0x83	0x00	EDIDMEMORY_REG_83	r	EDID_131[7]	EDID_131[6]	EDID_131[5]	EDID_131[4]	EDID_131[3]	EDID_131[2]	EDID_131[1]	EDID_131[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x84	0x00	EDIDMEMORY_REG_84	r	EDID_132[7]	EDID_132[6]	EDID_132[5]	EDID_132[4]	EDID_132[3]	EDID_132[2]	EDID_132[1]	EDID_132[0]
0x85	0x00	EDIDMEMORY_REG_85	r	EDID_133[7]	EDID_133[6]	EDID_133[5]	EDID_133[4]	EDID_133[3]	EDID_133[2]	EDID_133[1]	EDID_133[0]
0x86	0x00	EDIDMEMORY_REG_86	r	EDID_134[7]	EDID_134[6]	EDID_134[5]	EDID_134[4]	EDID_134[3]	EDID_134[2]	EDID_134[1]	EDID_134[0]
0x87	0x00	EDIDMEMORY_REG_87	r	EDID_135[7]	EDID_135[6]	EDID_135[5]	EDID_135[4]	EDID_135[3]	EDID_135[2]	EDID_135[1]	EDID_135[0]
0x88	0x00	EDIDMEMORY_REG_88	r	EDID_136[7]	EDID_136[6]	EDID_136[5]	EDID_136[4]	EDID_136[3]	EDID_136[2]	EDID_136[1]	EDID_136[0]
0x89	0x00	EDIDMEMORY_REG_89	r	EDID_137[7]	EDID_137[6]	EDID_137[5]	EDID_137[4]	EDID_137[3]	EDID_137[2]	EDID_137[1]	EDID_137[0]
0x8A	0x00	EDIDMEMORY_REG_8A	r	EDID_138[7]	EDID_138[6]	EDID_138[5]	EDID_138[4]	EDID_138[3]	EDID_138[2]	EDID_138[1]	EDID_138[0]
0x8B	0x00	EDIDMEMORY_REG_8B	r	EDID_139[7]	EDID_139[6]	EDID_139[5]	EDID_139[4]	EDID_139[3]	EDID_139[2]	EDID_139[1]	EDID_139[0]
0x8C	0x00	EDIDMEMORY_REG_8C	r	EDID_140[7]	EDID_140[6]	EDID_140[5]	EDID_140[4]	EDID_140[3]	EDID_140[2]	EDID_140[1]	EDID_140[0]
0x8D	0x00	EDIDMEMORY_REG_8D	r	EDID_141[7]	EDID_141[6]	EDID_141[5]	EDID_141[4]	EDID_141[3]	EDID_141[2]	EDID_141[1]	EDID_141[0]
0x8E	0x00	EDIDMEMORY_REG_8E	r	EDID_142[7]	EDID_142[6]	EDID_142[5]	EDID_142[4]	EDID_142[3]	EDID_142[2]	EDID_142[1]	EDID_142[0]
0x8F	0x00	EDIDMEMORY_REG_8F	r	EDID_143[7]	EDID_143[6]	EDID_143[5]	EDID_143[4]	EDID_143[3]	EDID_143[2]	EDID_143[1]	EDID_143[0]
0x90	0x00	EDIDMEMORY_REG_90	r	EDID_144[7]	EDID_144[6]	EDID_144[5]	EDID_144[4]	EDID_144[3]	EDID_144[2]	EDID_144[1]	EDID_144[0]
0x91	0x00	EDIDMEMORY_REG_91	r	EDID_145[7]	EDID_145[6]	EDID_145[5]	EDID_145[4]	EDID_145[3]	EDID_145[2]	EDID_145[1]	EDID_145[0]
0x92	0x00	EDIDMEMORY_REG_92	r	EDID_146[7]	EDID_146[6]	EDID_146[5]	EDID_146[4]	EDID_146[3]	EDID_146[2]	EDID_146[1]	EDID_146[0]
0x93	0x00	EDIDMEMORY_REG_93	r	EDID_147[7]	EDID_147[6]	EDID_147[5]	EDID_147[4]	EDID_147[3]	EDID_147[2]	EDID_147[1]	EDID_147[0]
0x94	0x00	EDIDMEMORY_REG_94	r	EDID_148[7]	EDID_148[6]	EDID_148[5]	EDID_148[4]	EDID_148[3]	EDID_148[2]	EDID_148[1]	EDID_148[0]
0x95	0x00	EDIDMEMORY_REG_95	r	EDID_149[7]	EDID_149[6]	EDID_149[5]	EDID_149[4]	EDID_149[3]	EDID_149[2]	EDID_149[1]	EDID_149[0]
0x96	0x00	EDIDMEMORY_REG_96	r	EDID_150[7]	EDID_150[6]	EDID_150[5]	EDID_150[4]	EDID_150[3]	EDID_150[2]	EDID_150[1]	EDID_150[0]
0x97	0x00	EDIDMEMORY_REG_97	r	EDID_151[7]	EDID_151[6]	EDID_151[5]	EDID_151[4]	EDID_151[3]	EDID_151[2]	EDID_151[1]	EDID_151[0]
0x98	0x00	EDIDMEMORY_REG_98	r	EDID_152[7]	EDID_152[6]	EDID_152[5]	EDID_152[4]	EDID_152[3]	EDID_152[2]	EDID_152[1]	EDID_152[0]
0x99	0x00	EDIDMEMORY_REG_99	r	EDID_153[7]	EDID_153[6]	EDID_153[5]	EDID_153[4]	EDID_153[3]	EDID_153[2]	EDID_153[1]	EDID_153[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x9A	0x00	EDIDMEMORY_REG_9A	r	EDID_154[7]	EDID_154[6]	EDID_154[5]	EDID_154[4]	EDID_154[3]	EDID_154[2]	EDID_154[1]	EDID_154[0]
0x9B	0x00	EDIDMEMORY_REG_9B	r	EDID_155[7]	EDID_155[6]	EDID_155[5]	EDID_155[4]	EDID_155[3]	EDID_155[2]	EDID_155[1]	EDID_155[0]
0x9C	0x00	EDIDMEMORY_REG_9C	r	EDID_156[7]	EDID_156[6]	EDID_156[5]	EDID_156[4]	EDID_156[3]	EDID_156[2]	EDID_156[1]	EDID_156[0]
0x9D	0x00	EDIDMEMORY_REG_9D	r	EDID_157[7]	EDID_157[6]	EDID_157[5]	EDID_157[4]	EDID_157[3]	EDID_157[2]	EDID_157[1]	EDID_157[0]
0x9E	0x00	EDIDMEMORY_REG_9E	r	EDID_158[7]	EDID_158[6]	EDID_158[5]	EDID_158[4]	EDID_158[3]	EDID_158[2]	EDID_158[1]	EDID_158[0]
0x9F	0x00	EDIDMEMORY_REG_9F	r	EDID_159[7]	EDID_159[6]	EDID_159[5]	EDID_159[4]	EDID_159[3]	EDID_159[2]	EDID_159[1]	EDID_159[0]
0xA0	0x00	EDIDMEMORY_REG_A0	r	EDID_160[7]	EDID_160[6]	EDID_160[5]	EDID_160[4]	EDID_160[3]	EDID_160[2]	EDID_160[1]	EDID_160[0]
0xA1	0x00	EDIDMEMORY_REG_A1	r	EDID_161[7]	EDID_161[6]	EDID_161[5]	EDID_161[4]	EDID_161[3]	EDID_161[2]	EDID_161[1]	EDID_161[0]
0xA2	0x00	EDIDMEMORY_REG_A2	r	EDID_162[7]	EDID_162[6]	EDID_162[5]	EDID_162[4]	EDID_162[3]	EDID_162[2]	EDID_162[1]	EDID_162[0]
0xA3	0x00	EDIDMEMORY_REG_A3	r	EDID_163[7]	EDID_163[6]	EDID_163[5]	EDID_163[4]	EDID_163[3]	EDID_163[2]	EDID_163[1]	EDID_163[0]
0xA4	0x00	EDIDMEMORY_REG_A4	r	EDID_164[7]	EDID_164[6]	EDID_164[5]	EDID_164[4]	EDID_164[3]	EDID_164[2]	EDID_164[1]	EDID_164[0]
0xA5	0x00	EDIDMEMORY_REG_A5	r	EDID_165[7]	EDID_165[6]	EDID_165[5]	EDID_165[4]	EDID_165[3]	EDID_165[2]	EDID_165[1]	EDID_165[0]
0xA6	0x00	EDIDMEMORY_REG_A6	r	EDID_166[7]	EDID_166[6]	EDID_166[5]	EDID_166[4]	EDID_166[3]	EDID_166[2]	EDID_166[1]	EDID_166[0]
0xA7	0x00	EDIDMEMORY_REG_A7	r	EDID_167[7]	EDID_167[6]	EDID_167[5]	EDID_167[4]	EDID_167[3]	EDID_167[2]	EDID_167[1]	EDID_167[0]
0xA8	0x00	EDIDMEMORY_REG_A8	r	EDID_168[7]	EDID_168[6]	EDID_168[5]	EDID_168[4]	EDID_168[3]	EDID_168[2]	EDID_168[1]	EDID_168[0]
0xA9	0x00	EDIDMEMORY_REG_A9	r	EDID_169[7]	EDID_169[6]	EDID_169[5]	EDID_169[4]	EDID_169[3]	EDID_169[2]	EDID_169[1]	EDID_169[0]
0xAA	0x00	EDIDMEMORY_REG_AA	r	EDID_170[7]	EDID_170[6]	EDID_170[5]	EDID_170[4]	EDID_170[3]	EDID_170[2]	EDID_170[1]	EDID_170[0]
0xAB	0x00	EDIDMEMORY_REG_AB	r	EDID_171[7]	EDID_171[6]	EDID_171[5]	EDID_171[4]	EDID_171[3]	EDID_171[2]	EDID_171[1]	EDID_171[0]
0xAC	0x00	EDIDMEMORY_REG_AC	r	EDID_172[7]	EDID_172[6]	EDID_172[5]	EDID_172[4]	EDID_172[3]	EDID_172[2]	EDID_172[1]	EDID_172[0]
0xAD	0x00	EDIDMEMORY_REG_AD	r	EDID_173[7]	EDID_173[6]	EDID_173[5]	EDID_173[4]	EDID_173[3]	EDID_173[2]	EDID_173[1]	EDID_173[0]
0xAE	0x00	EDIDMEMORY_REG_AE	r	EDID_174[7]	EDID_174[6]	EDID_174[5]	EDID_174[4]	EDID_174[3]	EDID_174[2]	EDID_174[1]	EDID_174[0]
0xAF	0x00	EDIDMEMORY_REG_AF	r	EDID_175[7]	EDID_175[6]	EDID_175[5]	EDID_175[4]	EDID_175[3]	EDID_175[2]	EDID_175[1]	EDID_175[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xB0	0x00	EDIDMEMORY_REG_B0	r	EDID_176[7]	EDID_176[6]	EDID_176[5]	EDID_176[4]	EDID_176[3]	EDID_176[2]	EDID_176[1]	EDID_176[0]
0xB1	0x00	EDIDMEMORY_REG_B1	r	EDID_177[7]	EDID_177[6]	EDID_177[5]	EDID_177[4]	EDID_177[3]	EDID_177[2]	EDID_177[1]	EDID_177[0]
0xB2	0x00	EDIDMEMORY_REG_B2	r	EDID_178[7]	EDID_178[6]	EDID_178[5]	EDID_178[4]	EDID_178[3]	EDID_178[2]	EDID_178[1]	EDID_178[0]
0xB3	0x00	EDIDMEMORY_REG_B3	r	EDID_179[7]	EDID_179[6]	EDID_179[5]	EDID_179[4]	EDID_179[3]	EDID_179[2]	EDID_179[1]	EDID_179[0]
0xB4	0x00	EDIDMEMORY_REG_B4	r	EDID_180[7]	EDID_180[6]	EDID_180[5]	EDID_180[4]	EDID_180[3]	EDID_180[2]	EDID_180[1]	EDID_180[0]
0xB5	0x00	EDIDMEMORY_REG_B5	r	EDID_181[7]	EDID_181[6]	EDID_181[5]	EDID_181[4]	EDID_181[3]	EDID_181[2]	EDID_181[1]	EDID_181[0]
0xB6	0x00	EDIDMEMORY_REG_B6	r	EDID_182[7]	EDID_182[6]	EDID_182[5]	EDID_182[4]	EDID_182[3]	EDID_182[2]	EDID_182[1]	EDID_182[0]
0xB7	0x00	EDIDMEMORY_REG_B7	r	EDID_183[7]	EDID_183[6]	EDID_183[5]	EDID_183[4]	EDID_183[3]	EDID_183[2]	EDID_183[1]	EDID_183[0]
0xB8	0x00	EDIDMEMORY_REG_B8	r	EDID_184[7]	EDID_184[6]	EDID_184[5]	EDID_184[4]	EDID_184[3]	EDID_184[2]	EDID_184[1]	EDID_184[0]
0xB9	0x00	EDIDMEMORY_REG_B9	r	EDID_185[7]	EDID_185[6]	EDID_185[5]	EDID_185[4]	EDID_185[3]	EDID_185[2]	EDID_185[1]	EDID_185[0]
0xBA	0x00	EDIDMEMORY_REG_BA	r	EDID_186[7]	EDID_186[6]	EDID_186[5]	EDID_186[4]	EDID_186[3]	EDID_186[2]	EDID_186[1]	EDID_186[0]
0xBB	0x00	EDIDMEMORY_REG_BB	r	EDID_187[7]	EDID_187[6]	EDID_187[5]	EDID_187[4]	EDID_187[3]	EDID_187[2]	EDID_187[1]	EDID_187[0]
0xBC	0x00	EDIDMEMORY_REG_BC	r	EDID_188[7]	EDID_188[6]	EDID_188[5]	EDID_188[4]	EDID_188[3]	EDID_188[2]	EDID_188[1]	EDID_188[0]
0xBD	0x00	EDIDMEMORY_REG_BD	r	EDID_189[7]	EDID_189[6]	EDID_189[5]	EDID_189[4]	EDID_189[3]	EDID_189[2]	EDID_189[1]	EDID_189[0]
0xBE	0x00	EDIDMEMORY_REG_BE	r	EDID_190[7]	EDID_190[6]	EDID_190[5]	EDID_190[4]	EDID_190[3]	EDID_190[2]	EDID_190[1]	EDID_190[0]
0xBF	0x00	EDIDMEMORY_REG_BF	r	EDID_191[7]	EDID_191[6]	EDID_191[5]	EDID_191[4]	EDID_191[3]	EDID_191[2]	EDID_191[1]	EDID_191[0]
0xC0	0x00	EDIDMEMORY_REG_C0	r	EDID_192[7]	EDID_192[6]	EDID_192[5]	EDID_192[4]	EDID_192[3]	EDID_192[2]	EDID_192[1]	EDID_192[0]
0xC1	0x00	EDIDMEMORY_REG_C1	r	EDID_193[7]	EDID_193[6]	EDID_193[5]	EDID_193[4]	EDID_193[3]	EDID_193[2]	EDID_193[1]	EDID_193[0]
0xC2	0x00	EDIDMEMORY_REG_C2	r	EDID_194[7]	EDID_194[6]	EDID_194[5]	EDID_194[4]	EDID_194[3]	EDID_194[2]	EDID_194[1]	EDID_194[0]
0xC3	0x00	EDIDMEMORY_REG_C3	r	EDID_195[7]	EDID_195[6]	EDID_195[5]	EDID_195[4]	EDID_195[3]	EDID_195[2]	EDID_195[1]	EDID_195[0]
0xC4	0x00	EDIDMEMORY_REG_C4	r	EDID_196[7]	EDID_196[6]	EDID_196[5]	EDID_196[4]	EDID_196[3]	EDID_196[2]	EDID_196[1]	EDID_196[0]
0xC5	0x00	EDIDMEMORY_REG_C5	r	EDID_197[7]	EDID_197[6]	EDID_197[5]	EDID_197[4]	EDID_197[3]	EDID_197[2]	EDID_197[1]	EDID_197[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xC6	0x00	EDIDMEMORY_REG_C6	r	EDID_198[7]	EDID_198[6]	EDID_198[5]	EDID_198[4]	EDID_198[3]	EDID_198[2]	EDID_198[1]	EDID_198[0]
0xC7	0x00	EDIDMEMORY_REG_C7	r	EDID_199[7]	EDID_199[6]	EDID_199[5]	EDID_199[4]	EDID_199[3]	EDID_199[2]	EDID_199[1]	EDID_199[0]
0xC8	0x00	EDIDMEMORY_REG_C8	r	EDID_200[7]	EDID_200[6]	EDID_200[5]	EDID_200[4]	EDID_200[3]	EDID_200[2]	EDID_200[1]	EDID_200[0]
0xC9	0x00	EDIDMEMORY_REG_C9	r	EDID_201[7]	EDID_201[6]	EDID_201[5]	EDID_201[4]	EDID_201[3]	EDID_201[2]	EDID_201[1]	EDID_201[0]
0xCA	0x00	EDIDMEMORY_REG_CA	r	EDID_202[7]	EDID_202[6]	EDID_202[5]	EDID_202[4]	EDID_202[3]	EDID_202[2]	EDID_202[1]	EDID_202[0]
0xCB	0x00	EDIDMEMORY_REG_CB	r	EDID_203[7]	EDID_203[6]	EDID_203[5]	EDID_203[4]	EDID_203[3]	EDID_203[2]	EDID_203[1]	EDID_203[0]
0xCC	0x00	EDIDMEMORY_REG_CC	r	EDID_204[7]	EDID_204[6]	EDID_204[5]	EDID_204[4]	EDID_204[3]	EDID_204[2]	EDID_204[1]	EDID_204[0]
0xCD	0x00	EDIDMEMORY_REG_CD	r	EDID_205[7]	EDID_205[6]	EDID_205[5]	EDID_205[4]	EDID_205[3]	EDID_205[2]	EDID_205[1]	EDID_205[0]
0xCE	0x00	EDIDMEMORY_REG_CE	r	EDID_206[7]	EDID_206[6]	EDID_206[5]	EDID_206[4]	EDID_206[3]	EDID_206[2]	EDID_206[1]	EDID_206[0]
0xCF	0x00	EDIDMEMORY_REG_CF	r	EDID_207[7]	EDID_207[6]	EDID_207[5]	EDID_207[4]	EDID_207[3]	EDID_207[2]	EDID_207[1]	EDID_207[0]
0xD0	0x00	EDIDMEMORY_REG_D0	r	EDID_208[7]	EDID_208[6]	EDID_208[5]	EDID_208[4]	EDID_208[3]	EDID_208[2]	EDID_208[1]	EDID_208[0]
0xD1	0x00	EDIDMEMORY_REG_D1	r	EDID_209[7]	EDID_209[6]	EDID_209[5]	EDID_209[4]	EDID_209[3]	EDID_209[2]	EDID_209[1]	EDID_209[0]
0xD2	0x00	EDIDMEMORY_REG_D2	r	EDID_210[7]	EDID_210[6]	EDID_210[5]	EDID_210[4]	EDID_210[3]	EDID_210[2]	EDID_210[1]	EDID_210[0]
0xD3	0x00	EDIDMEMORY_REG_D3	r	EDID_211[7]	EDID_211[6]	EDID_211[5]	EDID_211[4]	EDID_211[3]	EDID_211[2]	EDID_211[1]	EDID_211[0]
0xD4	0x00	EDIDMEMORY_REG_D4	r	EDID_212[7]	EDID_212[6]	EDID_212[5]	EDID_212[4]	EDID_212[3]	EDID_212[2]	EDID_212[1]	EDID_212[0]
0xD5	0x00	EDIDMEMORY_REG_D5	r	EDID_213[7]	EDID_213[6]	EDID_213[5]	EDID_213[4]	EDID_213[3]	EDID_213[2]	EDID_213[1]	EDID_213[0]
0xD6	0x00	EDIDMEMORY_REG_D6	r	EDID_214[7]	EDID_214[6]	EDID_214[5]	EDID_214[4]	EDID_214[3]	EDID_214[2]	EDID_214[1]	EDID_214[0]
0xD7	0x00	EDIDMEMORY_REG_D7	r	EDID_215[7]	EDID_215[6]	EDID_215[5]	EDID_215[4]	EDID_215[3]	EDID_215[2]	EDID_215[1]	EDID_215[0]
0xD8	0x00	EDIDMEMORY_REG_D8	r	EDID_216[7]	EDID_216[6]	EDID_216[5]	EDID_216[4]	EDID_216[3]	EDID_216[2]	EDID_216[1]	EDID_216[0]
0xD9	0x00	EDIDMEMORY_REG_D9	r	EDID_217[7]	EDID_217[6]	EDID_217[5]	EDID_217[4]	EDID_217[3]	EDID_217[2]	EDID_217[1]	EDID_217[0]
0xDA	0x00	EDIDMEMORY_REG_DA	r	EDID_218[7]	EDID_218[6]	EDID_218[5]	EDID_218[4]	EDID_218[3]	EDID_218[2]	EDID_218[1]	EDID_218[0]
0xDB	0x00	EDIDMEMORY_REG_DB	r	EDID_219[7]	EDID_219[6]	EDID_219[5]	EDID_219[4]	EDID_219[3]	EDID_219[2]	EDID_219[1]	EDID_219[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xDC	0x00	EDIDMEMORY_REG_DC	r	EDID_220[7]	EDID_220[6]	EDID_220[5]	EDID_220[4]	EDID_220[3]	EDID_220[2]	EDID_220[1]	EDID_220[0]
0xDD	0x00	EDIDMEMORY_REG_DD	r	EDID_221[7]	EDID_221[6]	EDID_221[5]	EDID_221[4]	EDID_221[3]	EDID_221[2]	EDID_221[1]	EDID_221[0]
0xDE	0x00	EDIDMEMORY_REG_DE	r	EDID_222[7]	EDID_222[6]	EDID_222[5]	EDID_222[4]	EDID_222[3]	EDID_222[2]	EDID_222[1]	EDID_222[0]
0xDF	0x00	EDIDMEMORY_REG_DF	r	EDID_223[7]	EDID_223[6]	EDID_223[5]	EDID_223[4]	EDID_223[3]	EDID_223[2]	EDID_223[1]	EDID_223[0]
0xE0	0x00	EDIDMEMORY_REG_E0	r	EDID_224[7]	EDID_224[6]	EDID_224[5]	EDID_224[4]	EDID_224[3]	EDID_224[2]	EDID_224[1]	EDID_224[0]
0xE1	0x00	EDIDMEMORY_REG_E1	r	EDID_225[7]	EDID_225[6]	EDID_225[5]	EDID_225[4]	EDID_225[3]	EDID_225[2]	EDID_225[1]	EDID_225[0]
0xE2	0x00	EDIDMEMORY_REG_E2	r	EDID_226[7]	EDID_226[6]	EDID_226[5]	EDID_226[4]	EDID_226[3]	EDID_226[2]	EDID_226[1]	EDID_226[0]
0xE3	0x00	EDIDMEMORY_REG_E3	r	EDID_227[7]	EDID_227[6]	EDID_227[5]	EDID_227[4]	EDID_227[3]	EDID_227[2]	EDID_227[1]	EDID_227[0]
0xE4	0x00	EDIDMEMORY_REG_E4	r	EDID_228[7]	EDID_228[6]	EDID_228[5]	EDID_228[4]	EDID_228[3]	EDID_228[2]	EDID_228[1]	EDID_228[0]
0xE5	0x00	EDIDMEMORY_REG_E5	r	EDID_229[7]	EDID_229[6]	EDID_229[5]	EDID_229[4]	EDID_229[3]	EDID_229[2]	EDID_229[1]	EDID_229[0]
0xE6	0x00	EDIDMEMORY_REG_E6	r	EDID_230[7]	EDID_230[6]	EDID_230[5]	EDID_230[4]	EDID_230[3]	EDID_230[2]	EDID_230[1]	EDID_230[0]
0xE7	0x00	EDIDMEMORY_REG_E7	r	EDID_231[7]	EDID_231[6]	EDID_231[5]	EDID_231[4]	EDID_231[3]	EDID_231[2]	EDID_231[1]	EDID_231[0]
0xE8	0x00	EDIDMEMORY_REG_E8	r	EDID_232[7]	EDID_232[6]	EDID_232[5]	EDID_232[4]	EDID_232[3]	EDID_232[2]	EDID_232[1]	EDID_232[0]
0xE9	0x00	EDIDMEMORY_REG_E9	r	EDID_233[7]	EDID_233[6]	EDID_233[5]	EDID_233[4]	EDID_233[3]	EDID_233[2]	EDID_233[1]	EDID_233[0]
0xEA	0x00	EDIDMEMORY_REG_EA	r	EDID_234[7]	EDID_234[6]	EDID_234[5]	EDID_234[4]	EDID_234[3]	EDID_234[2]	EDID_234[1]	EDID_234[0]
0xEB	0x00	EDIDMEMORY_REG_EB	r	EDID_235[7]	EDID_235[6]	EDID_235[5]	EDID_235[4]	EDID_235[3]	EDID_235[2]	EDID_235[1]	EDID_235[0]
0xEC	0x00	EDIDMEMORY_REG_EC	r	EDID_236[7]	EDID_236[6]	EDID_236[5]	EDID_236[4]	EDID_236[3]	EDID_236[2]	EDID_236[1]	EDID_236[0]
0xED	0x00	EDIDMEMORY_REG_ED	r	EDID_237[7]	EDID_237[6]	EDID_237[5]	EDID_237[4]	EDID_237[3]	EDID_237[2]	EDID_237[1]	EDID_237[0]
0xEE	0x00	EDIDMEMORY_REG_EE	r	EDID_238[7]	EDID_238[6]	EDID_238[5]	EDID_238[4]	EDID_238[3]	EDID_238[2]	EDID_238[1]	EDID_238[0]
0xEF	0x00	EDIDMEMORY_REG_EF	r	EDID_239[7]	EDID_239[6]	EDID_239[5]	EDID_239[4]	EDID_239[3]	EDID_239[2]	EDID_239[1]	EDID_239[0]
0xF0	0x00	EDIDMEMORY_REG_F0	r	EDID_240[7]	EDID_240[6]	EDID_240[5]	EDID_240[4]	EDID_240[3]	EDID_240[2]	EDID_240[1]	EDID_240[0]
0xF1	0x00	EDIDMEMORY_REG_F1	r	EDID_241[7]	EDID_241[6]	EDID_241[5]	EDID_241[4]	EDID_241[3]	EDID_241[2]	EDID_241[1]	EDID_241[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xF2	0x00	EDIDMEMORY_REG_F2	r	EDID_242[7]	EDID_242[6]	EDID_242[5]	EDID_242[4]	EDID_242[3]	EDID_242[2]	EDID_242[1]	EDID_242[0]
0xF3	0x00	EDIDMEMORY_REG_F3	r	EDID_243[7]	EDID_243[6]	EDID_243[5]	EDID_243[4]	EDID_243[3]	EDID_243[2]	EDID_243[1]	EDID_243[0]
0xF4	0x00	EDIDMEMORY_REG_F4	r	EDID_244[7]	EDID_244[6]	EDID_244[5]	EDID_244[4]	EDID_244[3]	EDID_244[2]	EDID_244[1]	EDID_244[0]
0xF5	0x00	EDIDMEMORY_REG_F5	r	EDID_245[7]	EDID_245[6]	EDID_245[5]	EDID_245[4]	EDID_245[3]	EDID_245[2]	EDID_245[1]	EDID_245[0]
0xF6	0x00	EDIDMEMORY_REG_F6	r	EDID_246[7]	EDID_246[6]	EDID_246[5]	EDID_246[4]	EDID_246[3]	EDID_246[2]	EDID_246[1]	EDID_246[0]
0xF7	0x00	EDIDMEMORY_REG_F7	r	EDID_247[7]	EDID_247[6]	EDID_247[5]	EDID_247[4]	EDID_247[3]	EDID_247[2]	EDID_247[1]	EDID_247[0]
0xF8	0x00	EDIDMEMORY_REG_F8	r	EDID_248[7]	EDID_248[6]	EDID_248[5]	EDID_248[4]	EDID_248[3]	EDID_248[2]	EDID_248[1]	EDID_248[0]
0xF9	0x00	EDIDMEMORY_REG_F9	r	EDID_249[7]	EDID_249[6]	EDID_249[5]	EDID_249[4]	EDID_249[3]	EDID_249[2]	EDID_249[1]	EDID_249[0]
0xFA	0x00	EDIDMEMORY_REG_FA	r	EDID_250[7]	EDID_250[6]	EDID_250[5]	EDID_250[4]	EDID_250[3]	EDID_250[2]	EDID_250[1]	EDID_250[0]
0xFB	0x00	EDIDMEMORY_REG_FB	r	EDID_251[7]	EDID_251[6]	EDID_251[5]	EDID_251[4]	EDID_251[3]	EDID_251[2]	EDID_251[1]	EDID_251[0]
0xFC	0x00	EDIDMEMORY_REG_FC	r	EDID_252[7]	EDID_252[6]	EDID_252[5]	EDID_252[4]	EDID_252[3]	EDID_252[2]	EDID_252[1]	EDID_252[0]
0xFD	0x00	EDIDMEMORY_REG_FD	r	EDID_253[7]	EDID_253[6]	EDID_253[5]	EDID_253[4]	EDID_253[3]	EDID_253[2]	EDID_253[1]	EDID_253[0]
0xFE	0x00	EDIDMEMORY_REG_FE	r	EDID_254[7]	EDID_254[6]	EDID_254[5]	EDID_254[4]	EDID_254[3]	EDID_254[2]	EDID_254[1]	EDID_254[0]
0xFF	0x00	EDIDMEMORY_REG_FF	r	EDID_255[7]	EDID_255[6]	EDID_255[5]	EDID_255[4]	EDID_255[3]	EDID_255[2]	EDID_255[1]	EDID_255[0]

1.8 TXB MAIN MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x41	0x50	MAIN_REG_41	rw	-	SYSTEM_PD	-	-	-	-	-	-
0x92	0x00	MAIN_REG_92	rw	CEC_CMD_INTR_MASK[7]	CEC_CMD_INTR_MASK[6]	CEC_CMD_INTR_MASK[5]	CEC_CMD_INTR_MASK[4]	CEC_CMD_INTR_MASK[3]	CEC_CMD_INTR_MASK[2]	CEC_CMD_INTR_MASK[1]	CEC_CMD_INTR_MASK[0]
0x93	0x00	MAIN_REG_93	rw	CEC_CMD_INTR[7]	CEC_CMD_INTR[6]	CEC_CMD_INTR[5]	CEC_CMD_INTR[4]	CEC_CMD_INTR[3]	CEC_CMD_INTR[2]	CEC_CMD_INTR[1]	CEC_CMD_INTR[0]
0x94	0xC0	MAIN_REG_94	rw	HPD_INTR_MASK	MSEN_INTR_MASK	VS_INTR_MASK	-	-	EDID_RDY_INTR_MASK	HDCP_CONTROLLER_STATE_4_INTR_MASK	RI_RDY_INTR_MASK
0x95	0x00	MAIN_REG_95	rw	HDCP_ERROR_INTR_MASK	BKSV_FLAG_INTR_MASK	TX_READY_INTR_MASK	TX_ARBITRATION_LOST_INTR_MASK	TX_RETRY_TIMEOUT_INTR_MASK	RX_READY_INTR_MASK[2]	RX_READY_INTR_MASK[1]	RX_READY_INTR_MASK[0]
0x96	0x00	MAIN_REG_96	rw	HPD_ST	MSEN_ST	VSYNC_ST	-	-	EDID_RDY_ST	HDCP_AUTH_ST	RI_RDY_ST
0x97	0x00	MAIN_REG_97	rw	HDCP_ERROR_ST	BKSV_FLAG_ST	TX_READY_INTR	TX_ARBITRATION_LOST_INTR	TX_RETRY_TIMEOUT_INTR	RX_READY_INTR[2]	RX_READY_INTR[1]	RX_READY_INTR[0]
0x98	0x00	MAIN_REG_98	rw	-	-	-	CEC_PD	-	-	-	-
0x9E	0x00	MAIN_REG_9E	rw	HIGH_VSYNC[1]	HIGH_VSYNC[0]	-	-	-	-	-	-
0x9F	0x00	MAIN_REG_9F	rw	-	-	HPD_DISABLE[1]	HPD_DISABLE[0]	-	-	-	-
0xAB	0x00	MAIN_REG_AB	rw	-	-	HDCP_START_DELAY[2]	HDCP_START_DELAY[1]	HDCP_START_DELAY[0]	-	-	-
0xAC	0x00	MAIN_REG_AC	rw	RI_FREQ_SEL[1]	RI_FREQ_SEL[0]	RI_DELAY_SEL[2]	RI_DELAY_SEL[1]	RI_DELAY_SEL[0]	BCAPS_DELAY[2]	BCAPS_DELAY[1]	BCAPS_DELAY[0]
0xAD	0x00	MAIN_REG_AD	rw	AN_DELAY[2]	AN_DELAY[1]	AN_DELAY[0]	AKSV_DELAY[2]	AKSV_DELAY[1]	AKSV_DELAY[0]	-	-
0xAE	0x00	MAIN_REG_AE	rw	SKIP_RI_128	HDCP_1P1_DIS	R0_WAIT_TIME[1]	R0_WAIT_TIME[0]	HDCP_REPEATER_TIMEOUT[1]	HDCP_REPEATER_TIMEOUT[0]	-	-
0xAF	0x14	MAIN_REG_AF	rw	HDCP_DESIRED	-	-	FRAME_ENC	-	TX_HDMI_MODE	EXT_HDMI_MODE	-
0xB8	0x00	MAIN_REG_B8	r	-	ENC_ON	-	KEYS_READ_ERROR	-	-	-	-
0xBE	0x00	MAIN_REG_BE	r	BCAPS[7]	BCAPS[6]	BCAPS[5]	BCAPS[4]	BCAPS[3]	BCAPS[2]	BCAPS[1]	BCAPS[0]
0xBF	0x00	MAIN_REG_BF	r	BKSV0[7]	BKSV0[6]	BKSV0[5]	BKSV0[4]	BKSV0[3]	BKSV0[2]	BKSV0[1]	BKSV0[0]
0xC0	0x00	MAIN_REG_C0	r	BKSV1[7]	BKSV1[6]	BKSV1[5]	BKSV1[4]	BKSV1[3]	BKSV1[2]	BKSV1[1]	BKSV1[0]
0xC1	0x00	MAIN_REG_C1	r	BKSV2[7]	BKSV2[6]	BKSV2[5]	BKSV2[4]	BKSV2[3]	BKSV2[2]	BKSV2[1]	BKSV2[0]
0xC2	0x00	MAIN_REG_C2	r	BKSV3[7]	BKSV3[6]	BKSV3[5]	BKSV3[4]	BKSV3[3]	BKSV3[2]	BKSV3[1]	BKSV3[0]
0xC3	0x00	MAIN_REG_C3	r	BKSV4[7]	BKSV4[6]	BKSV4[5]	BKSV4[4]	BKSV4[3]	BKSV4[2]	BKSV4[1]	BKSV4[0]
0xC4	0x00	MAIN_REG_C4	rw	EDID_SEGMENT[7]	EDID_SEGMENT[6]	EDID_SEGMENT[5]	EDID_SEGMENT[4]	EDID_SEGMENT[3]	EDID_SEGMENT[2]	EDID_SEGMENT[1]	EDID_SEGMENT[0]
0xC5	0x00	MAIN_REG_C5	rw	ERROR_FLAG	AN_STOP	HDCP_ENABLED	EDID_READY_FLAG	I2C_INTERRUPT	RI_FLAG	BKSV_UPDATE_FLAG	PJ_FLAG
0xC6	0x00	MAIN_REG_C6	r	-	-	-	HDMI_MODE	HDCP_REQUESTED	RX_SENSE	EEPROM_READ_OK	TMDSOUTPUTPWRDN
0xC7	0x00	MAIN_REG_C7	rw	BKSV_FLAG	BKSV_COUNT[6]	BKSV_COUNT[5]	BKSV_COUNT[4]	BKSV_COUNT[3]	BKSV_COUNT[2]	BKSV_COUNT[1]	BKSV_COUNT[0]
0xC8	0x00	MAIN_REG_C8	r	HDCP_CONTROLLER_ERROR[3]	HDCP_CONTROLLER_ERROR[2]	HDCP_CONTROLLER_ERROR[1]	HDCP_CONTROLLER_ERROR[0]	HDCP_CONTROLLER_STATE[3]	HDCP_CONTROLLER_STATE[2]	HDCP_CONTROLLER_STATE[1]	HDCP_CONTROLLER_STATE[0]
0xC9	0x03	MAIN_REG_C9	rw	-	-	-	EDID_READ_EN	EDID_TRIES[3]	EDID_TRIES[2]	EDID_TRIES[1]	EDID_TRIES[0]
0xE4	0x00	MAIN_REG_E4	r	PLL_LOCK_STATUS	-	-	-	-	-	-	-
0xEA	0x84	MAIN_REG_EA	rw	-	-	-	-	-	-	TMDS_CLK_INV_I2C	ENABLE_XXI_CLK_I2C

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xEB	0xFC	MAIN_REG_EB	rw	TRANSDRVENABLE_I2C[2]	TRANSDRVENABLE_I2C[1]	TRANSDRVENABLE_I2C[0]	-	-	-	-	-
0xFE	0x00	MAIN_REG_FE	rw	-	-	-	-	-	-	-	CHANNEL_SWAP

1.9 TXB EDID MAP

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x00	0x00	EDIDMEMORY_REG_00	r	EDID_0[7]	EDID_0[6]	EDID_0[5]	EDID_0[4]	EDID_0[3]	EDID_0[2]	EDID_0[1]	EDID_0[0]
0x01	0x00	EDIDMEMORY_REG_01	r	EDID_1[7]	EDID_1[6]	EDID_1[5]	EDID_1[4]	EDID_1[3]	EDID_1[2]	EDID_1[1]	EDID_1[0]
0x02	0x00	EDIDMEMORY_REG_02	r	EDID_2[7]	EDID_2[6]	EDID_2[5]	EDID_2[4]	EDID_2[3]	EDID_2[2]	EDID_2[1]	EDID_2[0]
0x03	0x00	EDIDMEMORY_REG_03	r	EDID_3[7]	EDID_3[6]	EDID_3[5]	EDID_3[4]	EDID_3[3]	EDID_3[2]	EDID_3[1]	EDID_3[0]
0x04	0x00	EDIDMEMORY_REG_04	r	EDID_4[7]	EDID_4[6]	EDID_4[5]	EDID_4[4]	EDID_4[3]	EDID_4[2]	EDID_4[1]	EDID_4[0]
0x05	0x00	EDIDMEMORY_REG_05	r	EDID_5[7]	EDID_5[6]	EDID_5[5]	EDID_5[4]	EDID_5[3]	EDID_5[2]	EDID_5[1]	EDID_5[0]
0x06	0x00	EDIDMEMORY_REG_06	r	EDID_6[7]	EDID_6[6]	EDID_6[5]	EDID_6[4]	EDID_6[3]	EDID_6[2]	EDID_6[1]	EDID_6[0]
0x07	0x00	EDIDMEMORY_REG_07	r	EDID_7[7]	EDID_7[6]	EDID_7[5]	EDID_7[4]	EDID_7[3]	EDID_7[2]	EDID_7[1]	EDID_7[0]
0x08	0x00	EDIDMEMORY_REG_08	r	EDID_8[7]	EDID_8[6]	EDID_8[5]	EDID_8[4]	EDID_8[3]	EDID_8[2]	EDID_8[1]	EDID_8[0]
0x09	0x00	EDIDMEMORY_REG_09	r	EDID_9[7]	EDID_9[6]	EDID_9[5]	EDID_9[4]	EDID_9[3]	EDID_9[2]	EDID_9[1]	EDID_9[0]
0x0A	0x00	EDIDMEMORY_REG_0A	r	EDID_10[7]	EDID_10[6]	EDID_10[5]	EDID_10[4]	EDID_10[3]	EDID_10[2]	EDID_10[1]	EDID_10[0]
0x0B	0x00	EDIDMEMORY_REG_0B	r	EDID_11[7]	EDID_11[6]	EDID_11[5]	EDID_11[4]	EDID_11[3]	EDID_11[2]	EDID_11[1]	EDID_11[0]
0x0C	0x00	EDIDMEMORY_REG_0C	r	EDID_12[7]	EDID_12[6]	EDID_12[5]	EDID_12[4]	EDID_12[3]	EDID_12[2]	EDID_12[1]	EDID_12[0]
0x0D	0x00	EDIDMEMORY_REG_0D	r	EDID_13[7]	EDID_13[6]	EDID_13[5]	EDID_13[4]	EDID_13[3]	EDID_13[2]	EDID_13[1]	EDID_13[0]
0x0E	0x00	EDIDMEMORY_REG_0E	r	EDID_14[7]	EDID_14[6]	EDID_14[5]	EDID_14[4]	EDID_14[3]	EDID_14[2]	EDID_14[1]	EDID_14[0]
0x0F	0x00	EDIDMEMORY_REG_0F	r	EDID_15[7]	EDID_15[6]	EDID_15[5]	EDID_15[4]	EDID_15[3]	EDID_15[2]	EDID_15[1]	EDID_15[0]
0x10	0x00	EDIDMEMORY_REG_10	r	EDID_16[7]	EDID_16[6]	EDID_16[5]	EDID_16[4]	EDID_16[3]	EDID_16[2]	EDID_16[1]	EDID_16[0]
0x11	0x00	EDIDMEMORY_REG_11	r	EDID_17[7]	EDID_17[6]	EDID_17[5]	EDID_17[4]	EDID_17[3]	EDID_17[2]	EDID_17[1]	EDID_17[0]
0x12	0x00	EDIDMEMORY_REG_12	r	EDID_18[7]	EDID_18[6]	EDID_18[5]	EDID_18[4]	EDID_18[3]	EDID_18[2]	EDID_18[1]	EDID_18[0]
0x13	0x00	EDIDMEMORY_REG_13	r	EDID_19[7]	EDID_19[6]	EDID_19[5]	EDID_19[4]	EDID_19[3]	EDID_19[2]	EDID_19[1]	EDID_19[0]
0x14	0x00	EDIDMEMORY_REG_14	r	EDID_20[7]	EDID_20[6]	EDID_20[5]	EDID_20[4]	EDID_20[3]	EDID_20[2]	EDID_20[1]	EDID_20[0]
0x15	0x00	EDIDMEMORY_REG_15	r	EDID_21[7]	EDID_21[6]	EDID_21[5]	EDID_21[4]	EDID_21[3]	EDID_21[2]	EDID_21[1]	EDID_21[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x16	0x00	EDIDMEMORY_REG_16	r	EDID_22[7]	EDID_22[6]	EDID_22[5]	EDID_22[4]	EDID_22[3]	EDID_22[2]	EDID_22[1]	EDID_22[0]
0x17	0x00	EDIDMEMORY_REG_17	r	EDID_23[7]	EDID_23[6]	EDID_23[5]	EDID_23[4]	EDID_23[3]	EDID_23[2]	EDID_23[1]	EDID_23[0]
0x18	0x00	EDIDMEMORY_REG_18	r	EDID_24[7]	EDID_24[6]	EDID_24[5]	EDID_24[4]	EDID_24[3]	EDID_24[2]	EDID_24[1]	EDID_24[0]
0x19	0x00	EDIDMEMORY_REG_19	r	EDID_25[7]	EDID_25[6]	EDID_25[5]	EDID_25[4]	EDID_25[3]	EDID_25[2]	EDID_25[1]	EDID_25[0]
0x1A	0x00	EDIDMEMORY_REG_1A	r	EDID_26[7]	EDID_26[6]	EDID_26[5]	EDID_26[4]	EDID_26[3]	EDID_26[2]	EDID_26[1]	EDID_26[0]
0x1B	0x00	EDIDMEMORY_REG_1B	r	EDID_27[7]	EDID_27[6]	EDID_27[5]	EDID_27[4]	EDID_27[3]	EDID_27[2]	EDID_27[1]	EDID_27[0]
0x1C	0x00	EDIDMEMORY_REG_1C	r	EDID_28[7]	EDID_28[6]	EDID_28[5]	EDID_28[4]	EDID_28[3]	EDID_28[2]	EDID_28[1]	EDID_28[0]
0x1D	0x00	EDIDMEMORY_REG_1D	r	EDID_29[7]	EDID_29[6]	EDID_29[5]	EDID_29[4]	EDID_29[3]	EDID_29[2]	EDID_29[1]	EDID_29[0]
0x1E	0x00	EDIDMEMORY_REG_1E	r	EDID_30[7]	EDID_30[6]	EDID_30[5]	EDID_30[4]	EDID_30[3]	EDID_30[2]	EDID_30[1]	EDID_30[0]
0x1F	0x00	EDIDMEMORY_REG_1F	r	EDID_31[7]	EDID_31[6]	EDID_31[5]	EDID_31[4]	EDID_31[3]	EDID_31[2]	EDID_31[1]	EDID_31[0]
0x20	0x00	EDIDMEMORY_REG_20	r	EDID_32[7]	EDID_32[6]	EDID_32[5]	EDID_32[4]	EDID_32[3]	EDID_32[2]	EDID_32[1]	EDID_32[0]
0x21	0x00	EDIDMEMORY_REG_21	r	EDID_33[7]	EDID_33[6]	EDID_33[5]	EDID_33[4]	EDID_33[3]	EDID_33[2]	EDID_33[1]	EDID_33[0]
0x22	0x00	EDIDMEMORY_REG_22	r	EDID_34[7]	EDID_34[6]	EDID_34[5]	EDID_34[4]	EDID_34[3]	EDID_34[2]	EDID_34[1]	EDID_34[0]
0x23	0x00	EDIDMEMORY_REG_23	r	EDID_35[7]	EDID_35[6]	EDID_35[5]	EDID_35[4]	EDID_35[3]	EDID_35[2]	EDID_35[1]	EDID_35[0]
0x24	0x00	EDIDMEMORY_REG_24	r	EDID_36[7]	EDID_36[6]	EDID_36[5]	EDID_36[4]	EDID_36[3]	EDID_36[2]	EDID_36[1]	EDID_36[0]
0x25	0x00	EDIDMEMORY_REG_25	r	EDID_37[7]	EDID_37[6]	EDID_37[5]	EDID_37[4]	EDID_37[3]	EDID_37[2]	EDID_37[1]	EDID_37[0]
0x26	0x00	EDIDMEMORY_REG_26	r	EDID_38[7]	EDID_38[6]	EDID_38[5]	EDID_38[4]	EDID_38[3]	EDID_38[2]	EDID_38[1]	EDID_38[0]
0x27	0x00	EDIDMEMORY_REG_27	r	EDID_39[7]	EDID_39[6]	EDID_39[5]	EDID_39[4]	EDID_39[3]	EDID_39[2]	EDID_39[1]	EDID_39[0]
0x28	0x00	EDIDMEMORY_REG_28	r	EDID_40[7]	EDID_40[6]	EDID_40[5]	EDID_40[4]	EDID_40[3]	EDID_40[2]	EDID_40[1]	EDID_40[0]
0x29	0x00	EDIDMEMORY_REG_29	r	EDID_41[7]	EDID_41[6]	EDID_41[5]	EDID_41[4]	EDID_41[3]	EDID_41[2]	EDID_41[1]	EDID_41[0]
0x2A	0x00	EDIDMEMORY_REG_2A	r	EDID_42[7]	EDID_42[6]	EDID_42[5]	EDID_42[4]	EDID_42[3]	EDID_42[2]	EDID_42[1]	EDID_42[0]
0x2B	0x00	EDIDMEMORY_REG_2B	r	EDID_43[7]	EDID_43[6]	EDID_43[5]	EDID_43[4]	EDID_43[3]	EDID_43[2]	EDID_43[1]	EDID_43[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x2C	0x00	EDIDMEMORY_REG_2C	r	EDID_44[7]	EDID_44[6]	EDID_44[5]	EDID_44[4]	EDID_44[3]	EDID_44[2]	EDID_44[1]	EDID_44[0]
0x2D	0x00	EDIDMEMORY_REG_2D	r	EDID_45[7]	EDID_45[6]	EDID_45[5]	EDID_45[4]	EDID_45[3]	EDID_45[2]	EDID_45[1]	EDID_45[0]
0x2E	0x00	EDIDMEMORY_REG_2E	r	EDID_46[7]	EDID_46[6]	EDID_46[5]	EDID_46[4]	EDID_46[3]	EDID_46[2]	EDID_46[1]	EDID_46[0]
0x2F	0x00	EDIDMEMORY_REG_2F	r	EDID_47[7]	EDID_47[6]	EDID_47[5]	EDID_47[4]	EDID_47[3]	EDID_47[2]	EDID_47[1]	EDID_47[0]
0x30	0x00	EDIDMEMORY_REG_30	r	EDID_48[7]	EDID_48[6]	EDID_48[5]	EDID_48[4]	EDID_48[3]	EDID_48[2]	EDID_48[1]	EDID_48[0]
0x31	0x00	EDIDMEMORY_REG_31	r	EDID_49[7]	EDID_49[6]	EDID_49[5]	EDID_49[4]	EDID_49[3]	EDID_49[2]	EDID_49[1]	EDID_49[0]
0x32	0x00	EDIDMEMORY_REG_32	r	EDID_50[7]	EDID_50[6]	EDID_50[5]	EDID_50[4]	EDID_50[3]	EDID_50[2]	EDID_50[1]	EDID_50[0]
0x33	0x00	EDIDMEMORY_REG_33	r	EDID_51[7]	EDID_51[6]	EDID_51[5]	EDID_51[4]	EDID_51[3]	EDID_51[2]	EDID_51[1]	EDID_51[0]
0x34	0x00	EDIDMEMORY_REG_34	r	EDID_52[7]	EDID_52[6]	EDID_52[5]	EDID_52[4]	EDID_52[3]	EDID_52[2]	EDID_52[1]	EDID_52[0]
0x35	0x00	EDIDMEMORY_REG_35	r	EDID_53[7]	EDID_53[6]	EDID_53[5]	EDID_53[4]	EDID_53[3]	EDID_53[2]	EDID_53[1]	EDID_53[0]
0x36	0x00	EDIDMEMORY_REG_36	r	EDID_54[7]	EDID_54[6]	EDID_54[5]	EDID_54[4]	EDID_54[3]	EDID_54[2]	EDID_54[1]	EDID_54[0]
0x37	0x00	EDIDMEMORY_REG_37	r	EDID_55[7]	EDID_55[6]	EDID_55[5]	EDID_55[4]	EDID_55[3]	EDID_55[2]	EDID_55[1]	EDID_55[0]
0x38	0x00	EDIDMEMORY_REG_38	r	EDID_56[7]	EDID_56[6]	EDID_56[5]	EDID_56[4]	EDID_56[3]	EDID_56[2]	EDID_56[1]	EDID_56[0]
0x39	0x00	EDIDMEMORY_REG_39	r	EDID_57[7]	EDID_57[6]	EDID_57[5]	EDID_57[4]	EDID_57[3]	EDID_57[2]	EDID_57[1]	EDID_57[0]
0x3A	0x00	EDIDMEMORY_REG_3A	r	EDID_58[7]	EDID_58[6]	EDID_58[5]	EDID_58[4]	EDID_58[3]	EDID_58[2]	EDID_58[1]	EDID_58[0]
0x3B	0x00	EDIDMEMORY_REG_3B	r	EDID_59[7]	EDID_59[6]	EDID_59[5]	EDID_59[4]	EDID_59[3]	EDID_59[2]	EDID_59[1]	EDID_59[0]
0x3C	0x00	EDIDMEMORY_REG_3C	r	EDID_60[7]	EDID_60[6]	EDID_60[5]	EDID_60[4]	EDID_60[3]	EDID_60[2]	EDID_60[1]	EDID_60[0]
0x3D	0x00	EDIDMEMORY_REG_3D	r	EDID_61[7]	EDID_61[6]	EDID_61[5]	EDID_61[4]	EDID_61[3]	EDID_61[2]	EDID_61[1]	EDID_61[0]
0x3E	0x00	EDIDMEMORY_REG_3E	r	EDID_62[7]	EDID_62[6]	EDID_62[5]	EDID_62[4]	EDID_62[3]	EDID_62[2]	EDID_62[1]	EDID_62[0]
0x3F	0x00	EDIDMEMORY_REG_3F	r	EDID_63[7]	EDID_63[6]	EDID_63[5]	EDID_63[4]	EDID_63[3]	EDID_63[2]	EDID_63[1]	EDID_63[0]
0x40	0x00	EDIDMEMORY_REG_40	r	EDID_64[7]	EDID_64[6]	EDID_64[5]	EDID_64[4]	EDID_64[3]	EDID_64[2]	EDID_64[1]	EDID_64[0]
0x41	0x00	EDIDMEMORY_REG_41	r	EDID_65[7]	EDID_65[6]	EDID_65[5]	EDID_65[4]	EDID_65[3]	EDID_65[2]	EDID_65[1]	EDID_65[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x42	0x00	EDIDMEMORY_REG_42	r	EDID_66[7]	EDID_66[6]	EDID_66[5]	EDID_66[4]	EDID_66[3]	EDID_66[2]	EDID_66[1]	EDID_66[0]
0x43	0x00	EDIDMEMORY_REG_43	r	EDID_67[7]	EDID_67[6]	EDID_67[5]	EDID_67[4]	EDID_67[3]	EDID_67[2]	EDID_67[1]	EDID_67[0]
0x44	0x00	EDIDMEMORY_REG_44	r	EDID_68[7]	EDID_68[6]	EDID_68[5]	EDID_68[4]	EDID_68[3]	EDID_68[2]	EDID_68[1]	EDID_68[0]
0x45	0x00	EDIDMEMORY_REG_45	r	EDID_69[7]	EDID_69[6]	EDID_69[5]	EDID_69[4]	EDID_69[3]	EDID_69[2]	EDID_69[1]	EDID_69[0]
0x46	0x00	EDIDMEMORY_REG_46	r	EDID_70[7]	EDID_70[6]	EDID_70[5]	EDID_70[4]	EDID_70[3]	EDID_70[2]	EDID_70[1]	EDID_70[0]
0x47	0x00	EDIDMEMORY_REG_47	r	EDID_71[7]	EDID_71[6]	EDID_71[5]	EDID_71[4]	EDID_71[3]	EDID_71[2]	EDID_71[1]	EDID_71[0]
0x48	0x00	EDIDMEMORY_REG_48	r	EDID_72[7]	EDID_72[6]	EDID_72[5]	EDID_72[4]	EDID_72[3]	EDID_72[2]	EDID_72[1]	EDID_72[0]
0x49	0x00	EDIDMEMORY_REG_49	r	EDID_73[7]	EDID_73[6]	EDID_73[5]	EDID_73[4]	EDID_73[3]	EDID_73[2]	EDID_73[1]	EDID_73[0]
0x4A	0x00	EDIDMEMORY_REG_4A	r	EDID_74[7]	EDID_74[6]	EDID_74[5]	EDID_74[4]	EDID_74[3]	EDID_74[2]	EDID_74[1]	EDID_74[0]
0x4B	0x00	EDIDMEMORY_REG_4B	r	EDID_75[7]	EDID_75[6]	EDID_75[5]	EDID_75[4]	EDID_75[3]	EDID_75[2]	EDID_75[1]	EDID_75[0]
0x4C	0x00	EDIDMEMORY_REG_4C	r	EDID_76[7]	EDID_76[6]	EDID_76[5]	EDID_76[4]	EDID_76[3]	EDID_76[2]	EDID_76[1]	EDID_76[0]
0x4D	0x00	EDIDMEMORY_REG_4D	r	EDID_77[7]	EDID_77[6]	EDID_77[5]	EDID_77[4]	EDID_77[3]	EDID_77[2]	EDID_77[1]	EDID_77[0]
0x4E	0x00	EDIDMEMORY_REG_4E	r	EDID_78[7]	EDID_78[6]	EDID_78[5]	EDID_78[4]	EDID_78[3]	EDID_78[2]	EDID_78[1]	EDID_78[0]
0x4F	0x00	EDIDMEMORY_REG_4F	r	EDID_79[7]	EDID_79[6]	EDID_79[5]	EDID_79[4]	EDID_79[3]	EDID_79[2]	EDID_79[1]	EDID_79[0]
0x50	0x00	EDIDMEMORY_REG_50	r	EDID_80[7]	EDID_80[6]	EDID_80[5]	EDID_80[4]	EDID_80[3]	EDID_80[2]	EDID_80[1]	EDID_80[0]
0x51	0x00	EDIDMEMORY_REG_51	r	EDID_81[7]	EDID_81[6]	EDID_81[5]	EDID_81[4]	EDID_81[3]	EDID_81[2]	EDID_81[1]	EDID_81[0]
0x52	0x00	EDIDMEMORY_REG_52	r	EDID_82[7]	EDID_82[6]	EDID_82[5]	EDID_82[4]	EDID_82[3]	EDID_82[2]	EDID_82[1]	EDID_82[0]
0x53	0x00	EDIDMEMORY_REG_53	r	EDID_83[7]	EDID_83[6]	EDID_83[5]	EDID_83[4]	EDID_83[3]	EDID_83[2]	EDID_83[1]	EDID_83[0]
0x54	0x00	EDIDMEMORY_REG_54	r	EDID_84[7]	EDID_84[6]	EDID_84[5]	EDID_84[4]	EDID_84[3]	EDID_84[2]	EDID_84[1]	EDID_84[0]
0x55	0x00	EDIDMEMORY_REG_55	r	EDID_85[7]	EDID_85[6]	EDID_85[5]	EDID_85[4]	EDID_85[3]	EDID_85[2]	EDID_85[1]	EDID_85[0]
0x56	0x00	EDIDMEMORY_REG_56	r	EDID_86[7]	EDID_86[6]	EDID_86[5]	EDID_86[4]	EDID_86[3]	EDID_86[2]	EDID_86[1]	EDID_86[0]
0x57	0x00	EDIDMEMORY_REG_57	r	EDID_87[7]	EDID_87[6]	EDID_87[5]	EDID_87[4]	EDID_87[3]	EDID_87[2]	EDID_87[1]	EDID_87[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x58	0x00	EDIDMEMORY_REG_58	r	EDID_88[7]	EDID_88[6]	EDID_88[5]	EDID_88[4]	EDID_88[3]	EDID_88[2]	EDID_88[1]	EDID_88[0]
0x59	0x00	EDIDMEMORY_REG_59	r	EDID_89[7]	EDID_89[6]	EDID_89[5]	EDID_89[4]	EDID_89[3]	EDID_89[2]	EDID_89[1]	EDID_89[0]
0x5A	0x00	EDIDMEMORY_REG_5A	r	EDID_90[7]	EDID_90[6]	EDID_90[5]	EDID_90[4]	EDID_90[3]	EDID_90[2]	EDID_90[1]	EDID_90[0]
0x5B	0x00	EDIDMEMORY_REG_5B	r	EDID_91[7]	EDID_91[6]	EDID_91[5]	EDID_91[4]	EDID_91[3]	EDID_91[2]	EDID_91[1]	EDID_91[0]
0x5C	0x00	EDIDMEMORY_REG_5C	r	EDID_92[7]	EDID_92[6]	EDID_92[5]	EDID_92[4]	EDID_92[3]	EDID_92[2]	EDID_92[1]	EDID_92[0]
0x5D	0x00	EDIDMEMORY_REG_5D	r	EDID_93[7]	EDID_93[6]	EDID_93[5]	EDID_93[4]	EDID_93[3]	EDID_93[2]	EDID_93[1]	EDID_93[0]
0x5E	0x00	EDIDMEMORY_REG_5E	r	EDID_94[7]	EDID_94[6]	EDID_94[5]	EDID_94[4]	EDID_94[3]	EDID_94[2]	EDID_94[1]	EDID_94[0]
0x5F	0x00	EDIDMEMORY_REG_5F	r	EDID_95[7]	EDID_95[6]	EDID_95[5]	EDID_95[4]	EDID_95[3]	EDID_95[2]	EDID_95[1]	EDID_95[0]
0x60	0x00	EDIDMEMORY_REG_60	r	EDID_96[7]	EDID_96[6]	EDID_96[5]	EDID_96[4]	EDID_96[3]	EDID_96[2]	EDID_96[1]	EDID_96[0]
0x61	0x00	EDIDMEMORY_REG_61	r	EDID_97[7]	EDID_97[6]	EDID_97[5]	EDID_97[4]	EDID_97[3]	EDID_97[2]	EDID_97[1]	EDID_97[0]
0x62	0x00	EDIDMEMORY_REG_62	r	EDID_98[7]	EDID_98[6]	EDID_98[5]	EDID_98[4]	EDID_98[3]	EDID_98[2]	EDID_98[1]	EDID_98[0]
0x63	0x00	EDIDMEMORY_REG_63	r	EDID_99[7]	EDID_99[6]	EDID_99[5]	EDID_99[4]	EDID_99[3]	EDID_99[2]	EDID_99[1]	EDID_99[0]
0x64	0x00	EDIDMEMORY_REG_64	r	EDID_100[7]	EDID_100[6]	EDID_100[5]	EDID_100[4]	EDID_100[3]	EDID_100[2]	EDID_100[1]	EDID_100[0]
0x65	0x00	EDIDMEMORY_REG_65	r	EDID_101[7]	EDID_101[6]	EDID_101[5]	EDID_101[4]	EDID_101[3]	EDID_101[2]	EDID_101[1]	EDID_101[0]
0x66	0x00	EDIDMEMORY_REG_66	r	EDID_102[7]	EDID_102[6]	EDID_102[5]	EDID_102[4]	EDID_102[3]	EDID_102[2]	EDID_102[1]	EDID_102[0]
0x67	0x00	EDIDMEMORY_REG_67	r	EDID_103[7]	EDID_103[6]	EDID_103[5]	EDID_103[4]	EDID_103[3]	EDID_103[2]	EDID_103[1]	EDID_103[0]
0x68	0x00	EDIDMEMORY_REG_68	r	EDID_104[7]	EDID_104[6]	EDID_104[5]	EDID_104[4]	EDID_104[3]	EDID_104[2]	EDID_104[1]	EDID_104[0]
0x69	0x00	EDIDMEMORY_REG_69	r	EDID_105[7]	EDID_105[6]	EDID_105[5]	EDID_105[4]	EDID_105[3]	EDID_105[2]	EDID_105[1]	EDID_105[0]
0x6A	0x00	EDIDMEMORY_REG_6A	r	EDID_106[7]	EDID_106[6]	EDID_106[5]	EDID_106[4]	EDID_106[3]	EDID_106[2]	EDID_106[1]	EDID_106[0]
0x6B	0x00	EDIDMEMORY_REG_6B	r	EDID_107[7]	EDID_107[6]	EDID_107[5]	EDID_107[4]	EDID_107[3]	EDID_107[2]	EDID_107[1]	EDID_107[0]
0x6C	0x00	EDIDMEMORY_REG_6C	r	EDID_108[7]	EDID_108[6]	EDID_108[5]	EDID_108[4]	EDID_108[3]	EDID_108[2]	EDID_108[1]	EDID_108[0]
0x6D	0x00	EDIDMEMORY_REG_6D	r	EDID_109[7]	EDID_109[6]	EDID_109[5]	EDID_109[4]	EDID_109[3]	EDID_109[2]	EDID_109[1]	EDID_109[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x6E	0x00	EDIDMEMORY_REG_6E	r	EDID_110[7]	EDID_110[6]	EDID_110[5]	EDID_110[4]	EDID_110[3]	EDID_110[2]	EDID_110[1]	EDID_110[0]
0x6F	0x00	EDIDMEMORY_REG_6F	r	EDID_111[7]	EDID_111[6]	EDID_111[5]	EDID_111[4]	EDID_111[3]	EDID_111[2]	EDID_111[1]	EDID_111[0]
0x70	0x00	EDIDMEMORY_REG_70	r	EDID_112[7]	EDID_112[6]	EDID_112[5]	EDID_112[4]	EDID_112[3]	EDID_112[2]	EDID_112[1]	EDID_112[0]
0x71	0x00	EDIDMEMORY_REG_71	r	EDID_113[7]	EDID_113[6]	EDID_113[5]	EDID_113[4]	EDID_113[3]	EDID_113[2]	EDID_113[1]	EDID_113[0]
0x72	0x00	EDIDMEMORY_REG_72	r	EDID_114[7]	EDID_114[6]	EDID_114[5]	EDID_114[4]	EDID_114[3]	EDID_114[2]	EDID_114[1]	EDID_114[0]
0x73	0x00	EDIDMEMORY_REG_73	r	EDID_115[7]	EDID_115[6]	EDID_115[5]	EDID_115[4]	EDID_115[3]	EDID_115[2]	EDID_115[1]	EDID_115[0]
0x74	0x00	EDIDMEMORY_REG_74	r	EDID_116[7]	EDID_116[6]	EDID_116[5]	EDID_116[4]	EDID_116[3]	EDID_116[2]	EDID_116[1]	EDID_116[0]
0x75	0x00	EDIDMEMORY_REG_75	r	EDID_117[7]	EDID_117[6]	EDID_117[5]	EDID_117[4]	EDID_117[3]	EDID_117[2]	EDID_117[1]	EDID_117[0]
0x76	0x00	EDIDMEMORY_REG_76	r	EDID_118[7]	EDID_118[6]	EDID_118[5]	EDID_118[4]	EDID_118[3]	EDID_118[2]	EDID_118[1]	EDID_118[0]
0x77	0x00	EDIDMEMORY_REG_77	r	EDID_119[7]	EDID_119[6]	EDID_119[5]	EDID_119[4]	EDID_119[3]	EDID_119[2]	EDID_119[1]	EDID_119[0]
0x78	0x00	EDIDMEMORY_REG_78	r	EDID_120[7]	EDID_120[6]	EDID_120[5]	EDID_120[4]	EDID_120[3]	EDID_120[2]	EDID_120[1]	EDID_120[0]
0x79	0x00	EDIDMEMORY_REG_79	r	EDID_121[7]	EDID_121[6]	EDID_121[5]	EDID_121[4]	EDID_121[3]	EDID_121[2]	EDID_121[1]	EDID_121[0]
0x7A	0x00	EDIDMEMORY_REG_7A	r	EDID_122[7]	EDID_122[6]	EDID_122[5]	EDID_122[4]	EDID_122[3]	EDID_122[2]	EDID_122[1]	EDID_122[0]
0x7B	0x00	EDIDMEMORY_REG_7B	r	EDID_123[7]	EDID_123[6]	EDID_123[5]	EDID_123[4]	EDID_123[3]	EDID_123[2]	EDID_123[1]	EDID_123[0]
0x7C	0x00	EDIDMEMORY_REG_7C	r	EDID_124[7]	EDID_124[6]	EDID_124[5]	EDID_124[4]	EDID_124[3]	EDID_124[2]	EDID_124[1]	EDID_124[0]
0x7D	0x00	EDIDMEMORY_REG_7D	r	EDID_125[7]	EDID_125[6]	EDID_125[5]	EDID_125[4]	EDID_125[3]	EDID_125[2]	EDID_125[1]	EDID_125[0]
0x7E	0x00	EDIDMEMORY_REG_7E	r	EDID_126[7]	EDID_126[6]	EDID_126[5]	EDID_126[4]	EDID_126[3]	EDID_126[2]	EDID_126[1]	EDID_126[0]
0x7F	0x00	EDIDMEMORY_REG_7F	r	EDID_127[7]	EDID_127[6]	EDID_127[5]	EDID_127[4]	EDID_127[3]	EDID_127[2]	EDID_127[1]	EDID_127[0]
0x80	0x00	EDIDMEMORY_REG_80	r	EDID_128[7]	EDID_128[6]	EDID_128[5]	EDID_128[4]	EDID_128[3]	EDID_128[2]	EDID_128[1]	EDID_128[0]
0x81	0x00	EDIDMEMORY_REG_81	r	EDID_129[7]	EDID_129[6]	EDID_129[5]	EDID_129[4]	EDID_129[3]	EDID_129[2]	EDID_129[1]	EDID_129[0]
0x82	0x00	EDIDMEMORY_REG_82	r	EDID_130[7]	EDID_130[6]	EDID_130[5]	EDID_130[4]	EDID_130[3]	EDID_130[2]	EDID_130[1]	EDID_130[0]
0x83	0x00	EDIDMEMORY_REG_83	r	EDID_131[7]	EDID_131[6]	EDID_131[5]	EDID_131[4]	EDID_131[3]	EDID_131[2]	EDID_131[1]	EDID_131[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x84	0x00	EDIDMEMORY_REG_84	r	EDID_132[7]	EDID_132[6]	EDID_132[5]	EDID_132[4]	EDID_132[3]	EDID_132[2]	EDID_132[1]	EDID_132[0]
0x85	0x00	EDIDMEMORY_REG_85	r	EDID_133[7]	EDID_133[6]	EDID_133[5]	EDID_133[4]	EDID_133[3]	EDID_133[2]	EDID_133[1]	EDID_133[0]
0x86	0x00	EDIDMEMORY_REG_86	r	EDID_134[7]	EDID_134[6]	EDID_134[5]	EDID_134[4]	EDID_134[3]	EDID_134[2]	EDID_134[1]	EDID_134[0]
0x87	0x00	EDIDMEMORY_REG_87	r	EDID_135[7]	EDID_135[6]	EDID_135[5]	EDID_135[4]	EDID_135[3]	EDID_135[2]	EDID_135[1]	EDID_135[0]
0x88	0x00	EDIDMEMORY_REG_88	r	EDID_136[7]	EDID_136[6]	EDID_136[5]	EDID_136[4]	EDID_136[3]	EDID_136[2]	EDID_136[1]	EDID_136[0]
0x89	0x00	EDIDMEMORY_REG_89	r	EDID_137[7]	EDID_137[6]	EDID_137[5]	EDID_137[4]	EDID_137[3]	EDID_137[2]	EDID_137[1]	EDID_137[0]
0x8A	0x00	EDIDMEMORY_REG_8A	r	EDID_138[7]	EDID_138[6]	EDID_138[5]	EDID_138[4]	EDID_138[3]	EDID_138[2]	EDID_138[1]	EDID_138[0]
0x8B	0x00	EDIDMEMORY_REG_8B	r	EDID_139[7]	EDID_139[6]	EDID_139[5]	EDID_139[4]	EDID_139[3]	EDID_139[2]	EDID_139[1]	EDID_139[0]
0x8C	0x00	EDIDMEMORY_REG_8C	r	EDID_140[7]	EDID_140[6]	EDID_140[5]	EDID_140[4]	EDID_140[3]	EDID_140[2]	EDID_140[1]	EDID_140[0]
0x8D	0x00	EDIDMEMORY_REG_8D	r	EDID_141[7]	EDID_141[6]	EDID_141[5]	EDID_141[4]	EDID_141[3]	EDID_141[2]	EDID_141[1]	EDID_141[0]
0x8E	0x00	EDIDMEMORY_REG_8E	r	EDID_142[7]	EDID_142[6]	EDID_142[5]	EDID_142[4]	EDID_142[3]	EDID_142[2]	EDID_142[1]	EDID_142[0]
0x8F	0x00	EDIDMEMORY_REG_8F	r	EDID_143[7]	EDID_143[6]	EDID_143[5]	EDID_143[4]	EDID_143[3]	EDID_143[2]	EDID_143[1]	EDID_143[0]
0x90	0x00	EDIDMEMORY_REG_90	r	EDID_144[7]	EDID_144[6]	EDID_144[5]	EDID_144[4]	EDID_144[3]	EDID_144[2]	EDID_144[1]	EDID_144[0]
0x91	0x00	EDIDMEMORY_REG_91	r	EDID_145[7]	EDID_145[6]	EDID_145[5]	EDID_145[4]	EDID_145[3]	EDID_145[2]	EDID_145[1]	EDID_145[0]
0x92	0x00	EDIDMEMORY_REG_92	r	EDID_146[7]	EDID_146[6]	EDID_146[5]	EDID_146[4]	EDID_146[3]	EDID_146[2]	EDID_146[1]	EDID_146[0]
0x93	0x00	EDIDMEMORY_REG_93	r	EDID_147[7]	EDID_147[6]	EDID_147[5]	EDID_147[4]	EDID_147[3]	EDID_147[2]	EDID_147[1]	EDID_147[0]
0x94	0x00	EDIDMEMORY_REG_94	r	EDID_148[7]	EDID_148[6]	EDID_148[5]	EDID_148[4]	EDID_148[3]	EDID_148[2]	EDID_148[1]	EDID_148[0]
0x95	0x00	EDIDMEMORY_REG_95	r	EDID_149[7]	EDID_149[6]	EDID_149[5]	EDID_149[4]	EDID_149[3]	EDID_149[2]	EDID_149[1]	EDID_149[0]
0x96	0x00	EDIDMEMORY_REG_96	r	EDID_150[7]	EDID_150[6]	EDID_150[5]	EDID_150[4]	EDID_150[3]	EDID_150[2]	EDID_150[1]	EDID_150[0]
0x97	0x00	EDIDMEMORY_REG_97	r	EDID_151[7]	EDID_151[6]	EDID_151[5]	EDID_151[4]	EDID_151[3]	EDID_151[2]	EDID_151[1]	EDID_151[0]
0x98	0x00	EDIDMEMORY_REG_98	r	EDID_152[7]	EDID_152[6]	EDID_152[5]	EDID_152[4]	EDID_152[3]	EDID_152[2]	EDID_152[1]	EDID_152[0]
0x99	0x00	EDIDMEMORY_REG_99	r	EDID_153[7]	EDID_153[6]	EDID_153[5]	EDID_153[4]	EDID_153[3]	EDID_153[2]	EDID_153[1]	EDID_153[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0x9A	0x00	EDIDMEMORY_REG_9A	r	EDID_154[7]	EDID_154[6]	EDID_154[5]	EDID_154[4]	EDID_154[3]	EDID_154[2]	EDID_154[1]	EDID_154[0]
0x9B	0x00	EDIDMEMORY_REG_9B	r	EDID_155[7]	EDID_155[6]	EDID_155[5]	EDID_155[4]	EDID_155[3]	EDID_155[2]	EDID_155[1]	EDID_155[0]
0x9C	0x00	EDIDMEMORY_REG_9C	r	EDID_156[7]	EDID_156[6]	EDID_156[5]	EDID_156[4]	EDID_156[3]	EDID_156[2]	EDID_156[1]	EDID_156[0]
0x9D	0x00	EDIDMEMORY_REG_9D	r	EDID_157[7]	EDID_157[6]	EDID_157[5]	EDID_157[4]	EDID_157[3]	EDID_157[2]	EDID_157[1]	EDID_157[0]
0x9E	0x00	EDIDMEMORY_REG_9E	r	EDID_158[7]	EDID_158[6]	EDID_158[5]	EDID_158[4]	EDID_158[3]	EDID_158[2]	EDID_158[1]	EDID_158[0]
0x9F	0x00	EDIDMEMORY_REG_9F	r	EDID_159[7]	EDID_159[6]	EDID_159[5]	EDID_159[4]	EDID_159[3]	EDID_159[2]	EDID_159[1]	EDID_159[0]
0xA0	0x00	EDIDMEMORY_REG_A0	r	EDID_160[7]	EDID_160[6]	EDID_160[5]	EDID_160[4]	EDID_160[3]	EDID_160[2]	EDID_160[1]	EDID_160[0]
0xA1	0x00	EDIDMEMORY_REG_A1	r	EDID_161[7]	EDID_161[6]	EDID_161[5]	EDID_161[4]	EDID_161[3]	EDID_161[2]	EDID_161[1]	EDID_161[0]
0xA2	0x00	EDIDMEMORY_REG_A2	r	EDID_162[7]	EDID_162[6]	EDID_162[5]	EDID_162[4]	EDID_162[3]	EDID_162[2]	EDID_162[1]	EDID_162[0]
0xA3	0x00	EDIDMEMORY_REG_A3	r	EDID_163[7]	EDID_163[6]	EDID_163[5]	EDID_163[4]	EDID_163[3]	EDID_163[2]	EDID_163[1]	EDID_163[0]
0xA4	0x00	EDIDMEMORY_REG_A4	r	EDID_164[7]	EDID_164[6]	EDID_164[5]	EDID_164[4]	EDID_164[3]	EDID_164[2]	EDID_164[1]	EDID_164[0]
0xA5	0x00	EDIDMEMORY_REG_A5	r	EDID_165[7]	EDID_165[6]	EDID_165[5]	EDID_165[4]	EDID_165[3]	EDID_165[2]	EDID_165[1]	EDID_165[0]
0xA6	0x00	EDIDMEMORY_REG_A6	r	EDID_166[7]	EDID_166[6]	EDID_166[5]	EDID_166[4]	EDID_166[3]	EDID_166[2]	EDID_166[1]	EDID_166[0]
0xA7	0x00	EDIDMEMORY_REG_A7	r	EDID_167[7]	EDID_167[6]	EDID_167[5]	EDID_167[4]	EDID_167[3]	EDID_167[2]	EDID_167[1]	EDID_167[0]
0xA8	0x00	EDIDMEMORY_REG_A8	r	EDID_168[7]	EDID_168[6]	EDID_168[5]	EDID_168[4]	EDID_168[3]	EDID_168[2]	EDID_168[1]	EDID_168[0]
0xA9	0x00	EDIDMEMORY_REG_A9	r	EDID_169[7]	EDID_169[6]	EDID_169[5]	EDID_169[4]	EDID_169[3]	EDID_169[2]	EDID_169[1]	EDID_169[0]
0xAA	0x00	EDIDMEMORY_REG_AA	r	EDID_170[7]	EDID_170[6]	EDID_170[5]	EDID_170[4]	EDID_170[3]	EDID_170[2]	EDID_170[1]	EDID_170[0]
0xAB	0x00	EDIDMEMORY_REG_AB	r	EDID_171[7]	EDID_171[6]	EDID_171[5]	EDID_171[4]	EDID_171[3]	EDID_171[2]	EDID_171[1]	EDID_171[0]
0xAC	0x00	EDIDMEMORY_REG_AC	r	EDID_172[7]	EDID_172[6]	EDID_172[5]	EDID_172[4]	EDID_172[3]	EDID_172[2]	EDID_172[1]	EDID_172[0]
0xAD	0x00	EDIDMEMORY_REG_AD	r	EDID_173[7]	EDID_173[6]	EDID_173[5]	EDID_173[4]	EDID_173[3]	EDID_173[2]	EDID_173[1]	EDID_173[0]
0xAE	0x00	EDIDMEMORY_REG_AE	r	EDID_174[7]	EDID_174[6]	EDID_174[5]	EDID_174[4]	EDID_174[3]	EDID_174[2]	EDID_174[1]	EDID_174[0]
0xAF	0x00	EDIDMEMORY_REG_AF	r	EDID_175[7]	EDID_175[6]	EDID_175[5]	EDID_175[4]	EDID_175[3]	EDID_175[2]	EDID_175[1]	EDID_175[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xB0	0x00	EDIDMEMORY_REG_B0	r	EDID_176[7]	EDID_176[6]	EDID_176[5]	EDID_176[4]	EDID_176[3]	EDID_176[2]	EDID_176[1]	EDID_176[0]
0xB1	0x00	EDIDMEMORY_REG_B1	r	EDID_177[7]	EDID_177[6]	EDID_177[5]	EDID_177[4]	EDID_177[3]	EDID_177[2]	EDID_177[1]	EDID_177[0]
0xB2	0x00	EDIDMEMORY_REG_B2	r	EDID_178[7]	EDID_178[6]	EDID_178[5]	EDID_178[4]	EDID_178[3]	EDID_178[2]	EDID_178[1]	EDID_178[0]
0xB3	0x00	EDIDMEMORY_REG_B3	r	EDID_179[7]	EDID_179[6]	EDID_179[5]	EDID_179[4]	EDID_179[3]	EDID_179[2]	EDID_179[1]	EDID_179[0]
0xB4	0x00	EDIDMEMORY_REG_B4	r	EDID_180[7]	EDID_180[6]	EDID_180[5]	EDID_180[4]	EDID_180[3]	EDID_180[2]	EDID_180[1]	EDID_180[0]
0xB5	0x00	EDIDMEMORY_REG_B5	r	EDID_181[7]	EDID_181[6]	EDID_181[5]	EDID_181[4]	EDID_181[3]	EDID_181[2]	EDID_181[1]	EDID_181[0]
0xB6	0x00	EDIDMEMORY_REG_B6	r	EDID_182[7]	EDID_182[6]	EDID_182[5]	EDID_182[4]	EDID_182[3]	EDID_182[2]	EDID_182[1]	EDID_182[0]
0xB7	0x00	EDIDMEMORY_REG_B7	r	EDID_183[7]	EDID_183[6]	EDID_183[5]	EDID_183[4]	EDID_183[3]	EDID_183[2]	EDID_183[1]	EDID_183[0]
0xB8	0x00	EDIDMEMORY_REG_B8	r	EDID_184[7]	EDID_184[6]	EDID_184[5]	EDID_184[4]	EDID_184[3]	EDID_184[2]	EDID_184[1]	EDID_184[0]
0xB9	0x00	EDIDMEMORY_REG_B9	r	EDID_185[7]	EDID_185[6]	EDID_185[5]	EDID_185[4]	EDID_185[3]	EDID_185[2]	EDID_185[1]	EDID_185[0]
0xBA	0x00	EDIDMEMORY_REG_BA	r	EDID_186[7]	EDID_186[6]	EDID_186[5]	EDID_186[4]	EDID_186[3]	EDID_186[2]	EDID_186[1]	EDID_186[0]
0xBB	0x00	EDIDMEMORY_REG_BB	r	EDID_187[7]	EDID_187[6]	EDID_187[5]	EDID_187[4]	EDID_187[3]	EDID_187[2]	EDID_187[1]	EDID_187[0]
0xBC	0x00	EDIDMEMORY_REG_BC	r	EDID_188[7]	EDID_188[6]	EDID_188[5]	EDID_188[4]	EDID_188[3]	EDID_188[2]	EDID_188[1]	EDID_188[0]
0xBD	0x00	EDIDMEMORY_REG_BD	r	EDID_189[7]	EDID_189[6]	EDID_189[5]	EDID_189[4]	EDID_189[3]	EDID_189[2]	EDID_189[1]	EDID_189[0]
0xBE	0x00	EDIDMEMORY_REG_BE	r	EDID_190[7]	EDID_190[6]	EDID_190[5]	EDID_190[4]	EDID_190[3]	EDID_190[2]	EDID_190[1]	EDID_190[0]
0xBF	0x00	EDIDMEMORY_REG_BF	r	EDID_191[7]	EDID_191[6]	EDID_191[5]	EDID_191[4]	EDID_191[3]	EDID_191[2]	EDID_191[1]	EDID_191[0]
0xC0	0x00	EDIDMEMORY_REG_C0	r	EDID_192[7]	EDID_192[6]	EDID_192[5]	EDID_192[4]	EDID_192[3]	EDID_192[2]	EDID_192[1]	EDID_192[0]
0xC1	0x00	EDIDMEMORY_REG_C1	r	EDID_193[7]	EDID_193[6]	EDID_193[5]	EDID_193[4]	EDID_193[3]	EDID_193[2]	EDID_193[1]	EDID_193[0]
0xC2	0x00	EDIDMEMORY_REG_C2	r	EDID_194[7]	EDID_194[6]	EDID_194[5]	EDID_194[4]	EDID_194[3]	EDID_194[2]	EDID_194[1]	EDID_194[0]
0xC3	0x00	EDIDMEMORY_REG_C3	r	EDID_195[7]	EDID_195[6]	EDID_195[5]	EDID_195[4]	EDID_195[3]	EDID_195[2]	EDID_195[1]	EDID_195[0]
0xC4	0x00	EDIDMEMORY_REG_C4	r	EDID_196[7]	EDID_196[6]	EDID_196[5]	EDID_196[4]	EDID_196[3]	EDID_196[2]	EDID_196[1]	EDID_196[0]
0xC5	0x00	EDIDMEMORY_REG_C5	r	EDID_197[7]	EDID_197[6]	EDID_197[5]	EDID_197[4]	EDID_197[3]	EDID_197[2]	EDID_197[1]	EDID_197[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xC6	0x00	EDIDMEMORY_REG_C6	r	EDID_198[7]	EDID_198[6]	EDID_198[5]	EDID_198[4]	EDID_198[3]	EDID_198[2]	EDID_198[1]	EDID_198[0]
0xC7	0x00	EDIDMEMORY_REG_C7	r	EDID_199[7]	EDID_199[6]	EDID_199[5]	EDID_199[4]	EDID_199[3]	EDID_199[2]	EDID_199[1]	EDID_199[0]
0xC8	0x00	EDIDMEMORY_REG_C8	r	EDID_200[7]	EDID_200[6]	EDID_200[5]	EDID_200[4]	EDID_200[3]	EDID_200[2]	EDID_200[1]	EDID_200[0]
0xC9	0x00	EDIDMEMORY_REG_C9	r	EDID_201[7]	EDID_201[6]	EDID_201[5]	EDID_201[4]	EDID_201[3]	EDID_201[2]	EDID_201[1]	EDID_201[0]
0xCA	0x00	EDIDMEMORY_REG_CA	r	EDID_202[7]	EDID_202[6]	EDID_202[5]	EDID_202[4]	EDID_202[3]	EDID_202[2]	EDID_202[1]	EDID_202[0]
0xCB	0x00	EDIDMEMORY_REG_CB	r	EDID_203[7]	EDID_203[6]	EDID_203[5]	EDID_203[4]	EDID_203[3]	EDID_203[2]	EDID_203[1]	EDID_203[0]
0xCC	0x00	EDIDMEMORY_REG_CC	r	EDID_204[7]	EDID_204[6]	EDID_204[5]	EDID_204[4]	EDID_204[3]	EDID_204[2]	EDID_204[1]	EDID_204[0]
0xCD	0x00	EDIDMEMORY_REG_CD	r	EDID_205[7]	EDID_205[6]	EDID_205[5]	EDID_205[4]	EDID_205[3]	EDID_205[2]	EDID_205[1]	EDID_205[0]
0xCE	0x00	EDIDMEMORY_REG_CE	r	EDID_206[7]	EDID_206[6]	EDID_206[5]	EDID_206[4]	EDID_206[3]	EDID_206[2]	EDID_206[1]	EDID_206[0]
0xCF	0x00	EDIDMEMORY_REG_CF	r	EDID_207[7]	EDID_207[6]	EDID_207[5]	EDID_207[4]	EDID_207[3]	EDID_207[2]	EDID_207[1]	EDID_207[0]
0xD0	0x00	EDIDMEMORY_REG_D0	r	EDID_208[7]	EDID_208[6]	EDID_208[5]	EDID_208[4]	EDID_208[3]	EDID_208[2]	EDID_208[1]	EDID_208[0]
0xD1	0x00	EDIDMEMORY_REG_D1	r	EDID_209[7]	EDID_209[6]	EDID_209[5]	EDID_209[4]	EDID_209[3]	EDID_209[2]	EDID_209[1]	EDID_209[0]
0xD2	0x00	EDIDMEMORY_REG_D2	r	EDID_210[7]	EDID_210[6]	EDID_210[5]	EDID_210[4]	EDID_210[3]	EDID_210[2]	EDID_210[1]	EDID_210[0]
0xD3	0x00	EDIDMEMORY_REG_D3	r	EDID_211[7]	EDID_211[6]	EDID_211[5]	EDID_211[4]	EDID_211[3]	EDID_211[2]	EDID_211[1]	EDID_211[0]
0xD4	0x00	EDIDMEMORY_REG_D4	r	EDID_212[7]	EDID_212[6]	EDID_212[5]	EDID_212[4]	EDID_212[3]	EDID_212[2]	EDID_212[1]	EDID_212[0]
0xD5	0x00	EDIDMEMORY_REG_D5	r	EDID_213[7]	EDID_213[6]	EDID_213[5]	EDID_213[4]	EDID_213[3]	EDID_213[2]	EDID_213[1]	EDID_213[0]
0xD6	0x00	EDIDMEMORY_REG_D6	r	EDID_214[7]	EDID_214[6]	EDID_214[5]	EDID_214[4]	EDID_214[3]	EDID_214[2]	EDID_214[1]	EDID_214[0]
0xD7	0x00	EDIDMEMORY_REG_D7	r	EDID_215[7]	EDID_215[6]	EDID_215[5]	EDID_215[4]	EDID_215[3]	EDID_215[2]	EDID_215[1]	EDID_215[0]
0xD8	0x00	EDIDMEMORY_REG_D8	r	EDID_216[7]	EDID_216[6]	EDID_216[5]	EDID_216[4]	EDID_216[3]	EDID_216[2]	EDID_216[1]	EDID_216[0]
0xD9	0x00	EDIDMEMORY_REG_D9	r	EDID_217[7]	EDID_217[6]	EDID_217[5]	EDID_217[4]	EDID_217[3]	EDID_217[2]	EDID_217[1]	EDID_217[0]
0xDA	0x00	EDIDMEMORY_REG_DA	r	EDID_218[7]	EDID_218[6]	EDID_218[5]	EDID_218[4]	EDID_218[3]	EDID_218[2]	EDID_218[1]	EDID_218[0]
0xDB	0x00	EDIDMEMORY_REG_DB	r	EDID_219[7]	EDID_219[6]	EDID_219[5]	EDID_219[4]	EDID_219[3]	EDID_219[2]	EDID_219[1]	EDID_219[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xDC	0x00	EDIDMEMORY_REG_DC	r	EDID_220[7]	EDID_220[6]	EDID_220[5]	EDID_220[4]	EDID_220[3]	EDID_220[2]	EDID_220[1]	EDID_220[0]
0xDD	0x00	EDIDMEMORY_REG_DD	r	EDID_221[7]	EDID_221[6]	EDID_221[5]	EDID_221[4]	EDID_221[3]	EDID_221[2]	EDID_221[1]	EDID_221[0]
0xDE	0x00	EDIDMEMORY_REG_DE	r	EDID_222[7]	EDID_222[6]	EDID_222[5]	EDID_222[4]	EDID_222[3]	EDID_222[2]	EDID_222[1]	EDID_222[0]
0xDF	0x00	EDIDMEMORY_REG_DF	r	EDID_223[7]	EDID_223[6]	EDID_223[5]	EDID_223[4]	EDID_223[3]	EDID_223[2]	EDID_223[1]	EDID_223[0]
0xE0	0x00	EDIDMEMORY_REG_E0	r	EDID_224[7]	EDID_224[6]	EDID_224[5]	EDID_224[4]	EDID_224[3]	EDID_224[2]	EDID_224[1]	EDID_224[0]
0xE1	0x00	EDIDMEMORY_REG_E1	r	EDID_225[7]	EDID_225[6]	EDID_225[5]	EDID_225[4]	EDID_225[3]	EDID_225[2]	EDID_225[1]	EDID_225[0]
0xE2	0x00	EDIDMEMORY_REG_E2	r	EDID_226[7]	EDID_226[6]	EDID_226[5]	EDID_226[4]	EDID_226[3]	EDID_226[2]	EDID_226[1]	EDID_226[0]
0xE3	0x00	EDIDMEMORY_REG_E3	r	EDID_227[7]	EDID_227[6]	EDID_227[5]	EDID_227[4]	EDID_227[3]	EDID_227[2]	EDID_227[1]	EDID_227[0]
0xE4	0x00	EDIDMEMORY_REG_E4	r	EDID_228[7]	EDID_228[6]	EDID_228[5]	EDID_228[4]	EDID_228[3]	EDID_228[2]	EDID_228[1]	EDID_228[0]
0xE5	0x00	EDIDMEMORY_REG_E5	r	EDID_229[7]	EDID_229[6]	EDID_229[5]	EDID_229[4]	EDID_229[3]	EDID_229[2]	EDID_229[1]	EDID_229[0]
0xE6	0x00	EDIDMEMORY_REG_E6	r	EDID_230[7]	EDID_230[6]	EDID_230[5]	EDID_230[4]	EDID_230[3]	EDID_230[2]	EDID_230[1]	EDID_230[0]
0xE7	0x00	EDIDMEMORY_REG_E7	r	EDID_231[7]	EDID_231[6]	EDID_231[5]	EDID_231[4]	EDID_231[3]	EDID_231[2]	EDID_231[1]	EDID_231[0]
0xE8	0x00	EDIDMEMORY_REG_E8	r	EDID_232[7]	EDID_232[6]	EDID_232[5]	EDID_232[4]	EDID_232[3]	EDID_232[2]	EDID_232[1]	EDID_232[0]
0xE9	0x00	EDIDMEMORY_REG_E9	r	EDID_233[7]	EDID_233[6]	EDID_233[5]	EDID_233[4]	EDID_233[3]	EDID_233[2]	EDID_233[1]	EDID_233[0]
0xEA	0x00	EDIDMEMORY_REG_EA	r	EDID_234[7]	EDID_234[6]	EDID_234[5]	EDID_234[4]	EDID_234[3]	EDID_234[2]	EDID_234[1]	EDID_234[0]
0xEB	0x00	EDIDMEMORY_REG_EB	r	EDID_235[7]	EDID_235[6]	EDID_235[5]	EDID_235[4]	EDID_235[3]	EDID_235[2]	EDID_235[1]	EDID_235[0]
0xEC	0x00	EDIDMEMORY_REG_EC	r	EDID_236[7]	EDID_236[6]	EDID_236[5]	EDID_236[4]	EDID_236[3]	EDID_236[2]	EDID_236[1]	EDID_236[0]
0xED	0x00	EDIDMEMORY_REG_ED	r	EDID_237[7]	EDID_237[6]	EDID_237[5]	EDID_237[4]	EDID_237[3]	EDID_237[2]	EDID_237[1]	EDID_237[0]
0xEE	0x00	EDIDMEMORY_REG_EE	r	EDID_238[7]	EDID_238[6]	EDID_238[5]	EDID_238[4]	EDID_238[3]	EDID_238[2]	EDID_238[1]	EDID_238[0]
0xEF	0x00	EDIDMEMORY_REG_EF	r	EDID_239[7]	EDID_239[6]	EDID_239[5]	EDID_239[4]	EDID_239[3]	EDID_239[2]	EDID_239[1]	EDID_239[0]
0xF0	0x00	EDIDMEMORY_REG_F0	r	EDID_240[7]	EDID_240[6]	EDID_240[5]	EDID_240[4]	EDID_240[3]	EDID_240[2]	EDID_240[1]	EDID_240[0]
0xF1	0x00	EDIDMEMORY_REG_F1	r	EDID_241[7]	EDID_241[6]	EDID_241[5]	EDID_241[4]	EDID_241[3]	EDID_241[2]	EDID_241[1]	EDID_241[0]

ADD	DEF	REGISTER NAME	ACC	7	6	5	4	3	2	1	0
0xF2	0x00	EDIDMEMORY_REG_F2	r	EDID_242[7]	EDID_242[6]	EDID_242[5]	EDID_242[4]	EDID_242[3]	EDID_242[2]	EDID_242[1]	EDID_242[0]
0xF3	0x00	EDIDMEMORY_REG_F3	r	EDID_243[7]	EDID_243[6]	EDID_243[5]	EDID_243[4]	EDID_243[3]	EDID_243[2]	EDID_243[1]	EDID_243[0]
0xF4	0x00	EDIDMEMORY_REG_F4	r	EDID_244[7]	EDID_244[6]	EDID_244[5]	EDID_244[4]	EDID_244[3]	EDID_244[2]	EDID_244[1]	EDID_244[0]
0xF5	0x00	EDIDMEMORY_REG_F5	r	EDID_245[7]	EDID_245[6]	EDID_245[5]	EDID_245[4]	EDID_245[3]	EDID_245[2]	EDID_245[1]	EDID_245[0]
0xF6	0x00	EDIDMEMORY_REG_F6	r	EDID_246[7]	EDID_246[6]	EDID_246[5]	EDID_246[4]	EDID_246[3]	EDID_246[2]	EDID_246[1]	EDID_246[0]
0xF7	0x00	EDIDMEMORY_REG_F7	r	EDID_247[7]	EDID_247[6]	EDID_247[5]	EDID_247[4]	EDID_247[3]	EDID_247[2]	EDID_247[1]	EDID_247[0]
0xF8	0x00	EDIDMEMORY_REG_F8	r	EDID_248[7]	EDID_248[6]	EDID_248[5]	EDID_248[4]	EDID_248[3]	EDID_248[2]	EDID_248[1]	EDID_248[0]
0xF9	0x00	EDIDMEMORY_REG_F9	r	EDID_249[7]	EDID_249[6]	EDID_249[5]	EDID_249[4]	EDID_249[3]	EDID_249[2]	EDID_249[1]	EDID_249[0]
0xFA	0x00	EDIDMEMORY_REG_FA	r	EDID_250[7]	EDID_250[6]	EDID_250[5]	EDID_250[4]	EDID_250[3]	EDID_250[2]	EDID_250[1]	EDID_250[0]
0xFB	0x00	EDIDMEMORY_REG_FB	r	EDID_251[7]	EDID_251[6]	EDID_251[5]	EDID_251[4]	EDID_251[3]	EDID_251[2]	EDID_251[1]	EDID_251[0]
0xFC	0x00	EDIDMEMORY_REG_FC	r	EDID_252[7]	EDID_252[6]	EDID_252[5]	EDID_252[4]	EDID_252[3]	EDID_252[2]	EDID_252[1]	EDID_252[0]
0xFD	0x00	EDIDMEMORY_REG_FD	r	EDID_253[7]	EDID_253[6]	EDID_253[5]	EDID_253[4]	EDID_253[3]	EDID_253[2]	EDID_253[1]	EDID_253[0]
0xFE	0x00	EDIDMEMORY_REG_FE	r	EDID_254[7]	EDID_254[6]	EDID_254[5]	EDID_254[4]	EDID_254[3]	EDID_254[2]	EDID_254[1]	EDID_254[0]
0xFF	0x00	EDIDMEMORY_REG_FF	r	EDID_255[7]	EDID_255[6]	EDID_255[5]	EDID_255[4]	EDID_255[3]	EDID_255[2]	EDID_255[1]	EDID_255[0]

2 SIGNAL DOCUMENTATION

2.1 IO MAP

Reg	Bits	Description	
CLK_IN_FREQ_SEL[1:0]			R/W
0x04	00000<u>00</u>0	A control to set the CLK_IN frequency used. 00 - 27 MHz 01 - 28.63636 MHz 10 - 24.567 MHz 11 - 24.000MHz	
CORE_PDN			R/W
0x0B	0000000<u>0</u>	A power-down control for digital sections of the HDMI core. 0 - Powers up digital sections of HDMI block 1 - Powers down the digital section of HDMI block.	
CLK_IN_PDN			R/W
0x0B	0000000<u>0</u>	A power-down control for the CLK_IN in the digital blocks. 0 - Powers up CLK_IN buffer to the digital core. 1 - Powers down CLK_IN buffer to the digital core	
POWER_DOWN			R/W
0x0C	01<u>1</u>00000	A control to enable power-down mode. This is the main I2C power-down control. 0 - Chip is operational 1 - Enables chip power down	
PWR_SAVE_MODE			R/W
0x0C	0110<u>0</u>000	A control to enable power-save mode. 0 - Disables power save mode 1 - Enables power save mode	
DR_STR[1:0]			R/W
0x14	01<u>10</u>0000	A control to set the drive strength of the data output drivers. 00 - Reserved 01 - Medium low (2x) 10 - Medium high (3x) 11 - High (4x)	
TXA SOFT RESET			SC
0x1B	<u>0</u>0000000	Soft reset for HDMI Tx A	
TXB SOFT RESET			SC
0x1B	0<u>0</u>000000	Soft reset for HDMI Tx B	
HPA_MAN_VALUE_A			R/W
0x20	<u>0</u>0000000	A manual control for the value of HPA on Port A. Only valid if HPA_MANUAL is set to 1. 0 - 0 V applied to HPA_A pin 1 - High level applied to HPA_A pin	
HPA_MAN_VALUE_B			R/W
0x20	0<u>0</u>000000	A manual control for the value of HPA on Port B. Only valid if HPA_MANUAL is set to 1. 0 - 0 V applied to HPA_B pin 1 - High level applied to HPA_B pin	
HPA_MAN_VALUE_C			R/W
0x20	00<u>0</u>00000	A manual control for the value of HPA on Port C. Only valid if HPA_MANUAL is set to 1. 0 - 0 V applied to HPA_C pin 1 - High level applied to HPA_C pin	
HPA_MAN_VALUE_D			R/W
0x20	000<u>0</u>0000	A manual control for the value of HPA on Port D. Only valid if HPA_MANUAL is set to 1. 0 - 0 V applied to HPA_D pin 1 - High level applied to HPA_D pin	

Reg	Bits	Description	
HPA_TRISTATE_A			R/W
0x20	0000**0**000	Tristate HPA output pin for Port A. 0 - HPA_A pin active 1 - Tristate HPA_A pin	
HPA_TRISTATE_B			R/W
0x20	000000**0**0	Tristate HPA output pin for Port B 0 - HPA_B pin active 1 - Tristate HPA_B pin	
HPA_TRISTATE_C			R/W
0x20	0000000**0**	Tristate HPA output pin for Port C. 0 - HPA_C pin active 1 - Tristate HPA_C pin	
HPA_TRISTATE_D			R/W
0x20	0000000**0**	Tristate HPA output pin for Port D. 0 - HPA_D pin active 1 - Tristate HPA_D pin	
HPA_STATUS_PORT_A			R
0x21	0000**0**000	Readback of HPA status for RX port A 0 - +5V not applied to HPA_A pin by chip 1 - +5V applied to HPA_A pin by chip	
HPA_STATUS_PORT_B			R
0x21	000000**0**0	Readback of HPA status for RX port B 0 - +5V not applied to HPA_B pin by chip 1 - +5V applied to HPA_B pin by chip	
HPA_STATUS_PORT_C			R
0x21	0000000**0**	Readback of HPA status for RX port C 0 - +5V not applied to HPA_C pin by chip 1 - +5V applied to HPA_C pin by chip	
HPA_STATUS_PORT_D			R
0x21	0000000**0**	Readback of HPA status for RX port D 0 - +5V not applied to HPA_D pin by chip 1 - +5V applied to HPA_D pin by chip	
SET INPUT TXA DDC SDA			R/W
0x2C	0000000**0**	Sets the TX DDC_SDA as input	
SET INPUT TXB DDC SDA			R/W
0x32	0000000**0**	Sets the TX DDC_SDA as input	
INTRQ_TX_B_RAW			R
0x3F	000000**0**0	Status of the interrupt signal from HDMI TX B. If an interrupt event that has been enabled for the HDMI TX B has occurred this bit will be set to 0. Interrupts for HDMI TX B are set via the interrupt 1 mask bits. This bit will remain set to 0 until all status for interrupts enabled on HDMI TX B are cleared. 0 - An interrupt event for Tx B has occurred 1 - No interrupt on Tx B	
INTRQ_TX_A_RAW			R
0x3F	000000**0**0	Status of the interrupt signal from HDMI TX A. If an interrupt event that has been enabled for the HDMI TX A has occurred this bit will be set to 0. Interrupts for HDMI TX A are set via the interrupt 1 mask bits. This bit will remain set to 0 until all status for interrupts enabled on HDMI TX A are cleared. 0 - An interrupt event for Tx A has occurred 1 - No interrupt on Tx A	
INTRQ_RAW			R
0x3F	0000000**0**	Status of the interrupt signal from HDMI RX. If an interrupt event that has been enabled for the HDMI RX has occurred this bit will be set to 1. Interrupts for HDMI RX are set via the interrupt 1 mask bits. This bit will remain set to 1 until all status for interrupts enabled on HDMI RX are cleared. 0 - No interrupt on HDMI Rx 1 - An interrupt event for HDMI Rx has occurred.	

Reg	Bits	Description	
INTRQ_DUR_SEL[1:0]			R/W
0x40	00100000	A control to select the interrupt signal duration for the interrupt signal on INT1 0 - 4 CLK_IN periods 1 - 16 CLK_IN periods 2 - 64 CLK_IN periods 3 - Active until cleared	
STORE_UNMASKED_IRQS			R/W
0x40	00100000	STORE_MASKED_IRQS allows the HDMI status flags for any HDMI interrupt to be triggered regardless of whether the mask bits are set. This bit allows a HDMI interrupt to trigger and allows this interrupt to be read back through the corresponding status bit without triggering an interrupt on the interrupt pin. The status is stored until the clear bit is used to clear the status register and allows another interrupt to occur. 0 - Does not allow x_ST flag of any HDMI interrupt to be set independently of mask bits 1 - Allows x_ST flag of any HDMI interrupt to be set independently of mask bits	
EN_UMASK_RAW_INTRQ			R/W
0x40	00100000	A control to apply the internal raw interrupts signal 1 on INT1 interrupt pin. 0 - Does not output raw interrupt 1 on INT1 1 - Outputs audio raw interrupt 1 on INT1	
MPU_STIM_INTRQ			R/W
0x40	00100000	Manual interrupt set control. This feature should be used for test purposes only. Note that the appropriate mask bit must be set to generate an interrupt at the pin 0 - Disables manual interrupt mode 1 - Enables manual interrupt mode	
INTRQ_OP_SEL[1:0]			R/W
0x40	00100000	Interrupt signal configuration control for INT1 00 - Open drain 01 - Drives low when active 10 - Drives high when active 11 - Disabled	
MPU_STIM_INTRQ_RAW			R
0x47	00000000	Raw status of manual forced interrupt signal. 0 - Manual forced interrupt not applied 1 - Manual forced interrupt applied	
MPU_STIM_INTRQ_ST			R
0x48	00000000	Latched signal status of Manual Forced interrupt signal. Once set this bit will remain high until the interrupt has been cleared via MPU_STIM_INTRQ_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - Forced manual interrupt event has not occurred. 1 - Force manual interrupt even has occurred.	
MPU_STIM_INTRQ_CLR			SC
0x49	00000000	Clear bit for Manual Forced interrupt signal. 0 - Does not clear MPU_STIM_INT_ST bit 1 - Clears MPU_STIM_INT_ST bit	
MPU_STIM_INTRQ_MB1			R/W
0x4B	00000000	INT1 interrupt mask for Manual forced interrupt signal. When set the Manual Forced interrupt will trigger the INT1 interrupt and MPU_STIM_INTRQ_ST will indicate the interrupt status. 0 - Disables Manual forced interrupt for INT1 1 - Enables Manual forced interrupt for INT1	
ISRC2_PCKT_RAW			R
0x60	00000000	Raw status signal of International Standard Recording Code 2 (ISRC2) Packet detection signal. 0 - No ISRC2 packets received since the last HDMI packet detection reset. 1 - ISRC2 packets have been received. This bit will reset to zero after an HDMI packet detection reset or upon writing to ISRC2_PACKET_ID.	
ISRC1_PCKT_RAW			R
0x60	00000000	Raw status signal of International Standard Recording Code 1 (ISRC1) Packet detection signal. 0 - No ISRC1 packets received since the last HDMI packet detection reset. 1 - ISRC1 packets have been received. This bit will reset to zero after an HDMI packet detection reset or upon writing to ISRC1_PACKET_ID.	

Reg	Bits	Description	
ACP_PCKT_RAW			R
0x60	00**0**00000	Raw status signal of Audio Content Protection Packet detection signal. 0 - No ACP packet received within the last 600 ms or since the last HDMI packet detection reset. 1 - ACP packets have been received within the last 600 ms. This bit will reset to zero after an HDMI packet detection reset or upon writing to ACP_PACKET_ID.	
VS_INFO_RAW			R
0x60	000**0**0000	Raw status signal of Vendor specific Infoframe detection signal. 0 - No new VS infoframe has been received since the last HDMI packet detection reset. 1 - A new VS infoframe has been received. This bit will reset to zero after an HDMI packet detection reset or upon writing to VS_PACKET_ID.	
MS_INFO_RAW			R
0x60	0000**0**000	Raw status signal of MPEG Source Infoframe detection signal. 0 - No source product description Infoframe received within the last three VSyncs or since the last HDMI packet detection reset. 1 - MPEG Source InfoFrame received. This bit will reset to zero after an HDMI packet detection reset or upon writing to MS_PACKET_ID.	
SPD_INFO_RAW			R
0x60	00000**0**00	Raw status of SPD Infoframe detected signal. 0 - No source product description InfoFrame received since the last HDMI packet detection reset. 1 - Source product description InfoFrame received. This bit will reset to zero after an HDMI packet detection reset or upon writing to SPD_PACKET_ID.	
AUDIO_INFO_RAW			R
0x60	000000**0**0	Raw status of Audio InfoFrame detected signal. 0 - No AVI InfoFrame has been received within the last three VSyncs or since the last HDMI packet detection reset. 1 - An Audio InfoFrame has been received within the last three VSyncs. This bit will reset to zero on the fourth VSync leading edge following an Audio InfoFrame, after an HDMI packet detection reset or upon writing to AUD_PACKET_ID.	
AVI_INFO_RAW			R
0x60	0000000**0**	Raw status of AVI InfoFrame detected signal. This bit is set to one when an AVI InfoFrame is received and is reset to zero if no AVI InfoFrame is received for more than 7 VSyncs (on the eighth VSync leading edge following the last received AVI InfoFrame), after an HDMI packet detection reset or upon writing to AVI_PACKET_ID. 0 - No AVI InfoFrame has been received within the last seven VSyncs or since the last HDMI packet detection reset 1 - An AVI InfoFrame has been received within the last seven VSyncs	
ISRC2_PCKT_ST			R
0x61	**0**0000000	Latched status of ISRC2 Packet detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via ISRC2_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - ISRC2_PCKT_RAW has changed. Interrupt has been generated.	
ISRC1_PCKT_ST			R
0x61	0**0**000000	Latched status of ISRC1 Packet detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via ISRC1_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - ISRC1_PCKT_RAW has changed. Interrupt has been generated.	
ACP_PCKT_ST			R
0x61	00**0**00000	Latched status of Audio Content Protection Packet detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via ACP_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - ACP_PCKT_RAW has changed. Interrupt has been generated.	
VS_INFO_ST			R
0x61	000**0**0000	Latched status of Vendor Specific Infoframe detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via VS_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - VS_INFO_RAW has changed. Interrupt has been generated.	

Reg	Bits	Description	
MS_INFO_ST			R
0x61	0000**0**000	Latched status of MPEG Source Infoframe detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via MS_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - MS_INFO_RAW has changed. Interrupt has been generated.	
SPD_INFO_ST			R
0x61	00000**0**00	Latched status of SPD Infoframe detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via SPD_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - SPD_INFO_RAW has changed. Interrupt has been generated.	
AUDIO_INFO_ST			R
0x61	000000**0**0	Latched status of Audio Infoframe detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via AUDIO_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No interrupt generated from this register 1 - AUDIO_INFO_RAW has changed. Interrupt has been generated.	
AVI_INFO_ST			R
0x61	0000000**0**	Latched status of AVI_INFO_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. Once set this bit will remain high until the interrupt has been cleared via AVI_INFO_CLR. 0 - AVI_INFO_RAW has not changed state 1 - AVI_INFO_RAW has changed state	
ISRC2_PCKT_CLR			SC
0x62	**0**0000000	Clear bit for ISRC2 Packet detection interrupt signal. 0 - Does not clear 1 - Clears ISRC1_PCKT_ST	
ISRC1_PCKT_CLR			SC
0x62	0**0**000000	Clear bit for ISRC1 Packet detection interrupt signal. 0 - Does not clear ISRC1_INFO_ST 1 - Clears ISRC1_INFO_ST	
ACP_PCKT_CLR			SC
0x62	00**0**00000	Clear bit for Audio Content Protection Packet detected interrupt signal. 0 - Does not clear ACP_INFO_ST 1 - Clears ACP_INFO_ST	
VS_INFO_CLR			SC
0x62	000**0**0000	Clear bit for Vendor Specific Infoframe interrupt signal. 0 - Does not clear VS_INFO_ST 1 - Clears VS_INFO_ST	
MS_INFO_CLR			SC
0x62	0000**0**000	Clear bit for MPEG Source Infoframe interrupt signal. 0 - Does not clear MS_INFO_ST 1 - Clears MS_INFO_ST	
SPD_INFO_CLR			SC
0x62	00000**0**00	Clear bit for SPD Infoframe interrupt signal. 0 - Does not clear SPD_INFO_ST 1 - Clears SPD_INFO_ST	
AUDIO_INFO_CLR			SC
0x62	000000**0**0	Clear bit for Audio Infoframe interrupt signal. 0 - Does not clear AUDIO_INFO_ST 1 - Clears AUDIO_INFO_ST	
AVI_INFO_CLR			SC
0x62	0000000**0**	Clear bit for AVI_INFO_RAW and AVI_INFO_ST bits. 0 - No function 1 - Clear AVI_INFO_RAW and AVI_INFO_ST	

Reg	Bits	Description	
ISRC2_PCKT_MB2			R/W
0x63	0000000	INT2 interrupt mask for ISRC2 Packet detection interrupt. When set the ISRC2 Packet detection interrupt will trigger the INT2 interrupt and ISRC2_INFO_ST will indicate the interrupt status. 0 - Disables ISRC2 Infoframe detection interrupt for INT2 1 - Enables ISRC2 Infoframe detection interrupt for INT2	
ISRC1_PCKT_MB2			R/W
0x63	0000000	INT2 interrupt mask for ISRC1 Packet detection interrupt. When set the ISRC1 Packet detection interrupt will trigger the INT2 interrupt and ISRC1_INFO_ST will indicate the interrupt status. 0 - Disables ISRC1 Infoframe detection interrupt for INT2 1 - Enables ISRC1 Infoframe detection interrupt for INT2	
ACP_PCKT_MB2			R/W
0x63	0000000	INT2 interrupt mask for Audio Content Protection Packet detection interrupt. When set the Audio Content Protection Infoframe detection interrupt will trigger the INT2 interrupt and ACP_INFO_ST will indicate the interrupt status. 0 - Disables Audio Content Protection Infoframe detection interrupt for INT2 1 - Enables Audio Content Protection Infoframe detection interrupt for INT2	
VS_INFO_MB2			R/W
0x63	0000000	INT2 interrupt mask for Vendor Specific Infoframe detection interrupt. When set the Vendor Specific Infoframe detection interrupt will trigger the INT2 interrupt and VS_INFO_ST will indicate the interrupt status. 0 - Disables Vendor Specific Infoframe detection interrupt for INT2 1 - Enables Vendor Specific Infoframe detection interrupt for INT2	
MS_INFO_MB2			R/W
0x63	0000000	INT2 interrupt mask for MPEG source Infoframe detection interrupt. When set the MPEG Source Infoframe detection interrupt will trigger the INT2 interrupt and MS_INFO_ST will indicate the interrupt status. 0 - Disables MPEG source Info frame detection interrupt for INT2 1 - Enables MPEG source Info frame detection interrupt for INT2	
SPD_INFO_MB2			R/W
0x63	0000000	INT2 interrupt mask for SPD Infoframe detection interrupt. When set the SPD Infoframe detection interrupt will trigger the INT2 interrupt and SPD_INFO_ST will indicate the interrupt status. 0 - Disables SPD Info frame detection interrupt for INT2 1 - Enables SPD Info frame detection interrupt for INT2	
AUDIO_INFO_MB2			R/W
0x63	0000000	INT2 interrupt mask for Audio Infoframe detection interrupt. When set the Audio Infoframe detection interrupt will trigger the INT2 interrupt and AVI_INFO_ST will indicate the interrupt status. 0 - Disables AUDIO Info frame detection interrupt for INT2 1 - Enables AUDIO Info frame detection interrupt for INT2	
AVI_INFO_MB2			R/W
0x63	0000000	INT2 interrupt mask for AVI Infoframe detection interrupt. When set an AVI Infoframe detection event will cause AVI_INFO_ST to be set and an interrupt will be generated on INT2. 0 - Disables AVI Info frame detection interrupt for INT2 1 - Enables AVI Info frame detection interrupt for INT2	
ISRC2_PCKT_MB1			R/W
0x64	0000000	INT1 interrupt mask for ISRC2 Infoframe detection interrupt. When set the ISRC2 Infoframe detection interrupt will trigger the INT1 interrupt and ISRC2_INFO_ST will indicate the interrupt status. 0 - Disables ISRC2 Packet detection interrupt for INT1 1 - Enables ISRC2 Packet detection interrupt for INT1	
ISRC1_PCKT_MB1			R/W
0x64	0000000	INT1 interrupt mask for ISRC1 Infoframe detection interrupt. When set the ISRC1 Infoframe detection interrupt will trigger the INT1 interrupt and ISRC1_INFO_ST will indicate the interrupt status. 0 - Disables ISRC1 Infoframe detection interrupt for INT1 1 - Enables ISRC1 Infoframe detection interrupt for INT1	
ACP_PCKT_MB1			R/W
0x64	0000000	INT1 interrupt mask for Audio Content Protection Packet detection interrupt. When set the Audio Content Protection Packet detection interrupt will trigger the INT1 interrupt and ACP_INFO_ST will indicate the interrupt status. 0 - Disables Audio Content Protection Infoframe detection interrupt for INT1 1 - Enables Audio Content Protection Infoframe detection interrupt for INT1	

Reg	Bits	Description	
VS_INFO_MB1			R/W
0x64	0000**0**0000	INT1 interrupt mask for Vendor Specific Infoframe detection interrupt. When set the Vendor Specific Infoframe detection interrupt will trigger the INT1 interrupt and VS_INFO_ST will indicate the interrupt status. 0 - Disables Vendor Specific Infoframe detection interrupt for INT1 1 - Enables Vendor Specific Infoframe detection interrupt for INT1	
MS_INFO_MB1			R/W
0x64	0000**0**000	INT1 interrupt mask for MPEG source Infoframe detection interrupt. When set the MPEG source Infoframe detection interrupt will trigger the INT1 interrupt and MS_INFO_ST will indicate the interrupt status. 0 - Disables MPEG source Infoframe detection interrupt for INT1 1 - Enables MPEG source Infoframe detection interrupt for INT1	
SPD_INFO_MB1			R/W
0x64	00000**0**00	INT1 interrupt mask for SPD Infoframe detection interrupt. When set the SPD Infoframe detection interrupt will trigger the INT1 interrupt and SPD_INFO_ST will indicate the interrupt status. 0 - Disables SPD Info frame detection interrupt for INT1 1 - Enables SPD Info frame detection interrupt for INT1	
AUDIO_INFO_MB1			R/W
0x64	000000**0**0	INT1 interrupt mask for Audio Infoframe detection interrupt. When set the Audio Infoframe detection interrupt will trigger the INT1 interrupt and AVI_INFO_ST will indicate the interrupt status. 0 - Disables AUDIO Info frame detection interrupt for INT1 1 - Enables AUDIO Info frame detection interrupt for INT1	
AVI_INFO_MB1			R/W
0x64	0000000**0**	INT1 interrupt mask for AVI Infoframe detection interrupt. When set an AVI Infoframe detection event will cause AVI_INFO_ST to be set and an interrupt will be generated on INT1. 0 - Disables AVI Info frame detection interrupt for INT1 1 - Enables AVI Info frame detection interrupt for INT1	
AV_MUTE_RAW			R
0x65	00**0**00000	Raw status signal of AV Mute detection signal. 0 - No AV mute raw received since last HDMI reset condition 1 - AV mute received	
GEN_CTL_PCKT_RAW			R
0x65	00000**0**00	Raw status signal of General Control Packet detection signal. 0 - No general control packets received since the last HDMI reset condition 1 - General control packets received	
AUDIO_C_PCKT_RAW			R
0x65	000000**0**0	Raw status signal of Audio Clock Regeneration Packet detection signal. 0 - No audio clock regeneration packets received since the last HDMI reset condition 1 - Audio clock regeneration packets received	
GAMUT_MDATA_RAW			R
0x65	0000000**0**	Raw status signal of Gamut Metadata Packet detection signal. 0 - No Gamut Metadata packet has been received in the last video frame or since the last HDMI packet detection reset. 1 - A Gamut Metadata packet has been received in the last video frame. This bit will reset to zero after an HDMI packet detection reset or upon writing to GAMUT_PACKET_ID.	
AV_MUTE_ST			R
0x66	00**0**00000	Latched status of AV Mute detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via AV_MUTE_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - AV_MUTE_RAW has not changed. An interrupt has not been generated. 1 - AV_MUTE_RAW has changed. An interrupt has been generated.	
GEN_CTL_PCKT_ST			R
0x66	00000**0**00	Latched status of General Control Packet interrupt signal. Once set this bit will remain high until the interrupt has been cleared via GEN_CTL_PCKT_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - GEN_CTL_PCKT_RAW has not changed. Interrupt has not been generated from this register. 1 - GEN_CTL_PCKT_RAW has changed. Interrupt has been generated from this register.	

Reg	Bits	Description	
AUDIO_C_PCKT_ST			R
0x66	0000000<u>0</u>	Latched status of Audio Clock Regeneration Packet interrupt signal. Once set this bit will remain high until the interrupt has been cleared via AUDIO_PCKT_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - AUDIO_C_PCKT_RAW has not changed. Interrupt has not been generated from this register 1 - AUDIO_C_PCKT_RAW has changed. Interrupt has been generated from this register.	
GAMUT_MDATA_ST			R
0x66	0000000<u>0</u>	Latched status of Gamut Metadata Packet detected interrupt signal. Once set this bit will remain high until the interrupt has been cleared via GAMUT_MDATA_PCKT_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - GAMUT_MDATA_RAW has not changed. Interrupt has not been generated from this register 1 - GAMUT_MDATA_RAW has changed. Interrupt has been generated from this register.	
AV_MUTE_CLR			SC
0x67	00<u>0</u>00000	Clear bit for AV Mute Detected interrupt signal. 0 - Does not clear AV_MUTE_ST 1 - Clears AV_MUTE_ST	
GEN_CTL_PCKT_CLR			SC
0x67	00000<u>0</u>00	Clear bit for General Control Packet detection interrupt signal. 0 - Does not clear GEN_CTL_PCKT_ST 1 - Clears GEN_CTL_PCKT_ST	
AUDIO_C_PCKT_CLR			SC
0x67	0000000<u>0</u>	Clear bit for Audio Clock Regeneration Packet detection interrupt signal. 0 - Does not clear AUDIO_C_PCKT_ST 1 - Clears AUDIO_C_PCKT_ST	
GAMUT_MDATA_CLR			SC
0x67	0000000<u>0</u>	Clear bit for Gamut Metadata Packet detection interrupt signal. 0 - Does not clear GAMUT_MDATA_ST 1 - Clears GAMUT_MDATA_ST	
AV_MUTE_MB2			R/W
0x68	00<u>0</u>00000	INT2 interrupt mask for AV Mute detected interrupt. When set the AV Mute detected interrupt will trigger the INT2 interrupt and AV_MUTE_ST will indicate the interrupt status. 0 - Disables AV Mute detected interrupt for INT2 1 - Enables AV Mute detected interrupt for INT2	
GEN_CTL_PCKT_MB2			R/W
0x68	00000<u>0</u>00	INT2 interrupt mask for General Control Packet detection interrupt. When set the General Control Packet detection interrupt will trigger the INT2 interrupt and AUDIO_C_PCKT_ST will indicate the interrupt status. 0 - Disables General Control Packet detection interrupt for INT2 1 - Enables General Control Packet detection interrupt for INT2	
AUDIO_C_PCKT_MB2			R/W
0x68	0000000<u>0</u>	INT2 interrupt mask for Audio Clock Regeneration Packet detection interrupt. When set the Audio Clock Regeneration Packet detection interrupt will trigger the INT2 interrupt and AUDIO_C_PCKT_ST will indicate the interrupt status. 0 - Disables Audio Clock Regeneration Packet detection interrupt for INT2 1 - Enables Audio Clock Regeneration Packet detection interrupt for INT2	
GAMUT_MDATA_MB2			R/W
0x68	0000000<u>0</u>	INT2 interrupt mask for Gamut Metadata Packet detection interrupt. When set the Gamut Metadata Packet detection interrupt will trigger the INT2 interrupt and GAMUT_MDATA_PCKT_ST will indicate the interrupt status. 0 - Disables Gamut Metadata Packet detection interrupt for INT2 1 - Enables Gamut Metadata Packet detection interrupt for INT2	
AV_MUTE_MB1			R/W
0x69	00<u>0</u>00000	INT1 interrupt mask for AV Mute detected interrupt. When set the AV Mute detected interrupt will trigger the INT1 interrupt and AV_MUTE_ST will indicate the interrupt status. 0 - Disables AV Mute detected interrupt for INT1 1 - Enables AV Mute detected interrupt for INT1	

Reg	Bits	Description	
GEN_CTL_PCKT_MB1			R/W
0x69	000000<u>0</u>00	INT1 interrupt mask for General Control Packet detection interrupt. When set the General Control Packet detection interrupt will trigger the INT1 interrupt and GEN_CTL_PCKT_ST will indicate the interrupt status. 0 - Disables General Control Packet detection interrupt for INT1 1 - Enables General Control Packet detection interrupt for INT1	
AUDIO_C_PCKT_MB1			R/W
0x69	0000000<u>0</u>0	INT1 interrupt mask for Audio Clock Regeneration Packet detection interrupt. When set the Audio Clock Regeneration Packet detection interrupt will trigger the INT1 interrupt and AUDIO_C_PCKT_ST will indicate the interrupt status. 0 - Disables Audio Clock Regeneration Packet detection interrupt for INT1 1 - Enables Audio Clock Regeneration Packet detection interrupt for INT1	
GAMUT_MDATA_MB1			R/W
0x69	00000000<u>0</u>	INT1 interrupt mask for Gamut Metadata Packet detection interrupt. When set the Gamut Metadata Packet detection interrupt will trigger the INT1 interrupt and GAMUT_MDATA_PCKT_ST will indicate the interrupt status. 0 - Disables Gamut Metadata Packet detection interrupt for INT1 1 - Enables Gamut Metadata Packet detection interrupt for INT1	
TMDSPLL_LCK_A_RAW			R
0x6A	<u>0</u>0000000	A readback to indicate the raw status of the Port A TMDS PLL lock signal. 0 - TMDS PLL on Port A is not locked 1 - TMDS PLL on Port A is locked to the incoming clock	
TMDSPLL_LCK_B_RAW			R
0x6A	0<u>0</u>000000	A readback to indicate the raw status of the Port B TMDS PLL lock signal. 0 - TMDS PLL on Port B is not locked 1 - TMDS PLL on Port B is locked to the incoming clock	
TMDSPLL_LCK_C_RAW			R
0x6A	00<u>0</u>00000	A readback to indicate the raw status of the Port C TMDS PLL lock signal. 0 - TMDS PLL on Port C is not locked 1 - TMDS PLL on Port C is locked to the incoming clock	
TMDSPLL_LCK_D_RAW			R
0x6A	000<u>0</u>0000	A readback to indicate the raw status of the Port D TMDS PLL lock signal. 0 - TMDS PLL on Port D is not locked 1 - TMDS PLL on Port D is locked to the incoming clock	
TMDS_CLK_A_RAW			R
0x6A	0000<u>0</u>000	Raw status of Port A TMDS clock detection signal. 0 - No TMDS clock detected on Port A 1 - TMDS clock detected on Port A	
TMDS_CLK_B_RAW			R
0x6A	00000<u>0</u>00	Raw status of Port B TMDS clock detection signal. 0 - No TMDS clock detected on Port B 1 - TMDS clock detected on Port B	
TMDS_CLK_C_RAW			R
0x6A	000000<u>0</u>0	Raw status of Port C TMDS clock detection signal. 0 - No TMDS clock detected on Port C 1 - TMDS clock detected on Port C	
TMDS_CLK_D_RAW			R
0x6A	00000000<u>0</u>	Raw status of Port D TMDS clock detection signal. 0 - No TMDS clock detected on Port D 1 - TMDS clock detected on Port D	
TMDSPLL_LCK_A_ST			R
0x6B	<u>0</u>0000000	Latched status of Port A TMDS PLL Lock interrupt signal. Once set this bit will remain high until the interrupt has been cleared via TMDSPLL_LCK_A_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - TMDSPLL_LCK_A_RAW has not changed. An interrupt has not been generated. 1 - TMDSPLL_LCK_A_RAW has changed. An interrupt has been generated.	

Reg	Bits	Description	
TMDSPLL_LCK_B_ST			R
0x6B	0<u>0</u>000000	Latched status of Port B TMDS PLL Lock interrupt signal. Once set this bit will remain high until the interrupt has been cleared via TMDSPLL_LCK_B_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - TMDSPLL_LCK_B_RAW has not changed. An interrupt has not been generated. 1 - TMDSPLL_LCK_B_RAW has changed. An interrupt has been generated.	
TMDSPLL_LCK_C_ST			R
0x6B	00<u>0</u>00000	Latched status of Port C TMDS PLL Lock interrupt signal. Once set this bit will remain high until the interrupt has been cleared via TMDSPLL_LCK_C_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - TMDSPLL_LCK_C_RAW has not changed. An interrupt has not been generated. 1 - TMDSPLL_LCK_C_RAW has changed. An interrupt has been generated.	
TMDSPLL_LCK_D_ST			R
0x6B	000<u>0</u>0000	Latched status of Port D TMDS PLL Lock interrupt signal. Once set this bit will remain high until the interrupt has been cleared via TMDSPLL_LCK_D_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - TMDSPLL_LCK_D_RAW has not changed. An interrupt has not been generated. 1 - TMDSPLL_LCK_D_RAW has changed. An interrupt has been generated.	
TMDS_CLK_A_ST			R
0x6B	0000<u>0</u>000	Latched status of Port A TMDS Clock Detection interrupt signal. Once set this bit will remain high until the interrupt has been cleared via TMDS_CLK_A_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - TMDS_CLK_A_RAW has not changed. An interrupt has not been generated. 1 - TMDS_CLK_A_RAW has changed. An interrupt has been generated.	
TMDS_CLK_B_ST			R
0x6B	00000<u>0</u>00	Latched status of Port B TMDS Clock Detection interrupt signal .Once set this bit will remain high until the interrupt has been cleared via TMDS_CLK_B_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - TMDS_CLK_B_RAW has not changed. An interrupt has not been generated. 1 - TMDS_CLK_B_RAW has changed. An interrupt has been generated.	
TMDS_CLK_C_ST			R
0x6B	000000<u>0</u>0	Latched status of Port C TMDS Clock Detection interrupt signal. Once set this bit will remain high until the interrupt has been cleared via TMDS_CLK_C_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - TMDS_CLK_C_RAW has not changed. An interrupt has not been generated. 1 - TMDS_CLK_C_RAW has changed. An interrupt has been generated.	
TMDS_CLK_D_ST			R
0x6B	0000000<u>0</u>	Latched status of Port D TMDS Clock Detection interrupt signal. Once set this bit will remain high until the interrupt has been cleared via TMDS_CLK_D_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - TMDS_CLK_D_RAW has not changed. An interrupt has not been generated. 1 - TMDS_CLK_D_RAW has changed. An interrupt has been generated.	
TMDSPLL_LCK_A_CLR			SC
0x6C	<u>0</u>0000000	Clear bit for Port A TMDS PLL Lock interrupt signal. 0 - Does not clear TMDSPLL_LCK_A_ST 1 - Clears TMDSPLL_LCK_A_ST	
TMDSPLL_LCK_B_CLR			SC
0x6C	0<u>0</u>000000	Clear bit for Port B TMDS PLL Lock interrupt signal. 0 - Does not clear TMDSPLL_LCK_B_ST 1 - Clears TMDSPLL_LCK_B_ST	
TMDSPLL_LCK_C_CLR			SC
0x6C	00<u>0</u>00000	Clear bit for Port C TMDS PLL Lock interrupt signal. 0 - Does not clear TMDSPLL_LCK_C_ST 1 - Clears TMDSPLL_LCK_C_ST	
TMDSPLL_LCK_D_CLR			SC
0x6C	000<u>0</u>0000	Clear bit for Port D TMDS PLL Lock interrupt signal. 0 - Does not clear TMDSPLL_LCK_D_ST 1 - Clears TMDSPLL_LCK_D_ST	
TMDS_CLK_A_CLR			SC
0x6C	0000<u>0</u>000	Clear bit for Port A TMDS Clock Detection interrupt signal. 0 - Does not clear TMDS_CLK_A_ST 1 - Clears TMDS_CLK_A_ST	

Reg	Bits	Description	
TMDS_CLK_B_CLR			SC
0x6C	00000000	Clear bit for Port B TMDS Clock Detection interrupt signal. 0 - Does not clear TMDS_CLK_B_ST 1 - Clears TMDS_CLK_B_ST	
TMDS_CLK_C_CLR			SC
0x6C	00000000	Clear bit for Port C TMDS Clock Detection interrupt signal. 0 - Does not clear TMDS_CLK_C_ST 1 - Clears TMDS_CLK_C_ST	
TMDS_CLK_D_CLR			SC
0x6C	00000000	Clear bit for Port D TMDS Clock Detection interrupt signal. 0 - Does not clear TMDS_CLK_D_ST 1 - Clears TMDS_CLK_D_ST	
TMDSPLL_LCK_A_MB1			R/W
0x6E	00000000	INT1 interrupt mask for Port A TMDS PLL Lock interrupt. When set the Port A TMDS PLL Lock interrupt will trigger the INT1 interrupt and TMDSPLL_LCK_A_ST will indicate the interrupt status. 0 - Disables Port A TMDSPLL Lock interrupt for INT1 1 - Enables Port A TMDSPLL Lock interrupt for INT1	
TMDSPLL_LCK_B_MB1			R/W
0x6E	00000000	INT1 interrupt mask for Port B TMDS PLL Lock interrupt. When set the Port B TMDS PLL Lock interrupt will trigger the INT1 interrupt and TMDSPLL_LCK_B_ST will indicate the interrupt status. 0 - Disables Port B TMDSPLL Lock interrupt for INT1 1 - Enables Port B TMDSPLL Lock interrupt for INT1	
TMDSPLL_LCK_C_MB1			R/W
0x6E	00000000	INT1 interrupt mask for Port C TMDS PLL Lock interrupt. When set the Port C TMDS PLL Lock interrupt will trigger the INT1 interrupt and TMDSPLL_LCK_C_ST will indicate the interrupt status. 0 - Disables Port C TMDSPLL Lock interrupt for INT1 1 - Enables Port C TMDSPLL Lock interrupt for INT1	
TMDSPLL_LCK_D_MB1			R/W
0x6E	00000000	INT1 interrupt mask for Port D TMDS PLL Lock interrupt. When set the Port D TMDS PLL Lock interrupt will trigger the INT1 interrupt and TMDSPLL_LCK_D_ST will indicate the interrupt status. 0 - Disables Port D TMDSPLL Lock interrupt for INT1 1 - Enables Port D TMDSPLL Lock interrupt for INT1	
TMDS_CLK_A_MB1			R/W
0x6E	00000000	INT1 interrupt mask for Port A TMDS Clock detection interrupt. When set the Port A TMDS Clock detection interrupt will trigger the INT1 interrupt and TMDS_CLK_A_ST will indicate the interrupt status. 0 - Disables Port A TMDS Clock Detection interrupt for INT1 1 - Enables Port A TMDS Clock Detection interrupt for INT1	
TMDS_CLK_B_MB1			R/W
0x6E	00000000	INT1 interrupt mask for Port B TMDS Clock detection interrupt. When set the Port B TMDS Clock detection interrupt will trigger the INT1 interrupt and TMDS_CLK_B_ST will indicate the interrupt status. 0 - Disables Port B TMDS Clock Detection interrupt for INT1 1 - Enables Port B TMDS Clock Detection interrupt for INT1	
TMDS_CLK_C_MB1			R/W
0x6E	00000000	INT1 interrupt mask for Port C TMDS Clock detection interrupt. When set the Port C TMDS Clock detection interrupt will trigger the INT1 interrupt and TMDS_CLK_C_ST will indicate the interrupt status. 0 - Disables Port C TMDS Clock Detection interrupt for INT1 1 - Enables Port C TMDS Clock Detection interrupt for INT1	
TMDS_CLK_D_MB1			R/W
0x6E	00000000	INT1 interrupt mask for Port D TMDS Clock detection interrupt. When set the Port D TMDS Clock detection interrupt will trigger the INT1 interrupt and TMDS_CLK_D_ST will indicate the interrupt status. 0 - Disables Port D TMDS Clock Detection interrupt for INT1 1 - Enables Port D TMDS Clock Detection interrupt for INT1	
HDMI_ENCRPT_A_RAW			R
0x6F	00000000	Raw status of Port A encryption detection signal. 0 - Current frame in Port A is not encrypted 1 - Current frame in Port A is encrypted	

Reg	Bits	Description	
HDMI_ENCRPT_B_RAW			R
0x6F	0[0]000000	Raw status of Port B encryption detection signal. 0 - Current frame in Port B is not encrypted 1 - Current frame in Port B is encrypted	
HDMI_ENCRPT_C_RAW			R
0x6F	00[0]00000	Raw status of Port C encryption detection signal. 0 - Current frame in Port C is not encrypted 1 - Current frame in Port C is encrypted	
HDMI_ENCRPT_D_RAW			R
0x6F	000[0]0000	Raw status of Port D encryption detection signal. 0 - Current frame in Port D is not encrypted 1 - Current frame in Port D is encrypted	
CABLE_DET_A_RAW			R
0x6F	0000[0]000	Raw status of Port A +5 V cable detection signal. 0 - No cable detected on Port A 1 - Cable detected on Port A (high level on RXA_5V)	
CABLE_DET_B_RAW			R
0x6F	00000[0]00	Raw status of Port B +5 V cable detection signal. 0 - No cable detected on Port B 1 - Cable detected on Port B (high level on RXB_5V)	
CABLE_DET_C_RAW			R
0x6F	000000[0]0	Raw status of Port C +5 V cable detection signal. 0 - No cable detected on Port C 1 - Cable detected on Port C (high level on RXC_5V)	
CABLE_DET_D_RAW			R
0x6F	00000000	Raw status of Port D +5 V cable detection signal. 0 - No cable detected on Port D 1 - Cable detected on Port D (high level on RXD_5V)	
HDMI_ENCRPT_A_ST			R
0x70	0[0]000000	Latched status for Port A Encryption detection interrupt signal. Once set this bit will remain high until the interrupt has been cleared via HDMI_ENCRPT_A_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - HDMI_ENCRPT_A_RAW has not changed. An interrupt has not been generated. 1 - HDMI_ENCRPT_A_RAW has changed. An interrupt has been generated.	
HDMI_ENCRPT_B_ST			R
0x70	0[0]000000	Latched status for Port B Encryption detection interrupt signal. Once set this bit will remain high until the interrupt has been cleared via HDMI_ENCRPT_B_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - HDMI_ENCRPT_B_RAW has not changed. An interrupt has not been generated. 1 - HDMI_ENCRPT_B_RAW has changed. An interrupt has been generated.	
HDMI_ENCRPT_C_ST			R
0x70	00[0]00000	Latched status for Port C Encryption detection interrupt signal. Once set this bit will remain high until the interrupt has been cleared via HDMI_ENCRPT_C_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - HDMI_ENCRPT_C_RAW has not changed. An interrupt has not been generated. 1 - HDMI_ENCRPT_C_RAW has changed. An interrupt has been generated.	
HDMI_ENCRPT_D_ST			R
0x70	000[0]0000	Latched status for Port D Encryption detection interrupt signal. Once set this bit will remain high until the interrupt has been cleared via HDMI_ENCRPT_D_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - HDMI_ENCRPT_D_RAW has not changed. An interrupt has not been generated. 1 - HDMI_ENCRPT_D_RAW has changed. An interrupt has been generated.	
CABLE_DET_A_ST			R
0x70	0000[0]000	Latched status for Port A +5V cable detection interrupt signal. Once set this bit will remain high until the interrupt has been cleared via CABLE_DET_A_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - CABLE_DET_A_RAW has not changed. Interrupt has not been generated from this register. 1 - CABLE_DET_A_RAW has changed. Interrupt has been generated from this register.	

Reg	Bits	Description	
CABLE_DET_B_ST			R
0x70	000000**0**0	Latched status for Port B +5V cable detection interrupt signal. Once set this bit will remain high until the interrupt has been cleared via CABLE_DET_B_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - CABLE_DET_B_RAW has not changed. Interrupt has not been generated from this register. 1 - CABLE_DET_B_RAW has changed. Interrupt has been generated from this register.	
CABLE_DET_C_ST			R
0x70	00000**0**00	Latched status for Port C +5V cable detection interrupt signal. Once set this bit will remain high until the interrupt has been cleared via CABLE_DET_C_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - CABLE_DET_C_RAW has not changed. Interrupt has not been generated from this register. 1 - CABLE_DET_C_RAW has changed. Interrupt has been generated from this register.	
CABLE_DET_D_ST			R
0x70	0000000**0**	Latched status for Port D +5V cable detection interrupt signal. Once set this bit will remain high until the interrupt has been cleared via CABLE_DET_D_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - CABLE_DET_D_RAW has not changed. Interrupt has not been generated from this register. 1 - CABLE_DET_D_RAW has changed. Interrupt has been generated from this register.	
HDMI_ENCRPT_A_CLR			SC
0x71	**0**0000000	Clear bit for Port A Encryption detection interrupt signal. 0 - Does not clear HDMI_ENCRPT_A_ST 1 - Clears HDMI_ENCRPT_A_ST	
HDMI_ENCRPT_B_CLR			SC
0x71	0**0**000000	Clear bit for Port B Encryption detection interrupt signal. 0 - Does not clear HDMI_ENCRPT_B_ST 1 - Clears HDMI_ENCRPT_B_ST	
HDMI_ENCRPT_C_CLR			SC
0x71	00**0**00000	Clear bit for Port C Encryption detection interrupt signal. 0 - Does not clear HDMI_ENCRPT_C_ST 1 - Clears HDMI_ENCRPT_C_ST	
HDMI_ENCRPT_D_CLR			SC
0x71	000**0**0000	Clear bit for Port D Encryption detection interrupt signal. 0 - Does not clear HDMI_ENCRPT_D_ST 1 - Clears HDMI_ENCRPT_D_ST	
CABLE_DET_A_CLR			SC
0x71	0000**0**000	Clear bit for Port A +5V cable detection interrupt signal. 0 - Does not clear 1 - Clears CABLE_DET_A_ST	
CABLE_DET_B_CLR			SC
0x71	00000**0**00	Clear bit for Port B +5V cable detection interrupt signal. 0 - Does not clear 1 - Clears CABLE_DET_B_ST	
CABLE_DET_C_CLR			SC
0x71	000000**0**0	Clear bit for Port C +5V cable detection interrupt signal. 0 - Does not clear 1 - Clears CABLE_DET_C_ST	
CABLE_DET_D_CLR			SC
0x71	0000000**0**	Clear bit for Port D +5V cable detection interrupt signal. 0 - Does not clear 1 - Clears CABLE_DET_D_ST	
HDMI_ENCRPT_A_MB1			R/W
0x73	**0**0000000	INT1 interrupt mask for Port A Encryption detection interrupt. When set the Port A Encryption detection interrupt will trigger the INT1 interrupt and HDMI_ENCRPT_A_ST will indicate the interrupt status. 0 - Disables Port A HDMI Encryption detection interrupt for INT1 1 - Enables Port A HDMI Encryption detection interrupt for INT1	

Reg	Bits	Description	
HDMI_ENCRPT_B_MB1			R/W
0x73	0<u>0</u>000000	INT1 interrupt mask for Port B Encryption detection interrupt. When set the Port B Encryption detection interrupt will trigger the INT1 interrupt and HDMI_ENCRPT_B_ST will indicate the interrupt status. 0 - Disables Port B HDMI Encryption detection interrupt for INT1 1 - Enables Port B HDMI Encryption detection interrupt for INT1	
HDMI_ENCRPT_C_MB1			R/W
0x73	00<u>0</u>00000	INT1 interrupt mask for Port C Encryption detection interrupt. When set the Port C Encryption detection interrupt will trigger the INT1 interrupt and HDMI_ENCRPT_C_ST will indicate the interrupt status. 0 - Disables Port C HDMI Encryption detection interrupt for INT1 1 - Enables Port C HDMI Encryption detection interrupt for INT1	
HDMI_ENCRPT_D_MB1			R/W
0x73	000<u>0</u>0000	INT1 interrupt mask for Port D Encryption detection interrupt. When set the Port D Encryption detection interrupt will trigger the INT1 interrupt and HDMI_ENCRPT_D_ST will indicate the interrupt status. 0 - Disables Port D HDMI Encryption detection interrupt for INT1 1 - Enables Port D HDMI Encryption detection interrupt for INT1	
CABLE_DET_A_MB1			R/W
0x73	0000<u>0</u>000	INT1 interrupt mask for Port A +5V cable detection interrupt. When set the Port A +5V cable detection interrupt will trigger the INT1 interrupt and CABLE_DET_A_ST will indicate the interrupt status. 0 - Disables Port A +5V Cable Detection interrupt for INT1 1 - Enables Port A +5V Cable Detection interrupt for INT1	
CABLE_DET_B_MB1			R/W
0x73	00000<u>0</u>00	INT1 interrupt mask for Port B +5V cable detection interrupt. When set the Port B +5V cable detection interrupt will trigger the INT1 interrupt and CABLE_DET_B_ST will indicate the interrupt status. 0 - Disables Port B +5V Cable Detection interrupt for INT1 1 - Enables Port B +5V Cable Detection interrupt for INT1	
CABLE_DET_C_MB1			R/W
0x73	000000<u>0</u>0	INT1 interrupt mask for Port C +5V cable detection interrupt. When set the Port C +5V cable detection interrupt will trigger the INT1 interrupt and CABLE_DET_C_ST will indicate the interrupt status. 0 - Disables Port C +5V Cable Detection interrupt for INT1 1 - Enables Port C +5V Cable Detection interrupt for INT1	
CABLE_DET_D_MB1			R/W
0x73	0000000<u>0</u>	INT1 interrupt mask for Port D +5V cable detection interrupt. When set the Port D +5V cable detection interrupt will trigger the INT1 interrupt and CABLE_DET_D_ST will indicate the interrupt status. 0 - Disables Port D +5V Cable Detection interrupt for INT1 1 - Enables Port D +5V Cable Detection interrupt for INT1	
VIDEO_3D_RAW			R
0x74	00000<u>0</u>00	Raw status of the Video 3D signal. 0 - Video 3D not detected 1 - Video 3D detected	
VIDEO_3D_ST			R
0x75	00000<u>0</u>00	Latched status for the Video 3D interupt. Once set this bit will remain high until the interrupt has been cleared via VIDEO_3D_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - VIDEO_3D_RAW has not changed. An interrupt has not been generated. 1 - VIDEO_3D_RAW has changed. An interrupt has been generated.	
VIDEO_3D_CLR			SC
0x76	00000<u>0</u>00	Clear bit for Video 3D Interrupt 0 - Does not clear VIDEO_3D_ST 1 - Clears VIDEO_3D_ST	
VIDEO_3D_MB2			R/W
0x77	00000<u>0</u>00	INT2 interrupt mask for Video 3D interrupt. When set the Video 3D interrupt will trigger the INT2 interrupt and VIDEO_3D_ST will indicate the interrupt status. 0 - Disables Video 3D interrupt on INT2 1 - Enables Video 3D interrupt on INT2	

Reg	Bits	Description	
VIDEO_3D_MB1			R/W
0x78	00000000	INT1 interrupt mask for Video 3D interrupt. When set the Video 3D interrupt will trigger the INT1 interrupt and VIDEO_3D_ST will indicate the interrupt status. 0 - Disables Video 3D interrupt on INT1 1 - Enables Video 3D interrupt on INT1	
NEW_ISRC2_PCKT_RAW			R
0x79	00000000	Status of the New ISRC2 interrupt signal. When set to 1 it indicates a that an ISRC2 packet has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_ISRC2_PCKT_CLR. 0 - No new ISRC2 packet received 1 - ISRC2 packet with new content received	
NEW_ISRC1_PCKT_RAW			R
0x79	00000000	Status of the New ISRC1 interrupt signal. When set to 1 it indicates a that an ISRC1 packet has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_ISRC1_PCKT_CLR. 0 - No new ISRC1 packet received 1 - ISRC1 packet with new content received	
NEW_ACP_PCKT_RAW			R
0x79	00000000	Status of the New ACP Packet interrupt signal. When set to 1 it indicates a that an ACP packet has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_ACP_PCKT_CLR. 0 - No new ACP packet received 1 - ACP packet with new content received	
NEW_VS_INFO_RAW			R
0x79	00000000	Status of the New Vendor Specific Infoframe interrupt signal. When set to 1 it indicates a that an Vendor Specific Infoframe has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_VS_INFO_CLR. 0 - No new VS packet received 1 - VS packet with new content received	
NEW_MS_INFO_RAW			R
0x79	00000000	Status of the New MPEG Source Infoframe interrupt signal. When set to 1 it indicates a that an MPEG Source Infoframe has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_MS_INFO_CLR. 0 - No new MPEG source InfoFrame received 1 - MPEG source InfoFrame with new content received	
NEW_SPD_INFO_RAW			R
0x79	00000000	Status of the New Source Product Descriptor Packet interrupt signal. When set to 1 it indicates a that an Source Product Descriptor packet has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_SPD_INFO_CLR. 0 - No new SPD InfoFrame received 1 - SPD InfoFrame with new content received	
NEW_AUDIO_INFO_RAW			R
0x79	00000000	Status of the New Audio Infoframe interrupt signal. When set to 1 it indicates a that an Audio Infoframe has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_AUDIO_INFO_CLR. 0 - No new audio InfoFrame received 1 - Audio InfoFrame with new content received	
NEW_AVI_INFO_RAW			R
0x79	00000000	Status of the New AVI Infoframe interrupt signal. When set to 1 it indicates that an AVI Infoframe has been received with new contents. Once set this bit will remain high until the interrupt has been cleared via NEW_AVI_INFO_CLR. 0 - No new AVI InfoFrame received 1 - AVI InfoFrame with new content received	
NEW_ISRC2_PCKT_ST			R
0x7A	00000000	Latched status for the New ISRC2 Packet interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_ISRC2_PCKT_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No new ISRC2 packet received. An interrupt has not been generated. 1 - ISRC2 packet with new content received. An interrupt has been generated.	
NEW_ISRC1_PCKT_ST			R
0x7A	00000000	Latched status for the New ISRC1 Packet interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_ISRC1_PCKT_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No new ISRC1 packet received. An interrupt has not been generated. 1 - ISRC1 packet with new content received. An interrupt has been generated.	

Reg	Bits	Description	
NEW_ACP_PCKT_ST			R
0x7A	00**0**00000	Latched status for the New ACP Packet interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_ACP_PCKT_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No new ACP packet received. An interrupt has not been generated. 1 - ACP packet with new content received. An interrupt has been generated.	
NEW_VS_INFO_ST			R
0x7A	000**0**0000	Latched status for the New Vendor Specific Infoframe interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_VS_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No new VS packet received. An interrupt has not been generated. 1 - VS packet with new content received. An interrupt has been generated.	
NEW_MS_INFO_ST			R
0x7A	0000**0**000	Latched status for the New MPEG Source Infoframe interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_MS_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No new MPEG Source InfoFrame received. Interrupt has not been generated. 1 - MPEG Source InfoFrame with new content received. Interrupt has been generated.	
NEW_SPD_INFO_ST			R
0x7A	00000**0**00	Latched status for the New Source Product Descriptor Infoframe interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_SPD_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No new SPD InfoFrame received. Interrupt has not been generated. 1 - SPD InfoFrame with new content received. Interrupt has been generated.	
NEW_AUDIO_INFO_ST			R
0x7A	000000**0**0	Latched status for the New Audio Infoframe interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_AUDIO_INFO_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No new Audio InfoFrame received. Interrupt has not been generated. 1 - Audio InfoFrame with new content received. Interrupt has been generated.	
NEW_AVI_INFO_ST			R
0x7A	0000000**0**	Latched status for the NEW_AVI_INFO_RAW. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. Once set this bit will remain high until the interrupt has been cleared via NEW_AVI_INFO_CLR. 0 - NEW_AVI_INFO_RAW has not changed state 1 - NEW_AVI_INFO_RAW has changed state	
NEW_ISRC2_PCKT_CLR			SC
0x7B	**0**0000000	Clear bit for NEW_ISRC2_PCKT_RAW and NEW_ISRC2_PCKT_ST bits. 0 - No function 1 - Clear NEW_ISRC2_PCKT_RAW and NEW_ISRC2_PCKT_ST	
NEW_ISRC1_PCKT_CLR			SC
0x7B	0**0**000000	Clear bit for NEW_ISRC1_PCKT_RAW and NEW_ISCR1_PCKT_ST bits. 0 - No function 1 - Clear NEW_ISRC1_PCKT_RAW and NEW_ISRC1_PCKT_ST	
NEW_ACP_PCKT_CLR			SC
0x7B	00**0**00000	Clear bit for NEW_ACP_PCKT_RAW and NEW_ACP_PCKT_ST bits. 0 - No function 1 - Clear NEW_ACP_PCKT_RAW and NEW_ACP_PCKT_ST	
NEW_VS_INFO_CLR			SC
0x7B	000**0**0000	Clear bit for NEW_VS_INFO_RAW and NEW_VS_INFO_ST bits. 0 - No function 1 - Clear NEW_VS_INFO_RAW and NEW_VS_INFO_ST	
NEW_MS_INFO_CLR			SC
0x7B	0000**0**000	Clear bit for NEW_MS_INFO_RAW and NEW_MS_INFO_ST bits. 0 - No function 1 - Clear NEW_MS_INFO_RAW and NEW_MS_INFO_ST	

Reg	Bits	Description	
NEW_SPD_INFO_CLR			SC
0x7B	00000000	Clear bit for NEW_SPD_INFO_RAW and NEW_SPD_INFO_ST bits. 0 - No function 1 - Clear NEW_SPD_INFO_RAW and NEW_SPD_INFO_ST	
NEW_AUDIO_INFO_CLR			SC
0x7B	00000000	Clear bit for NEW_AUDIO_INFO_RAW and NEW_AUDIO_INFO_ST bits. 0 - No function 1 - Clear NEW_AUDIO_INFO_RAW and NEW_AUDIO_INFO_ST	
NEW_AVI_INFO_CLR			SC
0x7B	00000000	Clear bit for NEW_AVI_INFO_RAW and NEW_AVI_INFO_ST bits. 0 - No function 1 - Clear NEW_AVI_INFO_RAW and NEW_AVI_INFO_ST	
NEW_ISRC2_PCKT_MB2			R/W
0x7C	00000000	INT2 interrupt mask for New ISRC2 Packet interrupt. When set the New ISRC2 interrupt will trigger the INT2 interrupt and NEW_ISRC2_ST will indicate the interrupt status. 0 - Disables New ISRC2 Packet interrupt for INT2 1 - Enables New ISRC2 Packet interrupt for INT2	
NEW_ISRC1_PCKT_MB2			R/W
0x7C	00000000	INT2 interrupt mask for New ISRC1 Packet interrupt. When set the New ISRC2 interrupt will trigger the INT2 interrupt and NEW_ISRC1_ST will indicate the interrupt status. 0 - Disables New ISRC1 Packet interrupt for INT2 1 - Enables New ISRC1 Packet interrupt for INT2	
NEW_ACP_PCKT_MB2			R/W
0x7C	00000000	INT2 interrupt mask for New ACP Packet interrupt. When set the New ACP interrupt will trigger the INT2 interrupt and NEW_ACP_ST will indicate the interrupt status. 0 - Disables New ACP Packet interrupt for INT2 1 - Enables New ACP Packet interrupt for INT2	
NEW_VS_INFO_MB2			R/W
0x7C	00000000	INT2 interrupt mask for New Vendor Specific Infoframe interrupt. When set the New Vendor Specific Infoframe interrupt will trigger the INT2 interrupt and NEW_VS_INFO_ST will indicate the interrupt status. 0 - Disables New VS Infoframe interrupt for INT2 1 - Enables New VS Infoframe interrupt for INT2	
NEW_MS_INFO_MB2			R/W
0x7C	00000000	INT2 interrupt mask for New MPEG Source Infoframe interrupt. When set the New MPEG Source Infoframe interrupt will trigger the INT2 interrupt and NEW_SPD_INFO_ST will indicate the interrupt status. 0 - Disables New MS Infoframe interrupt for INT2 1 - Enables New MS Infoframe interrupt for INT2	
NEW_SPD_INFO_MB2			R/W
0x7C	00000000	INT2 interrupt mask for New Source Product Descriptor Infoframe interrupt. When set the New Source Product Descriptor Infoframe interrupt will trigger the INT2 interrupt and NEW_SPD_INFO_ST will indicate the interrupt status. 0 - Disables New SPD Infoframe interrupt for INT2 1 - Enables New SPD Infoframe interrupt for INT2	
NEW_AUDIO_INFO_MB2			R/W
0x7C	00000000	INT2 interrupt mask for New Audio Infoframe interrupt. When set the New Audio Infoframe interrupt will trigger the INT2 interrupt and NEW_AUDIO_INFO_ST will indicate the interrupt status. 0 - Disables New Audio Infoframe interrupt for INT2 1 - Enables New Audio Infoframe interrupt for INT2	
NEW_AVI_INFO_MB2			R/W
0x7C	00000000	INT2 interrupt mask for New AVI Infoframe detection interrupt. When set a new AVI InfoFrame detection event will cause NEW_AVI_INFO_ST to be set and an interrupt will be generated on INT2. 0 - Disables New SPD Infoframe interrupt for INT2 1 - Enables New SPD Infoframe interrupt for INT2	

Reg	Bits	Description
NEW_ISRC2_PCKT_MB1		R/W
0x7D	0xxxxxxx	INT1 interrupt mask for New ISRC2 Packet interrupt. When set the New ISRC2 interrupt will trigger the INT1 interrupt and NEW_ISRC2_ST will indicate the interrupt status. 0 - Disables New ISRC2 Packet interrupt for INT1 1 - Enables New ISRC2 Packet interrupt for INT1
NEW_ISRC1_PCKT_MB1		R/W
0x7D	x0xxxxxx	INT1 interrupt mask for New ISRC1 Packet interrupt. When set the New ISRC2 interrupt will trigger the INT1 interrupt and NEW_ISRC1_ST will indicate the interrupt status. 0 - Disables New ISRC1 Packet interrupt for INT1 1 - Enables New ISRC1 Packet interrupt for INT1
NEW_ACP_PCKT_MB1		R/W
0x7D	xx0xxxxx	INT1 interrupt mask for New ACP Packet interrupt. When set the New ACP interrupt will trigger the INT1 interrupt and NEW_ACP_ST will indicate the interrupt status. 0 - Disables New ACP Packet interrupt for INT1 1 - Enables New ACP Packet interrupt for INT1
NEW_VS_INFO_MB1		R/W
0x7D	xxx0xxxx	INT1 interrupt mask for New Vendor Specific Infoframe interrupt. When set the New Vendor Specific Infoframe interrupt will trigger the INT1 interrupt and NEW_VS_INFO_ST will indicate the interrupt status. 0 - Disables New VS Infoframe interrupt for INT1 1 - Enables New VS Infoframe interrupt for INT1
NEW_MS_INFO_MB1		R/W
0x7D	xxxx0xxx	INT1 interrupt mask for New MPEG Source Infoframe interrupt. When set the New MPEG Source Infoframe interrupt will trigger the INT1 interrupt and NEW_SPD_INFO_ST will indicate the interrupt status. 0 - Disables New MS Infoframe interrupt for INT1 1 - Enables New MS Infoframe interrupt for INT1
NEW_SPD_INFO_MB1		R/W
0x7D	xxxxx0xx	INT1 interrupt mask for New Source Product Descriptor Infoframe interrupt. When set the New Source Product Descriptor Infoframe interrupt will trigger the INT1 interrupt and NEW_SPD_INFO_ST will indicate the interrupt status. 0 - Disables New SPD Infoframe interrupt for INT1 1 - Enables New SPD Infoframe interrupt for INT1
NEW_AUDIO_INFO_MB1		R/W
0x7D	xxxxxx0x	INT1 interrupt mask for New Audio Infoframe interrupt. When set the New Audio Infoframe interrupt will trigger the INT1 interrupt and NEW_AUDIO_INFO_ST will indicate the interrupt status. 0 - Disables New Audio Infoframe interrupt for INT1 1 - Enables New Audio Infoframe interrupt for INT1
NEW_AVI_INFO_MB1		R/W
0x7D	xxxxxxx0	INT1 interrupt mask for New AVI Infoframe detection interrupt. When set a new AVI InfoFrame detection event will cause NEW_AVI_INFO_ST to be set and an interrupt will be generated on INT1. 0 - Disable new AVI Infoframe interrupt for INT1 1 - Enable new AVI Infoframe interrupt for INT1
PACKET_ERROR_RAW		R
0x7E	xxxxx0xx	Status of the Packet Error interrupt signal. When set to 1 it indicates a that an any packet has been received with an uncorrectable EEC error in either the header or body. Once set, this bit will remain high until it is cleared via PACKET_ERROR_CLR. 0 - No uncorrectable error detected in packet header 1 - Uncorrectable error detected in an unknown packet (error in packet header)
NEW_GAMUT_MDATA_RAW		R
0x7E	xxxxxxx0	Status of the New Gamut Metadata Packet interrupt signal. When set to 1 it indicates a that a Gamut Metadata packet has been received with new contents. Once set, this bit will remain high until it is cleared via NEW_GAMUT_MDATA_PCKT_CLR. 0 - No new Gamut metadata packet received or no change has taken place 1 - New Gamut metadata packet received that triggered this interrupt
PACKET_ERROR_ST		R
0x7F	xxxxx0xx	Latched status for the Packet Error interrupt. Once set this bit will remain high until the interrupt has been cleared via PACKET_ERROR_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No uncorrectable error detected in packet header. An interrupt has not been generated. 1 - Uncorrectable error detected in an unknown packet (in packet header). An interrupt has been generated.

Reg	Bits	Description
NEW_GAMUT_MDATA_ST		R
0x7F	0000000<u>0</u>	Latched status for the New Gamut Metadata Packet interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_GAMUT_MDATA_PCKT_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No new Gamut metadata packet received or no change has taken place. An interrupt has not been generated. 1 - New Gamut metadata packet received. An interrupt has been generated.
PACKET_ERROR_CLR		SC
0x80	00000<u>0</u>00	Clear bit for Packet Error interrupt. 0 - Does not clear PACKET_ERROR_ST 1 - Clears PACKET_ERROR_ST
NEW_GAMUT_MDATA_CLR		SC
0x80	0000000<u>0</u>	Clear bit for New Gamut Metadata Packet interrupt. 0 - Does not clear NEW_GAMUT_MDATA_ST 1 - Clears NEW_GAMUT_MDATA_ST
PACKET_ERROR_MB2		R/W
0x81	00000<u>0</u>00	INT2 interrupt mask for Packet Error interrupt. When set the Audio Packet Error interrupt will trigger the INT2 interrupt and PACKET_ERROR_ST will indicate the interrupt status. 0 - Disables Packet Error interrupt for INT2 1 - Enables Packet Error interrupt for INT2
NEW_GAMUT_MDATA_MB2		R/W
0x81	0000000<u>0</u>	INT2 interrupt mask for New Gamut Metadata packet interrupt. When set the New Gamut Metadata packet interrupt will trigger the INT2 interrupt and NEW_GAMUT_MDATA_PCKT_ST will indicate the interrupt status. 0 - Disables New Gamut metadata Infoframe interrupt for INT2 1 - Enables New SPD Infoframe interrupt for INT2
PACKET_ERROR_MB1		R/W
0x82	00000<u>0</u>00	INT1 interrupt mask for Packet Error interrupt. When set the Audio Packet Error interrupt will trigger the INT1 interrupt and PACKET_ERROR_ST will indicate the interrupt status. 0 - Disables Packet Error interrupt for INT1 1 - Enables Packet Error interrupt for INT1
NEW_GAMUT_MDATA_MB1		R/W
0x82	0000000<u>0</u>	INT1 interrupt mask for New Gamut Metadata packet interrupt. When set the New Gamut Metadata packet interrupt will trigger the INT1 interrupt and NEW_GAMUT_MDATA_PCKT_ST will indicate the interrupt status. 0 - Disables New Gamut METADATA Infoframe interrupt for INT1 1 - Enables New SPD Infoframe interrupt for INT1
DEEP_COLOR_CHNG_RAW		R
0x83	<u>0</u>0000000	Status of Deep Color Mode Changed Interrupt signal. When set to 1 it indicates a change in the deep color mode has been detected. Once set, this bit will remain high until it is cleared via DEEP_COLOR_CHNG_CLR. 0 - Deep color mode has not changed 1 - Change in deep color triggered this interrupt
VCLK_CHNG_RAW		R
0x83	0<u>0</u>000000	Status of Video Clock Changed Interrupt signal. When set to 1 it indicates that irregular or missing pulses are detected in the TMDS clock. Once set, this bit will remain high until it is cleared via VCLK_CHNG_CLR. 0 - No irregular or missing pulse detected in TMDS clock 1 - Irregular or missing pulses detected in TMDS clock triggered this interrupt
NEW_TMDS_FRQ_RAW		R
0x83	000000<u>0</u>0	Status of New TMDS Frequency interrupt signal. When set to 1 it indicates the TMDS frequency has changed by more than the tolerance set in FREQTOLERANCE[3:0]. Once set, this bit will remain high until it is cleared via NEW_TMDS_FREQ_CLR. 0 - TMDS frequency has not changed by more than tolerance set in FREQTOLERANCE[3:0] in the HDMI Map 1 - TMDS frequency has changed by more than tolerance set in FREQTOLERANCE[3:0] in the HDMI Map
DEEP_COLOR_CHNG_ST		R
0x84	<u>0</u>0000000	Latched status of Deep Color Mode Change Interrupt. Once set this bit will remain high until the interrupt has been cleared via DEEP_COLOR_CHNG_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - Deep color mode has not changed 1 - Change in deep color has been detected

Reg	Bits	Description	
VCLK_CHNG_ST			R
0x84	00000000	Latched status of Video Clock Change Interrupt. Once set this bit will remain high until the interrupt has been cleared via VCLK_CHNG_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - No irregular or missing pulse detected in TMDS clock 1 - Irregular or missing pulses detected in TMDS clock	
NEW_TMDS_FRQ_ST			R
0x84	00000000	Latched status of New TMDS Frequency Interrupt. Once set this bit will remain high until the interrupt has been cleared via NEW_TMDS_FREQ_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - TMDS frequency has not changed by more than tolerance 1 - TMDS frequency has changed by more than tolerance	
DEEP_COLOR_CHNG_CLR			SC
0x85	00000000	Clear bit for the Deep Color Mode Change Interrupt. 0 - Does not clear DEEP_COLOR_CHNG_ST 1 - Clears DEEP_COLOR_CHNG_ST	
VCLK_CHNG_CLR			SC
0x85	00000000	Clear bit for the Video Clock Change Interrupt. 0 - Does not clear VCLK_CHNG_ST 1 - Clears VCLK_CHNG_ST	
NEW_TMDS_FRQ_CLR			SC
0x85	00000000	Clear bit for the New TMDS Frequency Interrupt. 0 - Does not clear NEW_TMDS_FRQ_ST 1 - Clears NEW_TMDS_FRQ_ST	
DEEP_COLOR_CHNG_MB2			R/W
0x86	00000000	INT2 interrupt mask for Deep Color Mode Changed interrupt. When set the Deep Color Mode Changed interrupt will trigger the INT2 interrupt and DEEP_COLOR_CHNG_ST will indicate the interrupt status. 0 - Disable Deep Color Mode Changed interrupt on INT2 1 - Enable Deep Color Mode Changed interrupt on INT2	
DEEP_COLOR_CHNG_MB1			R/W
0x87	00000000	INT1 interrupt mask for Deep Color Mode Changed interrupt. When set the Deep Color Mode Changed interrupt will trigger the INT1 interrupt and DEEP_COLOR_CHNG_ST will indicate the interrupt status. 0 - Disable Deep Color Mode Change interrupt on INT1 1 - Enable Deep Color Mode interrupt on INT1	
VCLK_CHNG_MB1			R/W
0x87	00000000	INT1 interrupt mask for Video Clock Changed interrupt. When set the Video Clock Changed interrupt will trigger the INT1 interrupt and VCLK_CHNG_ST will indicate the interrupt status. 0 - Disable Video Clock Change interrupt on INT1 1 - Enable Video Clock Change interrupt on INT1	
NEW_TMDS_FRQ_MB1			R/W
0x87	00000000	INT1 interrupt mask for New TMDS Frequency interrupt. When set the New TMDS Frequency interrupt will trigger the INT1 interrupt and NEW_TMDS_FREQ_ST will indicate the interrupt status. 0 - Disable New TMDS Frequency interrupt on INT1 1 - Enable New TMDS Frequency interrupt on INT1	
MS_INF_CKS_ERR_RAW			R
0x88	00000000	Status of MPEG Source Infoframe Checksum Error interrupt signal. When set to 1 it indicates that a checksum error has been detected for an MPEG Source Infoframe. Once set, this bit will remain high until it is cleared via MS_INF_CKS_ERR_CLR. 0 - No MPEG source infoframe checksum error has occurred 1 - An MPEG source infoframe checksum error has occurred	
SPD_INF_CKS_ERR_RAW			R
0x88	00000000	Status of SPD Infoframe Checksum Error interrupt signal. When set to 1 it indicates that a checksum error has been detected for an SPD Infoframe. Once set, this bit will remain high until it is cleared via ASPD_INF_CKS_ERR_CLR. 0 - No SPD infoframe checksum error has occurred 1 - An SPD infoframe checksum error has occurred	

Reg	Bits	Description
AUD_INF_CKS_ERR_RAW		R
0x88	00**0**00000	Status of Audio Infoframe Checksum Error interrupt signal. When set to 1 it indicates that a checksum error has been detected for an Audio Infoframe. Once set, this bit will remain high until it is cleared via AUDIO_INF_CKS_ERR_CLR. 0 - No Audio infoframe checksum error has occurred 1 - An Audio infoframe checksum error has occurred
AVI_INF_CKS_ERR_RAW		R
0x88	000**0**0000	Status of AVI Infoframe Checksum Error interrupt signal. When set to 1 it indicates that a checksum error has been detected for an AVI InfoFrame. Once set, this bit will remain high until it is cleared via AVI_INF_CKS_ERR_CLR. 0 - No AVI infoframe checksum error has occurred 1 - An AVI infoframe checksum error has occurred
AKSV_UPDATE_A_RAW		R
0x88	0000**0**000	Status of Port A AKSV Update interrupt signal. When set to 1, it indicates that the transmitter has written its AKSV into the HDCP registers for Port A. Once set, this bit will remain high until it is cleared via AKSV_UPDATE_A_CLR. 0 - No AKSV updates on Port A 1 - Detected a write access to the AKSV register on Port A
AKSV_UPDATE_B_RAW		R
0x88	00000**0**00	Status of Port B AKSV Update interrupt signal. When set to 1, it indicates that the transmitter has written its AKSV into the HDCP registers for Port B. Once set, this bit will remain high until it is cleared via AKSV_UPDATE_B_CLR. 0 - No AKSV updates on Port B 1 - Detected a write access to the AKSV register on Port B
AKSV_UPDATE_C_RAW		R
0x88	000000**0**0	Status of Port C AKSV Update interrupt signal. When set to 1, it indicates that the transmitter has written its AKSV into the HDCP registers for Port C. Once set, this bit will remain high until it is cleared via AKSV_UPDATE_C_CLR. 0 - No AKSV updates on Port C 1 - Detected a write access to the AKSV register on Port C
AKSV_UPDATE_D_RAW		R
0x88	0000000**0**	Status of Port D AKSV Update interrupt signal. When set to 1, it indicates that the transmitter has written its AKSV into the HDCP registers for Port D. Once set, this bit will remain high until it is cleared via AKSV_UPDATE_D_CLR. 0 - No AKSV updates on Port D 1 - Detected a write access to the AKSV register on Port D
MS_INF_CKS_ERR_ST		R
0x89	**0**0000000	Latched status of MPEG Source Infoframe Checksum Error interrupt. Once set this bit will remain high until the interrupt has been cleared via MS_INF_CKS_ERR_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No change in MPEG source infoframe checksum error 1 - An MPEG source infoframe checksum error has triggered this interrupt
SPD_INF_CKS_ERR_ST		R
0x89	0**0**000000	Latched status of SPD Infoframe Checksum Error interrupt. Once set this bit will remain high until the interrupt has been cleared via SPD_INF_CKS_ERR_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No change in SPD infoframe checksum error 1 - An SPD infoframe checksum error has triggered this interrupt
AUD_INF_CKS_ERR_ST		R
0x89	00**0**00000	Latched status of Audio Infoframe Checksum Error interrupt. Once set this bit will remain high until the interrupt has been cleared via AUDIO_INF_CKS_ERR_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No change in Audio infoframe checksum error 1 - An Audio infoframe checksum error has triggered this interrupt
AVI_INF_CKS_ERR_ST		R
0x89	000**0**0000	Latched status of AVI Infoframe Checksum Error interrupt. Once set this bit will remain high until the interrupt has been cleared via AVI_INF_CKS_ERR_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No change in AVI infoframe checksum error 1 - An AVI infoframe checksum error has triggered this interrupt
AKSV_UPDATE_A_ST		R
0x89	0000**0**000	Latched status of Port A AKSV Update Interrupt. Once set this bit will remain high until the interrupt has been cleared via AKSV_UPDATE_A_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - No AKSV updates on port A 1 - Detected a write access to the AKSV register on port A

Reg	Bits	Description	
AKSV_UPDATE_B_ST			R
0x89	000000<u>0</u>00	Latched status of Port B AKSV Update Interrupt. Once set this bit will remain high until the interrupt has been cleared via AKSV_UPDATE_B_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - No AKSV updates on port B 1 - Detected a write access to the AKSV register on port B	
AKSV_UPDATE_C_ST			R
0x89	0000000<u>0</u>0	Latched status of Port C AKSV Update Interrupt. Once set this bit will remain high until the interrupt has been cleared via AKSV_UPDATE_C_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - No AKSV updates on port C 1 - Detected a write access to the AKSV register on port C	
AKSV_UPDATE_D_ST			R
0x89	00000000<u>0</u>	Latched status of Port D AKSV Update Interrupt. Once set this bit will remain high until the interrupt has been cleared via AKSV_UPDATE_D_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - No AKSV updates on port D 1 - Detected a write access to the AKSV register on port D	
MS_INF_CKS_ERR_CLR			SC
0x8A	<u>0</u>0000000	Clear bit for the MPEG Source Infoframe Checksum Error Interrupt. 0 - Does not clear MS_INF_CKS_ERR_ST 1 - Clears MS_INF_CKS_ERR_ST	
SPD_INF_CKS_ERR_CLR			SC
0x8A	0<u>0</u>000000	Clear bit for the SPD Infoframe Checksum Error Interrupt. 0 - Does not clear 1 - Clears SPD_INF_CKS_ERR_ST	
AUD_INF_CKS_ERR_CLR			SC
0x8A	00<u>0</u>00000	Clear bit for the Audio Infoframe Checksum Error Interrupt. 0 - Does not clear AUD_INF_CKS_ERR_ST 1 - Clears AUD_INF_CKS_ERR_ST	
AVI_INF_CKS_ERR_CLR			SC
0x8A	000<u>0</u>0000	Clear bit for the AVI Infoframe Checksum Error Interrupt. 0 - Does not clear AVI_INF_CKS_ERR_ST 1 - Clears AVI_INF_CKS_ERR_ST	
AKSV_UPDATE_A_CLR			SC
0x8A	0000<u>0</u>000	Clear bit for the Port A AKSV Update Interrupt. 0 - Does not clear 1 - Clears AKSV_UPDATE_A_ST	
AKSV_UPDATE_B_CLR			SC
0x8A	000000<u>0</u>00	Clear bit for the Port B AKSV Update Interrupt. 0 - Does not clear AKSV_UPDATE_B_ST 1 - Clears AKSV_UPDATE_B_ST	
AKSV_UPDATE_C_CLR			SC
0x8A	0000000<u>0</u>0	Clear bit for the Port C AKSV Update Interrupt. 0 - Does not clear AKSV_UPDATE_C_ST 1 - Clears AKSV_UPDATE_C_ST	
AKSV_UPDATE_D_CLR			SC
0x8A	00000000<u>0</u>	Clear bit for the Port D AKSV Update Interrupt. 0 - Does not clear AKSV_UPDATE_D_ST 1 - Clears AKSV_UPDATE_D_ST	
MS_INF_CKS_ERR_MB2			R/W
0x8B	<u>0</u>0000000	INT2 interrupt mask for MPEG Source Infoframe Checksum Error interrupt. When set the MPEG Source Infoframe Checksum Error interrupt will trigger the INT2 interrupt and MS_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable MPEG Source Infoframe Checksum Error interrupt on INT2 1 - Enable MPEG Source Infoframe Checksum Error interrupt on INT2	

Reg	Bits	Description
SPD_INF_CKS_ERR_MB2		R/W
0x8B	0<u>0</u>000000	INT2 interrupt mask for SPD Infoframe Checksum Error interrupt. When set the SPD Infoframe Checksum Error interrupt will trigger the INT2 interrupt and SPD_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable SPD Infoframe Checksum Error interrupt on INT2 1 - Enable SPD Infoframe Checksum Error interrupt on INT2
AUD_INF_CKS_ERR_MB2		R/W
0x8B	00<u>0</u>00000	INT2 interrupt mask for Audio Infoframe Checksum Error interrupt. When set the Audio Infoframe Checksum Error interrupt will trigger the INT2 interrupt and AUDIO_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable Audio Infoframe Checksum Error interrupt on INT2 1 - Enable Audio Infoframe Checksum Error interrupt on INT2
AVI_INF_CKS_ERR_MB2		R/W
0x8B	000<u>0</u>0000	INT2 interrupt mask for AVI Infoframe Checksum Error interrupt. When set the AVI Infoframe Checksum Error interrupt will trigger the INT2 interrupt and AVI_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable AVI Infoframe Checksum Error interrupt on INT2 1 - Enable AVI Infoframe Checksum Error interrupt on INT2
MS_INF_CKS_ERR_MB1		R/W
0x8C	<u>0</u>0000000	INT1 interrupt mask for MPEG Source Infoframe Checksum Error interrupt. When set the MPEG Source Infoframe Checksum Error interrupt will trigger the INT1 interrupt and MS_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable SPD Infoframe Checksum Error interrupt on INT1 1 - Enable SPD Infoframe Checksum Error interrupt on INT1
SPD_INF_CKS_ERR_MB1		R/W
0x8C	0<u>0</u>000000	INT1 interrupt mask for SPD Infoframe Checksum Error interrupt. When set the SPD Infoframe Checksum Error interrupt will trigger the INT1 interrupt and SPD_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable SPD Infoframe Checksum Error interrupt on INT1 1 - Enable SPD Infoframe Checksum Error interrupt on INT1
AUD_INF_CKS_ERR_MB1		R/W
0x8C	00<u>0</u>00000	INT1 interrupt mask for Audio Infoframe Checksum Error interrupt. When set the Audio Infoframe Checksum Error interrupt will trigger the INT1 interrupt and AUDIO_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable Audio Infoframe Checksum Error interrupt on INT1 1 - Enable Audio Infoframe Checksum Error interrupt on INT1
AVI_INF_CKS_ERR_MB1		R/W
0x8C	000<u>0</u>0000	INT1 interrupt mask for AVI Infoframe Checksum Error interrupt. When set the AVI Infoframe Checksum Error interrupt will trigger the INT1 interrupt and AVI_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable AVI Infoframe Checksum Error interrupt on INT1 1 - Enable AVI Infoframe Checksum Error interrupt on INT1
AKSV_UPDATE_A_MB1		R/W
0x8C	0000<u>0</u>000	INT1 interrupt mask for Port A AKSV Update interrupt. When set the Port A AKSV Update interrupt will trigger the INT1 interrupt and AKSV_UPDATE_A_ST will indicate the interrupt status. 0 - Disable Port A AKSV Update interrupt on INT1 1 - Enable Port A AKSV Update interrupt on INT1
AKSV_UPDATE_B_MB1		R/W
0x8C	00000<u>0</u>00	INT1 interrupt mask for Port B AKSV Update interrupt. When set the Port B AKSV Update interrupt will trigger the INT1 interrupt and AKSV_UPDATE_B_ST will indicate the interrupt status. 0 - Disable Port B AKSV Update interrupt on INT1 1 - Enable Port B AKSV Update interrupt on INT1
AKSV_UPDATE_C_MB1		R/W
0x8C	000000<u>0</u>0	INT1 interrupt mask for Port C AKSV Update interrupt. When set the Port C AKSV Update interrupt will trigger the INT1 interrupt and AKSV_UPDATE_C_ST will indicate the interrupt status. 0 - Disable Port C AKSV Update interrupt on INT1 1 - Enable Port C AKSV Update interrupt on INT1
AKSV_UPDATE_D_MB1		R/W
0x8C	0000000<u>0</u>	INT1 interrupt mask for Port D AKSV Update interrupt. When set the Port D AKSV Update interrupt will trigger the INT1 interrupt and AKSV_UPDATE_D_ST will indicate the interrupt status. 0 - Disable Port D AKSV Update interrupt on INT1 1 - Enable Port D AKSV Update interrupt on INT1

Reg	Bits	Description
RI_EXPIRED_A_RAW		R
0x8D	0000000	Status of port A Ri expired Interrupt signal. When set to 1 it indicates that HDCP cipher Ri value for port A expired. Once set, this bit will remain high until it is cleared via RI_EXPIRED_A_CLR. 0 - No Ri expired on port 1 - Ri expired on port
RI_EXPIRED_B_RAW		R
0x8D	000000	Status of port B Ri expired Interrupt signal. When set to 1 it indicates that HDCP cipher Ri value for port B expired. Once set, this bit will remain high until it is cleared via RI_EXPIRED_A_CLR. 0 - No Ri expired on port 1 - Ri expired on port
RI_EXPIRED_C_RAW		R
0x8D	00000	Status of port C Ri expired Interrupt signal. When set to 1 it indicates that HDCP cipher Ri value for port C expired. Once set, this bit will remain high until it is cleared via RI_EXPIRED_A_CLR. 0 - No Ri expired on port 1 - Ri expired on port
RI_EXPIRED_D_RAW		R
0x8D	0000	Status of port D Ri expired Interrupt signal. When set to 1 it indicates that HDCP cipher Ri value for port D expired. Once set, this bit will remain high until it is cleared via RI_EXPIRED_A_CLR. 0 - No Ri expired on port 1 - Ri expired on port
BG_MEAS_DONE_RAW		R
0x8D	000000	Status of background port measurement completed interrupt signal. When set to 1 it indicates measurements of TMDS frequency and video parameters on the selected background port have been completed. Once set, this bit will remain high until it is cleared via BG_MEAS_DONE_CLR. 0 - Measurements of TMDS frequency and video parameters of background port not finished or not requested 1 - Measurements of TMDS frequency and video parameters of background port are ready
VS_INF_CKS_ERR_RAW		R
0x8D	0000000	Status of Vendor Specific Infoframe Checksum Error interrupt signal. When set to 1 it indicates that a checksum error has been detected for an Vendor Specific Infoframe. Once set, this bit will remain high until it is cleared via VS_INF_CKS_ERR_CLR. 0 - No VS infoframe checksum error has occurred 1 - A VS infoframe checksum error has occurred
RI_EXPIRED_A_ST		R
0x8E	0000000	Latched status of port A Ri expired Interrupt. Once set this bit will remain high until the interrupt has been cleared via RI_EXPIRED_A_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - No Ri expired on port A 1 - Ri expired on port A
RI_EXPIRED_B_ST		R
0x8E	000000	Latched status of port B Ri expired Interrupt. Once set this bit will remain high until the interrupt has been cleared via RI_EXPIRED_B_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - No Ri expired on port B 1 - Ri expired on port B
RI_EXPIRED_C_ST		R
0x8E	00000	Latched status of port C Ri expired Interrupt. Once set this bit will remain high until the interrupt has been cleared via RI_EXPIRED_C_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - No Ri expired on port C 1 - Ri expired on port C
RI_EXPIRED_D_ST		R
0x8E	0000	Latched status of port D Ri expired Interrupt. Once set this bit will remain high until the interrupt has been cleared via RI_EXPIRED_D_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit 0 - No Ri expired on port D 1 - Ri expired on port D

Reg	Bits	Description	
BG_MEAS_DONE_ST			R
0x8E	0000000<u>0</u>	Latched status of Background Port Measurement completed interrupt. Once set this bit will remain high until the interrupt has been cleared via BG_MEAS_DONE_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit. 0 - Measurements of TMDS frequency and video parameters of background port not finished or not requested. 1 - Measurements of TMDS frequency and video parameters of background port are ready	
VS_INF_CKS_ERR_ST			R
0x8E	0000000<u>0</u>	Latched status of MPEG Source Infoframe Checksum Error interrupt. Once set this bit will remain high until the interrupt has been cleared via MS_INF_CKS_ERR_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit 0 - No change in VS infoframe checksum error 1 - A VS infoframe checksum error has triggered this interrupt	
RI_EXPIRED_A_CLR			SC
0x8F	<u>0</u>0000000	Clear bit for the port A Ri expired Interrupt. 0 - Does not clear RI_EXPIRED_A_ST 1 - Clears RI_EXPIRED_A_ST	
RI_EXPIRED_B_CLR			SC
0x8F	0<u>0</u>000000	Clear bit for the port B Ri expired Interrupt. 0 - Does not clear RI_EXPIRED_B_ST 1 - Clears RI_EXPIRED_B_ST	
RI_EXPIRED_C_CLR			SC
0x8F	00<u>0</u>00000	Clear bit for the port C Ri expired Interrupt. 0 - Does not clear RI_EXPIRED_C_ST 1 - Clears RI_EXPIRED_C_ST	
RI_EXPIRED_D_CLR			SC
0x8F	000<u>0</u>0000	Clear bit for the port D Ri expired Interrupt. 0 - Does not clear RI_EXPIRED_D_ST 1 - Clears RI_EXPIRED_D_ST	
BG_MEAS_DONE_CLR			SC
0x8F	0000000<u>0</u>	Clear bit for the Background Port Measurement completed Interrupt. 0 - Does not clear BG_MEAS_DONE_ST 1 - Clears BG_MEAS_DONE_ST	
VS_INF_CKS_ERR_CLR			SC
0x8F	0000000<u>0</u>	Clear bit for the Vendor Specific Infoframe Checksum Error Interrupt. 0 - Does not clear 1 - Clears VS_INF_CKS_ERR_ST	
VS_INF_CKS_ERR_MB2			R/W
0x90	0000000<u>0</u>	INT2 interrupt mask for Vendor Specific Infoframe Checksum Error interrupt. When set the Vendor Specific Infoframe Checksum Error interrupt will trigger the INT2 interrupt and VS_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable Vendor Specific Infoframe Checksum Error interrupt on INT2 1 - Enable Vendor Specific Infoframe Checksum Error interrupt on INT2	
RI_EXPIRED_A_MB1			R/W
0x91	<u>0</u>0000000	INT1 interrupt mask for port A Ri expired interrupt. When set the port A AKSV Update interrupt will trigger the INT1 interrupt and RI_EXPIRED_A_ST will indicate the interrupt status. 0 - Disable port A Ri expired interrupt on INT1 1 - Enable port A Ri expired interrupt on INT1	
RI_EXPIRED_B_MB1			R/W
0x91	0<u>0</u>000000	INT1 interrupt mask for port B Ri expired interrupt. When set the port B AKSV Update interrupt will trigger the INT1 interrupt and RI_EXPIRED_A_ST will indicate the interrupt status. 0 - Disable port B Ri expired interrupt on INT1 1 - Enable port B Ri expired interrupt on INT1	
RI_EXPIRED_C_MB1			R/W
0x91	00<u>0</u>00000	INT1 interrupt mask for port C Ri expired interrupt. When set the port C AKSV Update interrupt will trigger the INT1 interrupt and RI_EXPIRED_A_ST will indicate the interrupt status. 0 - Disable port C Ri expired interrupt on INT1 1 - Enable port C Ri expired interrupt on INT1	

Reg	Bits	Description
RI_EXPIRED_D_MB1		R/W
0x91	0000**0**0000	INT1 interrupt mask for port D Ri expired interrupt. When set the port D AKSV Update interrupt will trigger the INT1 interrupt and RI_EXPIRED_A_ST will indicate the interrupt status. 0 - Disable port D Ri expired interrupt on INT1 1 - Enable port D Ri expired interrupt on INT1
BG_MEAS_DONE_MB1		R/W
0x91	000000**0**0	INT1 interrupt mask for Background port Measurement completed interrupt. When set the Background port Measurement completed interrupt will trigger the INT1 interrupt and BG_MEAS_DONE_ST will indicate the interrupt status. 0 - Disable Background port Measurement Completed interrupt on INT1 1 - Enable Background port Measurement Completed interrupt on INT1
VS_INF_CKS_ERR_MB1		R/W
0x91	0000000**0**	INT1 interrupt mask for Vendor Specific Infoframe Checksum Error interrupt. When set the Vendor Specific Infoframe Checksum Error interrupt will trigger the INT1 interrupt and VS_INF_CKS_ERR_ST will indicate the interrupt status. 0 - Disable Vendor Specific Checksum Error interrupt on INT1 1 - Enable Vendor Specific Checksum Error interrupt on INT1
CEC_RX_RDY2_RAW		R
0x92	00**0**00000	Raw status of CEC Receiver Buffer 2 Ready signal. When set to 1 it indicates that a CEC frame has been received and is waiting to be read in receiver frame buffer 2. 0 - No change 1 - CEC Rx buffer 2 has received a complete message which is ready be read by the host
CEC_RX_RDY1_RAW		R
0x92	0000**0**0000	Raw status of CEC Receiver Buffer 1 Ready signal. When set to 1 it indicates that a CEC frame has been received and is waiting to be read in receiver frame buffer 1. 0 - No change 1 - CEC Rx buffer 1 has received a complete message which is ready be read by the host
CEC_RX_RDY0_RAW		R
0x92	00000**0**000	Raw status of CEC Receiver Buffer 0 Ready signal. When set to 1 it indicates that a CEC frame has been received and is waiting to be read in receiver frame buffer 0. 0 - No change 1 - CEC Rx buffer 0 has received a complete message which is ready be read by the host
CEC_TX_RETRY_TIMEOUT_RAW		R
0x92	00000**0**00	Raw status of CEC Transmitter retry timeout signal. 0 - No change 1 - CEC TX has retried to send the current message by the no. of times specified in the TX_RETRY_REGISTER but it was unsuccessful every time
CEC_TX_ARBITRATION_LOST_RAW		R
0x92	000000**0**0	Raw status of CEC Transmitter Arbitration lost signal. 0 - No change 1 - CEC TX has lost arbitration to another TX
CEC_TX_READY_RAW		R
0x92	0000000**0**	Raw status of CEC Transmitter 'message sent' signal. This bit will be go high whenever the TX has successfully sent a message. 0 - No change 1 - CEC TX has successfully sent the last outgoing message
CEC_RX_RDY2_ST		R
0x93	00**0**00000	Latched status of CEC_RX_RDY2_RAW signal. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit. When a message has been received into buffer 2 this bit is set. Once set this bit will remain high until the interrupt has been cleared via CEC_RX_RDY2_CLR. 0 - No change 1 - New CEC message received in buffer 2
CEC_RX_RDY1_ST		R
0x93	0000**0**0000	Latched status of CEC_RX_RDY1_RAW signal. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit. When a message has been received into buffer 1 this bit is set. Once set this bit will remain high until the interrupt has been cleared via CEC_RX_RDY1_CLR. 0 - No change 1 - New CEC message received in buffer 1

Reg	Bits	Description	
CEC_RX_RDY0_ST			R
0x93	0000**0**000	Latched status of CEC_RX_RDY0_RAW signal. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit. When a message has been received into buffer 0 this bit is set. Once set this bit will remain high until the interrupt has been cleared via CEC_RX_RDY0_CLR. 0 - No change 1 - New CEC message received in buffer 0	
CEC_TX_RETRY_TIMEOUT_ST			R
0x93	00000**0**00	Latched status of CEC_TX_RETRY_TIMEOUT_RAW signal. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit. If the CEC TX fails to send the current message within the number of retry attempts specified by CEC_TX_RETRY this bit is set. Once set this bit will remain high until the interrupt has been cleared via CEC_TX_RETRY_TIMEOUT_CLR. 0 - No change 1 - CEC TX has tried but failed to resend the current message for the number of times specified by CEC_TX_RETRY	
CEC_TX_ARBITRATION_LOST_ST			R
0x93	000000**0**0	Latched status of CEC_TX_ARBITRATION_LOST_RAW signal. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit. If the CEC TX loses arbitration while trying to send a message this bit is set. Once set this bit will remain high until the interrupt has been cleared via CEC_TX_ARBITRATION_LOST_CLR. 0 - No change 1 - The CEC TX has lost arbitration to another TX	
CEC_TX_READY_ST			R
0x93	0000000**0**	Latched status of CEC_TX_READY_RAW signal. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit. When the CEC TX successfully sends the current message this bit is set. Once set this bit will remain high until the interrupt has been cleared via CEC_TX_READY_CLR. 0 - No change 1 - Message transmitted successfully	
CEC_RX_RDY2_CLR			SC
0x94	00**0**00000	Clear bit for CEC Receiver Buffer 2 Ready interrupt. 0 - Does not clear CEC_RX_RDY2_ST 1 - Clears CEC_RX_RDY2_ST	
CEC_RX_RDY1_CLR			SC
0x94	000**0**0000	Clear bit for CEC Receiver Buffer 1 Ready interrupt. 0 - Does not clear CEC_RX_RDY1_ST 1 - Clears CEC_RX_RDY1_ST	
CEC_RX_RDY0_CLR			SC
0x94	0000**0**000	Clear bit for CEC Receiver Buffer 0 Ready interrupt. 0 - Does not clear CEC_RX_RDY0_ST 1 - Clears CEC_RX_RDY0_ST	
CEC_TX_RETRY_TIMEOUT_CLR			SC
0x94	00000**0**00	Clear bit for CEC Transmitter Retry Timeout interrupt. 0 - Does not clear CEC_TX_RETRY_TIMEOUT_ST 1 - Clears CEC_TX_RETRY_TIMEOUT_ST	
CEC_TX_ARBITRATION_LOST_CLR			SC
0x94	000000**0**0	Clear bit for CEC Transmitter Arbitration Lost interrupt. 0 - Does not clear CEC_TX_ARBITRATION_LOST_ST 1 - Clears CEC_TX_ARBITRATION_LOST_ST	
CEC_TX_READY_CLR			SC
0x94	0000000**0**	Clear bit for CEC Transmitter Ready interrupt. 0 - Does not clear CEC_TX_READY_ST 1 - Clears CEC_TX_READY_ST	
CEC_RX_RDY2_MB1			R/W
0x96	00**0**00000	INT1 interrupt mask for CEC Receiver Buffer 2 Ready interrupt. When set the CEC Receiver Buffer 2 Ready interrupt will trigger the INT1 interrupt and CEC_RX_RDY2_ST will indicate the interrupt status. 0 - Disables CEC Receiver Buffer 2 Ready interrupt on INT1 1 - Enables CEC Receiver Buffer 2 Ready interrupt on INT1	

Reg	Bits	Description	
CEC_RX_RDY1_MB1			R/W
0x96	0000<u>0</u>0000	INT1 interrupt mask for CEC Receiver Buffer 2 Ready interrupt. When set the CEC Receiver Buffer 2 Ready interrupt will trigger the INT1 interrupt and CEC_RX_RDY2_ST will indicate the interrupt status. 0 - Disables CEC Receiver Buffer 1 Ready interrupt on INT1 1 - Enables CEC Receiver Buffer 1 Ready interrupt on INT1	
CEC_RX_RDY0_MB1			R/W
0x96	0000<u>0</u>000	INT1 interrupt mask for CEC Receiver Buffer 0 Ready interrupt. When set the CEC Receiver Buffer 0 Ready interrupt will trigger the INT1 interrupt and CEC_RX_RDY0_ST will indicate the interrupt status. 0 - Disables CEC Receiver Buffer 0 Ready interrupt on INT1 1 - Enables CEC Receiver Buffer 0 Ready interrupt on INT1	
CEC_TX_RETRY_TIMEOUT_MB1			R/W
0x96	00000<u>0</u>00	INT1 interrupt mask for CEC Transmitter Retry Timeout interrupt. When set the CEC Transmitter Retry Timeout interrupt will trigger the INT1 interrupt and CEC_TX_RETRY_TIMEOUT_ST will indicate the interrupt status. 0 - Disables CEC Receiver Transmitter Timeout Retry interrupt on INT1 1 - Enables CEC Receiver Transmitter Timeout Retry interrupt on INT1	
CEC_TX_ARBITRATION_LOST_MB1			R/W
0x96	000000<u>0</u>0	INT1 interrupt mask for CEC Transmitter Arbitration Lost interrupt. When set the CEC Transmitter Arbitration Lost interrupt will trigger the INT1 interrupt and CEC_TX_ARBIRATION_LOST_ST will indicate the interrupt status. 0 - Disables CEC Receiver Transmitter Arbitration Lost interrupt on INT1 1 - Enables CEC Receiver Transmitter Arbitration Lost interrupt on INT1	
CEC_TX_READY_MB1			R/W
0x96	0000000<u>0</u>	INT1 interrupt mask for CEC Transmitter Ready interrupt. When set the CEC Transmitter Ready interrupt will trigger the INT1 interrupt and CEC_TX_RDY_ST will indicate the interrupt status. 0 - Disables CEC Receiver Transmitter Ready interrupt on INT1 1 - Enables CEC Receiver Transmitter Ready interrupt on INT1	
CEC_INTERRUPT_BYTE[7:0]			R
0x97	<u>00000000</u>	One of the 8 preprogrammed commands received 00 - No change 01 - opcode 1 received. 02 - opcode 2 received. 04 - opcode 3 received. 08 - opcode 4 received. 10 - opcode 5 received. 20 - opcode 6 received. 40 - opcode 7 received. 80 - opcode 8 received.	
CEC_INTERRUPT_BYTE_ST[7:0]			R
0x98	<u>00000000</u>	0 - No change 1 - one of the 8 opcodes received	
CEC_INTERRUPT_BYTE_CLR[7:0]			SC
0x99	<u>00000000</u>	0 - Does not clear 1 - Clears CEC_INTERRUPT_BYTE_ST	
CEC_INTERRUPT_BYTE_MB1[7:0]			R/W
0x9B	<u>00000000</u>	0 - Masks CEC_INTERRUPT_BYTE_ST 1 - Umasks CEC_INTERRUPT_BYTE_ST	

Reg	Bits	Description	
ARC_TX_PWRDN[3:0]			R/W
0xAC	0000<u>1111</u>	Powerdown control for ARC transmitters 0000 - Power up all ARC TX channels 0001 - Power down ARC TX channel A 0010 - Power down ARC TX channel B 0011 - Power down ARC TX channels A, B 0100 - Power down ARC TX channel C 0101 - Power down ARC TX channels A, C 0110 - Power down ARC TX channel B, C 0111 - Power down ARC TX channel A, B, C 1000 - Power down ARC TX channel D 1001 - Power down ARC TX channels A, D 1010 - Power down ARC TX channels B, D 1011 - Power down ARC TX channels A, B, D 1100 - Power down ARC TX channels C, D 1101 - Power down ARC TX channels A, C, D 1110 - Power down ARC TX channels B, C, D 1111 - Power down all ARC TX channels	
INV_SPDIF_IN[3:0]			R/W
0xAD	<u>0000</u>0000	Inverts SPDIF_IN signal to ARC TX 0000 - Non inverted SPDIF to ARC TX ports 0001 - Inverted SPDIF to ARC TX port A 0010 - Inverted SPDIF to ARC TX port B 0011 - Inverted SPDIF to ARC TX port A,B 0100 - Inverted SPDIF to ARC TX port C 0101 - Inverted SPDIF to ARC TX port A, C 0110 - Inverted SPDIF to ARC TX port B, C 0111 - Inverted SPDIF to ARC TX port A, B, C 1000 - Inverted SPDIF to ARC TX port D 1001 - Inverted SPDIF to ARC TX port A, D 1010 - Inverted SPDIF to ARC TX port B, D 1011 - Inverted SPDIF to ARC TX port A, B, D 1100 - Inverted SPDIF to ARC TX port C, D 1101 - Inverted SPDIF to ARC TX port A, C, D 1110 - Inverted SPDIF to ARC TX port B, C, D 1111 - Inverted SPDIF to ARC TX all ports	
ZERO_SPDIF_IN[3:0]			R/W
0xAD	0000<u>0000</u>	Mutes ARC TX on selected ports 0000 - Functional mode for ARC TX all ports 0001 - Zero SPDIF input to ARC TX port A 0010 - Zero SPDIF input to ARC TX port B 0011 - Zero SPDIF input to ARC TX port A,B 0100 - Zero SPDIF input to ARC TX port C 0101 - Zero SPDIF input to ARC TX port A, C 0110 - Zero SPDIF input to ARC TX port B, C 0111 - Zero SPDIF input to ARC TX port A, B, C 1000 - Zero SPDIF input to ARC TX port D 1001 - Zero SPDIF input to ARC TX port A, D 1010 - Zero SPDIF input to ARC TX port B, D 1011 - Zero SPDIF input to ARC TX port A, B, D 1100 - Zero SPDIF input to ARC TX port C, D 1101 - Zero SPDIF input to ARC TX port A, C, D 1110 - Zero SPDIF input to ARC TX port B, C, D 1111 - Zero SPDIF input to ARC TX all ports	
ARC_RX_I2C_PWRDN			R/W
0xC5	0000<u>0</u>000	Powers down ARC receiver. 0 - Default value	
SPDIF_OUT_EN			R/W
0xC5	00000<u>0</u>00	Outputs ARC on SPDIF pad 0 - Disables output of received ARC 1 - Enables output of received ARC on SPDIF_OUT pin	

Reg	Bits	Description	
ARC_RX_SINGLE_ENDED			R/W
0xC5	0000000<u>0</u>	Selects input mode of ARC RX 0 - ARC RX common mode 1 - ARC RX single ended.	
ARC_RX_SPDIF_INV			R/W
0xC5	0000000<u>0</u>	Inverts the output of the ARC RX block. 0 - ARC RX not inverted. 1 - ARC RX inverted.	
RD_INFO[15:0]			R
0xE1 0xE2	<u>00000000</u> <u>00000000</u>	Chip revision code 0x4040 - ADV7630	
TXB_MAIN_SLAVE_ADDR[6:0]			R/W
0xEA	<u>0000000</u>0	Programmable I2C slave address for TXB Main map 000000 - Map not accessible (default) xxxxxx - I2C Address	
TXB_EDID_SLAVE_ADDR[6:0]			R/W
0xEC	<u>0000000</u>0	Programmable I2C slave address for TXB EDID map 000000 - Map not accessible (default) xxxxxx - I2C Address	
TXA_MAIN_SLAVE_ADDR[6:0]			R/W
0xEE	<u>0000000</u>0	Programmable I2C slave address for TXA Main map	
TXA_UDP_SLAVE_ADDR[6:0]			R/W
0xEF	<u>0000000</u>0	Programmable I2C slave address for TXA UDP map 000000 - Map not accessible (default) xxxxxx - I2C Address	
TXA_EDID_SLAVE_ADDR[6:0]			R/W
0xF0	<u>0000000</u>0	Programmable I2C slave address for TXA EDID map 000000 - Map not accessible (default) xxxxxx - I2C Address	
CEC_SLAVE_ADDR[6:0]			R/W
0xF4	<u>0000000</u>0	Programmable I2C slave address for CEC map 000000 - Map not accessible (default) xxxxxx - I2C Address	
INFOFRAME_SLAVE_ADDR[6:0]			R/W
0xF5	<u>0000000</u>0	Programmable I2C slave address for Infoframe map 000000 - Map not accessible (default) xxxxxx - I2C Address	
KSV_SLAVE_ADDR[6:0]			R/W
0xF9	<u>0000000</u>0	Programmable I2C slave address for KSV map 000000 - Map not accessible (default) xxxxxx - I2C Address	
EDID_SLAVE_ADDR[6:0]			R/W
0xFA	<u>0000000</u>0	Programmable I2C slave address for EDID map 000000 - Map not accessible (default) xxxxxx - I2C Address	
HDMI_SLAVE_ADDR[6:0]			R/W
0xFB	<u>0000000</u>0	Programmable I2C slave address for HDMI map 000000 - Map not accessible (default) xxxxxx - I2C Address	
MAIN_RESET			SC
0xFF	<u>0</u>0000000	Main reset where everything, all I2C registers will be reset to their default values. 0 - Normal operation 1 - Apply Main I2C reset	

2.2 HDMI MAP

Reg	Bits	Description	
BG_MEAS_PORT_SEL[2:0]			R/W
0x00	00000000	BG_MEAS_PORT_SEL[1:0] selects a background port on which HDMI measurements are to be made and provided in the background measurement registers. The port in question must be set as a background port in order for this setting to be effective. This register can be also used with ports selected by HDMI_PORT_SELECT_TXA or HDMI_PORT_SELECT_TXB. 000 - Port A 001 - Port B 010 - Port C 011 - Port D	
HDMI_PORT_SELECT_TX_A[2:0]			R/W
0x00	00000000	This 3-bit control is used to select the HDMI port for the primary path (i.e. for TxA) 000 - Port A 001 - Port B 010 - Port C 011 - Port D	
TERM_AUTO			R/W
0x01	00000000	This bit allows the user to select automatic or manual control of clock termination. If automatic mode termination is enabled, then the termination on the port selected via HDMI_PORT_SELECT[1:0] is enabled. The termination is disabled on all other ports. 0 - Disable automatic control of the TMDS terminations 1 - Enable automatic control of the TMDS terminations	
EN_BG_PORT_D			R/W
0x02	00000000	Background mode enable for Port D. Sets Port D in background mode to establish a HDCP link with its source even if the port is not selected by HDMI_PORT_SELECT. This control has no effect if the port is selected by HDMI_PORT_SELECT. 0 - Port D disabled, unless selected with HDMI_PORT_SELECT_TX_A or HDMI_PORT_SELECT_TX_B 1 - Port D enabled in background mode	
EN_BG_PORT_C			R/W
0x02	00000000	Background mode enable for Port C. Sets Port C in background mode to establish a HDCP link with its source, even if the port is not selected by HDMI_PORT_SELECT. This control has no effect if the port is selected by HDMI_PORT_SELECT. 0 - Port C disabled, unless selected with HDMI_PORT_SELECT_TX_A or HDMI_PORT_SELECT_TX_B 1 - Port C enabled in background mode	
EN_BG_PORT_B			R/W
0x02	00000000	Background mode enable for Port B. Sets the Port B in background mode to establish a HDCP link with its source even if the port is not selected by HDMI_PORT_SELECT. This control has no effect if the port is selected by HDMI_PORT_SELECT. 0 - Port B disabled, unless selected with HDMI_PORT_SELECT_TX_A or HDMI_PORT_SELECT_TX_B 1 - Port B enabled in background mode	
EN_BG_PORT_A			R/W
0x02	00000000	Background mode enable for Port A. Sets Port A in background mode to establish a HDCP link with its source even if the port is not selected by HDMI_PORT_SELECT. This control has no effect if the port is selected by HDMI_PORT_SELECT. 0 - Port A disabled, unless selected with HDMI_PORT_SELECT_TX_A or HDMI_PORT_SELECT_TX_B 1 - Port A enabled in background mode	
AV_MUTE			R
0x04	00000000	Readback of AVMUTE status received in the last General Control packet received. 0 - AVMUTE not set 1 - AVMUTE set	
HDCP_KEYS_READ			R
0x04	00000000	A readback to indicate a successful read of the HDCP keys and/or KSV from the internal HDCP key OTP ROM. A logic high is returned when the read is successful. 0 - HDCP keys and/or KSV not yet read 1 - HDCP keys and/or KSV HDCP keys read	
HDCP_KEY_ERROR			R
0x04	00000000	A readback to indicate if a checksum error occurred while reading the HDCP and/or KSV from the HDCP key ROM. Returns high when HDCP key master encounters an error while reading the HDCP key OTP ROM. This register refers to a primary HDMI port selected. 0 - No error occurred while reading HDCP keys 1 - HDCP keys read error	

Reg	Bits	Description	
HDCP_RI_EXPIRED			R
0x04	0000<u>0</u>000	Readback high when a calculated Ri has not been read by the source TX, on the active port. It remains high until next Aksv update. This register refers to a primary HDMI port selected. 0 - Default 1 - Ri has not been read by the source TX	
TMDS_PLL_LOCKED			R
0x04	000000<u>0</u>0	A readback to indicate if the TMDS PLL is locked to the TMDS clock input of the selected HDMI port. 0 - TMDS PLL is not locked 1 - TMDS PLL is locked to the TMDS clock input of the selected HDMI port	
HDMI_MODE			R
0x05	<u>0</u>0000000	A readback to indicate if the stream processed by the HDMI core is a DVI or an HDMI stream. This register refers to a primary HDMI port selected. 0 - DVI Mode Detected 1 - HDMI Mode Detected	
HDMI_CONTENT_ENCRYPTED			R
0x05	0<u>0</u>000000	A readback to indicate if the input stream processed by the HDMI core is HDCP encrypted or not. This register refers to a primary HDMI port selected. 0 - Input stream processed by the HDMI core is not HDCP encrypted 1 - Input stream processed by the HDMI core is HDCP encrypted	
DVI_HSYNC_POLARITY			R
0x05	00<u>0</u>00000	A readback to indicate the polarity of the HSync encoded in the input stream. This register refers to a primary HDMI port selected. 0 - The HSync is active low 1 - The HSync is active high	
DVI_VSYNC_POLARITY			R
0x05	000<u>0</u>0000	A readback to indicate the polarity of the VSync encoded in the input stream. This register refers to a primary HDMI port selected. 0 - The VSync is active low 1 - The VSync is active high	
HDMI_PIXEL_REPETITION[3:0]			R
0x05	0000<u>0000</u>	A readback to provide the current HDMI pixel repetition value decoded from the AVI Infoframe received. The HDMI receiver automatically discards repeated pixel data and divides the pixel clock frequency appropriately as per the pixel repetition value. This register refers to a primary HDMI port selected. 0000 - 1x 0001 - 2x 0010 - 3x 0011 - 4x 0100 - 5x 0101 - 6x 0110 - 7x 0111 - 8x 1000 - 9x 1001 - 10x 1010 - 1111 - Reserved	
DEEP_COLOR_MODE[1:0]			R
0x0B	<u>00</u>000000	A readback of the deep color mode information extracted from the general control packet. This register refers to a primary HDMI port selected. 00 - 8-bits per channel 01 - 10-bits per channel 10 - 12-bits per channel 11 - 16-bits per channel (not supported)	
HDMI_PORT_SELECT_TX_B[2:0]			R/W
0x0D	0<u>000</u>0100	This 3-bit control is used to select the HDMI port for the secondary path (i.e. for TxB) 000 - Port A 001 - Port B 010 - Port C 011 - Port D	

Reg	Bits	Description	
FREQTOLERANCE[3:0]			R/W
0x0D	00000100	Sets the tolerance in MHz for new TMDS frequency detection. This tolerance is used for the audio mute mask MT_MSK_VCLK_CHNG and the HDMI status bit NEW_TMDS_FRQ_RAW. 0100 - Default tolerance in MHz for new TMDS frequency detection xxxx - Tolerance in MHz for new TMDS frequency detection	
PDN_PKT_PROCESSOR			R/W
0x1D	00000000	Power saving featura that disables the clocking of the tmds rate section of the packet processor. Note that the audio clocking can be stopped separately, from the digital PLL (clock generator). 0 - Packet processor is active 1 - Packet processor is stopped, (i.e. powererd down)	
ALWAYS_STORE_INF			R/W
0x47	00000000	A control to force InfoFrames with checksum errors to be stored. 0 - Store data from received InfoFrames only if their checksum is correct 1 - Always store the data from received InfoFrame regardless of their checksum	
DIS_CABLE_DET_RST			R/W
0x48	00000000	This control disables the reset effects of cable detection. DIS_CABLE_DET_RST should be set to 1 if the +5 V pins are unused and left unconnected. 0 - Reset the HDMI section if the 5 V input pin corresponding to the selected HDMI port (e.g. RXA_5V for port A) is inactive 1 - Do not use the 5 V input pins as reset signal for the HDMI section	
NEW_VS_PARAM			R/W
0x4C	00000000	Enables a new version of vertical parameter extraction. 0 - Disabled 1 - Enabled	
GAMUT_IRQ_NEXT_FIELD			R/W
0x50	00000000	A control set the NEW_GAMUT_MDATA_RAW interrupt to detect when the new contents are applicable to next field or to indicate that the Gamut packet is new. This is done using header information of the gamut packet. 0 - Interrupt flag indicates that Gamut packet is new 1 - Interrupt flag indicates that Gamut packet is to be applied next field	
TMDSFREQ[8:0]			R
0x51 0x52	00000000 00000000	This register provides a full precision integer TMDS frequency measurement. This register refers to a primary HDMI port selected. 000000000 - Outputs 9-bit TMDS frequency measurement in MHz xxxxxxxxx - Outputs 9-bit TMDS frequency measurement in MHz	
TMDSFREQ_FRAC[6:0]			R
0x52	00000000	A readback to indicate the fractional bits of measured frequency of PLL recovered TMDS clock. The unit is 1/128 MHz. This register refers to a primary HDMI port selected. 0000000 - Outputs 7-bit TMDS fractional frequency measurement in 1/128MHz xxxxxxx - Outputs 7-bit TMDS fractional frequency measurement in 1/128MHz	
HDMI_COLORSPACE[3:0]			R
0x53	00000000	A readback of the HDMI input colorspace decoded from the AVI infoframe. This register refers to a primary HDMI port selected. 0000 - RGB_LIMITED 0001 - RGB_FULL 0010 - YUV_601 0011 - YUV_709 0100 - XVYCC_601 0101 - XVYCC_709 0110 - YUV_601_FULL 0111 - YUV_709_FULL 1000 - sYCC 601 1001 - Adobe YCC 601 1010 - Adobe RGB	

Reg	Bits	Description
FILT_5V_DET_DIS		R/W
0x56	01011000	This bit is a control to disable the digital glitch filter on the HDMI 5V detect signals. The filtered signals are used as interrupt flags, and also used to reset the HDMI section. The filter works from an internal ring oscillator clock and is therefore available in power-down mode. The clock frequency of the ring oscillator is 42MHz +/-10%. Note: If the 5 V pins are not used and left unconnected, the 5 V detect circuitry should be disconnected from the HDMI reset signal by setting DIS_CABLE_DET_RST to 1. This avoids holding the HDMI section in reset. 0 - Enable 1 - Disable
FILT_5V_DET_TIMER[6:0]		R/W
0x56	01011000	This control is used to set the timer for the digital glitch filter on the HDMI +5 V detect inputs. The unit of this parameter is 2 clock cycles of the ring oscillator (~ 47 ns). The input must be constantly high for the duration of the timer, otherwise the filter output remains low. The output of the filter returns low as soon as any change in the +5 V power signal is detected. 1011000 - Approximately 4.2us xxxxxxx - Time duration of +5 V deglitch filter. The unit of this parameter is 2 clock cycles of the ring oscillator (~ 47ns)
HDCP_I2C_RESET_TX		SC
0x5A	00000000	Resets the HDCP engine of HDMI transmitter, so it restarts the authentification
BG_MEAS_REQ		SC
0x5A	00000000	This bit must be set to get the correct measurements of the selected background port. Setting this control sends a request to update the synchronization parameter measurements of the currently selected background port. The port on which the measurement will be made is selected by BG_MEAS_PORT_SEL[1:0]. This is a self clearing bit. 0 - No request to update selected background port synchronization parameter measurements 1 - Requests an update of the selected background port synchronization parameter measurements
HDCP_REPT_EDID_RESET		SC
0x5A	00000000	A reset control for the E-EDID/Repeater controller. When asserted it resets the E-EDID/Repeater controller. This is a self clearing bit. 0 - Normal operation 1 - Resets the E-EDID/repeater controller
HPA_DELAY_SEL[3:0]		R/W
0x6C	10100011	Sets a delay between +5 V detection and hot plug assertion on the HPA output pins, in increments of 100ms per bit. 0000 - No delay 0001 - 100 msec delay 0010 - 200 msec delay 1010 - 1 sec delay 1111 - 1.5 sec delay
HPA_OVR_TERM		R/W
0x6C	10100011	A control to set termination control to be overridden by the HPA setting. When this bit is set, termination on a specific port will be set according to the HPA status of that port. 0 - Automatic or manual I2C control of port termination 1 - Termination controls disabled and overridden by HPA controls
HPA_AUTO_INT_EDID[1:0]		R/W
0x6C	10100011	Selects the type of automatic control on the HPA output pins. This bit has no effect when HPA_MANUAL is set to 1 00 - The HPA of an HDMI port is asserted high immediately after the internal EDID has been activated for that port. The HPA of a specific HDMI port is de-asserted low immediately after the internal E-EDID is de-activated for that port. 01 - The HPA of an HDMI port is asserted high following a programmable delay after the part detects an HDMI cable plug on that port. The HPA of an HDMI port is immediately de-asserted after the part detects a cable disconnect on that HDMI port. 10 - The HPA of an HDMI port is asserted high after two conditions have been met. 1. The internal EDID is active for that port. 2. The delayed version of the cable detect signal CABLE_DET_X_RAW for that port is high. The HPA of an HDMI port is immediately de-asserted after either of the following two conditions have been met. 1. The internal EDID is de-activated for that port. 2. The cable detect signal CABLE_DET_X_RAW for that port is low. 11 - The HPA of an HDMI port is asserted high after three conditions have been met. 1. The internal EDID is active for that port. 2. The delayed version of the cable detect signal CABLE_DET_X_RAW for that port is high. 3. The user has set the manual HPA control for that port to 1 via the HPA_MAN_VALUE_X controls. The HPA of an HDMI port is immediately de-asserted after any of the following three conditions have been met 1.The internal EDID is de-activated for that port 2.The cable detect signal CABLE_DET_X_RAW for that port, is low. 3.The user sets the manual HPD control for that port to 0 via the HPA_MAN_VALUE_X controls.

Reg	Bits	Description	
HPA_MANUAL			R/W
0x6C	1010000<u>1</u>	Manual control enable for the Hot Plug Assert output pins. By setting this bit any automatic control of these pins is disabled. Manual control is determined by the HPA_MAN_VALUE_X (where X = A, B, C & D) 0 - HPA takes its value based on HPA_AUTO_INT_EDID 1 - HPA takes its value from HPA_MAN_VALUE_X	
DDC_PWRDN[7:0]			R/W
0x73	<u>00000000</u>	Powerdown control for the DDC pads. 0 - Power up all DDC pads 1 - Power down DDC pads on port A 2 - Power down DDC pads on port B 3 - Power down DDC pads on ports A, B 4 - Power down DDC pads on port C 5 - Power down DDC pads on ports A, C 6 - Power down DDC pads on ports B, C 7 - Power down DDC pads on ports A, B, C 8 - Power down DDC pads on port D 9 - Power down DDC pads on ports A, D 10 - Power down DDC pads on ports B, D 11 - Power down DDC pads on ports A, B, D 12 - Power down DDC pads on ports C, D 13 - Power down DDC pads on ports A, C, D 14 - Power down DDC pads on ports B, C, D 15 - Power down all DDC pads on ports A, B, C, D	
CLOCK_TERMD_DISABLE			R/W
0x83	1111<u>1</u>111	Disable clock termination on Port D. Can be used when TERM_AUTO is set to 0. 0 - Enable termination on Port D 1 - Disable termination on Port D	
CLOCK_TERMC_DISABLE			R/W
0x83	11111<u>1</u>11	Disable clock termination on Port C. Can be used when TERM_AUTO is set to 0. 0 - Enable termination on Port C 1 - Disable termination on Port C	
CLOCK_TERMB_DISABLE			R/W
0x83	111111<u>1</u>1	Disable clock termination on Port B. Can be used when TERM_AUTO is set to 0. 0 - Enable termination on Port B 1 - Disable termination on Port B	
CLOCK_TERMA_DISABLE			R/W
0x83	1111111<u>1</u>	Disable clock termination on Port A. Can be used when TERM_AUTO is set to 0. 0 - Enable termination on Port A 1 - Disable termination on Port A	
BG_TMDSFREQ[8:0]			R
0xE0 0xE1	<u>00000000</u> <u>0</u>0000000	This register provides a precision integer TMDS frequency measurement on the background port selected by BG_MEAS_PORT_SEL. The value provided is the result of a single measurement of the TMDS PLL frequency in MHz. This value is updated when an update request is made via the BG_MEAS_REQ control bit. This measurement is only valid when BG_PARAM_LOCK is set to 1. 000000000 - Outputs 9-bit TMDS frequency measurement in MHz xxxxxxxxx - Outputs 9-bit TMDS frequency measurement in MHz	
BG_TMDSFREQ_FRAC[6:0]			R
0xE1	0<u>0000000</u>	This register provides a precision fractional measurement of the TMDS frequency on the background port selected by BG_MEAS_PORT_SEL. The unit is 1/128 MHz and the value is updated when a update request is made via the BG_MEAS_REQ control bit. This measurement is only valid when BG_PARAM_LOCK is set to 1. 0000000 - Outputs 7-bit TMDS fractional frequency measurement in 1/128MHz xxxxxxx - Outputs 7-bit TMDS fractional frequency measurement in 1/128MHz	
BG_LINE_WIDTH[12:0]			R
0xE2 0xE3	000<u>00000</u> <u>00000000</u>	A horizontal synchronization measurement for the background HDMI Port determined by BG_MEAS_PORT_SEL[1:0]. The value represents the number of active pixels in a line and is updated when an update request is made via the BG_MEAS_REQ control bit. 0000000000000 - Number of active pixels per line on the background measurement port xxxxxxxxxxxxx - Number of active pixels per line on the background measurement port	

Reg	Bits	Description	
BG_TOTAL_LINE_WIDTH[13:0]			R
0xE4 0xE5	00000000 00000000	A horizontal synchronization measurement for the background HDMI Port determined by BG_MEAS_PORT_SEL[1:0]. The value represents the total number of pixels in a line and is updated when an update request is made via the BG_MEAS_REQ control bit. This measurement is only valid when BG_PARAM_LOCK is set to 1. xxxxxxxxxxxx - Total number of pixels per line on the background measurement port	
BG_FIELD_HEIGHT[12:0]			R
0xE6 0xE7	00000000 00000000	A vertical synchronization measurement for a background HDMI Port determined by BG_MEAS_PORT_SEL[1:0] 0000000000000 - Number of active lines in a Field on the background measurement port xxxxxxxxxxxxx - Number of active lines in a Field on the background measurement port	
BG_TOTAL_FIELD_HEIGHT[12:0]			R
0xE8 0xE9	00000000 00000000	A vertical synchronization measurement for the background HDMI Port determined by BG_MEAS_PORT_SEL[1:0]. The value represents the total number of lines in a field and is updated when an update request is made via the BG_MEAS_REQ control bit. 0000000000000 - Total number of lines in a Field on the background measurement port xxxxxxxxxxxxx - Total number of lines in a Field on the background measurement port	
BG_PIX_REP[3:0]			R
0xEA	00000000	Background port pixel repetition status for the background HDMI port determined by BG_MEAS_PORT_SEL[1:0]. The readback provides the pixel repetition value in AVI InfoFrame and is updated when an update request is made via the BG_MEAS_REQ control bit. This measurement is only valid when BG_PARAM_LOCK is set to 1. 0000 - 1x 0001 - 2x 0010 - 3x 0011 - 4x 0100 - 5x 0101 - 6x 0110 - 7x 0111 - 8x 1000 - 9x 1001 - 10x 1010 - 1111 - Reserved	
BG_DEEP_COLOR_MODE[1:0]			R
0xEA	00000000	This readback provides the deep-color status for the background HDMI port determined by BG_MEAS_PORT_SEL[1:0]. The readback provides the HDMI color depth and is updated when an update request is made via the BG_MEAS_REQ control bit. This measurement is only valid when BG_PARAM_LOCK is set to 1. 00 - 8-bit color per channel 01 - 10-bit color per channel 10 - 12-bit color per channel 11 - 16-bit color per channel	
BG_PARAM_LOCK			R
0xEA	00000000	A flag to indicate that vertical and horizontal parameters were locked during a background measurement. 0 - Horizontal and vertical were not locked when measurement for selected background HDMI port was taken 1 - Horizontal and Vvertical were locked when measurement for selected background HDMI port was taken	
BG_HDMI_INTERLACED			R
0xEA	00000000	Background port HDMI input interlace status is a vertical filter measurement for a background HDMI Port determined by BG_MEAS_PORT_SEL[1:0]. The status readback is updated when a update request is made via the BG_MEAS_REQ control bit. This measurement is only valid when BG_PARAM_LOCK is set to 1. 0 - Progressive video format 1 - Interlaced video format	
BG_HDMI_MODE			R
0xEB	00000000	This readback provides the HDMI/DVI mode status of the background port determined by BG_MEAS_PORT_SEL[1:0] and is updated continuously. 0 - DVI Mode detected on selected BG port 1 - HDMI Mode detected on selected BG port	
BG_AUDIO_LAYOUT			R
0xEE	00000000	Flags layout of audio channels in background port selected with BG_MEAS_PORT_SEL. Only valid when BG_AUDIO_DETECTED_BG flags audio sample packets or DSD audio packets have been detected 0 - Layout 0 1 - Layout 1	

Reg	Bits	Description	
BG_DST_DOUBLE			R
0xEE	0000<u>0</u>0000	Flags whether DST audio is sampled at single or double transfer rate in the background port with BG_MEAS_PORT_SEL. Only valid when BG_AUDIO_DETECTED flags DST packets have been received 0 - DST sample rate equals transfer rate 1 - DST sample rate doubles transfer rate	
BG_AUDIO_DETECTED[3:0]			R
0xEE	0000<u>0000</u>	Flags if audio samples were received on the background port and if so, their type. 0000 - No audio samples detected 0001 - Audio sample detected 0010 - DSD audio detected 0100 - DST audio detected 1000 - HBR audio detected	
BG_HEADER_REQUESTED[7:0]			R/W
0xEF	<u>10000010</u>	Selects the type of InfoFrame/packet to be provided for readback in the background port header and packet registers (0xF0 to 0xF5). The value set in this register is compared against the detected InfoFrame/packet header byte 0. If they match, header byte 1 and data bytes 1 to 5 are stored. Default value of 0x82 is the InfoFrame type of AVI infoFrame. xxxxxxxx - Header value requested. This will be compared with detected packet headers. If a match is found, data is stored in registers 0xF0 to 0xF5.	
BG_HEADER_BYTE1[7:0]			R
0xF0	<u>00000000</u>	Byte 1 of header for the InfoFrame/Packet selected to be read in background port. xxxxxxxx - Header byte 1 data . Only valid if BG_VALID_PACKET is high.	
BG_PACKET_BYTE1[7:0]			R
0xF1	<u>00000000</u>	Byte 1 of packet for the InfoFrame/Packet selected to be read in background port. xxxxxxxx - Packet byte 1 data . Only valid if BG_VALID_PACKET is high.	
BG_PACKET_BYTE2[7:0]			R
0xF2	<u>00000000</u>	Byte 2 of packet for the InfoFrame/Packet selected to be read in background port. xxxxxxxx - Packet byte 2 data . Only valid if BG_VALID_PACKET is high.	
BG_PACKET_BYTE3[7:0]			R
0xF3	<u>00000000</u>	Byte 3 of packet for the InfoFrame/Packet selected to be read in background port. xxxxxxxx - Packet byte 3 data . Only valid if BG_VALID_PACKET is high.	
BG_PACKET_BYTE4[7:0]			R
0xF4	<u>00000000</u>	Byte 4 of packet for the InfoFrame/Packet selected to be read in background port. xxxxxxxx - Packet byte 4 data . Only valid if BG_VALID_PACKET is high.	
BG_PACKET_BYTE5[7:0]			R
0xF5	<u>00000000</u>	Byte 5 of packet for the InfoFrame/Packet selected to be read in background port. xxxxxxxx - Packet byte 5 data . Only valid if BG_VALID_PACKET is high.	
BG_VALID_PACKET			R
0xF6	0000000<u>0</u>	Readbacks of packets in BG port are only valid if this signal is high 0 - BG header and packet readbacks not valid 1 - BG header and packet readbacks are valid	

2.3 REPEATER MAP

Reg	Bits	Description	
BKSV[39:0]			R
0x00 0x01 0x02 0x03 0x04	00000000 00000000 00000000 00000000 00000000	The HDMI receiver Key Selection Vector (BKSV) can be read back once the part has successfully accessed the HDCP ROM. The following registers contain the BKSV read from the EEPROM. 0x00[7:0] = BKSV[7:0], 0x01[7:0] = BKSV[15:8], 0x02[7:0] = BKSV[23:16], 0x03[7:0] = BKSV[31:24] and 0x04[7:0] = BKSV[39:32] 0x00 - BKSV[7:0] 0x01 - BKSV[15:8] 0x02 - BKSV[23:16] 0x03 - BKSV[31:24] 0x04 - BKSV[39:32]	
RI[15:0]			R
0x08 0x09	00000000 00000000	Ri generated by HDCP core	
PJ[7:0]			R
0x0A	00000000	Pj generated by HDCP core	
AKSV[39:0]			R/W
0x10 0x11 0x12 0x13 0x14	00000000 00000000 00000000 00000000 00000000	The AKSV of the transmitter attached to the active HDMI port can be read back after an AKSV update. The following registers contain the AKSV written by the Tx. 0x10[7:0] = AKSV[7:0], 0x11[7:0] = AKSV[15:8], 0x12[7:0] = AKSV[23:16], 0x13[7:0] = AKSV[31:24] and 0x14[7:0] = AKSV[39:32] 0x10 - AKSV[7:0] 0x11 - AKSV[15:8] 0x12 - AKSV[23:16] 0x13 - AKSV[31:24] 0x14 - AKSV[39:32]	
AINFO[7:0]			R/W
0x15	00000000	AINFO written by Tx	
AINFO_RB[7:0]			R
0x16	00000000	Readback of effective Ainfo value, the value in previous address is cleared after an AKSV update	
AN[63:0]			R/W
0x18 0x19 0x1A 0x1B 0x1C 0x1D 0x1E 0x1F	00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000	AN written by Tx	
SHA_A[31:0]			R/W
0x20 0x21 0x22 0x23	00000000 00000000 00000000 00000000	SHA Hash Part A generated by on chip micro	
SHA_B[31:0]			R/W
0x24 0x25 0x26 0x27	00000000 00000000 00000000 00000000	SHA Hash Part B generated by on chip micro	
SHA_C[31:0]			R/W
0x28 0x29 0x2A 0x2B	00000000 00000000 00000000 00000000	SHA Hash Part C generated by on chip micro	

Reg	Bits	Description	
SHA_D[31:0]			R/W
0x2C 0x2D 0x2E 0x2F	00000000 00000000 00000000 00000000	SHA Hash Part D generated by on chip micro	
SHA_E[31:0]			R/W
0x30 0x31 0x32 0x33	00000000 00000000 00000000 00000000	SHA Hash Part E generated by inchip micro	
BCAPS[7:0]			R/W
0x40	10000011	This is the BCAPS register presented to the Tx attached to the active HDMI port. 10000011 - Default BCAPS register value presented to the Tx xxxxxxxx - BCAPS register value presented to Tx	
BSTATUS[15:0]			R/W
0x41 0x42	00000000 00000000	These registers contain the BSTATUS information presented to the Tx attached to the active HDMI port. Bits [11:0] must be set by the system software acting as a repeater. 0x41[7:0] = BSTATUS[7:0], 0x42[7:0] = BSTATUS[15:8] xxxxxxxxxxxxxxxx - BSTATUS register presented to Tx 0000000000000000 - Reset value. BSTATUS register is reset only after power up.	
SPA_PORT_B[15:0]			R/W
0x52 0x53	00000000 00000000	Source physical address for port B. This is used for CEC and is located in the HDMI Vendor Specific data block in the E-EDID 0000000000000000 - Default value xxxxxxxxxxxxxxxx - Source physical address of Port B	
SPA_PORT_C[15:0]			R/W
0x54 0x55	00000000 00000000	Source physical address for port C. This is used for CEC and is located in the HDMI Vendor Specific data block in the E-EDID 0000000000000000 - Default value xxxxxxxxxxxxxxxx - Source physical address of Port C	
SPA_PORT_D[15:0]			R/W
0x56 0x57	00000000 00000000	Source physical address for port D. This is used for CEC and is located in the HDMI Vendor Specific data block in the E-EDID 0000000000000000 - Default value xxxxxxxxxxxxxxxx - Source physical address of Port D	
PORT_B_CHECKSUM[7:0]			R/W
0x61	00000000	This is the checksum for the second half of the Port B EDID. This is calculated automatically. 00000000 - Default value xxxxxxxx - Checksum for E-EDID block containing SPA for Port B	
PORT_C_CHECKSUM[7:0]			R/W
0x62	00000000	This is the checksum for the second half of the Port C EDID. This is calculated automatically. 00000000 - Default value xxxxxxxx - Checksum for E-EDID block containing SPA for Port C	
PORT_D_CHECKSUM[7:0]			R/W
0x63	00000000	This is the checksum for the second half of the Port D EDID. This is calculated automatically. 00000000 - Default value xxxxxxxx - Checksum for E-EDID block containing SPA for Port D	
SPA_LOCATION[7:0]			R/W
0x70	11000000	This is the location in the E-EDID record where the SPA is located. 11000000 - Default value xxxxxxxx - Location of source physical address in internal E-EDID of Ports B, C and D	
KSV_LIST_READY			R/W
0x71	00000000	The system sets this bit in order to indicate that the KSV list has been read from the Tx IC(s) and written into the Repeater Map. The system must also set bits [11:0] of Bstatus before setting this bit. 0 - KSV list not ready 1 - KSV list ready	

Reg	Bits	Description	
SPA_LOCATION_MSB			R/W
0x71	0000000<u>0</u>	Additional MSB of SPA_location (i.e. spa_location[8]) needed to point to SPAs stored in second segment. 0 - Default value	
EXT_EEPROM_TRI			R/W
0x72	0<u>0</u>000000	Tri-states the output pins to the external SPI EEPROM 0 - SPI interface outputs enabled 1 - SPI interface outputs tristated	
EXT_EEPROM_MAN_SELECT			R/W
0x72	00<u>0</u>00000	Manual override for external EEPROM memory addressing mode 0 - Automatic detection of external EEPROM type of adressing (8 or 16 bit address field) 1 - Manual override of type of external EEPROM (to be used with register ext_eeprom_man_value)	
EXT_EEPROM_MAN_VALUE			R/W
0x72	000<u>0</u>0000	Value for manual override of external EEPROM memory adressing mode 0 - External EEPROM uses 16 bit address field 1 - External EEPROM uses 8 bit address field	
MAN_EDID_D_ENABLE			R/W
0x74	0000<u>0</u>000	Manual enable for I2C access to internal EDID RAM from DDC port D, when the operations LOAD_EDID and CKSUM_CALC are finished. 0 - Manual enable not active for E-EDID on port D 1 - Manual enable active for E-EDID on port D	
MAN_EDID_C_ENABLE			R/W
0x74	00000<u>0</u>00	Manual enable for I2C access to internal EDID RAM from DDC port C, when the operations LOAD_EDID and CKSUM_CALC are finished. 0 - Manual enable not active for E-EDID on port C 1 - Manual enable active for E-EDID on port C	
MAN_EDID_B_ENABLE			R/W
0x74	000000<u>0</u>0	Manual enable for I2C access to internal EDID RAM from DDC port B, when the operations LOAD_EDID and CKSUM_CALC are finished. 0 - Manual enable not active for E-EDID on port B 1 - Manual enable active for E-EDID on port B	
MAN_EDID_A_ENABLE			R/W
0x74	0000000<u>0</u>	Manual enable for I2C access to internal EDID RAM from DDC port A, when the operations LOAD_EDID and CKSUM_CALC are finished. 0 - Manual enable not active for E-EDID on port A 1 - Manual enable active for E-EDID on port A	
EDID_D_ENABLED			R
0x76	0000<u>0</u>000	Resulting I2C enable readback for EDID access on port D, after a combination of manual and automatic functions. 0 - Disabled 1 - Enabled	
EDID_C_ENABLED			R
0x76	00000<u>0</u>00	Resulting I2C enable readback for EDID access on port C, after a combination of manual and automatic functions. 0 - Disabled 1 - Enabled	
EDID_B_ENABLED			R
0x76	000000<u>0</u>0	Resulting I2C enable readback for EDID access on port B, after a combination of manual and automatic functions. 0 - Disabled 1 - Enabled	
EDID_A_ENABLED			R
0x76	0000000<u>0</u>	Resulting I2C enable readback for EDID access on port A, after a combination of manual and automatic functions. 0 - Disabled 1 - Enabled	
CLEAR_KSV_LIST			SC
0x77	0000<u>0</u>000	Clears KSV list from memory	

Reg	Bits	Description	
CKSUM_CALC			SC
0x77	00000000	Force a full re-calculation of all checksums for the internal E-EDID for all ports 0 - No effect 1 - Calculate checksums of all internal EDID contents for all ports	
LOAD_EDID			SC
0x77	00000000	Trigger to force loading internal E-EDID RAM with external SPI EEPROM contents. This automatically triggers a CKSUM_CALC event 0 - No effect 1 - Load internal E-EDID with SPI EEPROM contents	
STORE_EDID			SC
0x77	00000000	Trigger to write contents of internal E-EDID RAM to external SPI EEPROM 0 - No effect 1 - Write contents of internal E-EDID to SPI EEPROM	
KSV_LIST_READY_CLR_D			SC
0x78	00000000	Clear BCAPS KSV list ready bit in port D 0 - No effect 1 - Clears BCAPS KSV list ready bit. (Self clearing bit)	
KSV_LIST_READY_CLR_C			SC
0x78	00000000	Clear BCAPS KSV list ready bit in port C 0 - No effect 1 - Clears BCAPS KSV list ready bit. (Self clearing bit)	
KSV_LIST_READY_CLR_B			SC
0x78	00000000	Clear BCAPS KSV list ready bit in port B 0 - No effect 1 - Clears BCAPS KSV list ready bit. (Self clearing bit)	
KSV_LIST_READY_CLR_A			SC
0x78	00000000	Clear BCAPS KSV list ready bit in port A 0 - No effect 1 - Clears BCAPS KSV list ready bit. (Self clearing bit)	
KSV_MAP_SELECT[2:0]			R/W
0x79	10001000	Selects which 128 bytes of KSV list will be accessed when reading or writing to addresses 0x80 to 0xFF in this map. Values from 5 and upwards are not valid	
AUTO_HDCP_MAP_ENABLE			R/W
0x79	10001000	Selects which port will be accessed for HDCP addresses: the HDMI active port (selected by HDMI_PORT_SELECT, HDMI Map) or the one selected in HDCP_MAP_SELECT. 0 - HDCP data read from port given by HDCP_MAP_SELECT 1 - HDCP data read from the active HDMI port	
HDCP_MAP_SELECT[2:0]			R/W
0x79	10001000	Selects which port will be accessed for HDCP addresses (0x00 to 0x42 in Repeater Map). This only takes effect when AUTO_HDCP_MAN_ENABLE is 0. 000 - Select Port A 001 - Select Port B 010 - Select Port C 011 - Select Port D	
DISABLE_AUTO_EDID			R/W
0x7A	00000100	Disables all automatic enables for internal E-EDID 0 - Automatic enable of internal E-EDID on HDMI ports when the part comes out of powerdown mode 1 - Disable automatic enable of internal E-EDID on HDMI ports when the part comes out of powerdown mode	
HDMI_EDID_SEGMENT_SEL			R/W
0x7A	00000100	Selects one of the 2 SRAM memory banks for HDMI EDID segments to be accessed via EDID I2C Map 0 - Main I2C EDID access for HDMI EDID segment 0 1 - Main I2C EDID access for HDMI EDID segment 1	

Reg	Bits	Description	
SPI_CFG[5:0]			R/W
0x7C	00000000	SPI configuration values read from the SPI EEPROM byte 0 in an EDID_LOAD opeartion, or to be written to the same byte during an EDID_STORE operation. Mapping is Byte0[5:0]=SPI_CFG[5:0] SPI_CFG[5] - SPA_BOUBLE_BYTE SPI_CFG[4] - VGA_EDID_PRESENT SPI_CFG[3] - Dual EDID present SPI_CFG[2] - Assert HPA in power off mode SPI_CFG[1:0] - NUM_256BYTE_BLOCKS_PRESENT	
DUAL_EDID_ENABLE_PORT_D			R/W
0x7D	00000000	Enables accessing a second EDID image on this port. Also affects SPA and checksum access	
DUAL_EDID_ENABLE_PORT_C			R/W
0x7D	00000000	Enables accessing a second EDID image on this port. Also affects SPA and checksum access	
DUAL_EDID_ENABLE_PORT_B			R/W
0x7D	00000000	Enables accessing a second EDID image on this port. Also affects SPA and checksum access	
DUAL_EDID_ENABLE_PORT_A			R/W
0x7D	00000000	Enables accessing a second EDID image on this port. Also affects SPA and checksum access	
SPA_SECONDARY_LOCATION[7:0]			R/W
0x7E	11000000	SPA location register for secondary EDID image 0 - Default value	
KSV_BYTE_0[7:0]			R/W
0x80	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_1[7:0]			R/W
0x81	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_2[7:0]			R/W
0x82	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_3[7:0]			R/W
0x83	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_4[7:0]			R/W
0x84	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_5[7:0]			R/W
0x85	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_6[7:0]			R/W
0x86	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_7[7:0]			R/W
0x87	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_8[7:0]			R/W
0x88	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_9[7:0]			R/W
0x89	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	

Reg	Bits	Description	
KSV_BYTE_10[7:0]			R/W
0x8A	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_11[7:0]			R/W
0x8B	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_12[7:0]			R/W
0x8C	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_13[7:0]			R/W
0x8D	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_14[7:0]			R/W
0x8E	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_15[7:0]			R/W
0x8F	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_16[7:0]			R/W
0x90	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_17[7:0]			R/W
0x91	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_18[7:0]			R/W
0x92	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_19[7:0]			R/W
0x93	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_20[7:0]			R/W
0x94	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_21[7:0]			R/W
0x95	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_22[7:0]			R/W
0x96	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_23[7:0]			R/W
0x97	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_24[7:0]			R/W
0x98	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_25[7:0]			R/W
0x99	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_26[7:0]			R/W
0x9A	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	

Reg	Bits	Description	
KSV_BYTE_27[7:0]			R/W
0x9B	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_28[7:0]			R/W
0x9C	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_29[7:0]			R/W
0x9D	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_30[7:0]			R/W
0x9E	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_31[7:0]			R/W
0x9F	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_32[7:0]			R/W
0xA0	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_33[7:0]			R/W
0xA1	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_34[7:0]			R/W
0xA2	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_35[7:0]			R/W
0xA3	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_36[7:0]			R/W
0xA4	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_37[7:0]			R/W
0xA5	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_38[7:0]			R/W
0xA6	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_39[7:0]			R/W
0xA7	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_40[7:0]			R/W
0xA8	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_41[7:0]			R/W
0xA9	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_42[7:0]			R/W
0xAA	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_43[7:0]			R/W
0xAB	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	

Reg	Bits	Description	
KSV_BYTE_44[7:0]			R/W
0xAC	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_45[7:0]			R/W
0xAD	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_46[7:0]			R/W
0xAE	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_47[7:0]			R/W
0xAF	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_48[7:0]			R/W
0xB0	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_49[7:0]			R/W
0xB1	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_50[7:0]			R/W
0xB2	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_51[7:0]			R/W
0xB3	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_52[7:0]			R/W
0xB4	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_53[7:0]			R/W
0xB5	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_54[7:0]			R/W
0xB6	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_55[7:0]			R/W
0xB7	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_56[7:0]			R/W
0xB8	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_57[7:0]			R/W
0xB9	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_58[7:0]			R/W
0xBA	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_59[7:0]			R/W
0xBB	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_60[7:0]			R/W
0xBC	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	

Reg	Bits	Description	
KSV_BYTE_61[7:0]			R/W
0xBD	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_62[7:0]			R/W
0xBE	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_63[7:0]			R/W
0xBF	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_64[7:0]			R/W
0xC0	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_65[7:0]			R/W
0xC1	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_66[7:0]			R/W
0xC2	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_67[7:0]			R/W
0xC3	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_68[7:0]			R/W
0xC4	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_69[7:0]			R/W
0xC5	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_70[7:0]			R/W
0xC6	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_71[7:0]			R/W
0xC7	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_72[7:0]			R/W
0xC8	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_73[7:0]			R/W
0xC9	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_74[7:0]			R/W
0xCA	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_75[7:0]			R/W
0xCB	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_76[7:0]			R/W
0xCC	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_77[7:0]			R/W
0xCD	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	

Reg	Bits	Description	
KSV_BYTE_78[7:0]			R/W
0xCE	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_79[7:0]			R/W
0xCF	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_80[7:0]			R/W
0xD0	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_81[7:0]			R/W
0xD1	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_82[7:0]			R/W
0xD2	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_83[7:0]			R/W
0xD3	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_84[7:0]			R/W
0xD4	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_85[7:0]			R/W
0xD5	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_86[7:0]			R/W
0xD6	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_87[7:0]			R/W
0xD7	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_88[7:0]			R/W
0xD8	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_89[7:0]			R/W
0xD9	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_90[7:0]			R/W
0xDA	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_91[7:0]			R/W
0xDB	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_92[7:0]			R/W
0xDC	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_93[7:0]			R/W
0xDD	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_94[7:0]			R/W
0xDE	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	

Reg	Bits	Description	
KSV_BYTE_95[7:0]			R/W
0xDF	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_96[7:0]			R/W
0xE0	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_97[7:0]			R/W
0xE1	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_98[7:0]			R/W
0xE2	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_99[7:0]			R/W
0xE3	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_100[7:0]			R/W
0xE4	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_101[7:0]			R/W
0xE5	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_102[7:0]			R/W
0xE6	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_103[7:0]			R/W
0xE7	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_104[7:0]			R/W
0xE8	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_105[7:0]			R/W
0xE9	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_106[7:0]			R/W
0xEA	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_107[7:0]			R/W
0xEB	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_108[7:0]			R/W
0xEC	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_109[7:0]			R/W
0xED	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_110[7:0]			R/W
0xEE	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_111[7:0]			R/W
0xEF	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	

Reg	Bits	Description	
KSV_BYTE_112[7:0]			R/W
0xF0	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_113[7:0]			R/W
0xF1	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_114[7:0]			R/W
0xF2	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_115[7:0]			R/W
0xF3	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_116[7:0]			R/W
0xF4	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_117[7:0]			R/W
0xF5	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_118[7:0]			R/W
0xF6	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_119[7:0]			R/W
0xF7	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_120[7:0]			R/W
0xF8	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_121[7:0]			R/W
0xF9	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_122[7:0]			R/W
0xFA	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_123[7:0]			R/W
0xFB	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_124[7:0]			R/W
0xFC	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_125[7:0]			R/W
0xFD	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_126[7:0]			R/W
0xFE	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	
KSV_BYTE_127[7:0]			R/W
0xFF	00000000	This is a byte in the KSV list used for the HDCP repeater protocol. This may come from any of 5 128 byte segments, controlled by KSV_MAP_SELECT	

2.4 INFOFRAME MAP

Reg	Bits	Description	
AVI_INF_PB[223:0]			R
0x00	00000000	AVI InfoFrame Data	
0x01	00000000		
0x02	00000000		
0x03	00000000		
0x04	00000000		
0x05	00000000		
0x06	00000000		
0x07	00000000		
0x08	00000000		
0x09	00000000		
0x0A	00000000		
0x0B	00000000		
0x0C	00000000		
0x0D	00000000		
0x0E	00000000		
0x0F	00000000		
0x10	00000000		
0x11	00000000		
0x12	00000000		
0x13	00000000		
0x14	00000000		
0x15	00000000		
0x16	00000000		
0x17	00000000		
0x18	00000000		
0x19	00000000		
0x1A	00000000		
0x1B	00000000		
AUD_INF_PB[111:0]			R
0x1C	00000000	Audio InfoFrame Data	
0x1D	00000000		
0x1E	00000000		
0x1F	00000000		
0x20	00000000		
0x21	00000000		
0x22	00000000		
0x23	00000000		
0x24	00000000		
0x25	00000000		
0x26	00000000		
0x27	00000000		
0x28	00000000		
0x29	00000000		

Reg	Bits	Description	
SPD_INF_PB[223:0]			R
0x2A	00000000	Source Product Descriptor InfoFrame Data	
0x2B	00000000		
0x2C	00000000		
0x2D	00000000		
0x2E	00000000		
0x2F	00000000		
0x30	00000000		
0x31	00000000		
0x32	00000000		
0x33	00000000		
0x34	00000000		
0x35	00000000		
0x36	00000000		
0x37	00000000		
0x38	00000000		
0x39	00000000		
0x3A	00000000		
0x3B	00000000		
0x3C	00000000		
0x3D	00000000		
0x3E	00000000		
0x3F	00000000		
0x40	00000000		
0x41	00000000		
0x42	00000000		
0x43	00000000		
0x44	00000000		
0x45	00000000		
MS_INF_PB[111:0]			R
0x46	00000000	Moving Picture Expert Group (MPEG) Source InfoFrame Data	
0x47	00000000		
0x48	00000000		
0x49	00000000		
0x4A	00000000		
0x4B	00000000		
0x4C	00000000		
0x4D	00000000		
0x4E	00000000		
0x4F	00000000		
0x50	00000000		
0x51	00000000		
0x52	00000000		
0x53	00000000		

Reg	Bits	Description	
VS_INF_PB[223:0]			R
0x54	00000000	Vendor Specific InfoFrame Data	
0x55	00000000		
0x56	00000000		
0x57	00000000		
0x58	00000000		
0x59	00000000		
0x5A	00000000		
0x5B	00000000		
0x5C	00000000		
0x5D	00000000		
0x5E	00000000		
0x5F	00000000		
0x60	00000000		
0x61	00000000		
0x62	00000000		
0x63	00000000		
0x64	00000000		
0x65	00000000		
0x66	00000000		
0x67	00000000		
0x68	00000000		
0x69	00000000		
0x6A	00000000		
0x6B	00000000		
0x6C	00000000		
0x6D	00000000		
0x6E	00000000		
0x6F	00000000		
ACP_PB[223:0]			R
0x70	00000000	ACP InfoFrame Data	
0x71	00000000		
0x72	00000000		
0x73	00000000		
0x74	00000000		
0x75	00000000		
0x76	00000000		
0x77	00000000		
0x78	00000000		
0x79	00000000		
0x7A	00000000		
0x7B	00000000		
0x7C	00000000		
0x7D	00000000		
0x7E	00000000		
0x7F	00000000		
0x80	00000000		
0x81	00000000		
0x82	00000000		
0x83	00000000		
0x84	00000000		
0x85	00000000		
0x86	00000000		
0x87	00000000		
0x88	00000000		
0x89	00000000		
0x8A	00000000		
0x8B	00000000		

Reg	Bits	Description	
ISRC1_PB[223:0]			R
0x8C	00000000	ISRC 1 InfoFrame Data	
0x8D	00000000		
0x8E	00000000		
0x8F	00000000		
0x90	00000000		
0x91	00000000		
0x92	00000000		
0x93	00000000		
0x94	00000000		
0x95	00000000		
0x96	00000000		
0x97	00000000		
0x98	00000000		
0x99	00000000		
0x9A	00000000		
0x9B	00000000		
0x9C	00000000		
0x9D	00000000		
0x9E	00000000		
0x9F	00000000		
0xA0	00000000		
0xA1	00000000		
0xA2	00000000		
0xA3	00000000		
0xA4	00000000		
0xA5	00000000		
0xA6	00000000		
0xA7	00000000		
ISRC2_PB[223:0]			R
0xA8	00000000	ISRC 2 InfoFrame Data	
0xA9	00000000		
0xAA	00000000		
0xAB	00000000		
0xAC	00000000		
0xAD	00000000		
0xAE	00000000		
0xAF	00000000		
0xB0	00000000		
0xB1	00000000		
0xB2	00000000		
0xB3	00000000		
0xB4	00000000		
0xB5	00000000		
0xB6	00000000		
0xB7	00000000		
0xB8	00000000		
0xB9	00000000		
0xBA	00000000		
0xBB	00000000		
0xBC	00000000		
0xBD	00000000		
0xBE	00000000		
0xBF	00000000		
0xC0	00000000		
0xC1	00000000		
0xC2	00000000		
0xC3	00000000		

Reg	Bits	Description	
GBD[223:0]			R
0xC4	00000000	Gamut InfoFrame Data	
0xC5	00000000		
0xC6	00000000		
0xC7	00000000		
0xC8	00000000		
0xC9	00000000		
0xCA	00000000		
0xCB	00000000		
0xCC	00000000		
0xCD	00000000		
0xCE	00000000		
0xCF	00000000		
0xD0	00000000		
0xD1	00000000		
0xD2	00000000		
0xD3	00000000		
0xD4	00000000		
0xD5	00000000		
0xD6	00000000		
0xD7	00000000		
0xD8	00000000		
0xD9	00000000		
0xDA	00000000		
0xDB	00000000		
0xDC	00000000		
0xDD	00000000		
0xDE	00000000		
0xDF	00000000		
AVI_PACKET_ID[7:0]			R/W
0xE0	10000010	AVI InfoFrame packet type value. 0xxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x00 to 0x1B 1xxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x00 to 0x1B	
AVI_INF_VERS[7:0]			R
0xE1	00000000	AVI InfoFrame Version xxxxxxxx - Readback value	
AVI_INF_LEN[7:0]			R
0xE2	00000000	AVI InfoFrame Length xxxxxxxx - Readback value	
AUD_PACKET_ID[7:0]			R/W
0xE3	10000100	Audio InfoFrame packet type value. xxxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x1C to 0x29	
AUD_INF_VERS[7:0]			R
0xE4	00000000	Audio InfoFrame Version xxxxxxxx - Readback value	
AUD_INF_LEN[7:0]			R
0xE5	00000000	Audio InfoFrame Length xxxxxxxx - Readback value	
SPD_PACKET_ID[7:0]			R/W
0xE6	10000011	Source Product Descriptor InfoFrame packet type value. xxxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x2A to 0x45	
SPD_INF_VERS[7:0]			R
0xE7	00000000	Source Product Descriptor InfoFrame Version xxxxxxxx - Readback value	
SPD_INF_LEN[7:0]			R
0xE8	00000000	Source Product Descriptor InfoFrame Length xxxxxxxx - Readback value	

Reg	Bits	Description	
MS_PACKET_ID[7:0]			R/W
0xE9	10000101	MPEG Source InfoFrame ID packet type value. xxxxxxxx - Packet type value of InfoFrame stored in InfoFrame Map, Address 0x46 to 0x53	
MS_INF_VERS[7:0]			R
0xEA	00000000	MPEG Source InfoFrame Version xxxxxxxx - Readback value	
MS_INF_LEN[7:0]			R
0xEB	00000000	MPEG Source InfoFrame Length xxxxxxxx - Readback value	
VS_PACKET_ID[7:0]			R/W
0xEC	10000001	Vendor Specific InfoFrame ID packet type value. xxxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x54 to 0x6F	
VS_INF_VERS[7:0]			R
0xED	00000000	Vendor Specific InfoFrame Version xxxxxxxx - Readback value	
VS_INF_LEN[7:0]			R
0xEE	00000000	Vendor Specific InfoFrame Length xxxxxxxx - Readback value	
ACP_PACKET_ID[7:0]			R/W
0xEF	00000100	ACP Packet ID packet type value. xxxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x70 to 0x8B	
ACP_TYPE[7:0]			R
0xF0	00000000	ACP Type xxxxxxxx - Readback value	
ACP_HEADER2[7:0]			R
0xF1	00000000	ACP Header 2 xxxxxxxx - Readback value	
ISRC1_PACKET_ID[7:0]			R/W
0xF2	00000101	ISRC1 Packet ID packet type value. xxxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0x8C to 0xA7	
ISRC1_HEADER1[7:0]			R
0xF3	00000000	ISRC1 Header 1 xxxxxxxx - Readback value	
ISRC1_HEADER2[7:0]			R
0xF4	00000000	ISRC1 Header 2 xxxxxxxx - Readback value	
ISRC2_PACKET_ID[7:0]			R/W
0xF5	00000110	ISRC2 Packet ID packet type value. xxxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0xA8 to 0xC3	
ISRC2_HEADER1[7:0]			R
0xF6	00000000	ISRC2 Header 1 xxxxxxxx - Readback value	
ISRC2_HEADER2[7:0]			R
0xF7	00000000	ISRC2 Header 2 xxxxxxxx - Readback value	
GAMUT_PACKET_ID[7:0]			R/W
0xF8	00001010	Gamut Metadata Packet ID packet type value. xxxxxxxx - Packet type value of packet stored in InfoFrame Map, Address 0xC4 to 0xDF	
GAMUT_HEADER1[7:0]			R
0xF9	00000000	Gamut Metadata Header 1 xxxxxxxx - Readback value	

Reg	Bits	Description	
GAMUT_HEADER2[7:0]			R
0xFA	00000000	Gamut Metadata Header 2	
PKT_CNT_ID[7:0]			R/W
0xFD	10000001	Select which type of packet is going to be counted during each frame. Any packet header ID is supported to detect the count, but only collectable packets can be stored. Default is 0x81 for Vendor Specific Infoframe. 10000001 - Default value	
EN_PKT_CNT_SEL			R/W
0xFE	0000**0**0000	Enable the feature whereby one can choose which of the multiple received packets per frame of type PKT_CNT_ID is to be collected. This feature is only relevant for packet types that can be stored in the Infoframe map. 0 - Disabled. Collect avery packet as it is received 1 - Enable selectively collecting one of multiple packets per frame of the same type	
PKT_CNT_SEL[3:0]			R/W
0xFE	0000**0000**	Select which one of the multplile received packets per frame of type PKT_CNT_ID is to be collected. Must be enabled with EN_PKT_CNT_SEL. It should be manually changed after receiving the corresponding new packet detect flag 0 - Select the 1st packet after VSync rising edge 1 - Select the 2nd packet after VSync rising edge x - Select the (X+1)th packet after VSync rising edge 14 - Select the 15th packet after VSync rising edge 15 - Undefined	
RB_PKT_CNT[3:0]			R
0xFF	0000**0000**	Readback the count of number of packets of type PKT_CNT_ID per frame, as detected between Vsync rising edges. The count readback is supported for any PKT_CNT_ID, even those that can not be stored in the Infoframe map (e.g. General control packets, and even custom ID packets). The count will saturate to the 15 maximum, even if more packets are received. A count of zero represents that no packet were detected. xxxx - Readback value	

2.5 CEC MAP

Reg	Bits	Description	
CEC_TX_FRAME_HEADER[7:0]			R/W
0x00	00000000	Header block in the transmitted frame	
CEC_TX_FRAME_DATA0[7:0]			R/W
0x01	00000000	Opcode block in the transmitted frame	
CEC_TX_FRAME_DATA1[7:0]			R/W
0x02	00000000	Operand 1 in the transmitted frame	
CEC_TX_FRAME_DATA2[7:0]			R/W
0x03	00000000	Operand 2 in the transmitted frame	
CEC_TX_FRAME_DATA3[7:0]			R/W
0x04	00000000	Operand 3 in the transmitted frame	
CEC_TX_FRAME_DATA4[7:0]			R/W
0x05	00000000	Operand 4 in the transmitted frame	
CEC_TX_FRAME_DATA5[7:0]			R/W
0x06	00000000	Operand 5 in the transmitted frame	
CEC_TX_FRAME_DATA6[7:0]			R/W
0x07	00000000	Operand 6 in the transmitted frame	
CEC_TX_FRAME_DATA7[7:0]			R/W
0x08	00000000	Operand 7 in the transmitted frame	
CEC_TX_FRAME_DATA8[7:0]			R/W
0x09	00000000	Operand 8 in the transmitted frame	
CEC_TX_FRAME_DATA9[7:0]			R/W
0x0A	00000000	Operand 9 in the transmitted frame	
CEC_TX_FRAME_DATA10[7:0]			R/W
0x0B	00000000	Operand 10 in the transmitted frame	
CEC_TX_FRAME_DATA11[7:0]			R/W
0x0C	00000000	Operand 11 in the transmitted frame	
CEC_TX_FRAME_DATA12[7:0]			R/W
0x0D	00000000	Operand 12 in the transmitted frame	
CEC_TX_FRAME_DATA13[7:0]			R/W
0x0E	00000000	Operand 13 in the transmitted frame	
CEC_TX_FRAME_DATA14[7:0]			R/W
0x0F	00000000	Operand 14 in the transmitted frame	
CEC_TX_FRAME_LENGTH[4:0]			R/W
0x10	00000000	Message size of the transmitted frame. This is the number of byte in the outgoing message including the header. xxxxx - Total number of bytes (including header byte) to be sent	

Reg	Bits	Description	
CEC_TX_ENABLE			R/W
0x11	0000000**0**	This bit enables the TX section. When set to 1 it initiates the start of transmission of the message in the outgoing message buffer. When the message transmission is completed this bit is automatically reset to 0. If it is manually set to 0 during a messa 0 - Transmission mode disabled 1 - Transmission mode enabled and message transmission started	
CEC_TX_RETRY[2:0]			R/W
0x12	0**001**0011	The number of times the CEC TX should try to retransmit the message if an error condition is encountered. Per the CEC spec this value should not be set to a value greater than 5. 001 - Try to retransmit the message 1 time if an error occurs xxx - Try to retransmit the message xxx times if an error occurs	
CEC_RETRY_SFT[3:0]			R/W
0x12	0001**0011**	Signal Free Time of periods for retransmission retry. This parameter should be set to a value equal to or greater than 3 and strictly less than 5.	
CEC_TX_SFT[3:0]			R/W
0x13	**0101**0111	Signal Free Time if the device is a new initiator. This parameter should be set to a value equal to or greater than 5 and strictly less than 7.	
CEC_TX_SFT[3:0]			R/W
0x13	0101**0111**	Signal Free Time if the device transmits a next frame immediately after its previous frame. This parameter should be set to a value equal to or greater than 7 and strictly less than 10.	
CEC_TX_LOWDRIVE_COUNTER[3:0]			R
0x14	**0000**0000	The number of times that the LOWDRIVE error condition was encountered while trying to send the current message. This register is reset to 0b0000 when CEC_TX_ENABLE is set to 1. 0000 - No error condition XXXX - The number of times the LOWDRIVE error condition was encountered	
CEC_TX_NACK_COUNTER[3:0]			R
0x14	0000**0000**	The number of times that the NACK error condition was encountered while trying to send the current message. This register is reset to 0b0000 when CEC_TX_ENABLE is set to 1. 0000 - No error condition XXXX - The number of times the NACK error condition was encountered	
CEC_BUF0_RX_FRAME_HEADER[7:0]			R
0x15	**00000000**	Header block of the received frame stored in receiver frame buffer 0.	
CEC_BUF0_RX_FRAME_DATA0[7:0]			R
0x16	**00000000**	Opcode block of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA1[7:0]			R
0x17	**00000000**	Operand 1 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA2[7:0]			R
0x18	**00000000**	Operand 2 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA3[7:0]			R
0x19	**00000000**	Operand 3 of the received frame in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA4[7:0]			R
0x1A	**00000000**	Operand 4 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA5[7:0]			R
0x1B	**00000000**	Operand 5 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA6[7:0]			R
0x1C	**00000000**	Operand 6 of the received frame stored in receiver frame buffer 0	

Reg	Bits	Description	
CEC_BUF0_RX_FRAME_DATA7[7:0]			R
0x1D	00000000	Operand 7 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA8[7:0]			R
0x1E	00000000	Operand 8 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA9[7:0]			R
0x1F	00000000	Operand 9 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA10[7:0]			R
0x20	00000000	Operand 10 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA11[7:0]			R
0x21	00000000	Operand 11 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA12[7:0]			R
0x22	00000000	Operand 12 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA13[7:0]			R
0x23	00000000	Operand 13 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_DATA14[7:0]			R
0x24	00000000	Operand 14 of the received frame stored in receiver frame buffer 0	
CEC_BUF0_RX_FRAME_LENGTH[4:0]			R
0x25	00000000	xxxxx - The total number of bytes (including header byte) that were received into buffer 0	
CEC_LOGICAL_ADDRESS_MASK[2:0]			R/W
0x27	00010000	Logical Address mask of the CEC logical devices. Up to 3 logical devices are supported. When the mask bits are set for a particular logical device, the logical device is enabled and messages whose destination address matches that of the selected logical a [4] - mask bit for logical device 0 [5] - mask bit for logical device 1 [6] - mask bit for logical device 2	
CEC_ERROR_REPORT_MODE			R/W
0x27	00010000	Error report mode 0 - Only report short bit period errors 1 - Report both short and long bit period errors	
CEC_ERROR_DET_MODE			R/W
0x27	00010000	Error detection mode 0 - If any short bit period error, except for start bit, is detected, the CEC controller immediately drives the CEC line low for 3.6ms 1 - If a short bit period is detected in the data block where the destination is the CEC section or a target CEC device, t	
CEC_FORCE_NACK			R/W
0x27	00010000	Force NO-ACK Control Setting this bit forces the CEC controller not acknowledge any received messages. 0 - Acknowledge received messages 1 - Do not acknowledge received messages	
CEC_FORCE_IGNORE			R/W
0x27	00010000	Force Ignore Control. Setting this bit forces the CEC controller to ignore any directly addressed messages. Normal operation should be kept for the broadcast message 0 - Do not ignore directly address messages 1 - Ignore any directly addressed message	
CEC_LOGICAL_ADDRESS1[3:0]			R/W
0x28	11111111	Logical address 1 - this address must be enabled by setting CEC_LOGICAL_ADDRESS_MASK[1] to 1 1111 - Default value xxxx - User specified logical address	

Reg	Bits	Description	
CEC_LOGICAL_ADDRESS0[3:0]			R/W
0x28	1111<u>1111</u>	Logical address 0 - this address must be enabled by setting CEC_LOGICAL_ADDRESS_MASK[0] to 1 1111 - Default value xxxx - User specified logical address	
CEC_LOGICAL_ADDRESS2[3:0]			R/W
0x29	0000<u>1111</u>	Logical address 2 - this address must be enabled by setting CEC_LOGICAL_ADDRESS_MASK[2] to 1 1111 - Default value xxxx - User specified logical address	
CEC_POWER_UP			R/W
0x2A	0011111<u>0</u>	Power Mode of CEC module 0 - Power down the CEC module 1 - Power up the CEC module	
CEC_GLITCH_FILTER_CTRL[5:0]			R/W
0x2B	00<u>000111</u>	The CEC input signal is sampled by the input clock (XTAL clock). CEC_GLITCH_FILTER_CTRL specifies the minimum pulse width requirement in input clock cycles. Pulses of widths less than the minimum specified width are considered glitches and will be removed 000000 - Disable the glitch filter 000001 - Filter out pulses with width less than 1 clock cycle 000010 - Filter out pulses with width less than 2 clock cycles - ... 000111 - Filter out pulses with width less than 7 clock cycles - ... 111111 - Filter out pulses wi	
CEC_CLR_RX_RDY2			SC
0x2C	0000<u>0</u>000	Clear control for CEC_RX_RDY2 0 - Retain the value of the CEC_RX_RDY2 flag 1 - Clear the value of the CEC_RX_RDY2 flag	
CEC_CLR_RX_RDY1			SC
0x2C	00000<u>0</u>00	Clear control for CEC_RX_RDY1 0 - Retain the value of the CEC_ RX_RDY1 flag 1 - Clear the value of the CEC_RX_RDY1 flag	
CEC_CLR_RX_RDY0			SC
0x2C	000000<u>0</u>0	Clear control for CEC_RX_RDY0 0 - Retain the value of the CEC_RX_RDY0 flag 1 - Clear the value of the CEC_RX_RDY0 flag	
CEC_SOFT_RESET			SC
0x2C	0000000<u>0</u>	CEC module software reset. 0 - No function 1 - Reset the CEC module	
CEC_DIS_AUTO_MODE			R/W
0x4C	00000<u>0</u>00	A control to disable the automatic CEC power up feature when in chip powerdown mode. 0 - Automatic power up feature enabled 1 - Automatic power up feature disabled	
CEC_BUF2_TIMESTAMP[1:0]			R
0x53	00<u>00</u>0000	Time stamp for frame stored in receiver frame buffer 2. This can be used to determine which frame should be read next from the receiver frame buffers. 00 - Invalid timestamp, no frame is available in this frame buffer 01 - Of the frames currently buffered, this frame was the first to be received 10 - Of the frames currently buffered, this frame was the second to be received 11 - Of the frames currently buff	
CEC_BUF1_TIMESTAMP[1:0]			R
0x53	0000<u>00</u>00	Time stamp for frame stored in receiver frame buffer 1. This can be used to determine which frame should be read next from the receiver frame buffers. 00 - Invalid timestamp, no frame is available in this frame buffer 01 - Of the frames currently buffered, this frame was the first to be received 10 - Of the frames currently buffered, this frame was the second to be received 11 - Of the frames currently buff	

Reg	Bits	Description	
CEC_BUF0_TIMESTAMP[1:0]			R
0x53	000000<u>00</u>	Time stamp for frame stored in receiver frame buffer 0. This can be used to determine which frame should be read next from the receiver frame buffers. 00 - Invalid timestamp, no frame is available in this frame buffer 01 - Of the frames currently buffered, this frame was the first to be received 10 - Of the frames currently buffered, this frame was the second to be received 11 - Of the frames currently buff	
CEC_BUF1_RX_FRAME_HEADER[7:0]			R
0x54	<u>00000000</u>	Header block of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA0[7:0]			R
0x55	<u>00000000</u>	Opcode block of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA1[7:0]			R
0x56	<u>00000000</u>	Operand 1 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA2[7:0]			R
0x57	<u>00000000</u>	Operand 2 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA3[7:0]			R
0x58	<u>00000000</u>	Operand 3 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA4[7:0]			R
0x59	<u>00000000</u>	Operand 4 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA5[7:0]			R
0x5A	<u>00000000</u>	Operand 5 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA6[7:0]			R
0x5B	<u>00000000</u>	Operand 6 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA7[7:0]			R
0x5C	<u>00000000</u>	Operand 7 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA8[7:0]			R
0x5D	<u>00000000</u>	Operand 8 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA9[7:0]			R
0x5E	<u>00000000</u>	Operand 9 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA10[7:0]			R
0x5F	<u>00000000</u>	Operand 10 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA11[7:0]			R
0x60	<u>00000000</u>	Operand 11 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA12[7:0]			R
0x61	<u>00000000</u>	Operand 12 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA13[7:0]			R
0x62	<u>00000000</u>	Operand 13 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_DATA14[7:0]			R
0x63	<u>00000000</u>	Operand 14 of the received frame in receiver frame buffer 1	
CEC_BUF1_RX_FRAME_LENGTH[4:0]			R
0x64	000<u>00000</u>	xxxxx - The total number of bytes (including header byte) that were received into buffer 1	

Reg	Bits	Description	
CEC_BUF2_RX_FRAME_HEADER[7:0]			R
0x65	00000000	Header block of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA0[7:0]			R
0x66	00000000	Opcode block of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA1[7:0]			R
0x67	00000000	Operand 1 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA2[7:0]			R
0x68	00000000	Operand 2 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA3[7:0]			R
0x69	00000000	Operand 3 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA4[7:0]			R
0x6A	00000000	Operand 4 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA5[7:0]			R
0x6B	00000000	Operand 5 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA6[7:0]			R
0x6C	00000000	Operand 6 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA7[7:0]			R
0x6D	00000000	Operand 7 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA8[7:0]			R
0x6E	00000000	Operand 8 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA9[7:0]			R
0x6F	00000000	Operand 9 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA10[7:0]			R
0x70	00000000	Operand 10 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA11[7:0]			R
0x71	00000000	Operand 11 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA12[7:0]			R
0x72	00000000	Operand 12 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA13[7:0]			R
0x73	00000000	Operand 13 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_DATA14[7:0]			R
0x74	00000000	Operand 14 of the received frame in receiver frame buffer 2	
CEC_BUF2_RX_FRAME_LENGTH[4:0]			R
0x75	00000000	xxxxx - The total number of bytes (including header byte) that were received into buffer 2	
CEC_RX_RDY2			R
0x76	0000000	CEC_RX_RDY2 flags that a CEC frame has been received and is waiting to be read in receiver frame buffer 2. This flag must be cleared via CEC_CLR_RX_RDY2 before another message can be received in receiver frame buffer 2. 0 - No CEC frame available in buffer 2 1 - A CEC frame is available in buffer 2	

Reg	Bits	Description	
CEC_RX_RDY1			R
0x76	0000000<u>0</u>	CEC_RX_RDY1 flags that a CEC frame has been received and is waiting to be read in receiver frame buffer 2. This flag must be cleared via CEC_CLR_RX_RDY1 before another message can be received in receiver frame buffer 1. 0 - No CEC frame available in buffer 1 1 - A CEC frame is available in buffer 1	
CEC_RX_RDY0			R
0x76	0000000<u>0</u>	CEC_RX_RDY0 flags that a CEC frame has been received and is waiting to be read in receiver frame buffer 2. This flag must be cleared via CEC_CLR_RX_RDY0 before another message can be received in receiver frame buffer 0. 0 - No CEC frame available in buffer 0 1 - A CEC frame is available in buffer 0	
CEC_USE_ALL_BUFS			R/W
0x77	0000000<u>0</u>	Control to enable supplementary receiver frame buffers. 0 - Use only buffer 0 to store CEC frames 1 - Use all 3 buffers to stores the CEC frames	
CEC_WAKE_OPCODE0[7:0]			R/W
0x78	<u>01101101</u>	CEC_WAKE_OPCODE0 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 01101101 - POWER ON xxxxxxxx - User specified OPCODE to respond to	
CEC_WAKE_OPCODE1[7:0]			R/W
0x79	<u>10001111</u>	CEC_WAKE_OPCODE1 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 10001111 - GIVE POWER STATUS xxxxxxxx - User specified OPCODE to respond to	
CEC_WAKE_OPCODE2[7:0]			R/W
0x7A	<u>10000010</u>	CEC_WAKE_OPCODE2 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 10000010 - ACTIVE SOURCE xxxxxxxx - User specified OPCODE to respond to	
CEC_WAKE_OPCODE3[7:0]			R/W
0x7B	<u>00000100</u>	CEC_WAKE_OPCODE3 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 00000100 - IMAGE VIEW ON xxxxxxxx - User specified OPCODE to respond to	
CEC_WAKE_OPCODE4[7:0]			R/W
0x7C	<u>00001101</u>	CEC_WAKE_OPCODE4 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 00001101 - TEXT VIEW ON xxxxxxxx - User specified OPCODE to respond to	
CEC_WAKE_OPCODE5[7:0]			R/W
0x7D	<u>01110000</u>	CEC_WAKE_OPCODE5 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 01110000 - SYSTEM AUDIO MODE REQUEST xxxxxxxx - User specified OPCODE to respond to	
CEC_WAKE_OPCODE6[7:0]			R/W
0x7E	<u>01000010</u>	CEC_WAKE_OPCODE6 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 01000010 - DECK CONTROL xxxxxxxx - User specified OPCODE to respond to	

Reg	Bits	Description	
CEC_WAKE_OPCODE7[7:0]			R/W
0x7F	01000001	CEC_WAKE_OPCODE7 This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response. 01000001 - PLAY xxxxxxxx - User specified OPCODE to respond to	

2.6 TXA MAIN MAP

Reg	Bits	Description	
SYSTEM_PD			R/W
0x41	01010000	1 to power down the whole chip, except I2C and some interrupts. Default is 1. 0 - Normal Operation 1 - TX Power Down	
CEC_CMD_INTR_MASK[7:0]			R/W
0x92	00000000	[7] = mask for interrupt detecting Wake_Opcode 7 in CEC message [6] = mask for interrupt detecting Wake_Opcode 6 in CEC message [5] = mask for interrupt detecting Wake_Opcode 5 in CEC message [4] = mask for interrupt detecting Wake_Opcode 4 in CEC message [3] = mask for interrupt detecting Wake_Opcode 3 in CEC message [2] = mask for interrupt detecting Wake_Opcode 2 in CEC message [1] = mask for interrupt detecting Wake_Opcode 1 in CEC message [0] = mask for interrupt detecting Wake_Opcode 0 in CEC message	
CEC_CMD_INTR[7:0]			R/W
0x93	00000000	[7] = interrupt detecting Wake_Opcode 7 in CEC message [6] = interrupt detecting Wake_Opcode 6 in CEC message [5] = interrupt detecting Wake_Opcode 5 in CEC message [4] = interrupt detecting Wake_Opcode 4 in CEC message [3] = interrupt detecting Wake_Opcode 3 in CEC message [2] = interrupt detecting Wake_Opcode 2 in CEC message [1] = interrupt detecting Wake_Opcode 1 in CEC message [0] = interrupt detecting Wake_Opcode 0 in CEC message	
HPD_INTR_MASK			R/W
0x94	11000000	Mask for HPD_intr	
MSEN_INTR_MASK			R/W
0x94	11000000	Mask for MSEN_intr	
VS_INTR_MASK			R/W
0x94	11000000	Mask for VS_intr	
EDID_RDY_INTR_MASK			R/W
0x94	11000000	Mask for EDID_rdy_intr	
HDCP_CONTROLLER_STATE_4_INTR_MASK			R/W
0x94	11000000	Mask for Ri_rdy_intr	
RI_RDY_INTR_MASK			R/W
0x94	11000000	Mask for Pj_rdy_intr	
HDCP_ERROR_INTR_MASK			R/W
0x95	00000000	Mask for HDCP_error_intr	
BKSV_FLAG_INTR_MASK			R/W
0x95	00000000	Mask for BKSV_flag	
TX_READY_INTR_MASK			R/W
0x95	00000000	Mask for cec tx_ready_intr	
TX_ARBITRATION_LOST_INTR_MASK			R/W
0x95	00000000	Mask for cec tx_arbitration_lost_intr	
TX_RETRY_TIMEOUT_INTR_MASK			R/W
0x95	00000000	Mask for cec tx_retry_timeout_intr	
RX_READY_INTR_MASK[2:0]			R/W
0x95	00000000	Mask for cec rx_ready_intr[2], cec_rx_ready_intr[1], cec rx_ready_intr[0]	
HPD_ST			R/W
0x96	00000000	intr for hot plug detection 0 - no interrupt detected 1 - interrupt detected	

Reg	Bits	Description	
MSEN_ST			R/W
0x96	0<u>0</u>000000	intr for monitor connection 0 - no interrupt detected 1 - interrupt detected	
VSYNC_ST			R/W
0x96	00<u>0</u>00000	intr for active VS edge 0 - no interrupt detected 1 - interrupt detected	
EDID_RDY_ST			R/W
0x96	00000<u>0</u>00	intr for EDID ready 0 - no interrupt detected 1 - interrupt detected	
HDCP_AUTH_ST			R/W
0x96	000000<u>0</u>0	the 128th Ri is available 0 - no interrupt detected 1 - interrupt detected	
RI_RDY_ST			R/W
0x96	0000000<u>0</u>	16th Ri is available 0 - no interrupt detected 1 - interrupt detected	
HDCP_ERROR_ST			R/W
0x97	<u>0</u>0000000	interrupt bit from HDCP master 0 - no interrupt detected 1 - interrupt detected	
BKSV_FLAG_ST			R/W
0x97	0<u>0</u>000000	1 to instruct the MPU to read the BKSV or the EDOD MEM for revocation list checking. 0 - Default value	
TX_READY_INTR			R/W
0x97	00<u>0</u>00000	Interrupt of tx ready 0 - no interrupt detected 1 - interrupt detected	
TX_ARBITRATION_LOST_INTR			R/W
0x97	000<u>0</u>0000	Interrupt of tx arbitration lost 0 - no interrupt detected 1 - interrupt detected	
TX_RETRY_TIMEOUT_INTR			R/W
0x97	0000<u>0</u>000	Interrupt of retry timeout 0 - no interrupt detected 1 - interrupt detected	
RX_READY_INTR[2:0]			R/W
0x97	00000<u>000</u>	3-bit interrupt bus signifying rx_rdy2, rx_rdy1, rx_rdy0 for the three CEC Frame Buffers respectively. A 1 implies interrupt for a frame received in the corresponding buffer while a 0 implies no frame in the corresponding buffer.	
CEC_PD			R/W
0x98	000<u>0</u>0000	1 to power down CEC logic and reset CEC I2C map. Default is 0. 0 - Disable 1 - Enable	
HIGH_VSYNC[1:0]			R/W
0x9E	<u>00</u>000000	00 and 11 for mormal refresh rate video 01 for 2x and 10 for 4x Default is 00. 00 - "normal" refresh rates 01 - 2x refresh rates 10 - 4x refresh rates 11 - "normal" refresh rates	

Reg	Bits	Description	
HPD_DISABLE[1:0]			R/W
0x9F	00000000	Internal HPD selection logic. 00 - HPD pin and CDC HPD 01 - CDC HPD 10 - HPD pin 11 - Logic 1	
HDCP_START_DELAY[2:0]			R/W
0xAB	00000000	Delay control programmability between HDCP Enable and read BKSV 000 - no delay 001 - 1ms 010 - 2ms 011 - 5ms 100 - 10ms 101 - 20ms 110 - 40ms 111 - 200ms	
RI_FREQ_SEL[1:0]			R/W
0xAC	00000000	Ri check frequency. 00 - 128 frames per check 01 - 64 frames per check 10 - 32 frame per check 11 - 16 frame per check	
RI_DELAY_SEL[2:0]			R/W
0xAC	00000000	Ri ready delay selection. 000 - no delay 001 - delay 8 hsync period 010 - delay 16 hsync period 011 - delay 32 hsync period 100 - delay 64 hsync period 101 - delay 128 hsync period 110 - delay 256 hsync period 111 - delay 512 hsync period	
BCAPS_DELAY[2:0]			R/W
0xAC	00000000	Delay control programmabilitybetween read BKSV and read BCAPS 000 - no delay 001 - 1ms 010 - 2ms 011 - 5ms 100 - 10ms 101 - 20ms 110 - 40ms 111 - 200ms	
AN_DELAY[2:0]			R/W
0xAD	00000000	AN delay selection. 000 - no delay 001 - 1ms 010 - 2ms 011 - 5ms 100 - 10ms 101 - 20ms 110 - 40ms 111 - 200ms	

Reg	Bits	Description	
AKSV_DELAY[2:0]			R/W
0xAD	00000000	Delay control programmability between write AN to sink and write AKSV to sink. 000 - no delay 001 - 1ms 010 - 2ms 011 - 5ms 100 - 10ms 101 - 20ms 110 - 40ms 111 - 200ms	
SKIP_RI_128			R/W
0xAE	00000000	This can only be used when Ri checking frequency is higher than 128 frames per Ri check. 0 - Do not skip 128th frame Ri checking 1 - Skip 128th frame Ri checking	
HDCP_1P1_DIS			R/W
0xAE	00000000	Remain in HDCP 1.0, even if the RX side supports HDCP 1.1. 0 - enabled 1 - disabled	
R0_WAIT_TIME[1:0]			R/W
0xAE	00000000	HDCP Ro' Read Delay 00 - 100ms 01 - 110ms 10 - 150ms 11 - 200ms	
HDCP_REPEATER_TIMEOUT[1:0]			R/W
0xAE	00000000	HDMI Tx Repeater Ready Bit Watchdog Timer 00 - 5s 01 - 6.5s 10 - 8s 11 - 10s	
HDCP_DESIRED			R/W
0xAF	00010100	1 means the input A/V content should be encrypted. 0 - A/V content not encrypted 1 - A/V content encrypted	
FRAME_ENC			R/W
0xAF	00010100	1 means the current frame should be encrypted 0 - current frame is not encrypted 1 - current frame is encrypted	
TX_HDMI_MODE			R/W
0xAF	00010100	0 to use on chip decision (get into HDMI mode by audio detection) 0 - automatic mode 1 - DVI/HDMI set by bit 1	
EXT_HDMI_MODE			R/W
0xAF	00010100	0 means DVI 1 means HDMI 0 - DVI 1 - HDMI	
ENC_ON			R
0xB8	00000000	1 means the A/V content is being encrypted at present. 0 - not encrypted 1 - encrypted	
KEYS_READ_ERROR			R
0xB8	00000000	1 means HDCP key reading error. 0 - Read HDCP keys correctly 1 - Encountered errors when reading the HDCP keys	

Reg	Bits	Description	
BCAPS[7:0]			R
0xBE	00000000	HDCP related register '[7] Reserved, [6] Repeater, [5] BKSV FIFO ready, [4] Fast DDC Bus, [3:2] Reserved, [1] HDMI 1.1, [0] Fast Re-Authentication	
BKSV0[7:0]			R
0xBF	00000000	Bksv read from Rx by the HDCP controller 0 - Default value	
BKSV1[7:0]			R
0xC0	00000000	Bksv read from Rx by the HDCP controller 0 - Default value	
BKSV2[7:0]			R
0xC1	00000000	Bksv read from Rx by the HDCP controller 0 - Default value	
BKSV3[7:0]			R
0xC2	00000000	Bksv read from Rx by the HDCP controller 0 - Default value	
BKSV4[7:0]			R
0xC3	00000000	Bksv read from Rx by the HDCP controller 0 - Default value	
EDID_SEGMENT[7:0]			R/W
0xC4	00000000	Sets the E-DDC segment used by the EDID Fetch routine. 0 - Default value	
ERROR_FLAG			R/W
0xC5	0	Set high by firmware on any error. 0 - no error 1 - error	
AN_STOP			R
0xC5	0	Set high by firmware to get An. Set low again if authentication is restarted.	
HDCP_ENABLED			R
0xC5	0	Set high by firmware after successful HDCP authentication.	
EDID_READY_FLAG			R
0xC5	0	Set high by firmware once EDID has been read. Goes low again if firmware uses data memory for HDCP repeater authentication.	
I2C_INTERRUPT			R
0xC5	0	Set high when an access to EDID i2c interface is detected. Cleared by firmware.	
RI_FLAG			R
0xC5	0	Goes high on positive edge of ri_update from HDCP engine. Reset by the firmware.	
BKSV_UPDATE_FLAG			R
0xC5	0	Sent to HDCP engine to signal new Bksv.	
PJ_FLAG			R
0xC5	0	Goes high on positive edge of pj_update from HDCP engine. Reset by the firmware. 0 - no Flag 1 - Flag	
HDMI_MODE			R
0xC6	0	HDMI mode selection. 0 - DVI 1 - HDMI	

Reg	Bits	Description	
HDCP_REQUESTED			R
0xC6	0000**0**000	HDCP enable/disable 0 - No HDCP request 1 - HDCP requested	
RX_SENSE			R
0xC6	00000**0**00	Receiver TMDS pull-ups detected.	
EEPROM_READ_OK			R
0xC6	000000**0**0	HDCP Engine read the eeprom/OTP OK.	
TMDSOUTPUTPWRDN			R
0xC6	0000000**0**	Set by the firmware to power off TMDS output drivers for 100ms in order to reset the receiver. X - Readback value	
BKSV_FLAG			R/W
0xC7	**0**0000000	Work with BKSV_Count. 0 - no detected 1 - detected	
BKSV_COUNT[6:0]			R
0xC7	**0000000**0	BKSVs Available in Sink's BKSV FIFO 0 - Default value	
HDCP_CONTROLLER_ERROR[3:0]			R
0xC8	**0000**0000	HDCP error information. 0000 - No Error 0001 - Bad Receiver BKSV 0010 - Ri Mismatch 0011 - Pj Mismatch 0100 - I2C Error (usually a no-ack) 0101 - Time Out Waiting for Downstream Repeater DONE 0110 - Max Cascade of Repeaters Exceeded 0111 - SHA-1 Hash Check of KSV List Failed 1000 - Too Many Devices Connected to Repeater Tree	
HDCP_CONTROLLER_STATE[3:0]			R
0xC8	0000**0000**	HDCP Controler status. 0000 - In Reset (No Hot Plug Detected) 0001 - Reading EDID 0010 - IDLE (Waiting for HDCP Requested) 0011 - Initializing HDCP 0100 - HDCP Enable 0101 - Initializing HDCP Repeater	
EDID_READ_EN			R/W
0xC9	000**0**0011	Manually Read the EDID if toggled from 0 to 1. This bit is edge sensitive, and is self-clearing. It should also be noted that it not possible to use this bit when the BKSV interrupt is active. 0 - disable 1 - enable	
EDID_TRIES[3:0]			R/W
0xC9	0000**0011**	Maximum number of times that the EDID read will be attempted if unsuccessful. EDID reading will begin upon setting of this register and on powerup. 3 - Default value	
PLL_LOCK_STATUS			R
0xE4	**0**0000000	PLL Lock Status 0 - PLL Not Locked 1 - PLL Locked	
TMDS_CLK_INV_I2C			R/W
0xEA	100001**0**0	TMDS Clock Inversion 0 - Normal TMDS Clock 1 - Inverted TMDS Clock	

Reg	Bits	Description	
ENABLE_XXI_CLK_I2C			R/W
0xEA	1000010<u>0</u>	control the cross-coupled inverters used to correct for duty cycle distortion 0 - disable cross_coupled inverters 1 - enable cross-coupled inverters for duty cycle	
TRANSDRVENABLE_I2C[2:0]			R/W
0xEB	<u>111</u>11100	111 to enable all 3 TMDS data output currents 0 - disable driver 1 - enable driver	
CHANNEL_SWAP			R/W
0xFE	0000000<u>0</u>	Swaps TX TMDS pins 1 - enable 0 - disable	

2.7 TXA EDID MAP

Reg	Bits	Description	
EDID_0[7:0]			R
0x00	00000000		
EDID_1[7:0]			R
0x01	00000000		
EDID_2[7:0]			R
0x02	00000000		
EDID_3[7:0]			R
0x03	00000000		
EDID_4[7:0]			R
0x04	00000000		
EDID_5[7:0]			R
0x05	00000000		
EDID_6[7:0]			R
0x06	00000000		
EDID_7[7:0]			R
0x07	00000000		
EDID_8[7:0]			R
0x08	00000000		
EDID_9[7:0]			R
0x09	00000000		
EDID_10[7:0]			R
0x0A	00000000		
EDID_11[7:0]			R
0x0B	00000000		
EDID_12[7:0]			R
0x0C	00000000		
EDID_13[7:0]			R
0x0D	00000000		
EDID_14[7:0]			R
0x0E	00000000		
EDID_15[7:0]			R
0x0F	00000000		
EDID_16[7:0]			R
0x10	00000000		
EDID_17[7:0]			R
0x11	00000000		

Reg	Bits	Description	
EDID_18[7:0]			R
0x12	00000000		
EDID_19[7:0]			R
0x13	00000000		
EDID_20[7:0]			R
0x14	00000000		
EDID_21[7:0]			R
0x15	00000000		
EDID_22[7:0]			R
0x16	00000000		
EDID_23[7:0]			R
0x17	00000000		
EDID_24[7:0]			R
0x18	00000000		
EDID_25[7:0]			R
0x19	00000000		
EDID_26[7:0]			R
0x1A	00000000		
EDID_27[7:0]			R
0x1B	00000000		
EDID_28[7:0]			R
0x1C	00000000		
EDID_29[7:0]			R
0x1D	00000000		
EDID_30[7:0]			R
0x1E	00000000		
EDID_31[7:0]			R
0x1F	00000000		
EDID_32[7:0]			R
0x20	00000000		
EDID_33[7:0]			R
0x21	00000000		
EDID_34[7:0]			R
0x22	00000000		
EDID_35[7:0]			R
0x23	00000000		
EDID_36[7:0]			R
0x24	00000000		

Reg	Bits	Description	
EDID_37[7:0]			R
0x25	00000000		
EDID_38[7:0]			R
0x26	00000000		
EDID_39[7:0]			R
0x27	00000000		
EDID_40[7:0]			R
0x28	00000000		
EDID_41[7:0]			R
0x29	00000000		
EDID_42[7:0]			R
0x2A	00000000		
EDID_43[7:0]			R
0x2B	00000000		
EDID_44[7:0]			R
0x2C	00000000		
EDID_45[7:0]			R
0x2D	00000000		
EDID_46[7:0]			R
0x2E	00000000		
EDID_47[7:0]			R
0x2F	00000000		
EDID_48[7:0]			R
0x30	00000000		
EDID_49[7:0]			R
0x31	00000000		
EDID_50[7:0]			R
0x32	00000000		
EDID_51[7:0]			R
0x33	00000000		
EDID_52[7:0]			R
0x34	00000000		
EDID_53[7:0]			R
0x35	00000000		
EDID_54[7:0]			R
0x36	00000000		
EDID_55[7:0]			R
0x37	00000000		

Reg	Bits	Description	
EDID_56[7:0]			R
0x38	00000000		
EDID_57[7:0]			R
0x39	00000000		
EDID_58[7:0]			R
0x3A	00000000		
EDID_59[7:0]			R
0x3B	00000000		
EDID_60[7:0]			R
0x3C	00000000		
EDID_61[7:0]			R
0x3D	00000000		
EDID_62[7:0]			R
0x3E	00000000		
EDID_63[7:0]			R
0x3F	00000000		
EDID_64[7:0]			R
0x40	00000000		
EDID_65[7:0]			R
0x41	00000000		
EDID_66[7:0]			R
0x42	00000000		
EDID_67[7:0]			R
0x43	00000000		
EDID_68[7:0]			R
0x44	00000000		
EDID_69[7:0]			R
0x45	00000000		
EDID_70[7:0]			R
0x46	00000000		
EDID_71[7:0]			R
0x47	00000000		
EDID_72[7:0]			R
0x48	00000000		
EDID_73[7:0]			R
0x49	00000000		
EDID_74[7:0]			R
0x4A	00000000		

Reg	Bits	Description	
EDID_75[7:0]			R
0x4B	00000000		
EDID_76[7:0]			R
0x4C	00000000		
EDID_77[7:0]			R
0x4D	00000000		
EDID_78[7:0]			R
0x4E	00000000		
EDID_79[7:0]			R
0x4F	00000000		
EDID_80[7:0]			R
0x50	00000000		
EDID_81[7:0]			R
0x51	00000000		
EDID_82[7:0]			R
0x52	00000000		
EDID_83[7:0]			R
0x53	00000000		
EDID_84[7:0]			R
0x54	00000000		
EDID_85[7:0]			R
0x55	00000000		
EDID_86[7:0]			R
0x56	00000000		
EDID_87[7:0]			R
0x57	00000000		
EDID_88[7:0]			R
0x58	00000000		
EDID_89[7:0]			R
0x59	00000000		
EDID_90[7:0]			R
0x5A	00000000		
EDID_91[7:0]			R
0x5B	00000000		
EDID_92[7:0]			R
0x5C	00000000		
EDID_93[7:0]			R
0x5D	00000000		

Reg	Bits	Description	
EDID_94[7:0]			R
0x5E	00000000		
EDID_95[7:0]			R
0x5F	00000000		
EDID_96[7:0]			R
0x60	00000000		
EDID_97[7:0]			R
0x61	00000000		
EDID_98[7:0]			R
0x62	00000000		
EDID_99[7:0]			R
0x63	00000000		
EDID_100[7:0]			R
0x64	00000000		
EDID_101[7:0]			R
0x65	00000000		
EDID_102[7:0]			R
0x66	00000000		
EDID_103[7:0]			R
0x67	00000000		
EDID_104[7:0]			R
0x68	00000000		
EDID_105[7:0]			R
0x69	00000000		
EDID_106[7:0]			R
0x6A	00000000		
EDID_107[7:0]			R
0x6B	00000000		
EDID_108[7:0]			R
0x6C	00000000		
EDID_109[7:0]			R
0x6D	00000000		
EDID_110[7:0]			R
0x6E	00000000		
EDID_111[7:0]			R
0x6F	00000000		
EDID_112[7:0]			R
0x70	00000000		

Reg	Bits	Description	
EDID_113[7:0]			R
0x71	00000000		
EDID_114[7:0]			R
0x72	00000000		
EDID_115[7:0]			R
0x73	00000000		
EDID_116[7:0]			R
0x74	00000000		
EDID_117[7:0]			R
0x75	00000000		
EDID_118[7:0]			R
0x76	00000000		
EDID_119[7:0]			R
0x77	00000000		
EDID_120[7:0]			R
0x78	00000000		
EDID_121[7:0]			R
0x79	00000000		
EDID_122[7:0]			R
0x7A	00000000		
EDID_123[7:0]			R
0x7B	00000000		
EDID_124[7:0]			R
0x7C	00000000		
EDID_125[7:0]			R
0x7D	00000000		
EDID_126[7:0]			R
0x7E	00000000		
EDID_127[7:0]			R
0x7F	00000000		
EDID_128[7:0]			R
0x80	00000000		
EDID_129[7:0]			R
0x81	00000000		
EDID_130[7:0]			R
0x82	00000000		
EDID_131[7:0]			R
0x83	00000000		

Reg	Bits	Description	
EDID_132[7:0]			R
0x84	00000000		
EDID_133[7:0]			R
0x85	00000000		
EDID_134[7:0]			R
0x86	00000000		
EDID_135[7:0]			R
0x87	00000000		
EDID_136[7:0]			R
0x88	00000000		
EDID_137[7:0]			R
0x89	00000000		
EDID_138[7:0]			R
0x8A	00000000		
EDID_139[7:0]			R
0x8B	00000000		
EDID_140[7:0]			R
0x8C	00000000		
EDID_141[7:0]			R
0x8D	00000000		
EDID_142[7:0]			R
0x8E	00000000		
EDID_143[7:0]			R
0x8F	00000000		
EDID_144[7:0]			R
0x90	00000000		
EDID_145[7:0]			R
0x91	00000000		
EDID_146[7:0]			R
0x92	00000000		
EDID_147[7:0]			R
0x93	00000000		
EDID_148[7:0]			R
0x94	00000000		
EDID_149[7:0]			R
0x95	00000000		
EDID_150[7:0]			R
0x96	00000000		

Reg	Bits	Description	
EDID_151[7:0]			R
0x97	00000000		
EDID_152[7:0]			R
0x98	00000000		
EDID_153[7:0]			R
0x99	00000000		
EDID_154[7:0]			R
0x9A	00000000		
EDID_155[7:0]			R
0x9B	00000000		
EDID_156[7:0]			R
0x9C	00000000		
EDID_157[7:0]			R
0x9D	00000000		
EDID_158[7:0]			R
0x9E	00000000		
EDID_159[7:0]			R
0x9F	00000000		
EDID_160[7:0]			R
0xA0	00000000		
EDID_161[7:0]			R
0xA1	00000000		
EDID_162[7:0]			R
0xA2	00000000		
EDID_163[7:0]			R
0xA3	00000000		
EDID_164[7:0]			R
0xA4	00000000		
EDID_165[7:0]			R
0xA5	00000000		
EDID_166[7:0]			R
0xA6	00000000		
EDID_167[7:0]			R
0xA7	00000000		
EDID_168[7:0]			R
0xA8	00000000		
EDID_169[7:0]			R
0xA9	00000000		

Reg	Bits	Description	
EDID_170[7:0]			R
0xAA	00000000		
EDID_171[7:0]			R
0xAB	00000000		
EDID_172[7:0]			R
0xAC	00000000		
EDID_173[7:0]			R
0xAD	00000000		
EDID_174[7:0]			R
0xAE	00000000		
EDID_175[7:0]			R
0xAF	00000000		
EDID_176[7:0]			R
0xB0	00000000		
EDID_177[7:0]			R
0xB1	00000000		
EDID_178[7:0]			R
0xB2	00000000		
EDID_179[7:0]			R
0xB3	00000000		
EDID_180[7:0]			R
0xB4	00000000		
EDID_181[7:0]			R
0xB5	00000000		
EDID_182[7:0]			R
0xB6	00000000		
EDID_183[7:0]			R
0xB7	00000000		
EDID_184[7:0]			R
0xB8	00000000		
EDID_185[7:0]			R
0xB9	00000000		
EDID_186[7:0]			R
0xBA	00000000		
EDID_187[7:0]			R
0xBB	00000000		
EDID_188[7:0]			R
0xBC	00000000		

Reg	Bits	Description	
EDID_189[7:0]			R
0xBD	00000000		
EDID_190[7:0]			R
0xBE	00000000		
EDID_191[7:0]			R
0xBF	00000000		
EDID_192[7:0]			R
0xC0	00000000		
EDID_193[7:0]			R
0xC1	00000000		
EDID_194[7:0]			R
0xC2	00000000		
EDID_195[7:0]			R
0xC3	00000000		
EDID_196[7:0]			R
0xC4	00000000		
EDID_197[7:0]			R
0xC5	00000000		
EDID_198[7:0]			R
0xC6	00000000		
EDID_199[7:0]			R
0xC7	00000000		
EDID_200[7:0]			R
0xC8	00000000		
EDID_201[7:0]			R
0xC9	00000000		
EDID_202[7:0]			R
0xCA	00000000		
EDID_203[7:0]			R
0xCB	00000000		
EDID_204[7:0]			R
0xCC	00000000		
EDID_205[7:0]			R
0xCD	00000000		
EDID_206[7:0]			R
0xCE	00000000		
EDID_207[7:0]			R
0xCF	00000000		

Reg	Bits	Description	
EDID_208[7:0]			R
0xD0	00000000		
EDID_209[7:0]			R
0xD1	00000000		
EDID_210[7:0]			R
0xD2	00000000		
EDID_211[7:0]			R
0xD3	00000000		
EDID_212[7:0]			R
0xD4	00000000		
EDID_213[7:0]			R
0xD5	00000000		
EDID_214[7:0]			R
0xD6	00000000		
EDID_215[7:0]			R
0xD7	00000000		
EDID_216[7:0]			R
0xD8	00000000		
EDID_217[7:0]			R
0xD9	00000000		
EDID_218[7:0]			R
0xDA	00000000		
EDID_219[7:0]			R
0xDB	00000000		
EDID_220[7:0]			R
0xDC	00000000		
EDID_221[7:0]			R
0xDD	00000000		
EDID_222[7:0]			R
0xDE	00000000		
EDID_223[7:0]			R
0xDF	00000000		
EDID_224[7:0]			R
0xE0	00000000		
EDID_225[7:0]			R
0xE1	00000000		
EDID_226[7:0]			R
0xE2	00000000		

Reg	Bits	Description	
EDID_227[7:0]			R
0xE3	00000000		
EDID_228[7:0]			R
0xE4	00000000		
EDID_229[7:0]			R
0xE5	00000000		
EDID_230[7:0]			R
0xE6	00000000		
EDID_231[7:0]			R
0xE7	00000000		
EDID_232[7:0]			R
0xE8	00000000		
EDID_233[7:0]			R
0xE9	00000000		
EDID_234[7:0]			R
0xEA	00000000		
EDID_235[7:0]			R
0xEB	00000000		
EDID_236[7:0]			R
0xEC	00000000		
EDID_237[7:0]			R
0xED	00000000		
EDID_238[7:0]			R
0xEE	00000000		
EDID_239[7:0]			R
0xEF	00000000		
EDID_240[7:0]			R
0xF0	00000000		
EDID_241[7:0]			R
0xF1	00000000		
EDID_242[7:0]			R
0xF2	00000000		
EDID_243[7:0]			R
0xF3	00000000		
EDID_244[7:0]			R
0xF4	00000000		
EDID_245[7:0]			R
0xF5	00000000		

Reg	Bits	Description	
EDID_246[7:0]			R
0xF6	00000000		
EDID_247[7:0]			R
0xF7	00000000		
EDID_248[7:0]			R
0xF8	00000000		
EDID_249[7:0]			R
0xF9	00000000		
EDID_250[7:0]			R
0xFA	00000000		
EDID_251[7:0]			R
0xFB	00000000		
EDID_252[7:0]			R
0xFC	00000000		
EDID_253[7:0]			R
0xFD	00000000		
EDID_254[7:0]			R
0xFE	00000000		
EDID_255[7:0]			R
0xFF	00000000		

2.8 TXB MAIN MAP

Reg	Bits	Description	
SYSTEM_PD			R/W
0x41	01010000	1 to power down the whole chip, except I2C and some interrupts. Default is 1. 0 - Normal Operation 1 - TX Power Down	
CEC_CMD_INTR_MASK[7:0]			R/W
0x92	00000000	[7] = mask for interrupt detecting Wake_Opcode 7 in CEC message [6] = mask for interrupt detecting Wake_Opcode 6 in CEC message [5] = mask for interrupt detecting Wake_Opcode 5 in CEC message [4] = mask for interrupt detecting Wake_Opcode 4 in CEC message [3] = mask for interrupt detecting Wake_Opcode 3 in CEC message [2] = mask for interrupt detecting Wake_Opcode 2 in CEC message [1] = mask for interrupt detecting Wake_Opcode 1 in CEC message [0] = mask for interrupt detecting Wake_Opcode 0 in CEC message	
CEC_CMD_INTR[7:0]			R/W
0x93	00000000	[7] = interrupt detecting Wake_Opcode 7 in CEC message [6] = interrupt detecting Wake_Opcode 6 in CEC message [5] = interrupt detecting Wake_Opcode 5 in CEC message [4] = interrupt detecting Wake_Opcode 4 in CEC message [3] = interrupt detecting Wake_Opcode 3 in CEC message [2] = interrupt detecting Wake_Opcode 2 in CEC message [1] = interrupt detecting Wake_Opcode 1 in CEC message [0] = interrupt detecting Wake_Opcode 0 in CEC message	
HPD_INTR_MASK			R/W
0x94	11000000	Mask for HPD_intr	
MSEN_INTR_MASK			R/W
0x94	11000000	Mask for MSEN_intr	
VS_INTR_MASK			R/W
0x94	11000000	Mask for VS_intr	
EDID_RDY_INTR_MASK			R/W
0x94	11000000	Mask for EDID_rdy_intr	
HDCP_CONTROLLER_STATE_4_INTR_MASK			R/W
0x94	11000000	Mask for Ri_rdy_intr	
RI_RDY_INTR_MASK			R/W
0x94	11000000	Mask for Pj_rdy_intr	
HDCP_ERROR_INTR_MASK			R/W
0x95	00000000	Mask for HDCP_error_intr	
BKSV_FLAG_INTR_MASK			R/W
0x95	00000000	Mask for BKSV_flag	
TX_READY_INTR_MASK			R/W
0x95	00000000	Mask for cec tx_ready_intr	
TX_ARBITRATION_LOST_INTR_MASK			R/W
0x95	00000000	Mask for cec tx_arbitration_lost_intr	
TX_RETRY_TIMEOUT_INTR_MASK			R/W
0x95	00000000	Mask for cec tx_retry_timeout_intr	
RX_READY_INTR_MASK[2:0]			R/W
0x95	00000000	Mask for cec rx_ready_intr[2], cec_rx_ready_intr[1], cec rx_ready_intr[0]	
HPD_ST			R/W
0x96	00000000	intr for hot plug detection 0 - no interrupt detected 1 - interrupt detected	

Reg	Bits	Description	
MSEN_ST			R/W
0x96	0<u>0</u>000000	intr for monitor connection 0 - no interrupt detected 1 - interrupt detected	
VSYNC_ST			R/W
0x96	00<u>0</u>00000	intr for active VS edge 0 - no interrupt detected 1 - interrupt detected	
EDID_RDY_ST			R/W
0x96	00000<u>0</u>00	intr for EDID ready 0 - no interrupt detected 1 - interrupt detected	
HDCP_AUTH_ST			R/W
0x96	000000<u>0</u>0	the 128th Ri is available 0 - no interrupt detected 1 - interrupt detected	
RI_RDY_ST			R/W
0x96	0000000<u>0</u>	16th Ri is available 0 - no interrupt detected 1 - interrupt detected	
HDCP_ERROR_ST			R/W
0x97	<u>0</u>0000000	interrupt bit from HDCP master 0 - no interrupt detected 1 - interrupt detected	
BKSV_FLAG_ST			R/W
0x97	0<u>0</u>000000	1 to instruct the MPU to read the BKSV or the EDOD MEM for revocation list checking. 0 - Default value	
TX_READY_INTR			R/W
0x97	00<u>0</u>00000	Interrupt of tx ready 0 - no interrupt detected 1 - interrupt detected	
TX_ARBITRATION_LOST_INTR			R/W
0x97	000<u>0</u>0000	Interrupt of tx arbitration lost 0 - no interrupt detected 1 - interrupt detected	
TX_RETRY_TIMEOUT_INTR			R/W
0x97	0000<u>0</u>000	Interrupt of retry timeout 0 - no interrupt detected 1 - interrupt detected	
RX_READY_INTR[2:0]			R/W
0x97	00000<u>000</u>	3-bit interrupt bus signifying rx_rdy2, rx_rdy1, rx_rdy0 for the three CEC Frame Buffers respectively. A 1 implies interrupt for a frame received in the corresponding buffer while a 0 implies no frame in the corresponding buffer.	
CEC_PD			R/W
0x98	000<u>0</u>0000	1 to power down CEC logic and reset CEC I2C map. Default is 0. 0 - Disable 1 - Enable	
HIGH_VSYNC[1:0]			R/W
0x9E	<u>00</u>000000	00 and 11 for mormal refresh rate video 01 for 2x and 10 for 4x Default is 00. 00 - "normal" refresh rates 01 - 2x refresh rates 10 - 4x refresh rates 11 - "normal" refresh rates	

Reg	Bits	Description	
HPD_DISABLE[1:0]			R/W
0x9F	00000000	Internal HPD selection logic. 00 - HPD pin and CDC HPD 01 - CDC HPD 10 - HPD pin 11 - Logic 1	
HDCP_START_DELAY[2:0]			R/W
0xAB	00000000	Delay control programmability between HDCP Enable and read BKSV 000 - no delay 001 - 1ms 010 - 2ms 011 - 5ms 100 - 10ms 101 - 20ms 110 - 40ms 111 - 200ms	
RI_FREQ_SEL[1:0]			R/W
0xAC	00000000	Ri check frequency. 00 - 128 frames per check 01 - 64 frames per check 10 - 32 frame per check 11 - 16 frame per check	
RI_DELAY_SEL[2:0]			R/W
0xAC	00000000	Ri ready delay selection. 000 - no delay 001 - delay 8 hsync period 010 - delay 16 hsync period 011 - delay 32 hsync period 100 - delay 64 hsync period 101 - delay 128 hsync period 110 - delay 256 hsync period 111 - delay 512 hsync period	
BCAPS_DELAY[2:0]			R/W
0xAC	00000000	Delay control programmabilitybetween read BKSV and read BCAPS 000 - no delay 001 - 1ms 010 - 2ms 011 - 5ms 100 - 10ms 101 - 20ms 110 - 40ms 111 - 200ms	
AN_DELAY[2:0]			R/W
0xAD	00000000	AN delay selection. 000 - no delay 001 - 1ms 010 - 2ms 011 - 5ms 100 - 10ms 101 - 20ms 110 - 40ms 111 - 200ms	

Reg	Bits	Description	
AKSV_DELAY[2:0]			R/W
0xAD	00000000	Delay control programmability between write AN to sink and write AKSV to sink. 000 - no delay 001 - 1ms 010 - 2ms 011 - 5ms 100 - 10ms 101 - 20ms 110 - 40ms 111 - 200ms	
SKIP_RI_128			R/W
0xAE	00000000	This can only be used when Ri checking frequency is higher than 128 frames per Ri check. 0 - Do not skip 128th frame Ri checking 1 - Skip 128th frame Ri checking	
HDCP_1P1_DIS			R/W
0xAE	00000000	Remain in HDCP 1.0, even if the RX side supports HDCP 1.1. 0 - enabled 1 - disabled	
R0_WAIT_TIME[1:0]			R/W
0xAE	00000000	HDCP Ro' Read Delay 00 - 100ms 01 - 110ms 10 - 150ms 11 - 200ms	
HDCP_REPEATER_TIMEOUT[1:0]			R/W
0xAE	00000000	HDMI Tx Repeater Ready Bit Watchdog Timer 00 - 5s 01 - 6.5s 10 - 8s 11 - 10s	
HDCP_DESIRED			R/W
0xAF	00010100	1 means the input A/V content should be encrypted. 0 - A/V content not encrypted 1 - A/V content encrypted	
FRAME_ENC			R/W
0xAF	00010100	1 means the current frame should be encrypted 0 - current frame is not encrypted 1 - current frame is encrypted	
TX_HDMI_MODE			R/W
0xAF	00010100	0 to use on chip decision (get into HDMI mode by audio detection) 0 - automatic mode 1 - DVI/HDMI set by bit 1	
EXT_HDMI_MODE			R/W
0xAF	00010100	0 means DVI 1 means HDMI 0 - DVI 1 - HDMI	
ENC_ON			R
0xB8	00000000	1 means the A/V content is being encrypted at present. 0 - not encrypted 1 - encrypted	
KEYS_READ_ERROR			R
0xB8	00000000	1 means HDCP key reading error. 0 - Read HDCP keys correctly 1 - Encountered errors when reading the HDCP keys	

Reg	Bits	Description	
BCAPS[7:0]			R
0xBE	00000000	HDCP related register '[7] Reserved, [6] Repeater, [5] BKSV FIFO ready, [4] Fast DDC Bus, [3:2] Reserved, [1] HDMI 1.1, [0] Fast Re-Authentication	
BKSV0[7:0]			R
0xBF	00000000	Bksv read from Rx by the HDCP controller 0 - Default value	
BKSV1[7:0]			R
0xC0	00000000	Bksv read from Rx by the HDCP controller 0 - Default value	
BKSV2[7:0]			R
0xC1	00000000	Bksv read from Rx by the HDCP controller 0 - Default value	
BKSV3[7:0]			R
0xC2	00000000	Bksv read from Rx by the HDCP controller 0 - Default value	
BKSV4[7:0]			R
0xC3	00000000	Bksv read from Rx by the HDCP controller 0 - Default value	
EDID_SEGMENT[7:0]			R/W
0xC4	00000000	Sets the E-DDC segment used by the EDID Fetch routine. 0 - Default value	
ERROR_FLAG			R/W
0xC5	0	Set high by firmware on any error. 0 - no error 1 - error	
AN_STOP			R
0xC5	0	Set high by firmware to get An. Set low again if authentication is restarted.	
HDCP_ENABLED			R
0xC5	0	Set high by firmware after successful HDCP authentication.	
EDID_READY_FLAG			R
0xC5	0	Set high by firmware once EDID has been read. Goes low again if firmware uses data memory for HDCP repeater authentication.	
I2C_INTERRUPT			R
0xC5	0	Set high when an access to EDID i2c interface is detected. Cleared by firmware.	
RI_FLAG			R
0xC5	0	Goes high on positive edge of ri_update from HDCP engine. Reset by the firmware.	
BKSV_UPDATE_FLAG			R
0xC5	0	Sent to HDCP engine to signal new Bksv.	
PJ_FLAG			R
0xC5	0	Goes high on positive edge of pj_update from HDCP engine. Reset by the firmware. 0 - no Flag 1 - Flag	
HDMI_MODE			R
0xC6	0	HDMI mode selection. 0 - DVI 1 - HDMI	

Reg	Bits	Description	
HDCP_REQUESTED			R
0xC6	0000**0**000	HDCP enable/disable 0 - No HDCP request 1 - HDCP requested	
RX_SENSE			R
0xC6	00000**0**00	Receiver TMDS pull-ups detected.	
EEPROM_READ_OK			R
0xC6	000000**0**0	HDCP Engine read the eeprom/OTP OK.	
TMDSOUTPUTPWRDN			R
0xC6	0000000**0**	Set by the firmware to power off TMDS output drivers for 100ms in order to reset the receiver. X - Readback value	
BKSV_FLAG			R/W
0xC7	**0**0000000	Work with BKSV_Count. 0 - no detected 1 - detected	
BKSV_COUNT[6:0]			R
0xC7	**0000000**0	BKSVs Available in Sink's BKSV FIFO 0 - Default value	
HDCP_CONTROLLER_ERROR[3:0]			R
0xC8	**0000**0000	HDCP error information. 0000 - No Error 0001 - Bad Receiver BKSV 0010 - Ri Mismatch 0011 - Pj Mismatch 0100 - I2C Error (usually a no-ack) 0101 - Time Out Waiting for Downstream Repeater DONE 0110 - Max Cascade of Repeaters Exceeded 0111 - SHA-1 Hash Check of KSV List Failed 1000 - Too Many Devices Connected to Repeater Tree	
HDCP_CONTROLLER_STATE[3:0]			R
0xC8	0000**0000**	HDCP Controler status. 0000 - In Reset (No Hot Plug Detected) 0001 - Reading EDID 0010 - IDLE (Waiting for HDCP Requested) 0011 - Initializing HDCP 0100 - HDCP Enable 0101 - Initializing HDCP Repeater	
EDID_READ_EN			R/W
0xC9	000**0**0011	Manually Read the EDID if toggled from 0 to 1. This bit is edge sensitive, and is self-clearing. It should also be noted that it not possible to use this bit when the BKSV interrupt is active. 0 - disable 1 - enable	
EDID_TRIES[3:0]			R/W
0xC9	0000**0011**	Maximum number of times that the EDID read will be attempted if unsuccessful. EDID reading will begin upon setting of this register and on powerup. 3 - Default value	
PLL_LOCK_STATUS			R
0xE4	**0**0000000	PLL Lock Status 0 - PLL Not Locked 1 - PLL Locked	
TMDS_CLK_INV_I2C			R/W
0xEA	100001**0**0	TMDS Clock Inversion 0 - Normal TMDS Clock 1 - Inverted TMDS Clock	

Reg	Bits	Description	
ENABLE_XXI_CLK_I2C			R/W
0xEA	1000010<u>0</u>	control the cross-coupled inverters used to correct for duty cycle distortion 0 - disable cross_coupled inverters 1 - enable cross-coupled inverters for duty cycle	
TRANSDRVENABLE_I2C[2:0]			R/W
0xEB	<u>111</u>11100	111 to enable all 3 TMDS data output currents 0 - disable driver 1 - enable driver	
CHANNEL_SWAP			R/W
0xFE	0000000<u>0</u>	Swaps TX TMDS pins 1 - enable 0 - disable	

2.9 TXB EDID MAP

Reg	Bits	Description	
EDID_0[7:0]			R
0x00	00000000		
EDID_1[7:0]			R
0x01	00000000		
EDID_2[7:0]			R
0x02	00000000		
EDID_3[7:0]			R
0x03	00000000		
EDID_4[7:0]			R
0x04	00000000		
EDID_5[7:0]			R
0x05	00000000		
EDID_6[7:0]			R
0x06	00000000		
EDID_7[7:0]			R
0x07	00000000		
EDID_8[7:0]			R
0x08	00000000		
EDID_9[7:0]			R
0x09	00000000		
EDID_10[7:0]			R
0x0A	00000000		
EDID_11[7:0]			R
0x0B	00000000		
EDID_12[7:0]			R
0x0C	00000000		
EDID_13[7:0]			R
0x0D	00000000		
EDID_14[7:0]			R
0x0E	00000000		
EDID_15[7:0]			R
0x0F	00000000		
EDID_16[7:0]			R
0x10	00000000		
EDID_17[7:0]			R
0x11	00000000		

Reg	Bits	Description	
EDID_18[7:0]			R
0x12	00000000		
EDID_19[7:0]			R
0x13	00000000		
EDID_20[7:0]			R
0x14	00000000		
EDID_21[7:0]			R
0x15	00000000		
EDID_22[7:0]			R
0x16	00000000		
EDID_23[7:0]			R
0x17	00000000		
EDID_24[7:0]			R
0x18	00000000		
EDID_25[7:0]			R
0x19	00000000		
EDID_26[7:0]			R
0x1A	00000000		
EDID_27[7:0]			R
0x1B	00000000		
EDID_28[7:0]			R
0x1C	00000000		
EDID_29[7:0]			R
0x1D	00000000		
EDID_30[7:0]			R
0x1E	00000000		
EDID_31[7:0]			R
0x1F	00000000		
EDID_32[7:0]			R
0x20	00000000		
EDID_33[7:0]			R
0x21	00000000		
EDID_34[7:0]			R
0x22	00000000		
EDID_35[7:0]			R
0x23	00000000		
EDID_36[7:0]			R
0x24	00000000		

Reg	Bits	Description	
EDID_37[7:0]			R
0x25	00000000		
EDID_38[7:0]			R
0x26	00000000		
EDID_39[7:0]			R
0x27	00000000		
EDID_40[7:0]			R
0x28	00000000		
EDID_41[7:0]			R
0x29	00000000		
EDID_42[7:0]			R
0x2A	00000000		
EDID_43[7:0]			R
0x2B	00000000		
EDID_44[7:0]			R
0x2C	00000000		
EDID_45[7:0]			R
0x2D	00000000		
EDID_46[7:0]			R
0x2E	00000000		
EDID_47[7:0]			R
0x2F	00000000		
EDID_48[7:0]			R
0x30	00000000		
EDID_49[7:0]			R
0x31	00000000		
EDID_50[7:0]			R
0x32	00000000		
EDID_51[7:0]			R
0x33	00000000		
EDID_52[7:0]			R
0x34	00000000		
EDID_53[7:0]			R
0x35	00000000		
EDID_54[7:0]			R
0x36	00000000		
EDID_55[7:0]			R
0x37	00000000		

Reg	Bits	Description	
EDID_56[7:0]			R
0x38	00000000		
EDID_57[7:0]			R
0x39	00000000		
EDID_58[7:0]			R
0x3A	00000000		
EDID_59[7:0]			R
0x3B	00000000		
EDID_60[7:0]			R
0x3C	00000000		
EDID_61[7:0]			R
0x3D	00000000		
EDID_62[7:0]			R
0x3E	00000000		
EDID_63[7:0]			R
0x3F	00000000		
EDID_64[7:0]			R
0x40	00000000		
EDID_65[7:0]			R
0x41	00000000		
EDID_66[7:0]			R
0x42	00000000		
EDID_67[7:0]			R
0x43	00000000		
EDID_68[7:0]			R
0x44	00000000		
EDID_69[7:0]			R
0x45	00000000		
EDID_70[7:0]			R
0x46	00000000		
EDID_71[7:0]			R
0x47	00000000		
EDID_72[7:0]			R
0x48	00000000		
EDID_73[7:0]			R
0x49	00000000		
EDID_74[7:0]			R
0x4A	00000000		

Reg	Bits	Description	
EDID_75[7:0]			R
0x4B	00000000		
EDID_76[7:0]			R
0x4C	00000000		
EDID_77[7:0]			R
0x4D	00000000		
EDID_78[7:0]			R
0x4E	00000000		
EDID_79[7:0]			R
0x4F	00000000		
EDID_80[7:0]			R
0x50	00000000		
EDID_81[7:0]			R
0x51	00000000		
EDID_82[7:0]			R
0x52	00000000		
EDID_83[7:0]			R
0x53	00000000		
EDID_84[7:0]			R
0x54	00000000		
EDID_85[7:0]			R
0x55	00000000		
EDID_86[7:0]			R
0x56	00000000		
EDID_87[7:0]			R
0x57	00000000		
EDID_88[7:0]			R
0x58	00000000		
EDID_89[7:0]			R
0x59	00000000		
EDID_90[7:0]			R
0x5A	00000000		
EDID_91[7:0]			R
0x5B	00000000		
EDID_92[7:0]			R
0x5C	00000000		
EDID_93[7:0]			R
0x5D	00000000		

Reg	Bits	Description	
EDID_94[7:0]			R
0x5E	00000000		
EDID_95[7:0]			R
0x5F	00000000		
EDID_96[7:0]			R
0x60	00000000		
EDID_97[7:0]			R
0x61	00000000		
EDID_98[7:0]			R
0x62	00000000		
EDID_99[7:0]			R
0x63	00000000		
EDID_100[7:0]			R
0x64	00000000		
EDID_101[7:0]			R
0x65	00000000		
EDID_102[7:0]			R
0x66	00000000		
EDID_103[7:0]			R
0x67	00000000		
EDID_104[7:0]			R
0x68	00000000		
EDID_105[7:0]			R
0x69	00000000		
EDID_106[7:0]			R
0x6A	00000000		
EDID_107[7:0]			R
0x6B	00000000		
EDID_108[7:0]			R
0x6C	00000000		
EDID_109[7:0]			R
0x6D	00000000		
EDID_110[7:0]			R
0x6E	00000000		
EDID_111[7:0]			R
0x6F	00000000		
EDID_112[7:0]			R
0x70	00000000		

Reg	Bits	Description	
EDID_113[7:0]			R
0x71	00000000		
EDID_114[7:0]			R
0x72	00000000		
EDID_115[7:0]			R
0x73	00000000		
EDID_116[7:0]			R
0x74	00000000		
EDID_117[7:0]			R
0x75	00000000		
EDID_118[7:0]			R
0x76	00000000		
EDID_119[7:0]			R
0x77	00000000		
EDID_120[7:0]			R
0x78	00000000		
EDID_121[7:0]			R
0x79	00000000		
EDID_122[7:0]			R
0x7A	00000000		
EDID_123[7:0]			R
0x7B	00000000		
EDID_124[7:0]			R
0x7C	00000000		
EDID_125[7:0]			R
0x7D	00000000		
EDID_126[7:0]			R
0x7E	00000000		
EDID_127[7:0]			R
0x7F	00000000		
EDID_128[7:0]			R
0x80	00000000		
EDID_129[7:0]			R
0x81	00000000		
EDID_130[7:0]			R
0x82	00000000		
EDID_131[7:0]			R
0x83	00000000		

Reg	Bits	Description	
EDID_132[7:0]			R
0x84	00000000		
EDID_133[7:0]			R
0x85	00000000		
EDID_134[7:0]			R
0x86	00000000		
EDID_135[7:0]			R
0x87	00000000		
EDID_136[7:0]			R
0x88	00000000		
EDID_137[7:0]			R
0x89	00000000		
EDID_138[7:0]			R
0x8A	00000000		
EDID_139[7:0]			R
0x8B	00000000		
EDID_140[7:0]			R
0x8C	00000000		
EDID_141[7:0]			R
0x8D	00000000		
EDID_142[7:0]			R
0x8E	00000000		
EDID_143[7:0]			R
0x8F	00000000		
EDID_144[7:0]			R
0x90	00000000		
EDID_145[7:0]			R
0x91	00000000		
EDID_146[7:0]			R
0x92	00000000		
EDID_147[7:0]			R
0x93	00000000		
EDID_148[7:0]			R
0x94	00000000		
EDID_149[7:0]			R
0x95	00000000		
EDID_150[7:0]			R
0x96	00000000		

Reg	Bits	Description	
EDID_151[7:0]			R
0x97	00000000		
EDID_152[7:0]			R
0x98	00000000		
EDID_153[7:0]			R
0x99	00000000		
EDID_154[7:0]			R
0x9A	00000000		
EDID_155[7:0]			R
0x9B	00000000		
EDID_156[7:0]			R
0x9C	00000000		
EDID_157[7:0]			R
0x9D	00000000		
EDID_158[7:0]			R
0x9E	00000000		
EDID_159[7:0]			R
0x9F	00000000		
EDID_160[7:0]			R
0xA0	00000000		
EDID_161[7:0]			R
0xA1	00000000		
EDID_162[7:0]			R
0xA2	00000000		
EDID_163[7:0]			R
0xA3	00000000		
EDID_164[7:0]			R
0xA4	00000000		
EDID_165[7:0]			R
0xA5	00000000		
EDID_166[7:0]			R
0xA6	00000000		
EDID_167[7:0]			R
0xA7	00000000		
EDID_168[7:0]			R
0xA8	00000000		
EDID_169[7:0]			R
0xA9	00000000		

Reg	Bits	Description	
EDID_170[7:0]			R
0xAA	00000000		
EDID_171[7:0]			R
0xAB	00000000		
EDID_172[7:0]			R
0xAC	00000000		
EDID_173[7:0]			R
0xAD	00000000		
EDID_174[7:0]			R
0xAE	00000000		
EDID_175[7:0]			R
0xAF	00000000		
EDID_176[7:0]			R
0xB0	00000000		
EDID_177[7:0]			R
0xB1	00000000		
EDID_178[7:0]			R
0xB2	00000000		
EDID_179[7:0]			R
0xB3	00000000		
EDID_180[7:0]			R
0xB4	00000000		
EDID_181[7:0]			R
0xB5	00000000		
EDID_182[7:0]			R
0xB6	00000000		
EDID_183[7:0]			R
0xB7	00000000		
EDID_184[7:0]			R
0xB8	00000000		
EDID_185[7:0]			R
0xB9	00000000		
EDID_186[7:0]			R
0xBA	00000000		
EDID_187[7:0]			R
0xBB	00000000		
EDID_188[7:0]			R
0xBC	00000000		

Reg	Bits	Description	
EDID_189[7:0]			R
0xBD	00000000		
EDID_190[7:0]			R
0xBE	00000000		
EDID_191[7:0]			R
0xBF	00000000		
EDID_192[7:0]			R
0xC0	00000000		
EDID_193[7:0]			R
0xC1	00000000		
EDID_194[7:0]			R
0xC2	00000000		
EDID_195[7:0]			R
0xC3	00000000		
EDID_196[7:0]			R
0xC4	00000000		
EDID_197[7:0]			R
0xC5	00000000		
EDID_198[7:0]			R
0xC6	00000000		
EDID_199[7:0]			R
0xC7	00000000		
EDID_200[7:0]			R
0xC8	00000000		
EDID_201[7:0]			R
0xC9	00000000		
EDID_202[7:0]			R
0xCA	00000000		
EDID_203[7:0]			R
0xCB	00000000		
EDID_204[7:0]			R
0xCC	00000000		
EDID_205[7:0]			R
0xCD	00000000		
EDID_206[7:0]			R
0xCE	00000000		
EDID_207[7:0]			R
0xCF	00000000		

Reg	Bits	Description	
EDID_208[7:0]			R
0xD0	00000000		
EDID_209[7:0]			R
0xD1	00000000		
EDID_210[7:0]			R
0xD2	00000000		
EDID_211[7:0]			R
0xD3	00000000		
EDID_212[7:0]			R
0xD4	00000000		
EDID_213[7:0]			R
0xD5	00000000		
EDID_214[7:0]			R
0xD6	00000000		
EDID_215[7:0]			R
0xD7	00000000		
EDID_216[7:0]			R
0xD8	00000000		
EDID_217[7:0]			R
0xD9	00000000		
EDID_218[7:0]			R
0xDA	00000000		
EDID_219[7:0]			R
0xDB	00000000		
EDID_220[7:0]			R
0xDC	00000000		
EDID_221[7:0]			R
0xDD	00000000		
EDID_222[7:0]			R
0xDE	00000000		
EDID_223[7:0]			R
0xDF	00000000		
EDID_224[7:0]			R
0xE0	00000000		
EDID_225[7:0]			R
0xE1	00000000		
EDID_226[7:0]			R
0xE2	00000000		

Reg	Bits	Description	
EDID_227[7:0]			R
0xE3	00000000		
EDID_228[7:0]			R
0xE4	00000000		
EDID_229[7:0]			R
0xE5	00000000		
EDID_230[7:0]			R
0xE6	00000000		
EDID_231[7:0]			R
0xE7	00000000		
EDID_232[7:0]			R
0xE8	00000000		
EDID_233[7:0]			R
0xE9	00000000		
EDID_234[7:0]			R
0xEA	00000000		
EDID_235[7:0]			R
0xEB	00000000		
EDID_236[7:0]			R
0xEC	00000000		
EDID_237[7:0]			R
0xED	00000000		
EDID_238[7:0]			R
0xEE	00000000		
EDID_239[7:0]			R
0xEF	00000000		
EDID_240[7:0]			R
0xF0	00000000		
EDID_241[7:0]			R
0xF1	00000000		
EDID_242[7:0]			R
0xF2	00000000		
EDID_243[7:0]			R
0xF3	00000000		
EDID_244[7:0]			R
0xF4	00000000		
EDID_245[7:0]			R
0xF5	00000000		

Reg	Bits	Description	
EDID_246[7:0]			R
0xF6	00000000		
EDID_247[7:0]			R
0xF7	00000000		
EDID_248[7:0]			R
0xF8	00000000		
EDID_249[7:0]			R
0xF9	00000000		
EDID_250[7:0]			R
0xFA	00000000		
EDID_251[7:0]			R
0xFB	00000000		
EDID_252[7:0]			R
0xFC	00000000		
EDID_253[7:0]			R
0xFD	00000000		
EDID_254[7:0]			R
0xFE	00000000		
EDID_255[7:0]			R
0xFF	00000000		

3 INDEX

ACP_HEADER2[7:0], 53
ACP_PACKET_ID[7:0], 53
ACP_PB[223:0], 52
ACP_PCKT_CLR, 21
ACP_PCKT_MB1, 22
ACP_PCKT_MB2, 21
ACP_PCKT_RAW, 20
ACP_PCKT_ST, 20
ACP_TYPE[7:0], 53
AINFO[7:0], 43
AINFO_RB[7:0], 43
AKSV[39:0], 43
AKSV_DELAY[2:0], 61, 74
AKSV_UPDATE_A_CLR, 32
AKSV_UPDATE_A_MB1, 32
AKSV_UPDATE_A_RAW, 31
AKSV_UPDATE_A_ST, 31
AKSV_UPDATE_B_CLR, 32
AKSV_UPDATE_B_MB1, 32
AKSV_UPDATE_B_RAW, 31
AKSV_UPDATE_B_ST, 31
AKSV_UPDATE_C_CLR, 32
AKSV_UPDATE_C_MB1, 32
AKSV_UPDATE_C_RAW, 31
AKSV_UPDATE_C_ST, 31
AKSV_UPDATE_D_CLR, 32
AKSV_UPDATE_D_MB1, 32
AKSV_UPDATE_D_RAW, 31
AKSV_UPDATE_D_ST, 31
ALWAYS_STORE_INF, 39
AN[63:0], 43
AN_DELAY[2:0], 61, 74
AN_STOP, 62, 75
ARC_RX_I2C_PWRDN, 36
ARC_RX_SINGLE_ENDED, 36
ARC_RX_SPDIF_INV, 36
ARC_TX_PWRDN[3:0], 36
AUD_INF_CKS_ERR_CLR, 32
AUD_INF_CKS_ERR_MB1, 32
AUD_INF_CKS_ERR_MB2, 32
AUD_INF_CKS_ERR_RAW, 31
AUD_INF_CKS_ERR_ST, 31
AUD_INF_LEN[7:0], 53
AUD_INF_PB[111:0], 51
AUD_INF_VERS[7:0], 53
AUD_PACKET_ID[7:0], 53
AUDIO_C_PCKT_CLR, 23
AUDIO_C_PCKT_MB1, 23
AUDIO_C_PCKT_MB2, 23
AUDIO_C_PCKT_RAW, 22
AUDIO_C_PCKT_ST, 22
AUDIO_INFO_CLR, 21
AUDIO_INFO_MB1, 22
AUDIO_INFO_MB2, 22
AUDIO_INFO_RAW, 20
AUDIO_INFO_ST, 21
AUTO_HDCP_MAP_ENABLE, 45
AV_MUTE, 38
AV_MUTE_CLR, 23
AV_MUTE_MB1, 23
AV_MUTE_MB2, 23
AV_MUTE_RAW, 22
AV_MUTE_ST, 22
AVI_INF_CKS_ERR_CLR, 32
AVI_INF_CKS_ERR_MB1, 32
AVI_INF_CKS_ERR_MB2, 32
AVI_INF_CKS_ERR_RAW, 31
AVI_INF_CKS_ERR_ST, 31
AVI_INF_LEN[7:0], 53
AVI_INF_PB[223:0], 51
AVI_INF_VERS[7:0], 53
AVI_INFO_CLR, 21
AVI_INFO_MB1, 22
AVI_INFO_MB2, 22

AVI_INFO_RAW, 20
AVI_INFO_ST, 21
AVI_PACKET_ID[7:0], 53
BCAPS[7:0], 43, 62, 75
BCAPS_DELAY[2:0], 61, 74
BG_AUDIO_DETECTED[3:0], 41
BG_AUDIO_LAYOUT, 41
BG_DEEP_COLOR_MODE[1:0], 41
BG_DST_DOUBLE, 41
BG_FIELD_HEIGHT[12:0], 41
BG_HDMI_INTERLACED, 41
BG_HDMI_MODE, 41
BG_HEADER_BYTE1[7:0], 42
BG_HEADER_REQUESTED[7:0], 41
BG_LINE_WIDTH[12:0], 41
BG_MEAS_DONE_CLR, 33
BG_MEAS_DONE_MB1, 34
BG_MEAS_DONE_RAW, 33
BG_MEAS_DONE_ST, 33
BG_MEAS_PORT_SEL[2:0], 38
BG_MEAS_REQ, 40
BG_PACKET_BYTE1[7:0], 42
BG_PACKET_BYTE2[7:0], 42
BG_PACKET_BYTE3[7:0], 42
BG_PACKET_BYTE4[7:0], 42
BG_PACKET_BYTE5[7:0], 42
BG_PARAM_LOCK, 41
BG_PIX_REP[3:0], 41
BG_TMDSFREQ[8:0], 40
BG_TMDSFREQ_FRAC[6:0], 41
BG_TOTAL_FIELD_HEIGHT[12:0], 41
BG_TOTAL_LINE_WIDTH[13:0], 41
BG_VALID_PACKET, 42
BKSV[39:0], 43
BKSV_COUNT[6:0], 63, 76
BKSV_FLAG, 63, 76
BKSV_FLAG_INTR_MASK, 60, 73
BKSV_FLAG_ST, 60, 73
BKSV_UPDATE_FLAG, 62, 75
BKSV0[7:0], 62, 75
BKSV1[7:0], 62, 75
BKSV2[7:0], 62, 75
BKSV3[7:0], 62, 75
BKSV4[7:0], 62, 75
BSTATUS[15:0], 43
CABLE_DET_A_CLR, 26
CABLE_DET_A_MB1, 26
CABLE_DET_A_RAW, 25
CABLE_DET_A_ST, 26
CABLE_DET_B_CLR, 26
CABLE_DET_B_MB1, 26
CABLE_DET_B_RAW, 25
CABLE_DET_B_ST, 26
CABLE_DET_C_CLR, 26
CABLE_DET_C_MB1, 27
CABLE_DET_C_RAW, 25
CABLE_DET_C_ST, 26
CABLE_DET_D_CLR, 26
CABLE_DET_D_MB1, 27
CABLE_DET_D_RAW, 25
CABLE_DET_D_ST, 26
CEC_BUF0_RX_FRAME_DATA0[7:0], 56
CEC_BUF0_RX_FRAME_DATA1[7:0], 56
CEC_BUF0_RX_FRAME_DATA10[7:0], 56
CEC_BUF0_RX_FRAME_DATA11[7:0], 56
CEC_BUF0_RX_FRAME_DATA12[7:0], 56
CEC_BUF0_RX_FRAME_DATA13[7:0], 56
CEC_BUF0_RX_FRAME_DATA14[7:0], 56
CEC_BUF0_RX_FRAME_DATA2[7:0], 56
CEC_BUF0_RX_FRAME_DATA3[7:0], 56
CEC_BUF0_RX_FRAME_DATA4[7:0], 56
CEC_BUF0_RX_FRAME_DATA5[7:0], 56
CEC_BUF0_RX_FRAME_DATA6[7:0], 56
CEC_BUF0_RX_FRAME_DATA7[7:0], 56
CEC_BUF0_RX_FRAME_DATA8[7:0], 56
CEC_BUF0_RX_FRAME_DATA9[7:0], 56
CEC_BUF0_RX_FRAME_HEADER[7:0], 55
CEC_BUF0_RX_FRAME_LENGTH[4:0], 56
CEC_BUF0_TIMESTAMP[1:0], 57

CEC_BUF1_RX_FRAME_DATA0[7:0], 57
CEC_BUF1_RX_FRAME_DATA1[7:0], 57
CEC_BUF1_RX_FRAME_DATA10[7:0], 57
CEC_BUF1_RX_FRAME_DATA11[7:0], 58
CEC_BUF1_RX_FRAME_DATA12[7:0], 58
CEC_BUF1_RX_FRAME_DATA13[7:0], 58
CEC_BUF1_RX_FRAME_DATA14[7:0], 58
CEC_BUF1_RX_FRAME_DATA2[7:0], 57
CEC_BUF1_RX_FRAME_DATA3[7:0], 57
CEC_BUF1_RX_FRAME_DATA4[7:0], 57
CEC_BUF1_RX_FRAME_DATA5[7:0], 57
CEC_BUF1_RX_FRAME_DATA6[7:0], 57
CEC_BUF1_RX_FRAME_DATA7[7:0], 57
CEC_BUF1_RX_FRAME_DATA8[7:0], 57
CEC_BUF1_RX_FRAME_DATA9[7:0], 57
CEC_BUF1_RX_FRAME_HEADER[7:0], 57
CEC_BUF1_RX_FRAME_LENGTH[4:0], 58
CEC_BUF1_TIMESTAMP[1:0], 57
CEC_BUF2_RX_FRAME_DATA0[7:0], 58
CEC_BUF2_RX_FRAME_DATA1[7:0], 58
CEC_BUF2_RX_FRAME_DATA10[7:0], 58
CEC_BUF2_RX_FRAME_DATA11[7:0], 58
CEC_BUF2_RX_FRAME_DATA12[7:0], 58
CEC_BUF2_RX_FRAME_DATA13[7:0], 58
CEC_BUF2_RX_FRAME_DATA14[7:0], 58
CEC_BUF2_RX_FRAME_DATA2[7:0], 58
CEC_BUF2_RX_FRAME_DATA3[7:0], 58
CEC_BUF2_RX_FRAME_DATA4[7:0], 58
CEC_BUF2_RX_FRAME_DATA5[7:0], 58
CEC_BUF2_RX_FRAME_DATA6[7:0], 58
CEC_BUF2_RX_FRAME_DATA7[7:0], 58
CEC_BUF2_RX_FRAME_DATA8[7:0], 58
CEC_BUF2_RX_FRAME_DATA9[7:0], 58
CEC_BUF2_RX_FRAME_HEADER[7:0], 58
CEC_BUF2_RX_FRAME_LENGTH[4:0], 58
CEC_BUF2_TIMESTAMP[1:0], 57
CEC_CLR_RX_RDY0, 57
CEC_CLR_RX_RDY1, 57
CEC_CLR_RX_RDY2, 57
CEC_CMD_INTR[7:0], 60, 73
CEC_CMD_INTR_MASK[7:0], 60, 73
CEC_DIS_AUTO_MODE, 57
CEC_ERROR_DET_MODE, 56
CEC_ERROR_REPORT_MODE, 56
CEC_FORCE_IGNORE, 56
CEC_FORCE_NACK, 56
CEC_GLITCH_FILTER_CTRL[5:0], 57
CEC_INTERRUPT_BYTE[7:0], 35
CEC_INTERRUPT_BYTE_CLR[7:0], 36
CEC_INTERRUPT_BYTE_MB1[7:0], 36
CEC_INTERRUPT_BYTE_ST[7:0], 35
CEC_LOGICAL_ADDRESS_MASK[2:0], 56
CEC_LOGICAL_ADDRESS0[3:0], 56
CEC_LOGICAL_ADDRESS1[3:0], 56
CEC_LOGICAL_ADDRESS2[3:0], 56
CEC_PD, 61, 74
CEC_POWER_UP, 56
CEC_RETRY_SFT[3:0], 55
CEC_RX_RDY0, 58
CEC_RX_RDY0_CLR, 35
CEC_RX_RDY0_MB1, 35
CEC_RX_RDY0_RAW, 34
CEC_RX_RDY0_ST, 34
CEC_RX_RDY1, 58
CEC_RX_RDY1_CLR, 35
CEC_RX_RDY1_MB1, 35
CEC_RX_RDY1_RAW, 34
CEC_RX_RDY1_ST, 34
CEC_RX_RDY2, 58
CEC_RX_RDY2_CLR, 35
CEC_RX_RDY2_MB1, 35

CEC_RX_RDY2_RAW, 34
CEC_RX_RDY2_ST, 34
CEC_SLAVE_ADDR[6:0], 37
CEC_SOFT_RESET, 57
CEC_TX_ARBITRATION_LOST_CLR, 35
CEC_TX_ARBITRATION_LOST_MB1, 35
CEC_TX_ARBITRATION_LOST_RAW, 34
CEC_TX_ARBITRATION_LOST_ST, 35
CEC_TX_ENABLE, 55
CEC_TX_FRAME_DATA0[7:0], 55
CEC_TX_FRAME_DATA1[7:0], 55
CEC_TX_FRAME_DATA10[7:0], 55
CEC_TX_FRAME_DATA11[7:0], 55
CEC_TX_FRAME_DATA12[7:0], 55
CEC_TX_FRAME_DATA13[7:0], 55
CEC_TX_FRAME_DATA14[7:0], 55
CEC_TX_FRAME_DATA2[7:0], 55
CEC_TX_FRAME_DATA3[7:0], 55
CEC_TX_FRAME_DATA4[7:0], 55
CEC_TX_FRAME_DATA5[7:0], 55
CEC_TX_FRAME_DATA6[7:0], 55
CEC_TX_FRAME_DATA7[7:0], 55
CEC_TX_FRAME_DATA8[7:0], 55
CEC_TX_FRAME_DATA9[7:0], 55
CEC_TX_FRAME_HEADER[7:0], 55
CEC_TX_FRAME_LENGTH[4:0], 55
CEC_TX_LOWDRIVE_COUNTER[3:0], 55
CEC_TX_NACK_COUNTER[3:0], 55
CEC_TX_READY_CLR, 35
CEC_TX_READY_MB1, 35
CEC_TX_READY_RAW, 34
CEC_TX_READY_ST, 35
CEC_TX_RETRY[2:0], 55
CEC_TX_RETRY_TIMEOUT_CLR, 35
CEC_TX_RETRY_TIMEOUT_MB1, 35
CEC_TX_RETRY_TIMEOUT_RAW, 34
CEC_TX_RETRY_TIMEOUT_ST, 35
CEC_TX_SFT[3:0], 55
CEC_USE_ALL_BUFS, 58
CEC_WAKE_OPCODE0[7:0], 58
CEC_WAKE_OPCODE1[7:0], 59
CEC_WAKE_OPCODE2[7:0], 59
CEC_WAKE_OPCODE3[7:0], 59
CEC_WAKE_OPCODE4[7:0], 59
CEC_WAKE_OPCODE5[7:0], 59
CEC_WAKE_OPCODE6[7:0], 59
CEC_WAKE_OPCODE7[7:0], 59
CHANNEL_SWAP, 63, 76
CKSUM_CALC, 44
CLEAR_KSV_LIST, 44
CLK_IN_FREQ_SEL[1:0], 18
CLK_IN_PDN, 18
CLOCK_TERMA_DISABLE, 40
CLOCK_TERMB_DISABLE, 40
CLOCK_TERMC_DISABLE, 40
CLOCK_TERMD_DISABLE, 40
CORE_PDN, 18
DDC_PWRDN[7:0], 40
DEEP_COLOR_CHNG_CLR, 30
DEEP_COLOR_CHNG_MB1, 30
DEEP_COLOR_CHNG_MB2, 30
DEEP_COLOR_CHNG_RAW, 30
DEEP_COLOR_CHNG_ST, 30
DEEP_COLOR_MODE[1:0], 39
DIS_CABLE_DET_RST, 39
DISABLE_AUTO_EDID, 45
DR_STR[1:0], 18
DUAL_EDID_ENABLE_PORT_A, 45
DUAL_EDID_ENABLE_PORT_B, 45
DUAL_EDID_ENABLE_PORT_C, 45
DUAL_EDID_ENABLE_PORT_D, 45
DVI_HSYNC_POLARITY, 38
DVI_VSYNC_POLARITY, 38
EDID_0[7:0], 64, 77
EDID_1[7:0], 64, 77
EDID_10[7:0], 64, 77
EDID_100[7:0], 67, 80
EDID_101[7:0], 67, 80
EDID_102[7:0], 67, 80
EDID_103[7:0], 67, 80
EDID_104[7:0], 67, 80
EDID_105[7:0], 67, 80

EDID_106[7:0], 67, 80
EDID_107[7:0], 67, 80
EDID_108[7:0], 67, 80
EDID_109[7:0], 67, 80
EDID_11[7:0], 64, 77
EDID_110[7:0], 67, 80
EDID_111[7:0], 67, 80
EDID_112[7:0], 67, 80
EDID_113[7:0], 67, 80
EDID_114[7:0], 67, 80
EDID_115[7:0], 67, 80
EDID_116[7:0], 67, 80
EDID_117[7:0], 67, 80
EDID_118[7:0], 68, 81
EDID_119[7:0], 68, 81
EDID_12[7:0], 64, 77
EDID_120[7:0], 68, 81
EDID_121[7:0], 68, 81
EDID_122[7:0], 68, 81
EDID_123[7:0], 68, 81
EDID_124[7:0], 68, 81
EDID_125[7:0], 68, 81
EDID_126[7:0], 68, 81
EDID_127[7:0], 68, 81
EDID_128[7:0], 68, 81
EDID_129[7:0], 68, 81
EDID_13[7:0], 64, 77
EDID_130[7:0], 68, 81
EDID_131[7:0], 68, 81
EDID_132[7:0], 68, 81
EDID_133[7:0], 68, 81
EDID_134[7:0], 68, 81
EDID_135[7:0], 68, 81
EDID_136[7:0], 68, 81
EDID_137[7:0], 68, 81
EDID_138[7:0], 68, 81
EDID_139[7:0], 68, 81
EDID_14[7:0], 64, 77
EDID_140[7:0], 68, 81
EDID_141[7:0], 68, 81
EDID_142[7:0], 68, 81
EDID_143[7:0], 68, 81
EDID_144[7:0], 68, 81
EDID_145[7:0], 68, 81
EDID_146[7:0], 68, 81
EDID_147[7:0], 68, 81
EDID_148[7:0], 68, 81
EDID_149[7:0], 69, 82
EDID_15[7:0], 64, 77
EDID_150[7:0], 69, 82
EDID_151[7:0], 69, 82
EDID_152[7:0], 69, 82
EDID_153[7:0], 69, 82
EDID_154[7:0], 69, 82
EDID_155[7:0], 69, 82
EDID_156[7:0], 69, 82
EDID_157[7:0], 69, 82
EDID_158[7:0], 69, 82
EDID_159[7:0], 69, 82
EDID_16[7:0], 64, 77
EDID_160[7:0], 69, 82
EDID_161[7:0], 69, 82
EDID_162[7:0], 69, 82
EDID_163[7:0], 69, 82
EDID_164[7:0], 69, 82
EDID_165[7:0], 69, 82
EDID_166[7:0], 69, 82
EDID_167[7:0], 69, 82
EDID_168[7:0], 69, 82
EDID_169[7:0], 69, 82
EDID_17[7:0], 64, 77
EDID_170[7:0], 69, 82
EDID_171[7:0], 69, 82
EDID_172[7:0], 69, 82
EDID_173[7:0], 69, 82
EDID_174[7:0], 69, 82
EDID_175[7:0], 69, 82
EDID_176[7:0], 69, 82
EDID_177[7:0], 69, 82
EDID_178[7:0], 70, 83
EDID_179[7:0], 70, 83
EDID_18[7:0], 64, 77
EDID_180[7:0], 70, 83
EDID_181[7:0], 70, 83
EDID_182[7:0], 70, 83
EDID_183[7:0], 70, 83

EDID_184[7:0], 70, 83
EDID_185[7:0], 70, 83
EDID_186[7:0], 70, 83
EDID_187[7:0], 70, 83
EDID_188[7:0], 70, 83
EDID_189[7:0], 70, 83
EDID_19[7:0], 64, 77
EDID_190[7:0], 70, 83
EDID_191[7:0], 70, 83
EDID_192[7:0], 70, 83
EDID_193[7:0], 70, 83
EDID_194[7:0], 70, 83
EDID_195[7:0], 70, 83
EDID_196[7:0], 70, 83
EDID_197[7:0], 70, 83
EDID_198[7:0], 70, 83
EDID_199[7:0], 70, 83
EDID_2[7:0], 64, 77
EDID_20[7:0], 64, 77
EDID_200[7:0], 70, 83
EDID_201[7:0], 70, 83
EDID_202[7:0], 70, 83
EDID_203[7:0], 70, 83
EDID_204[7:0], 70, 83
EDID_205[7:0], 70, 83
EDID_206[7:0], 70, 83
EDID_207[7:0], 70, 83
EDID_208[7:0], 70, 83
EDID_209[7:0], 71, 84
EDID_21[7:0], 64, 77
EDID_210[7:0], 71, 84
EDID_211[7:0], 71, 84
EDID_212[7:0], 71, 84
EDID_213[7:0], 71, 84
EDID_214[7:0], 71, 84
EDID_215[7:0], 71, 84
EDID_216[7:0], 71, 84
EDID_217[7:0], 71, 84
EDID_218[7:0], 71, 84
EDID_219[7:0], 71, 84
EDID_22[7:0], 64, 77
EDID_220[7:0], 71, 84
EDID_221[7:0], 71, 84
EDID_222[7:0], 71, 84
EDID_223[7:0], 71, 84
EDID_224[7:0], 71, 84
EDID_225[7:0], 71, 84
EDID_226[7:0], 71, 84
EDID_227[7:0], 71, 84
EDID_228[7:0], 71, 84
EDID_229[7:0], 71, 84
EDID_23[7:0], 64, 77
EDID_230[7:0], 71, 84
EDID_231[7:0], 71, 84
EDID_232[7:0], 71, 84
EDID_233[7:0], 71, 84
EDID_234[7:0], 71, 84
EDID_235[7:0], 71, 84
EDID_236[7:0], 71, 84
EDID_237[7:0], 71, 84
EDID_238[7:0], 72, 85
EDID_239[7:0], 72, 85
EDID_24[7:0], 64, 77
EDID_240[7:0], 72, 85
EDID_241[7:0], 72, 85
EDID_242[7:0], 72, 85
EDID_243[7:0], 72, 85
EDID_244[7:0], 72, 85
EDID_245[7:0], 72, 85
EDID_246[7:0], 72, 85
EDID_247[7:0], 72, 85
EDID_248[7:0], 72, 85
EDID_249[7:0], 72, 85
EDID_25[7:0], 64, 77
EDID_250[7:0], 72, 85
EDID_251[7:0], 72, 85
EDID_252[7:0], 72, 85
EDID_253[7:0], 72, 85
EDID_254[7:0], 72, 85
EDID_255[7:0], 72, 85
EDID_26[7:0], 64, 77
EDID_27[7:0], 64, 77
EDID_28[7:0], 64, 77
EDID_29[7:0], 65, 78
EDID_3[7:0], 64, 77
EDID_30[7:0], 65, 78

EDID_31[7:0], 65, 78
EDID_32[7:0], 65, 78
EDID_33[7:0], 65, 78
EDID_34[7:0], 65, 78
EDID_35[7:0], 65, 78
EDID_36[7:0], 65, 78
EDID_37[7:0], 65, 78
EDID_38[7:0], 65, 78
EDID_39[7:0], 65, 78
EDID_4[7:0], 64, 77
EDID_40[7:0], 65, 78
EDID_41[7:0], 65, 78
EDID_42[7:0], 65, 78
EDID_43[7:0], 65, 78
EDID_44[7:0], 65, 78
EDID_45[7:0], 65, 78
EDID_46[7:0], 65, 78
EDID_47[7:0], 65, 78
EDID_48[7:0], 65, 78
EDID_49[7:0], 65, 78
EDID_5[7:0], 64, 77
EDID_50[7:0], 65, 78
EDID_51[7:0], 65, 78
EDID_52[7:0], 65, 78
EDID_53[7:0], 65, 78
EDID_54[7:0], 65, 78
EDID_55[7:0], 65, 78
EDID_56[7:0], 65, 78
EDID_57[7:0], 65, 78
EDID_58[7:0], 66, 79
EDID_59[7:0], 66, 79
EDID_6[7:0], 64, 77
EDID_60[7:0], 66, 79
EDID_61[7:0], 66, 79
EDID_62[7:0], 66, 79
EDID_63[7:0], 66, 79
EDID_64[7:0], 66, 79
EDID_65[7:0], 66, 79
EDID_66[7:0], 66, 79
EDID_67[7:0], 66, 79
EDID_68[7:0], 66, 79
EDID_69[7:0], 66, 79
EDID_7[7:0], 64, 77
EDID_70[7:0], 66, 79
EDID_71[7:0], 66, 79
EDID_72[7:0], 66, 79
EDID_73[7:0], 66, 79
EDID_74[7:0], 66, 79
EDID_75[7:0], 66, 79
EDID_76[7:0], 66, 79
EDID_77[7:0], 66, 79
EDID_78[7:0], 66, 79
EDID_79[7:0], 66, 79
EDID_8[7:0], 64, 77
EDID_80[7:0], 66, 79
EDID_81[7:0], 66, 79
EDID_82[7:0], 66, 79
EDID_83[7:0], 66, 79
EDID_84[7:0], 66, 79
EDID_85[7:0], 66, 79
EDID_86[7:0], 66, 79
EDID_87[7:0], 66, 79
EDID_88[7:0], 66, 79
EDID_89[7:0], 67, 80
EDID_9[7:0], 64, 77
EDID_90[7:0], 67, 80
EDID_91[7:0], 67, 80
EDID_92[7:0], 67, 80
EDID_93[7:0], 67, 80
EDID_94[7:0], 67, 80
EDID_95[7:0], 67, 80
EDID_96[7:0], 67, 80
EDID_97[7:0], 67, 80
EDID_98[7:0], 67, 80
EDID_99[7:0], 67, 80
EDID_A_ENABLED, 44
EDID_B_ENABLED, 44
EDID_C_ENABLED, 44
EDID_D_ENABLED, 44
EDID_RDY_INTR_MASK, 60, 73
EDID_RDY_ST, 60, 73
EDID_READ_EN, 63, 76
EDID_READY_FLAG, 62, 75
EDID_SEGMENT[7:0], 62, 75
EDID_SLAVE_ADDR[6:0], 37
EDID_TRIES[3:0], 63, 76

EEPROM_READ_OK, 63, 76
EN_BG_PORT_A, 38
EN_BG_PORT_B, 38
EN_BG_PORT_C, 38
EN_BG_PORT_D, 38
EN_PKT_CNT_SEL, 54
EN_UMASK_RAW_INTRQ, 19
ENABLE_XXI_CLK_I2C, 63, 76
ENC_ON, 62, 75
ERROR_FLAG, 62, 75
EXT_EEPROM_MAN_SELECT, 44
EXT_EEPROM_MAN_VALUE, 44
EXT_EEPROM_TRI, 44
EXT_HDMI_MODE, 62, 75
FILT_5V_DET_DIS, 39
FILT_5V_DET_TIMER[6:0], 39
FRAME_ENC, 62, 75
FREQTOLERANCE[3:0], 39
GAMUT_HEADER1[7:0], 54
GAMUT_HEADER2[7:0], 54
GAMUT_IRQ_NEXT_FIELD, 39
GAMUT_MDATA_CLR, 23
GAMUT_MDATA_MB1, 23
GAMUT_MDATA_MB2, 23
GAMUT_MDATA_RAW, 22
GAMUT_MDATA_ST, 23
GAMUT_PACKET_ID[7:0], 54
GBD[223:0], 53
GEN_CTL_PCKT_CLR, 23
GEN_CTL_PCKT_MB1, 23
GEN_CTL_PCKT_MB2, 23
GEN_CTL_PCKT_RAW, 22
GEN_CTL_PCKT_ST, 22
HDCP_1P1_DIS, 61, 74
HDCP_AUTH_ST, 60, 73
HDCP_CONTROLLER_ERROR[3:0], 63, 76
HDCP_CONTROLLER_STATE[3:0], 63, 76
HDCP_CONTROLLER_STATE_4_INTR_MASK, 60, 73
HDCP_DESIRED, 62, 75
HDCP_ENABLED, 62, 75
HDCP_ERROR_INTR_MASK, 60, 73
HDCP_ERROR_ST, 60, 73
HDCP_I2C_RESET_TX, 40
HDCP_KEY_ERROR, 38
HDCP_KEYS_READ, 38
HDCP_MAP_SELECT[2:0], 45
HDCP_REPEATER_TIMEOUT[1:0], 62, 75
HDCP_REPT_EDID_RESET, 40
HDCP_REQUESTED, 63, 76
HDCP_RI_EXPIRED, 38
HDCP_START_DELAY[2:0], 61, 74
HDMI_COLORSPACE[3:0], 39
HDMI_CONTENT_ENCRYPTED, 38
HDMI_EDID_SEGMENT_SEL, 45
HDMI_ENCRPT_A_CLR, 26
HDMI_ENCRPT_A_MB1, 26
HDMI_ENCRPT_A_RAW, 25
HDMI_ENCRPT_A_ST, 25
HDMI_ENCRPT_B_CLR, 26
HDMI_ENCRPT_B_MB1, 26
HDMI_ENCRPT_B_RAW, 25
HDMI_ENCRPT_B_ST, 25
HDMI_ENCRPT_C_CLR, 26
HDMI_ENCRPT_C_MB1, 26
HDMI_ENCRPT_C_RAW, 25
HDMI_ENCRPT_C_ST, 25
HDMI_ENCRPT_D_CLR, 26
HDMI_ENCRPT_D_MB1, 26
HDMI_ENCRPT_D_RAW, 25
HDMI_ENCRPT_D_ST, 26
HDMI_MODE, 38, 63, 76
HDMI_PIXEL_REPETITION[3:0], 39
HDMI_PORT_SELECT_TX_A[2:0], 38
HDMI_PORT_SELECT_TX_B[2:0], 39
HDMI_SLAVE_ADDR[6:0], 37
HIGH_VSYNC[1:0], 61, 74
HPA_AUTO_INT_EDID[1:0], 40
HPA_DELAY_SEL[3:0], 40
HPA_MAN_VALUE_A, 19
HPA_MAN_VALUE_B, 19
HPA_MAN_VALUE_C, 19
HPA_MAN_VALUE_D, 19

HPA_MANUAL, 40
HPA_OVR_TERM, 40
HPA_STATUS_PORT_A, 19
HPA_STATUS_PORT_B, 19
HPA_STATUS_PORT_C, 19
HPA_STATUS_PORT_D, 19
HPA_TRISTATE_A, 19
HPA_TRISTATE_B, 19
HPA_TRISTATE_C, 19
HPA_TRISTATE_D, 19
HPD_DISABLE[1:0], 61, 74
HPD_INTR_MASK, 60, 73
HPD_ST, 60, 73
I2C_INTERRUPT, 62, 75
INFOFRAME_SLAVE_ADDR[6:0], 37
INTRQ_DUR_SEL[1:0], 19
INTRQ_OP_SEL[1:0], 20
INTRQ_RAW, 19
INTRQ_TX_A_RAW, 19
INTRQ_TX_B_RAW, 19
INV_SPDIF_IN[3:0], 36
ISRC1_HEADER1[7:0], 54
ISRC1_HEADER2[7:0], 54
ISRC1_PACKET_ID[7:0], 53
ISRC1_PB[223:0], 52
ISRC1_PCKT_CLR, 21
ISRC1_PCKT_MB1, 22
ISRC1_PCKT_MB2, 21
ISRC1_PCKT_RAW, 20
ISRC1_PCKT_ST, 20
ISRC2_HEADER1[7:0], 54
ISRC2_HEADER2[7:0], 54
ISRC2_PACKET_ID[7:0], 54
ISRC2_PB[223:0], 52
ISRC2_PCKT_CLR, 21
ISRC2_PCKT_MB1, 22
ISRC2_PCKT_MB2, 21
ISRC2_PCKT_RAW, 20
ISRC2_PCKT_ST, 20
KEYS_READ_ERROR, 62, 75
KSV_BYTE_0[7:0], 45
KSV_BYTE_1[7:0], 45
KSV_BYTE_10[7:0], 46
KSV_BYTE_100[7:0], 49
KSV_BYTE_101[7:0], 49
KSV_BYTE_102[7:0], 49
KSV_BYTE_103[7:0], 49
KSV_BYTE_104[7:0], 49
KSV_BYTE_105[7:0], 49
KSV_BYTE_106[7:0], 49
KSV_BYTE_107[7:0], 49
KSV_BYTE_108[7:0], 49
KSV_BYTE_109[7:0], 50
KSV_BYTE_11[7:0], 46
KSV_BYTE_110[7:0], 50
KSV_BYTE_111[7:0], 50
KSV_BYTE_112[7:0], 50
KSV_BYTE_113[7:0], 50
KSV_BYTE_114[7:0], 50
KSV_BYTE_115[7:0], 50
KSV_BYTE_116[7:0], 50
KSV_BYTE_117[7:0], 50
KSV_BYTE_118[7:0], 50
KSV_BYTE_119[7:0], 50
KSV_BYTE_12[7:0], 46
KSV_BYTE_120[7:0], 50
KSV_BYTE_121[7:0], 50
KSV_BYTE_122[7:0], 50
KSV_BYTE_123[7:0], 50
KSV_BYTE_124[7:0], 50
KSV_BYTE_125[7:0], 50
KSV_BYTE_126[7:0], 50
KSV_BYTE_127[7:0], 50
KSV_BYTE_13[7:0], 46
KSV_BYTE_14[7:0], 46
KSV_BYTE_15[7:0], 46
KSV_BYTE_16[7:0], 46
KSV_BYTE_17[7:0], 46
KSV_BYTE_18[7:0], 46
KSV_BYTE_19[7:0], 46
KSV_BYTE_2[7:0], 45
KSV_BYTE_20[7:0], 46
KSV_BYTE_21[7:0], 46
KSV_BYTE_22[7:0], 46
KSV_BYTE_23[7:0], 46
KSV_BYTE_24[7:0], 46

KSV_BYTE_25[7:0], 46
KSV_BYTE_26[7:0], 46
KSV_BYTE_27[7:0], 46
KSV_BYTE_28[7:0], 46
KSV_BYTE_29[7:0], 46
KSV_BYTE_3[7:0], 45
KSV_BYTE_30[7:0], 46
KSV_BYTE_31[7:0], 47
KSV_BYTE_32[7:0], 47
KSV_BYTE_33[7:0], 47
KSV_BYTE_34[7:0], 47
KSV_BYTE_35[7:0], 47
KSV_BYTE_36[7:0], 47
KSV_BYTE_37[7:0], 47
KSV_BYTE_38[7:0], 47
KSV_BYTE_39[7:0], 47
KSV_BYTE_4[7:0], 45
KSV_BYTE_40[7:0], 47
KSV_BYTE_41[7:0], 47
KSV_BYTE_42[7:0], 47
KSV_BYTE_43[7:0], 47
KSV_BYTE_44[7:0], 47
KSV_BYTE_45[7:0], 47
KSV_BYTE_46[7:0], 47
KSV_BYTE_47[7:0], 47
KSV_BYTE_48[7:0], 47
KSV_BYTE_49[7:0], 47
KSV_BYTE_5[7:0], 46
KSV_BYTE_50[7:0], 47
KSV_BYTE_51[7:0], 47
KSV_BYTE_52[7:0], 47
KSV_BYTE_53[7:0], 47
KSV_BYTE_54[7:0], 47
KSV_BYTE_55[7:0], 47
KSV_BYTE_56[7:0], 47
KSV_BYTE_57[7:0], 48
KSV_BYTE_58[7:0], 48
KSV_BYTE_59[7:0], 48
KSV_BYTE_6[7:0], 46
KSV_BYTE_60[7:0], 48
KSV_BYTE_61[7:0], 48
KSV_BYTE_62[7:0], 48
KSV_BYTE_63[7:0], 48
KSV_BYTE_64[7:0], 48
KSV_BYTE_65[7:0], 48
KSV_BYTE_66[7:0], 48
KSV_BYTE_67[7:0], 48
KSV_BYTE_68[7:0], 48
KSV_BYTE_69[7:0], 48
KSV_BYTE_7[7:0], 46
KSV_BYTE_70[7:0], 48
KSV_BYTE_71[7:0], 48
KSV_BYTE_72[7:0], 48
KSV_BYTE_73[7:0], 48
KSV_BYTE_74[7:0], 48
KSV_BYTE_75[7:0], 48
KSV_BYTE_76[7:0], 48
KSV_BYTE_77[7:0], 48
KSV_BYTE_78[7:0], 48
KSV_BYTE_79[7:0], 48
KSV_BYTE_8[7:0], 46
KSV_BYTE_80[7:0], 48
KSV_BYTE_81[7:0], 48
KSV_BYTE_82[7:0], 48
KSV_BYTE_83[7:0], 49
KSV_BYTE_84[7:0], 49
KSV_BYTE_85[7:0], 49
KSV_BYTE_86[7:0], 49
KSV_BYTE_87[7:0], 49
KSV_BYTE_88[7:0], 49
KSV_BYTE_89[7:0], 49
KSV_BYTE_9[7:0], 46
KSV_BYTE_90[7:0], 49
KSV_BYTE_91[7:0], 49
KSV_BYTE_92[7:0], 49
KSV_BYTE_93[7:0], 49
KSV_BYTE_94[7:0], 49
KSV_BYTE_95[7:0], 49
KSV_BYTE_96[7:0], 49
KSV_BYTE_97[7:0], 49
KSV_BYTE_98[7:0], 49
KSV_BYTE_99[7:0], 49
KSV_LIST_READY, 44
KSV_LIST_READY_CLR_A, 45
KSV_LIST_READY_CLR_B, 45
KSV_LIST_READY_CLR_C, 45

KSV_LIST_READY_CLR_D, 45
KSV_MAP_SELECT[2:0], 45
KSV_SLAVE_ADDR[6:0], 37
LOAD_EDID, 44
MAIN_RESET, 37
MAN_EDID_A_ENABLE, 44
MAN_EDID_B_ENABLE, 44
MAN_EDID_C_ENABLE, 44
MAN_EDID_D_ENABLE, 44
MPU_STIM_INTRQ, 20
MPU_STIM_INTRQ_CLR, 20
MPU_STIM_INTRQ_MB1, 20
MPU_STIM_INTRQ_RAW, 20
MPU_STIM_INTRQ_ST, 20
MS_INF_CKS_ERR_CLR, 31
MS_INF_CKS_ERR_MB1, 32
MS_INF_CKS_ERR_MB2, 32
MS_INF_CKS_ERR_RAW, 31
MS_INF_CKS_ERR_ST, 31
MS_INF_LEN[7:0], 53
MS_INF_PB[111:0], 51
MS_INF_VERS[7:0], 53
MS_INFO_CLR, 21
MS_INFO_MB1, 22
MS_INFO_MB2, 21
MS_INFO_RAW, 20
MS_INFO_ST, 21
MS_PACKET_ID[7:0], 53
MSEN_INTR_MASK, 60, 73
MSEN_ST, 60, 73
NEW_ACP_PCKT_CLR, 28
NEW_ACP_PCKT_MB1, 29
NEW_ACP_PCKT_MB2, 28
NEW_ACP_PCKT_RAW, 27
NEW_ACP_PCKT_ST, 28
NEW_AUDIO_INFO_CLR, 28
NEW_AUDIO_INFO_MB1, 29
NEW_AUDIO_INFO_MB2, 29
NEW_AUDIO_INFO_RAW, 27
NEW_AUDIO_INFO_ST, 28
NEW_AVI_INFO_CLR, 28
NEW_AVI_INFO_MB1, 29
NEW_AVI_INFO_MB2, 29
NEW_AVI_INFO_RAW, 27
NEW_AVI_INFO_ST, 28
NEW_GAMUT_MDATA_CLR, 30
NEW_GAMUT_MDATA_MB1, 30
NEW_GAMUT_MDATA_MB2, 30
NEW_GAMUT_MDATA_RAW, 29
NEW_GAMUT_MDATA_ST, 29
NEW_ISRC1_PCKT_CLR, 28
NEW_ISRC1_PCKT_MB1, 29
NEW_ISRC1_PCKT_MB2, 28
NEW_ISRC1_PCKT_RAW, 27
NEW_ISRC1_PCKT_ST, 27
NEW_ISRC2_PCKT_CLR, 28
NEW_ISRC2_PCKT_MB1, 29
NEW_ISRC2_PCKT_MB2, 28
NEW_ISRC2_PCKT_RAW, 27
NEW_ISRC2_PCKT_ST, 27
NEW_MS_INFO_CLR, 28
NEW_MS_INFO_MB1, 29
NEW_MS_INFO_MB2, 29
NEW_MS_INFO_RAW, 27
NEW_MS_INFO_ST, 28
NEW_SPD_INFO_CLR, 28
NEW_SPD_INFO_MB1, 29
NEW_SPD_INFO_MB2, 29
NEW_SPD_INFO_RAW, 27
NEW_SPD_INFO_ST, 28
NEW_TMDS_FRQ_CLR, 30
NEW_TMDS_FRQ_MB1, 30
NEW_TMDS_FRQ_RAW, 30
NEW_TMDS_FRQ_ST, 30
NEW_VS_INFO_CLR, 28
NEW_VS_INFO_MB1, 29
NEW_VS_INFO_MB2, 28
NEW_VS_INFO_RAW, 27
NEW_VS_INFO_ST, 28
PACKET_ERROR_CLR, 29
PACKET_ERROR_MB1, 30
PACKET_ERROR_MB2, 30
PACKET_ERROR_RAW, 29
PACKET_ERROR_ST, 29
PDN_PKT_PROCESSOR, 39
PJ[7:0], 43

PJ_FLAG, 62, 75
PKT_CNT_ID[7:0], 54
PKT_CNT_SEL[3:0], 54
PLL_LOCK_STATUS, 63, 76
PORT_B_CHECKSUM[7:0], 44
PORT_C_CHECKSUM[7:0], 44
PORT_D_CHECKSUM[7:0], 44
POWER_DOWN, 18
PWR_SAVE_MODE, 18
R0_WAIT_TIME[1:0], 62, 75
RB_PKT_CNT[3:0], 54
RD_INFO[15:0], 36
RI[15:0], 43
RI_DELAY_SEL[2:0], 61, 74
RI_EXPIRED_A_CLR, 33
RI_EXPIRED_A_MB1, 34
RI_EXPIRED_A_RAW, 33
RI_EXPIRED_A_ST, 33
RI_EXPIRED_B_CLR, 33
RI_EXPIRED_B_MB1, 34
RI_EXPIRED_B_RAW, 33
RI_EXPIRED_B_ST, 33
RI_EXPIRED_C_CLR, 33
RI_EXPIRED_C_MB1, 34
RI_EXPIRED_C_RAW, 33
RI_EXPIRED_C_ST, 33
RI_EXPIRED_D_CLR, 33
RI_EXPIRED_D_MB1, 34
RI_EXPIRED_D_RAW, 33
RI_EXPIRED_D_ST, 33
RI_FLAG, 62, 75
RI_FREQ_SEL[1:0], 61, 74
RI_RDY_INTR_MASK, 60, 73
RI_RDY_ST, 60, 73
RX_READY_INTR[2:0], 61, 74
RX_READY_INTR_MASK[2:0], 60, 73
RX_SENSE, 63, 76
SET INPUT TXA DDC SDA, 19
SET INPUT TXB DDC SDA, 19
SHA_A[31:0], 43
SHA_B[31:0], 43
SHA_C[31:0], 43
SHA_D[31:0], 43
SHA_E[31:0], 43
SKIP_RI_128, 61, 74
SPA_LOCATION[7:0], 44
SPA_LOCATION_MSB, 44
SPA_PORT_B[15:0], 43
SPA_PORT_C[15:0], 43
SPA_PORT_D[15:0], 43
SPA_SECONDARY_LOCATION[7:0], 45
SPD_INF_CKS_ERR_CLR, 32
SPD_INF_CKS_ERR_MB1, 32
SPD_INF_CKS_ERR_MB2, 32
SPD_INF_CKS_ERR_RAW, 31
SPD_INF_CKS_ERR_ST, 31
SPD_INF_LEN[7:0], 53
SPD_INF_PB[223:0], 51
SPD_INF_VERS[7:0], 53
SPD_INFO_CLR, 21
SPD_INFO_MB1, 22
SPD_INFO_MB2, 22
SPD_INFO_RAW, 20
SPD_INFO_ST, 21
SPD_PACKET_ID[7:0], 53
SPDIF_OUT_EN, 36
SPI_CFG[5:0], 45
STORE_EDID, 45
STORE_UNMASKED_IRQS, 19
SYSTEM_PD, 60, 73
TERM_AUTO, 38
TMDS_CLK_A_CLR, 24
TMDS_CLK_A_MB1, 25
TMDS_CLK_A_RAW, 23
TMDS_CLK_A_ST, 24
TMDS_CLK_B_CLR, 24
TMDS_CLK_B_MB1, 25
TMDS_CLK_B_RAW, 24
TMDS_CLK_B_ST, 24
TMDS_CLK_C_CLR, 24
TMDS_CLK_C_MB1, 25
TMDS_CLK_C_RAW, 24
TMDS_CLK_C_ST, 24
TMDS_CLK_D_CLR, 24
TMDS_CLK_D_MB1, 25
TMDS_CLK_D_RAW, 24

TMDS_CLK_D_ST, 24
TMDS_CLK_INV_I2C, 63, 76
TMDS_PLL_LOCKED, 38
TMDSFREQ[8:0], 39
TMDSFREQ_FRAC[6:0], 39
TMDSOUTPUTPWRDN, 63, 76
TMDSPLL_LCK_A_CLR, 24
TMDSPLL_LCK_A_MB1, 25
TMDSPLL_LCK_A_RAW, 23
TMDSPLL_LCK_A_ST, 24
TMDSPLL_LCK_B_CLR, 24
TMDSPLL_LCK_B_MB1, 25
TMDSPLL_LCK_B_RAW, 23
TMDSPLL_LCK_B_ST, 24
TMDSPLL_LCK_C_CLR, 24
TMDSPLL_LCK_C_MB1, 25
TMDSPLL_LCK_C_RAW, 23
TMDSPLL_LCK_C_ST, 24
TMDSPLL_LCK_D_CLR, 24
TMDSPLL_LCK_D_MB1, 25
TMDSPLL_LCK_D_RAW, 23
TMDSPLL_LCK_D_ST, 24
TRANSDRVENABLE_I2C[2:0], 63, 76
TX_ARBITRATION_LOST_INTR, 61, 74
TX_ARBITRATION_LOST_INTR_MASK, 60, 73
TX_HDMI_MODE, 62, 75
TX_READY_INTR, 60, 73
TX_READY_INTR_MASK, 60, 73
TX_RETRY_TIMEOUT_INTR, 61, 74
TX_RETRY_TIMEOUT_INTR_MASK, 60, 73
TXA SOFT RESET, 18
TXA_EDID_SLAVE_ADDR[6:0], 37
TXA_MAIN_SLAVE_ADDR[6:0], 36
TXA_UDP_SLAVE_ADDR[6:0], 36
TXB SOFT RESET, 18
TXB_EDID_SLAVE_ADDR[6:0], 36
TXB_MAIN_SLAVE_ADDR[6:0], 36
VCLK_CHNG_CLR, 30
VCLK_CHNG_MB1, 30
VCLK_CHNG_RAW, 30
VCLK_CHNG_ST, 30
VIDEO_3D_CLR, 27
VIDEO_3D_MB1, 27
VIDEO_3D_MB2, 27
VIDEO_3D_RAW, 27
VIDEO_3D_ST, 27
VS_INF_CKS_ERR_CLR, 34
VS_INF_CKS_ERR_MB1, 34
VS_INF_CKS_ERR_MB2, 34
VS_INF_CKS_ERR_RAW, 33
VS_INF_CKS_ERR_ST, 33
VS_INF_LEN[7:0], 53
VS_INF_PB[223:0], 51
VS_INF_VERS[7:0], 53
VS_INFO_CLR, 21
VS_INFO_MB1, 22
VS_INFO_MB2, 21
VS_INFO_RAW, 20
VS_INFO_ST, 21
VS_INTR_MASK, 60, 73
VS_PACKET_ID[7:0], 53
VSYNC_ST, 60, 73
ZERO_SPDIF_IN[3:0], 36