KWIK CIRCUIT FAQ

Discrete Anti-Aliasing Filter Design for Low Power Sigma Delta ADC

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FAQ: How to design a discrete low pass anti-aliasing filter for a low power Sigma Delta ADC?

Introduction

A KWIK (Know-how With Integrated Knowledge) Circuit application note offers a step-by-step guide to address a specific design challenge. For a given set of application circuit requirements, it illustrates how these are addressed using generic formulae and makes them easily scalable to other similar application specifications.

This KWIK circuit will focus on the elements to consider when designing an anti-aliasing filter with respect to the attenuation notch of a Sigma-Delta ADC and will provide a worked design example. An LTspice simulation schematic will be used to demonstrate the results.

Noise can be spread out across all frequencies as seen in **Figure 1**. Noise that occupies frequencies greater than one-half the sample frequency will be folded back into the first Nyquist zone and interfere with the signal of interest. To prevent this, an anti-aliasing filter before the ADC (low pass filter) is used to remove high frequency noise. Noise that is within the filter passband will still be observed (combined) with the signal.

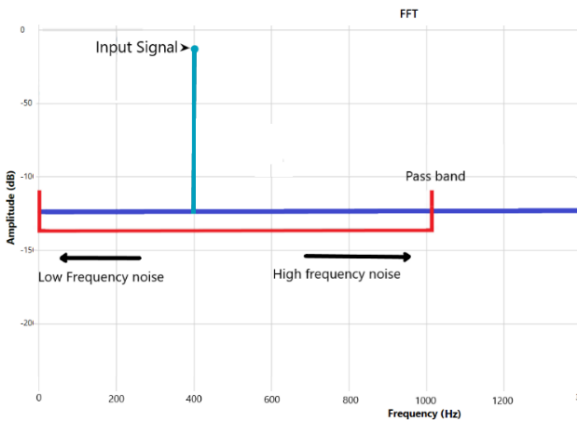

Figure 1. – Ideal Frequency response of 1KHz low pass filter.

For precision applications, the band of interest is almost always in the first Nyquist zone (f < Fs/2) and can be much less than Fs/2. In this KWIK note a two pole, passive R-C low pass filter is featured. The lowpass filter attenuates some of the noise in the first Nyquist zone and all of the noise at frequencies > Fs/2.

The ADC that will be used in the design example and simulations is the AD4130-8. This Sigma-Delta ADC is an ultra-low power 24-bit resolution ADC. A Sigma-Delta ADC architecture has an inherent noise-shape filter which allows the use of a simple passive R-C filter rather than an active filter that consumes more power. The AD4130-8 contains on chip programmable gain amplifier. The high impedance inputs ensure that current does not pass through the low pass filter resistors attenuating the sensor signal. The AD4130-8 also features SINC3 and SINC4 digital low pass filters that help reduce the high frequency noise that cannot be eliminated by the natural noise-shaping of the sigma-delta architecture. The SINC3 filter will be used in the design example. The signal of interest can also be amplified to maximize the signal's dynamic range with respect to the ADC, if needed, but is not addressed in this note.

The sigma-delta ADC modulation frequency (f_{MOD}) is the rate at which it digitally processes the incoming signal. At the modulation frequency the noise attenuation of the SINC filters is reduced. The modulation frequency can be found in the ADC datasheet.

In the AD4130-8 the modulation frequency where this problem occurs is at 76.8kHz. The analog RC filter is designed to combat this problem. **Figure 2** illustrates the effect of RC filters on this gap in filtering at the f_{MOD}. Noise that should be attenuated to -100dB is passed though at -25dB. Depending on how accurate the input signal needs to be, the order of the RC filter can be increased, and the noise can be attenuated much lower.

ADC Sigma Delta datasheets will generally not contain a plot showing the modulation frequency as shown in **Figure 2** below because external filtering is generally recommended in addition to the internal digital filters.

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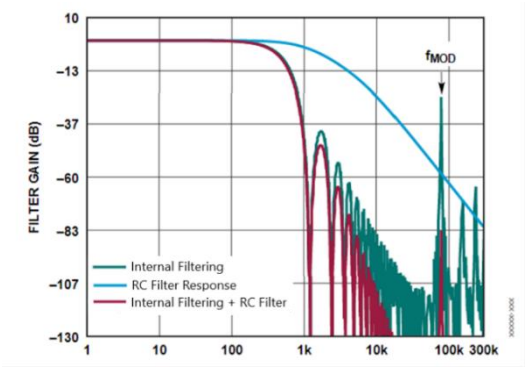

Figure 2. – Filtered and unfiltered responses of a 2nd order 1kHz discrete filter.

Design Specifications

The design choices for the circuit shown in **Figure 3** depend on the input signal and offset amplitude range and frequency. Example design key specifications of the circuit in **Figure 3** are listed in **Table 1**. The sensor chosen for this application is a strain gauge. A strain gauge is a sensor that has a resistance that increases as it is deformed by a force applied to it.

As a strain gauge has a resistive output rather than a voltage or current output that changes, it should be used as part of a Wheatstone bridge for the changes in strain to be measured. The chosen strain gauge is a FSS1500NSB from Honeywell.

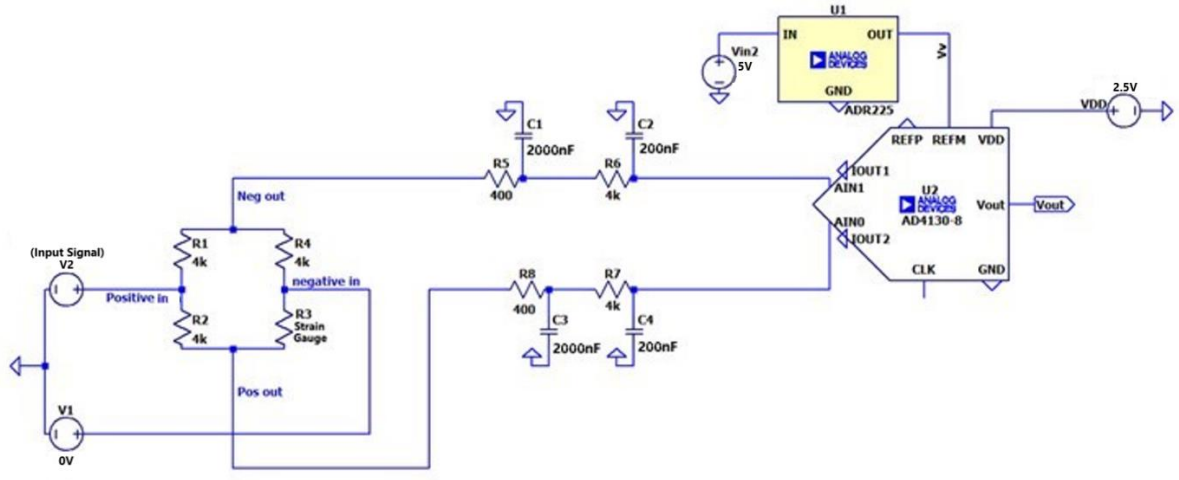

Figure 3. – *Strain gauge pressure sensor using a Wheatstone bridge circuit, with 2nd order discrete RC filtering on the differential inputs.*

Table 1. Design Specifications for Circuit in Figure 3

Filter Cutoff Frequency f_C	Attenuation at ∑-Δ ADC Modulation Frequency (f_{MOD})	∑-Δ ADC Modulation Frequency f_{MOD}	∑-Δ ADC output data rate (ODR)	Supplies +Vs/-Vs	Sensor (i.e. Load cell) sensitivity	Least Significant Bit (LSB) Size
120 Hz	> -100 dB	76.8 kHz	480 SPS	+3.3V/0V	0.12 mV/g	0.10mV/gram = 0.10mg/LSB

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Design Description

The circuit in **Figure 3** begins with four resistors arranged in a diamond to form a Wheatstone bridge with one of the resistors being a strain gauge load cell whose resistance will vary with the pressure applied. This section of the circuit acts as our sensor and outputs the differential Vsignal through the positive and negative outputs.

This is followed by a discrete 2nd order filter on both differential outputs to attenuate noise in general and most importantly at the f_{MOD} of the ADC. The circuit finishes with the differential inputs feeding into the AD4130-8 ADC. The internal Programmable-gain amplifier (PGA) has high input impedance which prevents the excitation source from becoming loaded and acts as a buffer between the filter and the ADC.

Design Tips / Considerations

1. Ratiometric/Power Supply noise

When using low voltage, precision sensors, it is important to consider the stability of the supply sources and the need to be filter noise. If the effect of the noise from the supply is above acceptable levels extra filtering may be needed on the supplies.

2. Capacitor sizing and system latency

When choosing a capacitor, the higher the capacitance the better. Having a larger filter capacitor helps attenuate the sampling charge injection from the modulator because more charge is available, better providing the instantaneous current needed to charge the sampling capacitors. The larger the filter capacitors, the more charge available to be used. It is recommended to use NP0/COG type ceramic capacitors because of their high Q-factor, low temperature coefficient, and stable electrical characteristics. Keep in mind that the larger the capacitor also causes increased RC time constant and requires a longer settling time/system latency.

3. Resistor Sizing and thermal noise

Adding resistor to the signal path adds thermal noise to the signal of interest. For this reason, it is important to keep resistors to the minimum resistance, while still drawing enough current to support the system.

Equation 3 below is used to calculate the noise density (Vn), of resistor thermal noise.

$$Vn\left(\frac{nV}{\sqrt{Hz}}\right)=\sqrt{4k\cdot T\cdot R}$$

k = Boltzmann's constant (1.38E-23 J/K)

T = temperature in degrees Kelvin.

R = Resistance in ohms

Design Procedure

The sensor used for this example is the FSS1500NSB strain gauge from Honeywell. Sensor spec table:

Table 2 . Strain Gauge Specifications

Parameter	Temperature	Specification
Sensitivity	25 °C	0.08 mV/gram (typ) 0.092 mV/gram (max)
Operating force	25 °C	0 to 1500 grams
Null offset	25 °C	+/- 9.9 mV (typ)
Null shift	2 °C to 40 °C	± 0.33 mV
Sensitivity shift	0 °C to 50 °C	5.5%

The ADC ref voltage is 2.5 V.

Step 1. Determining input range

The system will use an excitation of 3.3V to 0V based on the ADC's specifications. The equation for the strain gauge maximum nominal output voltage relative to the excitation is:

V_{OUT_MAX} = 1500 g * 0.092 mV/g = 139 mV

The maximum voltage at the sensor output, V_{MAX}, accounting for temperature effects and offsets is:

V_{MAX} = [V_{OUT_MAX}*(Sens shift) + Null Offset + Null Shift

= 139 mV*(1.055) + 9.9 mV + 0.33 mV = 157 mV

The total input range of the ADC is +/- (V_{REF}/GAIN), per the data sheet. Using an initial GAIN = 32 yields the following allowable V_{MAX}: V_{INp-p} = +/- (2.5V_{REF}/32) = +/- 78 mV, or 156.25 mVp-p.

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1 LSB at the sensor output:

$$1\ LSB=\frac{V_{INp-p}}{2^{24}-1}=\frac{156.25mV}{2^{24}-1}=9.3\ nV$$

(9.3 nV/LSB)/ (0.08 mV/gram) = 0.12 mg/LSB (nominal).

The gain is too large and is causing the input range to exceed the maximum nominal voltage. The gain needs to be lowered to 16.

Setting the gain to 16 yields a valid input range of:

V_{INp-p} = +/- ($2.5V_{REF}$/16) = +/- 156.25 mV, or 312.5 mVp-p.

1 LSB at the sensor output:

$$1\ LSB=\frac{V_{INp-p}}{2^{24}-1}=\frac{312.5mV}{2^{24}-1}=10\ nV$$

In grams, this represents a resolution of:

(10 nV/LSB)/ (0.08 mV/gram) = 0.10 mg/LSB (nominal).

This calculation uses the typical sensitivity from Table 1.

This represents the smallest change in strain that can be detected by a 24-bit Sigma-Delta ADC, ignoring the effect of noise for now.

The rate of change in the strain is on the order of < 125 Hz so the output data rate is set at 480 SPS.

Step 2. Choosing Cutoff Frequency and filter order

The internal Sinc3 filter of the AD4130-8 starts attenuating at 133 Hz and the ADC has a modulation frequency of 76.8kHz. The sensor will be measuring a slow changing signal from the strain gauge. The frequency will be low and should not exceed 100Hz. DC to 100Hz will be the application bandwidth. Based on this the chosen filter cutoff frequency is 120Hz. This doesn't attenuate the input from the sensor, and it is more than two decades below the modulation frequency of the ADC insuring good attenuation at 76.8KHz.

The modulation frequency is very important to consider as it is the main reason for having this extra RC filtering. From the datasheet for the AD4130-8 the modulation frequency is given as 76.8kHz. Based on the characteristics of the SINC3 filter the attenuation is -26dB at that frequency. The roll-off for an n-order RC is given by:

$$filter_{order}\cdot -20dB\ per\ decade$$

The chosen target accuracy is 0.01 grams, or 10 mg. Given a noise-free resolution of 0.10 mg/LSB, this translates to:

10 mg/(0.10 mg/LSB) = 100 LSBs. Consequently, the peak-to-peak noise should be much less than this.

At the ADC input, 1 LSB is:

$$1LSB=\frac{2\cdot V_{REF}}{2^{24}-1}=298nV$$

The limit on peak-to-peak noise in volts is:

100 LSBs * 298 nV/LSB = 29.8 uVp-p

This is an equivalent RMS noise voltage of:

Vp-p/6 ~= V_{RMS} = 29.8/6 = 4.97 uV_{RMS}.

The design goal is to attenuate the peak-to-peak noise by at least half at f_{MOD} to avoid interference from noise. The needed attenuation is:

20log10(29.8uV/2) = -96.54dB.

f_{MOD} is more than 2 decades higher than the target filter cutoff, so a 2nd order filter having a roll-off rate of -40dB per decade will provide sufficient attenuation at f_{MOD}. Note that to achieve a uniform roll-off of -40 dB/decade, both filter poles are placed at the same frequency. An approximation of the attenuation at the target frequency is:

$$f_{MOD}\ attenuation = \left(\frac{f_{MOD}-(fc\cdot 10\ for\ 2nd\ pole)}{(fc\cdot 1000\ for\ 3rd\ pole)-(fc\cdot 100\ for\ 2nd\ pole)}\cdot -40dB\right) + (-40dB\cdot 2\ for\ first\ 2\ decades)$$

$$f_{MOD}\ attenuation = \left(\frac{76{,}800-1200}{120{,}000-1200}\cdot -40dB\right)+(-40dB\cdot 2)=-105.5dB$$

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This cuts the modulation frequency down to -105.5dB and is above the target of -96.54dB.

To obtain a higher order filter additional stages of the filter can be cascaded. However, it is important to ensure that subsequent stages do not load the initial stage. A simple approach to prevent the loading is to increase the real impedance of each subsequent stage by a factor of ten. The resistors will be 400Ω and 4kΩ as they should have a 10x difference. They should also produce minimal thermal noise and will be easy to find with a 5% tolerance.

The first pole of the filter is set at the -3dB cutoff of the filter not the cutoff frequency. The following equations are needed to convert our target -3dB frequency into a cutoff frequency that can be used in the following equations to calculate the capacitor sizing. This will produce a discrete RC filter with the desired -3dB cutoff frequency that we seek for our first pole.

Cutoff frequency for 2nd order passive RC filter:

$$fc(Hz)=\frac{1}{2\pi\sqrt{R1\cdot R2\cdot C1\cdot C2}}$$

Cutoff frequency for 1st order passive RC filter:

$$fc(Hz)=\frac{1}{2\pi\cdot R\cdot C}$$

3dB frequency for n-th order low pass filter with cutoff f_C:

$$f_{-3dB}(Hz)=fc(Hz)\cdot\sqrt{2^{\frac{1}{n}}-1}$$

n = filter order
fc(Hz) = desired cutoff frequency
f(-3dB) = actual -3dB frequency of n-th order filter

$$186.45Hz=\frac{120Hz}{\sqrt{(2^{\frac{1}{2}})-1}}$$

$$fc(Hz)=\frac{1}{2\pi\cdot R\cdot C}$$

$$186.45Hz=\frac{1}{2\pi\cdot 400\cdot C}$$

$$C=\frac{1}{2\pi\cdot 400\cdot 186.45Hz}$$

$$C1=2.13e\text{-}6\ F = 2130nF$$

The calculated capacitor value is ideal. A standard value is 2000nF (2uF) with 5% tolerance. Using these RC values, the actual cutoff and 3dB frequencies are:

$$198.94Hz=\frac{1}{2\pi\cdot 400\cdot 2e\text{-}6}$$

$$128Hz=198.94Hz\sqrt{(2^{\frac{1}{n}})-1}$$

To find the value of the components in the second filter, the second capacitor needs to be 10x smaller and the resistor 10x larger than the previous stage.

$$R2=R1\cdot 10 = (400)(10) = 4K\Omega$$

$$C2=\frac{C1}{10}=\frac{(2e\text{-}6)}{(10)}=2e\text{-}7 = 200nF$$

We now have the values for the two RC filters in series. The first filter will have a R1 of 400Ω with a C1 of 2uF, the second filter will have a R2 of 4KΩ and a C2 of 200nF. This gives a -3dB cutoff frequency of 128Hz.

Step 3. Checking Thermal Noise

Thermal noise and capacitor latency need to be taken into account, and the ratio of resistance to capacitance tweaked to minimize our resistor values and maximize our capacitor size to a certain degree. The thermal resistance of each resistor needs to be calculated separately and added afterwards.

The thermal noise density is given by:

$$Vn\left(\frac{V}{\sqrt{Hz}}\right)=\sqrt{4\cdot k\cdot T\cdot R}$$

The root-mean-square value of the thermal noise is given by:

$$Vn(RMS)=\sqrt{4\cdot k\cdot T\cdot (ENBW)}$$

ENBW = equivalent noise bandwidth = fc (Hz) * pole correction factor

k = Boltzmann's constant (1.38e-23 J/K)

T = temperature in degrees Kelvin.

$$Vn(RMS)R1=\sqrt{(4\cdot k)(298°K)(400\Omega)(128Hz*1.22)}$$

$$Vn(RMS)R1=32nV_{RMS}$$

$$Vn(RMS)R2=\sqrt{(4\cdot k)(298°K)(4000\Omega)(128Hz*1.22)}$$

$$Vn(RMS)R2=101nV_{RMS}$$

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The total noise is the root-sum-square value:

$$\text{total } V_{nRMS}=\sqrt{(101)^2+(32)^2}\ nV_{RMS}=106\ nV_{RMS}$$

This is the noise at the PGA input. This must be adjusted for the gain to obtain the noise at the ADC input:

$$16*106nV_{RMS}=1.695uV_{RMS}.$$

This is less than the maximum allowable noise of 4.97 uV_{RMS} and provides margin for the sensor noise contribution.

Step 4. Tolerance of parts

Tolerance in the parts will make the cutoff frequency vary over a range that has to be calculated.

$$fc_{max}=\frac{1}{2\pi((R\cdot(1-tol))\cdot(C\cdot(1-tol))}=\frac{1}{2\pi\cdot RC\cdot(1-tol)^2}$$

$$fc_{min}=\frac{1}{2\pi((R\cdot(1+tol))\cdot(C\cdot(1+tol))}=\frac{1}{2\pi\cdot RC\cdot(1+tol)^2}$$

$$fc_{max}\ \text{Filter 1}=\frac{1}{2\pi((400\cdot(1-0.05))\cdot(2E\text{-}6\cdot(1-0.05))}=\frac{1}{(2\pi)\cdot(2E\text{-}6\cdot400)\cdot(0.95^2)}=220.5Hz$$

$$142Hz=220.5Hz\sqrt{(2^{\frac{1}{n}})-1}$$

$$fc_{min}\ \text{Filter 1}=\frac{1}{2\pi((400\cdot(1+0.05))\cdot(2E\text{-}6\cdot(1+0.05))}=\frac{1}{(2\pi)\cdot(2E\text{-}6\cdot400)\cdot(1.05^2)}=180.5Hz$$

$$116Hz=180.5Hz\sqrt{(2^{\frac{1}{n}})-1}$$

Since both filters have the same cutoff frequency and tolerances, the max and min frequencies of one filter are the same as the combined of both filters.

The signal from the sensor will have a much lower frequency than the minimum of 116Hz so this will not interfere with our signal. The maximum of 142Hz is only 22Hz higher than the planned cutoff of 120Hz, this increase in bandwidth should have a negligible effect on the noise allowed to pass through.

Design Simulations

Using the LTspice schematic shown in **Figure 3**, the cutoff frequency and attenuation of the circuit can be analyzed from the resulting graphing of the differential voltage of the filters and output from the ADC.

Calculated value

Rc filter attenuation at f_{MOD}

$$\frac{75.6KHz}{118.8KHz}=0.63$$

2+0.63=2.63 decades off attenuation

-40dB·2.63=105.5dB

2^{nd} order filter attenuation at f_{MOD} = [105.5dB]

Total attenuation at f_{MOD}

Rc filtering + internal SINC3 attenuation

105.5dB + 26dB=131.5dB

Table 3.Design Goal vs. Simulation.

Parameter	Design Goal	Simulation
Filter -3dB Cutoff Frequency	120Hz	120Hz
Attenuation at f_{MOD}	-131.5dB	-130dB

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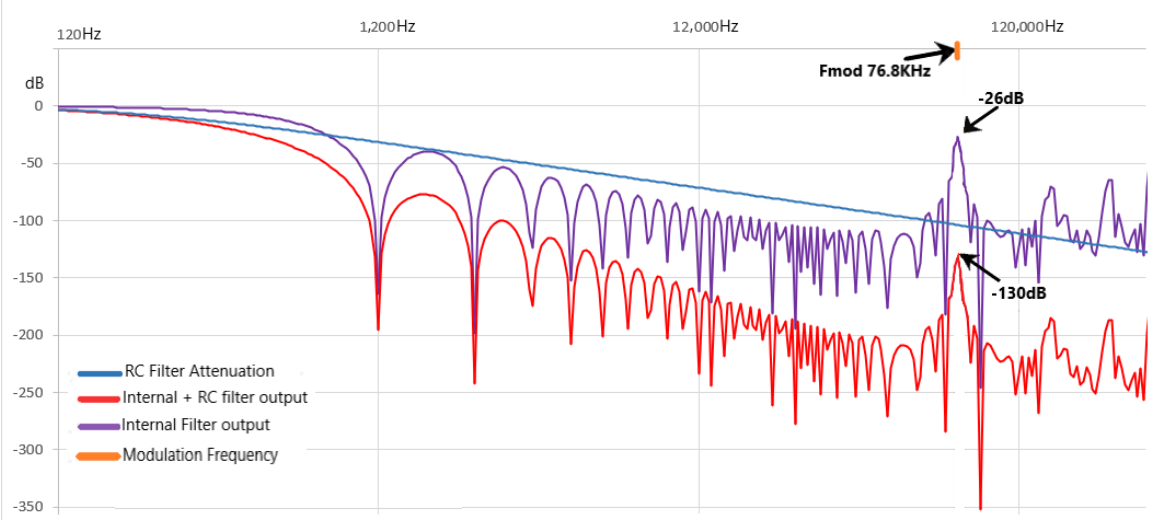

Figure 4: Frequency response of circuit with Fmod of the internal filtering marked.

Simulated Value

The internal filtering has an attenuation of -26dB at the f_{MOD}. The added RC filter achieves attenuation at f_{MOD} of -104B, making the total attenuation of the signal -130dB at the f_{MOD}.

Results

The simulated attenuation at f_{MOD} came out a few dB lower than calculated. This is only a small discrepancy caused by rounding the values in the equations and has a negligible effect on my circuit. The simulated values are within acceptable ranges and fulfill the intended purpose of the filter.

Design Devices

Table 4. ADC

Part Number	Resolution (bits)	FSAMPLE (Ksps)max	Input Type (SE or DIFF)	Vin SPAN (v) Vmin/Vmax	Data Interface (I2C, SPI, Parallel)
AD4130-8	24	2.4	FULLY DIFF	3.6	SPI

Table 5. Sensor (Performance at 5± 0.01 Vdc)

Part Number	Null Offset Min/Max (A)max	Sensitivity mV/gram min/typ/max	Input/output resistance Max/Min (KΩ)	Operating force Max/Min (grams)
FSS1500NSB	-15mV/+15mV	0.1/0.12/0.14	4 KΩ /6 KΩ	0g/1500g

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References

LTspice

LTspice® is a high-performance SPICE III simulator, schematic capture and waveform viewer with enhancements and models for easing the simulation of switching regulator, linear, and signal chain circuits.

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Acknowledgments

Key Analog Devices Consultants:

Jim Catt
Senior Applications Manager,
Industrial Platforms & Technology

Marie-Eve Carré
Signal Chain Design Engineer,
Industrial Platforms & Technology.

David Plourde
IC Design Engineer, Scientific
Instruments (SCI) group.

Padraic O'Reilly
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